

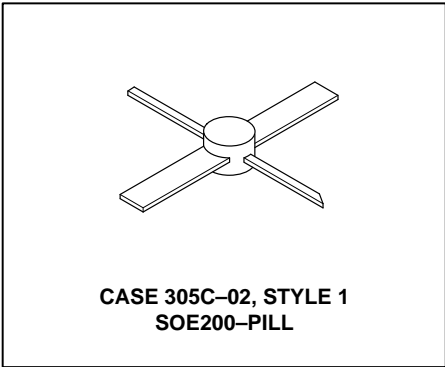
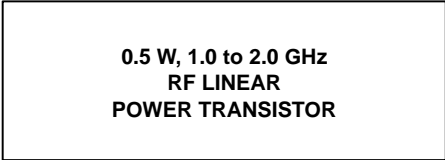
The RF Line

NPN Silicon

RF Power Transistor

The MRF6401 is designed for Class A common emitter, linear power amplifiers in the 1.0–2.0 GHz frequency range. It has been specifically designed for use in Personal Communications Network (PCN) base station and INMARSAT Standard M applications.

- Specified 20 Volts, 1.66 GHz Characteristics:
 - Output Power — 0.5 Watts
 - Gain — 10 dB Min
 - Class A Operation
- Specified 20 Volts, 1.88 GHz Characteristics:
 - Output Power — 0.5 Watts
 - Gain — 9.0 dB Min
 - Class A Operation
- Circuit Board Photomaster Available by Ordering Document MRF6401PHT/D from Motorola Literature Distribution.



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	22	Vdc
Collector–Base Voltage	V_{CB0}	45	Vdc
Emitter–Base Voltage	V_{EBO}	3.5	Vdc
Operating Junction Temperature	T_J	200	°C
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	5.8 0.033	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (1)	$R_{\theta JC}$	30	°C/W

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector–Emitter Breakdown Voltage ($I_C = 10 \text{ mAdc}$, $R_B = 75 \Omega$)	$V_{(BR)CER}$	28	—	—	Vdc
Emitter–Base Breakdown Voltage ($I_E = 0.25 \text{ mAdc}$)	$V_{(BR)EBO}$	3.5	—	—	Vdc
Collector–Base Breakdown Voltage ($I_C = 1 \text{ mAdc}$)	$V_{(BR)CBO}$	45	—	—	Vdc

(1) Thermal resistance is determined under specified RF operating condition.

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain ($I_C = 0.1 \text{ Adc}$, $V_{CE} = 5 \text{ Vdc}$)	h_{FE}	20	—	120	—
DYNAMIC CHARACTERISTICS					
Output Capacitance ($V_{CB} = 26 \text{ V}$, $I_E = 0$, $f = 1 \text{ MHz}$)	C_{ob}	—	1.4	—	pF
FUNCTIONAL TESTS ($V_{CC} = 20 \text{ V}$, $I_{CQ} = 80 \text{ mA}$)					
Common-Emitter Amplifier Power Gain ($f = 1660 \text{ MHz}$, $P_{out} = 0.5 \text{ W}$) ($f = 1880 \text{ MHz}$, $P_{out} = 0.5 \text{ W}$)	G_p	10 9	11 10	— —	dB
Load Mismatch ($f = 1660 \text{ MHz}$, $f = 1880 \text{ MHz}$, $P_{out} = 0.5 \text{ W}$, Load VSWR = 20:1, all phase angles at frequency of test)	ψ	No Degradation in Output Power			
Intermodulation Distortion ($P_{out} = 0.5 \text{ W PEP}$, $f_1 = 1659.2 \text{ MHz}$, $f_2 = 1660 \text{ MHz}$) ($P_{out} = 0.5 \text{ W PEP}$, $f_1 = 1879.2 \text{ MHz}$, $f_2 = 1880 \text{ MHz}$)	IMD	-30 -30	-35 -35	— —	dBc

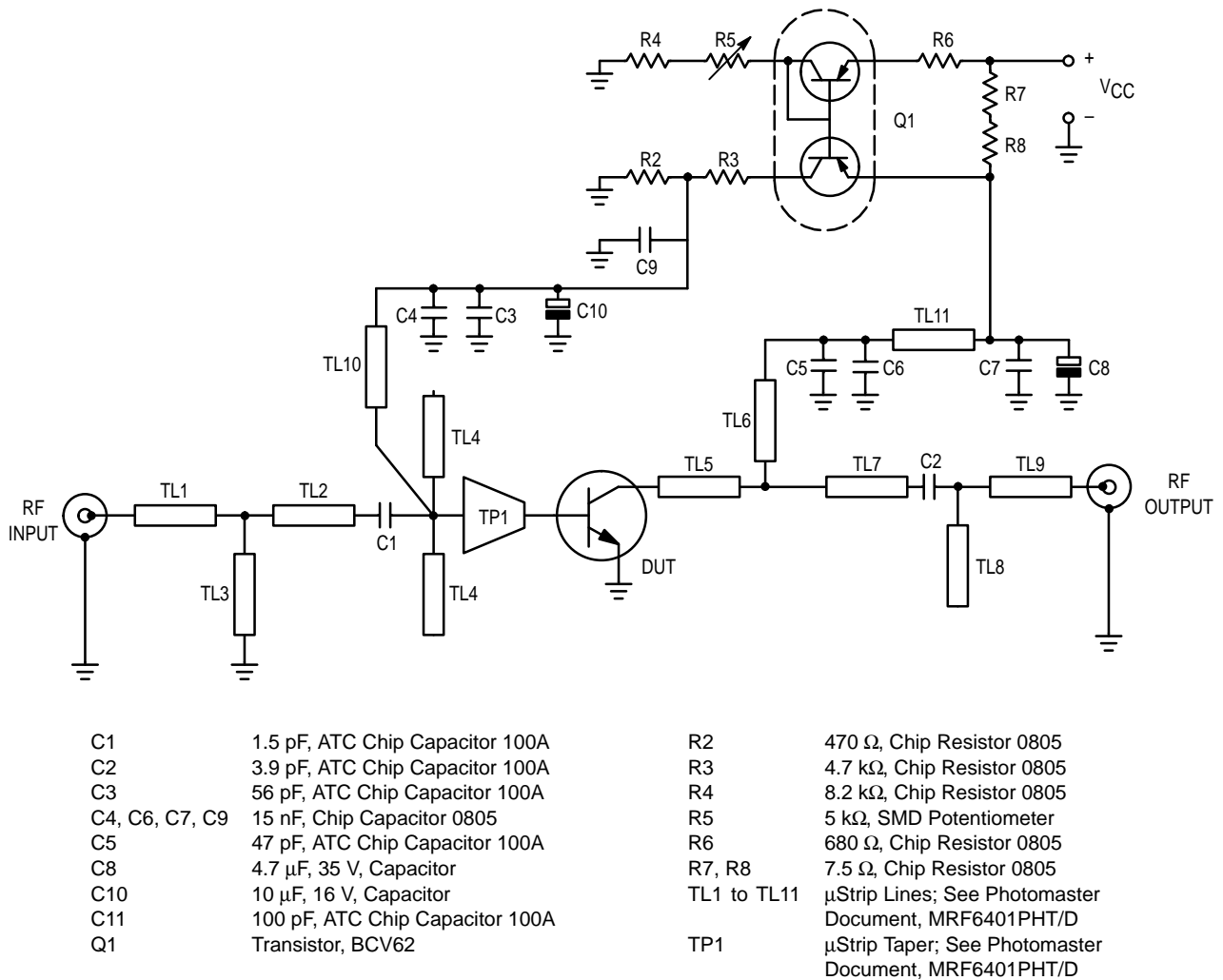


Figure 1. 1600–2000 MHz Broadband Application Amplifier Schematic

TYPICAL CHARACTERISTICS

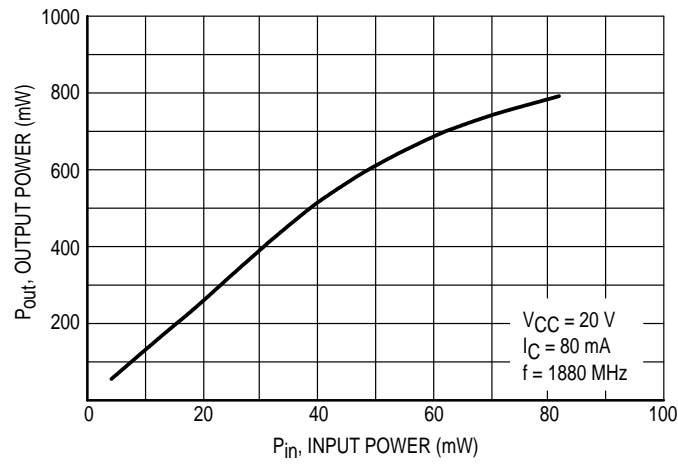


Figure 2. Output Power versus Input Power

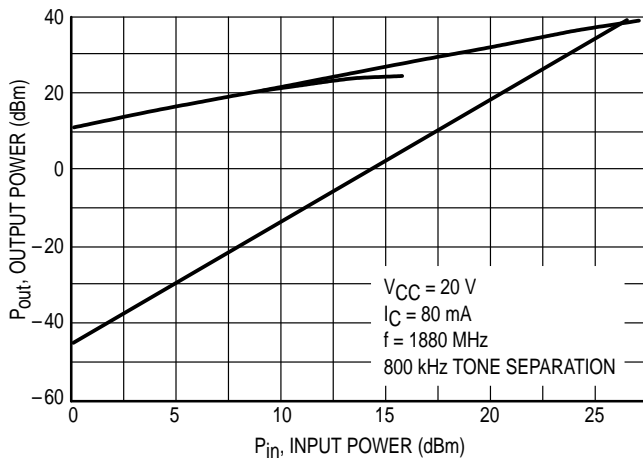


Figure 3. Third Order Intercept

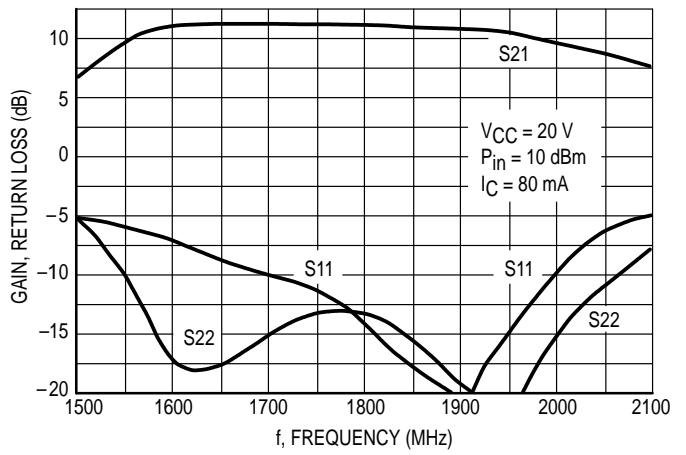


Figure 4. Performance in Broadband Test Fixture

Table 1. Common Emitter S-Parameters

$V_{CC} = 20\text{ V}$, $I_C = 80\text{ mA}$

POLAR S-PARAMETERS IN 50 Ω SYSTEM								
f MHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠ φ	S ₂₁	∠ φ	S ₁₂	∠ φ	S ₂₂	∠ φ
100	0.626	-118	28.4	127	0.0186	45	0.649	-40
200	0.718	-149	17.1	106	0.0230	35	0.434	-49
400	0.754	-171	9.10	88	0.0271	35	0.303	-53
600	0.761	179	6.15	77	0.0312	38	0.272	-56
800	0.762	171	4.65	68	0.0359	42	0.266	-62
1000	0.763	165	3.73	60	0.0409	44	0.271	-68
1200	0.758	159	3.13	52	0.0469	44	0.286	-75
1400	0.753	155	2.60	44	0.0490	46	0.291	-87
1600	0.765	150	2.30	39	0.0574	50	0.288	-93
1800	0.769	144	2.06	32	0.0665	49	0.303	-97
1900	0.768	142	1.98	29	0.0714	48	0.312	-100
2000	0.767	139	1.88	25	0.0756	48	0.322	-103

$V_{CC} = 20\text{ V}$, $I_C = 50\text{ mA}$

POLAR S-PARAMETERS IN 50 Ω SYSTEM								
f MHz	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠ φ	S ₂₁	∠ φ	S ₁₂	∠ φ	S ₂₂	∠ φ
100	0.618	-113	26.2	130	0.0195	45	0.678	-36
200	0.713	-145	16.2	108	0.0251	34	0.465	-47
400	0.758	-168	8.78	89.2	0.0288	32	0.331	-51
600	0.763	180	5.94	78	0.0323	35	0.297	-55
800	0.761	169	4.49	68	0.0363	39	0.290	-61
1000	0.764	166	3.61	60	0.0415	41	0.294	-68
1200	0.758	160	3.02	52	0.0467	42	0.310	-75
1400	0.757	155	2.52	44.5	0.0486	45	0.313	-87
1600	0.768	150	2.22	39	0.0566	48	0.311	-92
1800	0.772	145	2	32	0.0655	48	0.328	-97
1900	0.770	142	1.91	28	0.0705	47	0.335	-101
2000	0.772	140	1.81	25	0.0745	47	0.345	-104

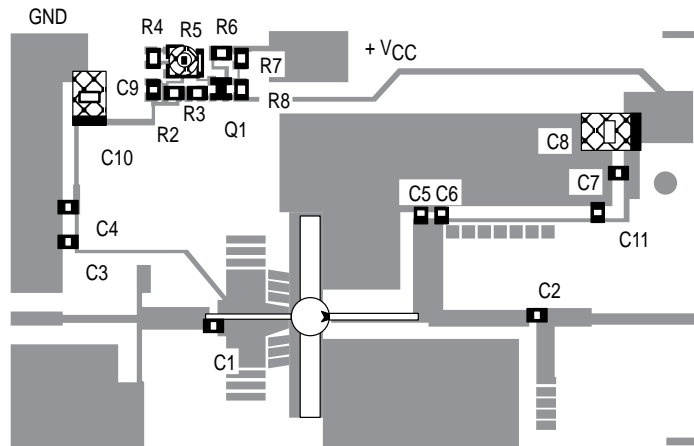
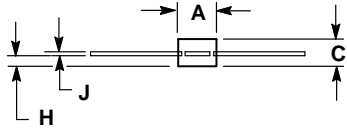
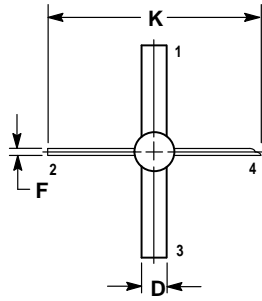


Figure 5. Test Circuit Components Layout

PACKAGE DIMENSIONS




- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.200	0.210	5.08	5.33
C	—	0.125	—	3.17
D	0.120	0.130	3.05	3.30
F	0.025	0.035	0.64	0.88
H	0.035	0.045	0.88	1.14
J	0.004	0.006	0.11	0.15
K	0.970	1.030	24.64	26.16

- STYLE 1:
 PIN 1. EMITTER
 2. BASE
 3. EMITTER
 4. COLLECTOR

**CASE 305C-02
 ISSUE A**

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MRF6401/D

