

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

RF Power transistors designed for applications operating at frequencies between 965 and 1215 MHz. These devices are suitable for use in pulsed applications.

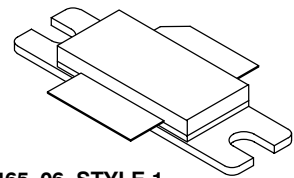
- Typical Pulsed Performance: $V_{DD} = 50$ Volts, $I_{DQ} = 200$ mA, $P_{out} = 500$ Watts Peak (50 W Avg.), $f = 1030$ MHz, Pulse Width = 128 μ sec, Duty Cycle = 10%
Power Gain — 19.7 dB
Drain Efficiency — 62%
- Capable of Handling 10:1 VSWR, @ 50 Vdc, 1030 MHz, 500 Watts Peak Power

Features

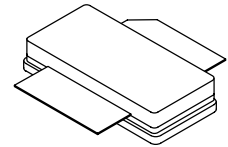
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Qualified Up to a Maximum of 50 V_{DD} Operation
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

MRF6V12500HR3
MRF6V12500HSR3

965 - 1215 MHz, 500 W, 50 V
PULSED
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465-06, STYLE 1
NI-780
MRF6V12500HR3



CASE 465A-06, STYLE 1
NI-780S
MRF6V12500HSR3

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +100	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature	T_J	200	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (1,2)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 500 W Pulsed, 128 μ sec Pulse Width, 10% Duty Cycle	$Z_{\theta JC}$	0.044	°C/W

1. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2 (Minimum)
Machine Model (per EIA/JESD22-A115)	B (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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Off Characteristics

Gate-Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	10	μAdc
Drain-Source Breakdown Voltage ($V_{GS} = 0\text{ Vdc}$, $I_D = 200\text{ mA}$)	$V_{(BR)DSS}$	110	—	—	Vdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 50\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	20	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 90\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	200	μAdc

On Characteristics

Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 1.32\text{ mA}$)	$V_{GS(th)}$	0.9	1.7	2.4	Vdc
Gate Quiescent Voltage ($V_{DD} = 50\text{ Vdc}$, $I_D = 200\text{ mAdc}$, Measured in Functional Test)	$V_{GS(Q)}$	1.7	2.4	3.2	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 3.26\text{ Adc}$)	$V_{DS(on)}$	—	0.25	—	Vdc

Dynamic Characteristics ⁽¹⁾

Reverse Transfer Capacitance ($V_{DS} = 50\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{rss}	—	0.2	—	pF
Output Capacitance ($V_{DS} = 50\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{oss}	—	697	—	pF
Input Capacitance ($V_{DS} = 50\text{ Vdc}$, $V_{GS} = 0\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz)	C_{iss}	—	1391	—	pF

Functional Tests (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 50\text{ Vdc}$, $I_{DQ} = 200\text{ mA}$, $P_{out} = 500\text{ W Peak}$ (50 W Avg.), $f = 1030\text{ MHz}$, Pulsed, 128 μsec Pulse Width, 10% Duty Cycle

Power Gain	G_{ps}	18.5	19.7	22	dB
Drain Efficiency	η_D	58	62	—	%
Input Return Loss	IRL	—	-18	-9	dB

1. Part internally matched both on input and output.

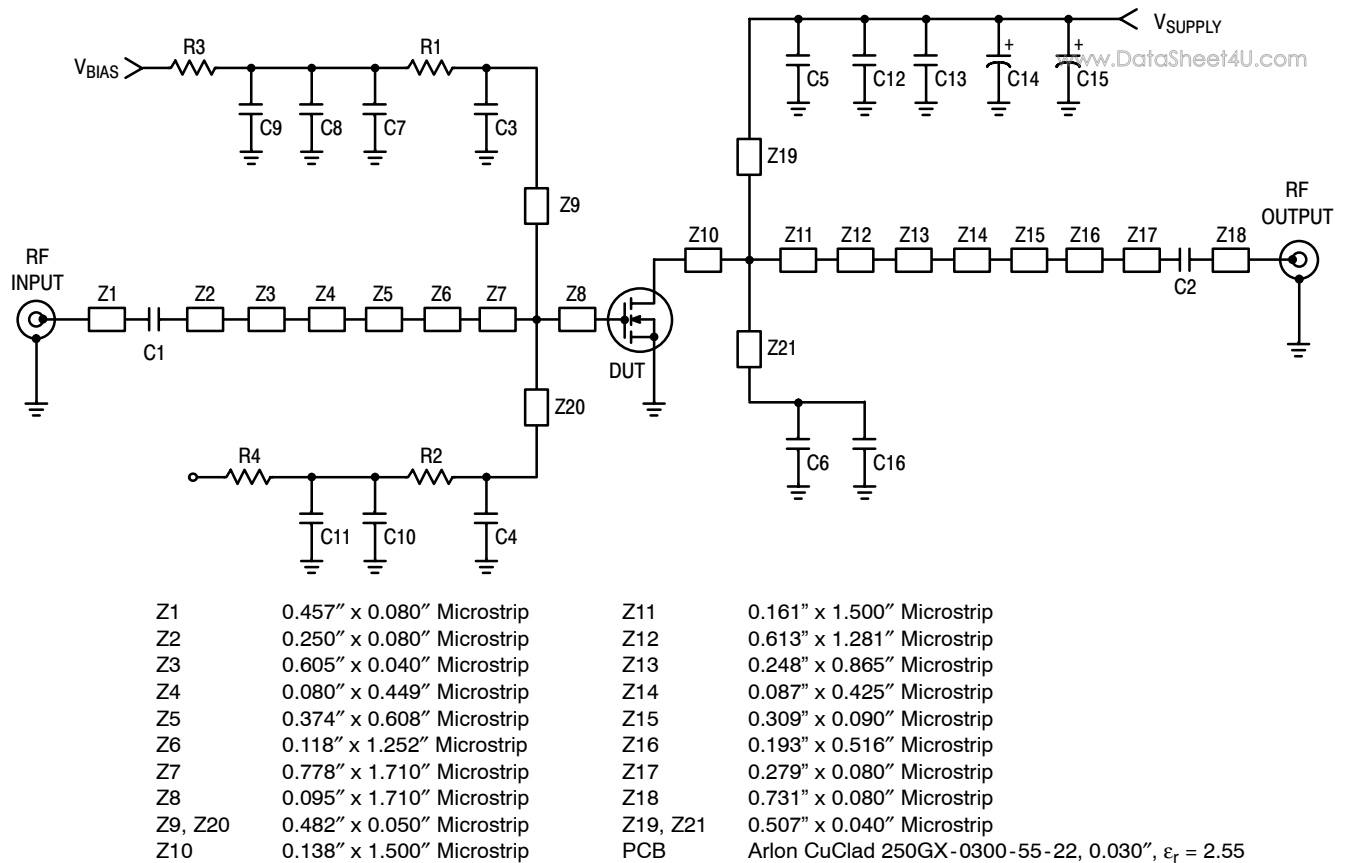


Figure 1. MRF6V12500HR3(HSR3) Test Circuit Schematic

Table 5. MRF6V12500HR3(HSR3) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2	5.1 pF Chip Capacitors	ATC100B5R1CT500XT	ATC
C3, C4, C5, C6	33 pF Chip Capacitors	ATC100B330JT500XT	ATC
C7, C10	10 μ F, 50 V Chip Capacitors	GRM55DR61H106KA88L	Murata
C8, C11, C13, C16	2.2 μ F, 100 V Chip Capacitors	2225X7R225KT3AB	ATC
C9	22 μ F, 25 V Chip Capacitor	TPSD226M025R0200	AVX
C12	1 μ F, 100 V Chip Capacitor	GRM31CR72A105KA01L	Murata
C14, C15	470 μ F, 63 V Electrolytic Capacitors	MCGPR63V477M13X26 - RH	Multicomp
R1, R2	56 Ω , 1/4 W Chip Resistors	CRCW120656R0FKEA	Vishay
R3, R4	0 Ω , 3 A Chip Resistors	CRCW12060000Z0EA	Vishay

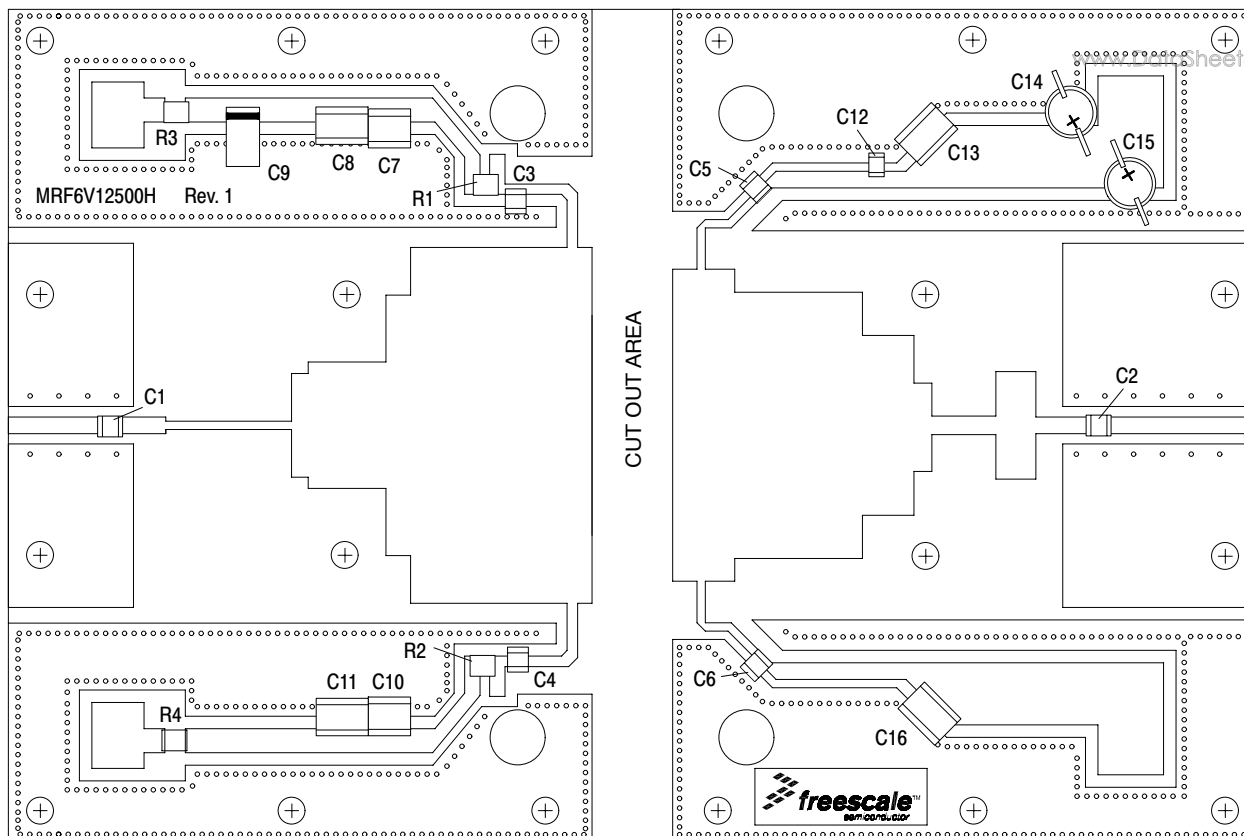


Figure 2. MRF6V12500HR3(HSR3) Test Circuit Component Layout

TYPICAL CHARACTERISTICS

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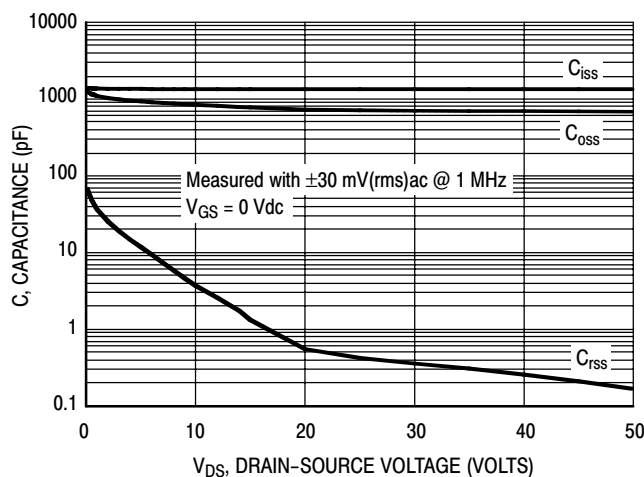


Figure 3. Capacitance versus Drain-Source Voltage

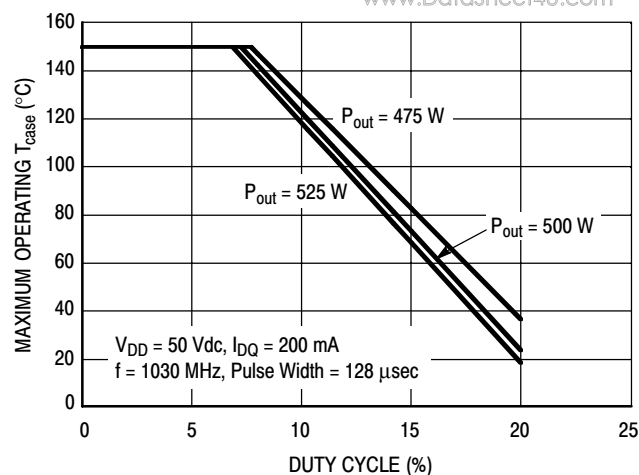


Figure 4. Safe Operating Area

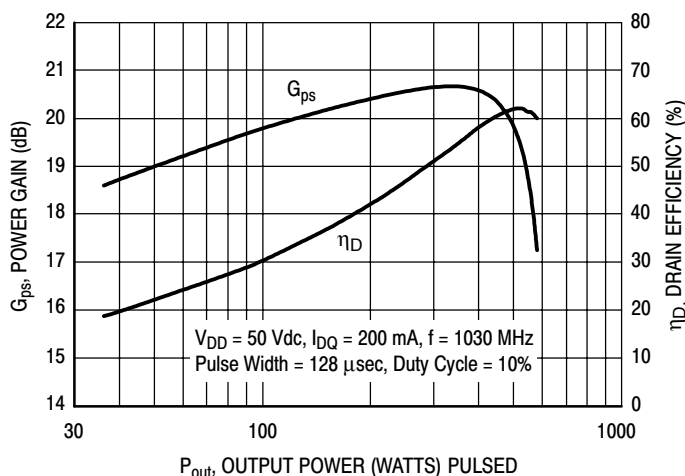


Figure 5. Pulsed Power Gain and Drain Efficiency versus Output Power

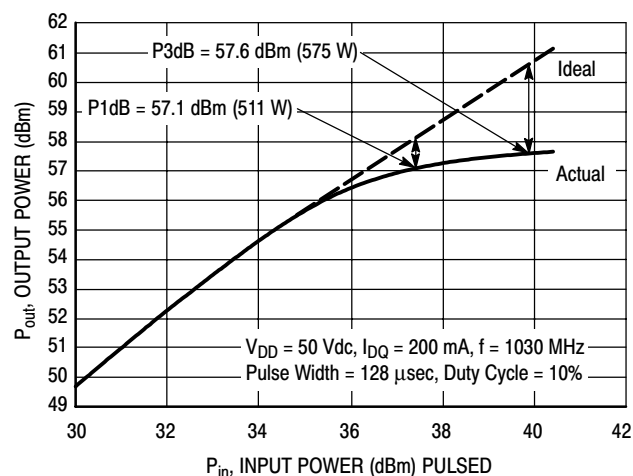


Figure 6. Pulsed Output Power versus Input Power

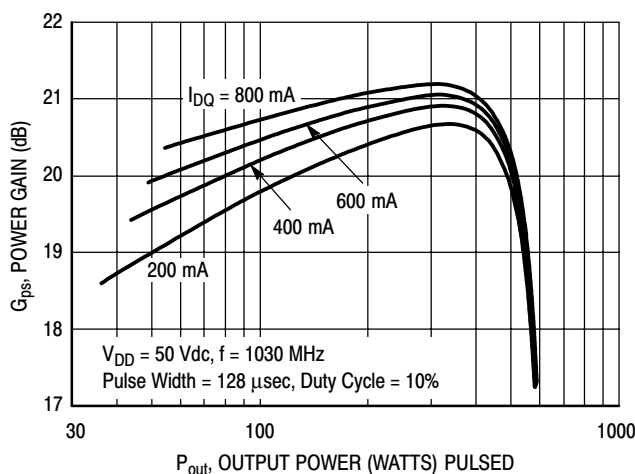


Figure 7. Pulsed Power Gain versus Output Power

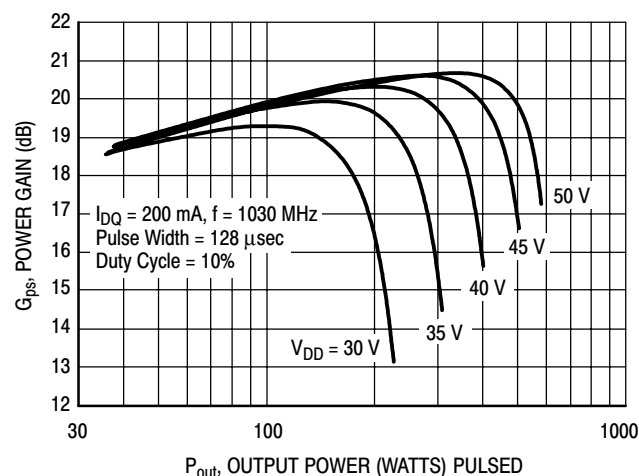


Figure 8. Pulsed Power Gain versus Output Power

TYPICAL CHARACTERISTICS

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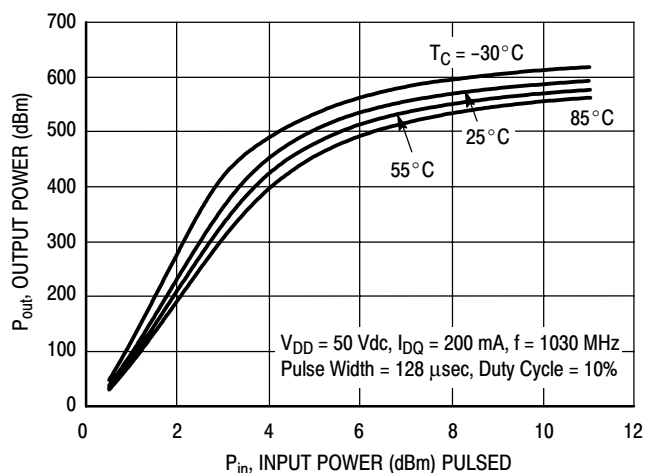


Figure 9. Pulsed Output Power versus Input Power

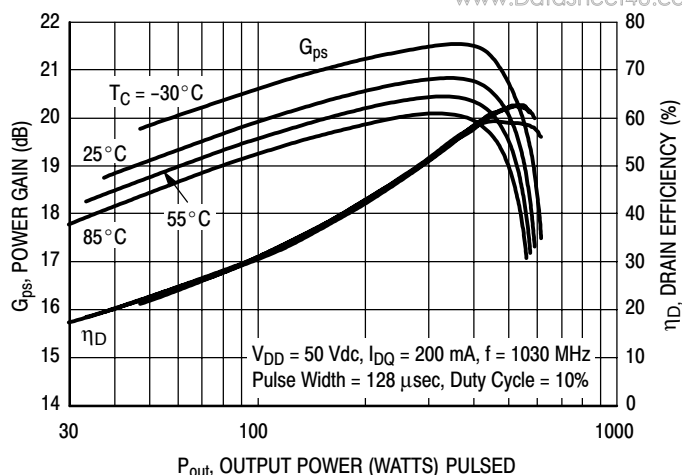
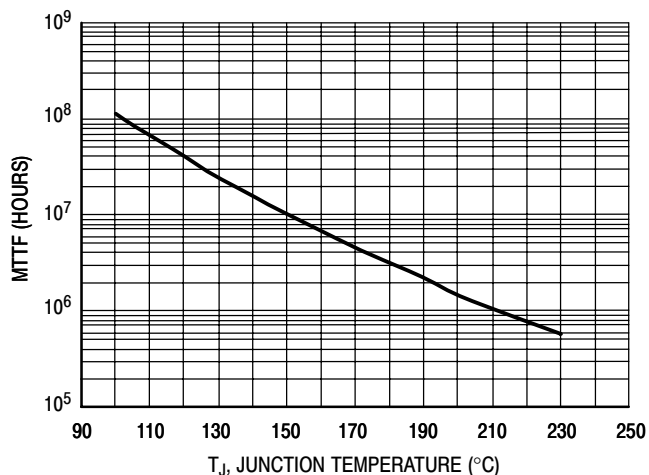


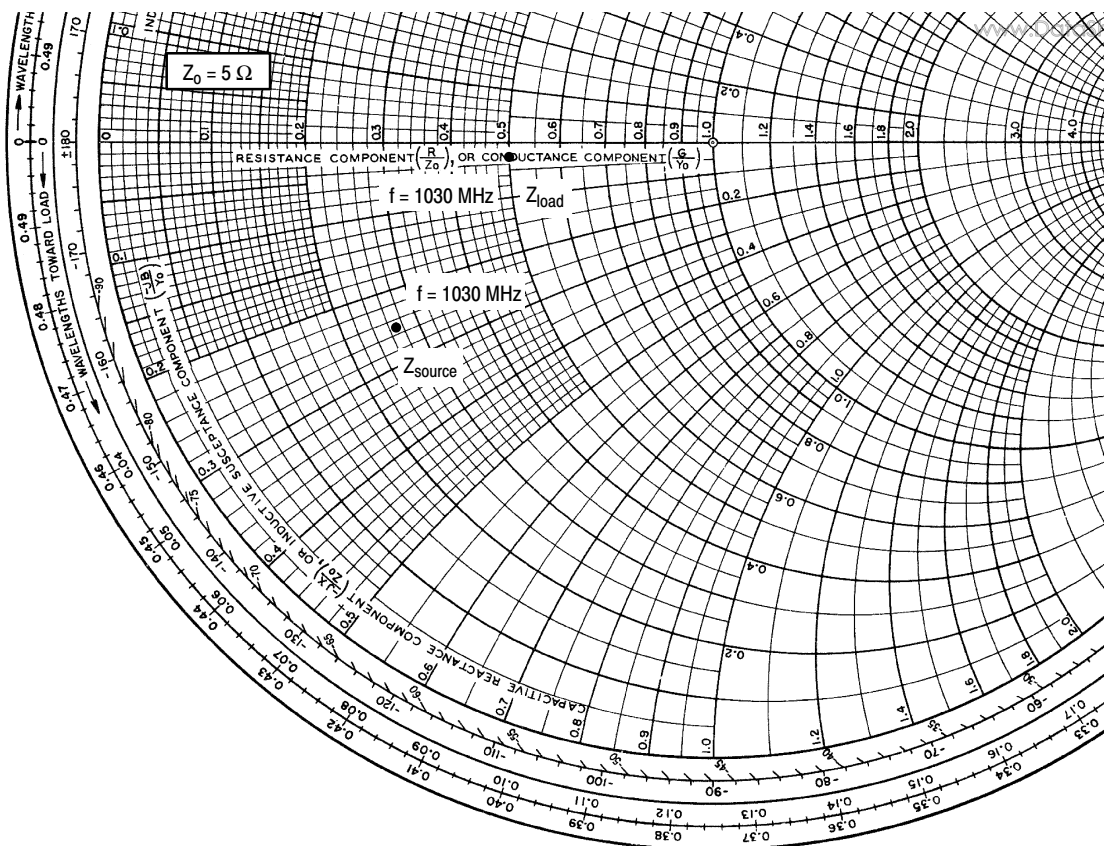
Figure 10. Pulsed Power Gain and Drain Efficiency versus Output Power



This above graph displays calculated MTTF in hours when the device is operated at $V_{DD} = 50$ Vdc, $P_{out} = 500$ W Peak, Pulse Width = 128 μ sec, Duty Cycle = 10%, and $\eta_D = 62\%$.

MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 11. MTTF versus Junction Temperature



$V_{DD} = 50 \text{ Vdc}$, $I_{DQ} = 200 \text{ mA}$, $P_{out} = 500 \text{ W Peak}$

f MHz	Z_{source} Ω	Z_{load} Ω
1030	1.36 - j1.27	2.50 - j0.17

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

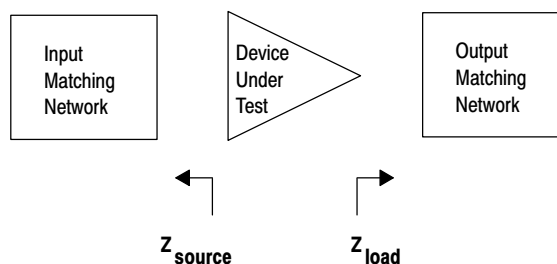
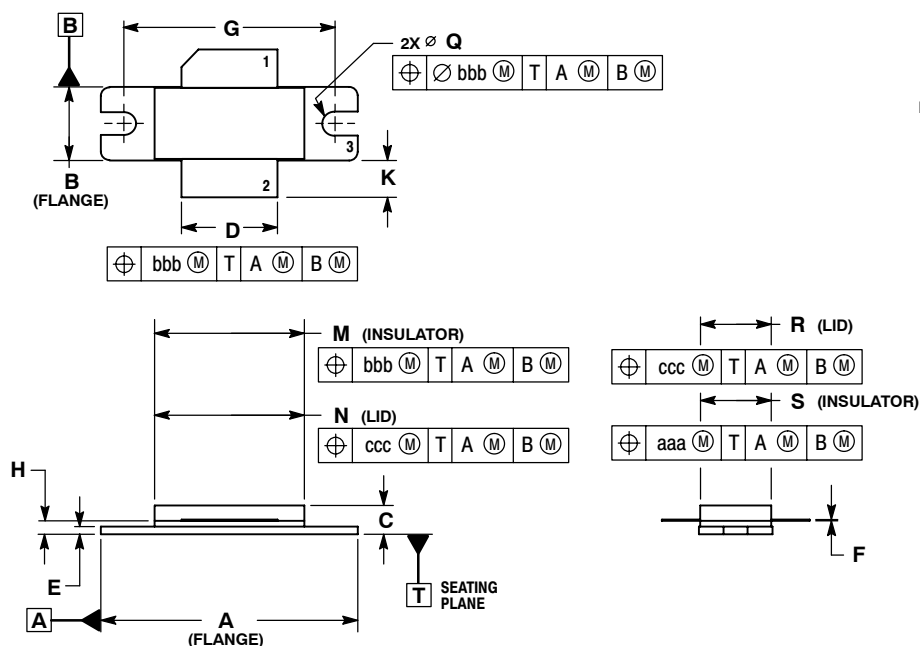


Figure 12. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS

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NOTES:

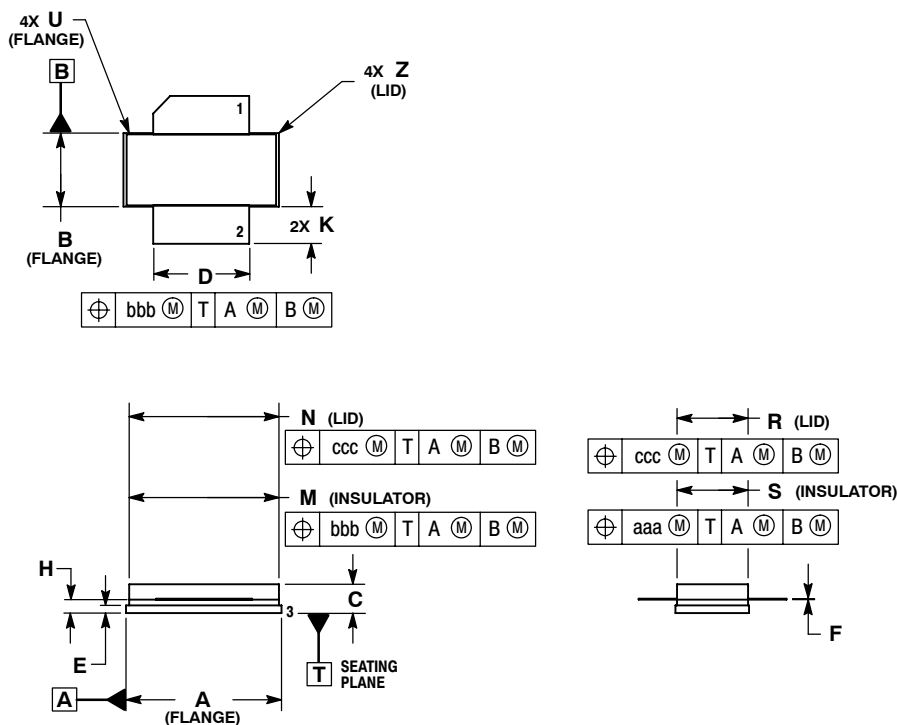
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.66	19.96
N	0.772	0.788	19.60	20.00
Q	Ø.118	Ø.138	Ø3.00	Ø3.51
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:

- PIN 1. DRAIN
- GATE
- SOURCE

CASE 465-06
ISSUE G
NI-780
MRF6V12500HR3



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.805	0.815	20.45	20.70
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.61	20.02
N	0.772	0.788	19.61	20.02
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
U	---	0.040	---	1.02
Z	---	0.030	---	0.76
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:

- PIN 1. DRAIN
- GATE
- SOURCE

CASE 465A-06
ISSUE H
NI-780S
MRF6V12500HSR3

MRF6V12500HR3 MRF6V12500HSR3

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RF Device Data
 Freescale Semiconductor

PRODUCT DOCUMENTATION, TOOLS AND SOFTWARE

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Refer to the following documents, tools and software to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator

For Software and Tools, do a Part Number search at <http://www.freescale.com>, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Sept. 2009	• Initial Release of Data Sheet

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