

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

RF Power transistors designed for applications operating at frequencies between 1200 and 1400 MHz, 1% to 12% duty cycle. These devices are suitable for use in pulsed applications.

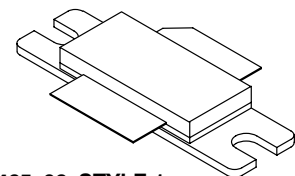
- Typical Pulsed Performance: $V_{DD} = 50$ Volts, $I_{DQ} = 150$ mA, $P_{out} = 330$ Watts Peak (39.6 W Avg.), $f = 1400$ MHz, Pulse Width = 300 μ sec, Duty Cycle = 12%
Power Gain — 18 dB
Drain Efficiency — 60.5%
- Capable of Handling 5:1 VSWR, @ 50 Vdc, 1400 MHz, 330 Watts Peak Power

Features

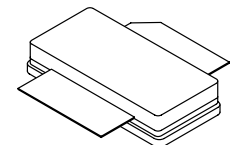
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Qualified Up to a Maximum of 50 V_{DD} Operation
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

MRF6V14300HR3
MRF6V14300HSR3

1400 MHz, 330 W, 50 V
PULSED
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465-06, STYLE 1
NI-780
MRF6V14300HR3



CASE 465A-06, STYLE 1
NI-780S
MRF6V14300HSR3

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +100	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature	T_J	200	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (1,2)	Unit
Thermal Resistance, Junction to Case Case Temperature 65°C, 330 W Pulsed, 300 μ sec Pulse Width, 12% Duty Cycle	$R_{\theta JC}$	0.13	°C/W

1. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1C (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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Off Characteristics

Gate-Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	10	μAdc
Drain-Source Breakdown Voltage ($V_{GS} = 0\text{ Vdc}$, $I_D = 100\text{ mA}$)	$V_{(BR)DSS}$	100	—	—	Vdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 50\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	50	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 90\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	2.5	mA

On Characteristics

Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 662\text{ }\mu\text{Adc}$)	$V_{GS(th)}$	0.9	1.6	2.4	Vdc
Gate Quiescent Voltage ($V_{DD} = 50\text{ Vdc}$, $I_D = 150\text{ mAdc}$, Measured in Functional Test)	$V_{GS(Q)}$	1.5	2.4	3	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 1.63\text{ Adc}$)	$V_{DS(on)}$	—	0.26	—	Vdc

Dynamic Characteristics ⁽¹⁾

Reverse Transfer Capacitance ($V_{DS} = 50\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{rss}	—	0.6	—	pF
Output Capacitance ($V_{DS} = 50\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{oss}	—	350	—	pF
Input Capacitance ($V_{DS} = 50\text{ Vdc}$, $V_{GS} = 0\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz)	C_{iss}	—	330	—	pF

Functional Tests (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 50\text{ Vdc}$, $I_{DQ} = 150\text{ mA}$, $P_{out} = 330\text{ W Peak}$ (39.6 W Avg.), $f = 1400\text{ MHz}$, Pulsed, 300 μsec Pulse Width, 12% Duty Cycle

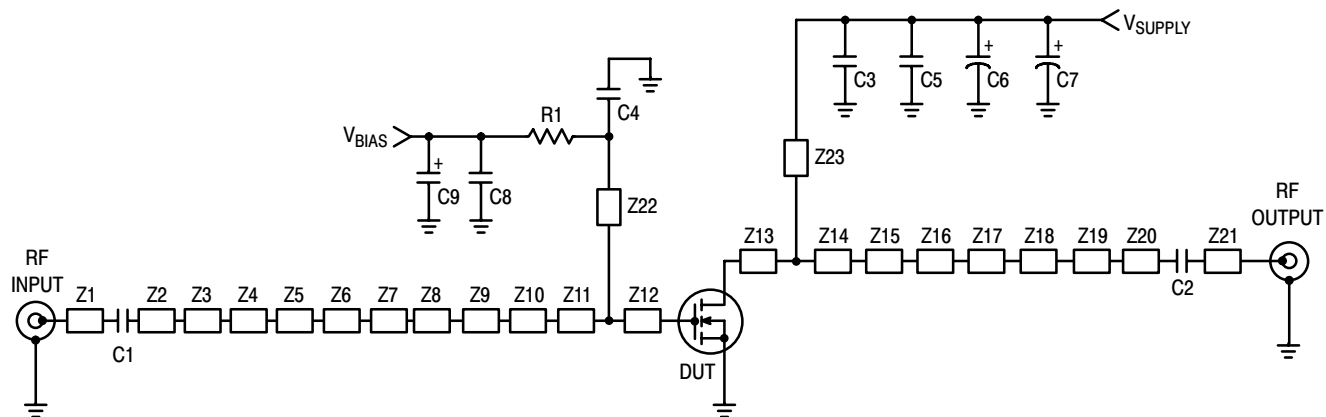
Power Gain	G_{ps}	16.5	18	19.5	dB
Drain Efficiency	η_D	59 ⁽²⁾	60.5 ⁽²⁾	—	%
Input Return Loss	IRL	—	-12	-9	dB

Pulsed RF Performance (In Freescale Application Test Fixture, 50 ohm system) $V_{DD} = 50\text{ Vdc}$, $I_{DQ} = 150\text{ mA}$, $P_{out} = 330\text{ W Peak}$ (39.6 W Avg.), $f_1 = 1200\text{ MHz}$, $f_2 = 1300\text{ MHz}$ and $f_3 = 1400\text{ MHz}$, Pulsed, 300 μsec Pulse Width, 12% Duty Cycle, $t_r = 50\text{ ns}$

Relative Insertion Phase	$ \Delta\Phi $	—	10	—	°
Gain Flatness	G_F	—	0.5	—	dB
Pulse Amplitude Droop	D_{rp}	—	0.3	—	dB
Harmonic 2nd and 3rd	H2 & H3	—	-20	—	dBc
Spurious Response		—	-65	—	dBc
Load Mismatch Stability (VSWR = 3:1 at all Phase Angles)	VSWR-S	All Spurs Below -60 dBc			
Load Mismatch Tolerance (VSWR = 5:1 at all Phase Angles)	VSWR-T	No Degradation in Output Power			

1. Part internally matched both on input and output.

2. Drain efficiency is calculated by: $\eta_D = \frac{100 \times P_{out}}{V_{DD} \times I_{peak}}$ where: $I_{peak} = (I_{AVG} - I_{DQ}) / \text{Duty Cycle (\%)} + I_{DQ}$.



Z1	0.205" x 0.080" Microstrip	Z13	0.110" x 0.866" Microstrip
Z2	0.721" x 0.022" Microstrip	Z14	0.630" x 0.866" Microstrip
Z3	0.080" x 0.104" Microstrip	Z15	0.307" x 0.470" Microstrip
Z4	0.128" x 0.022" Microstrip	Z16	0.045" x 0.221" Microstrip
Z5	0.062" x 0.134" Microstrip	Z17	0.171" x 0.136" Microstrip
Z6	0.440" x 0.022" Microstrip	Z18	0.120" x 0.430" Microstrip
Z7	0.262" x 0.496" Microstrip	Z19	0.964" x 0.136" Microstrip
Z8	0.030" x 0.138" Microstrip	Z20	0.177" x 0.078" Microstrip
Z9	0.256" x 0.028" Microstrip	Z21	0.215" x 0.078" Microstrip
Z10	0.058" x 0.254" Microstrip	Z22	1.577" x 0.070" Microstrip
Z11	0.344" x 0.087" Microstrip	Z23	1.459" x 0.070" Microstrip
Z12	0.110" x 0.087" Microstrip	PCB	Arlon CuClad 250GX-0300-55-22, 0.030", $\epsilon_r = 2.55$

Figure 1. MRF6V14300HR3(HSR3) Test Circuit Schematic

Table 5. MRF6V14300HR3(HSR3) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	43 pF Chip Capacitor	ATC100B430JT500XT	ATC
C2	18 pF Chip Capacitor	ATC100B180JT500XT	ATC
C3	33 pF Chip Capacitor	ATC100B330JT500XT	ATC
C4	27 pF Chip Capacitor	ATC100B270JT500XT	ATC
C5	2.2 μ F, 100 V Chip Capacitor	2225X7R225KT3AB	ATC
C6	470 μ F, 63 V Electrolytic Capacitor	EMVY630GTR471MMH0S	Multicomp
C7	330 pF, 63 V Electrolytic Capacitor	EMVY630GTR331MMH0S	Multicomp
C8	0.1 μ F, 35 V Chip Capacitor	CDR33BX104AKYS	Kemet
C9	10 μ F, 35 V Tantalum Capacitor	T491D106K035AT	Kemet
R1	10 Ω , 1/4 W Chip Resistor	CRCW120610R0FKEA	Vishay

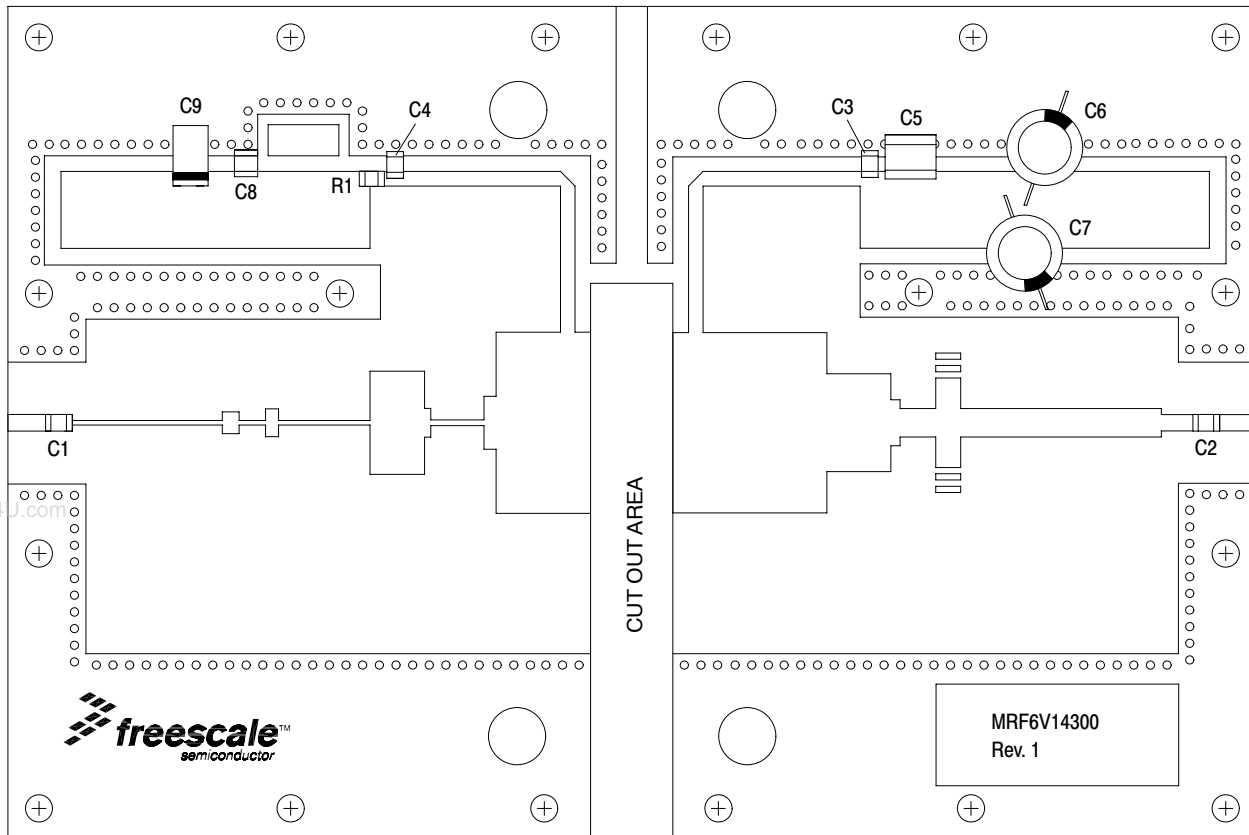


Figure 2. MRF6V14300HR3(HSR3) Test Circuit Component Layout

TYPICAL CHARACTERISTICS

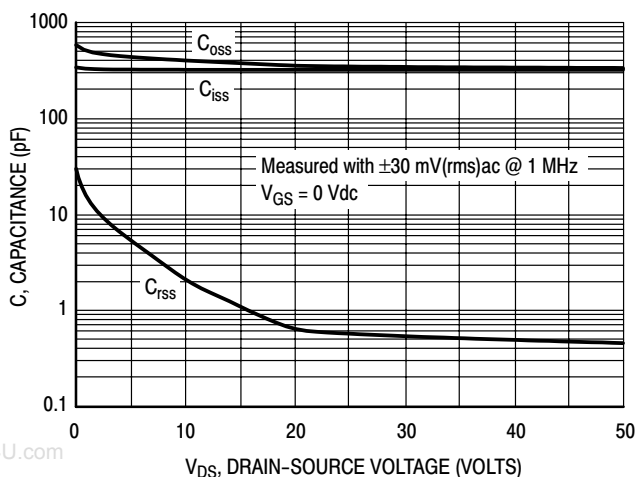


Figure 3. Capacitance versus Drain-Source Voltage

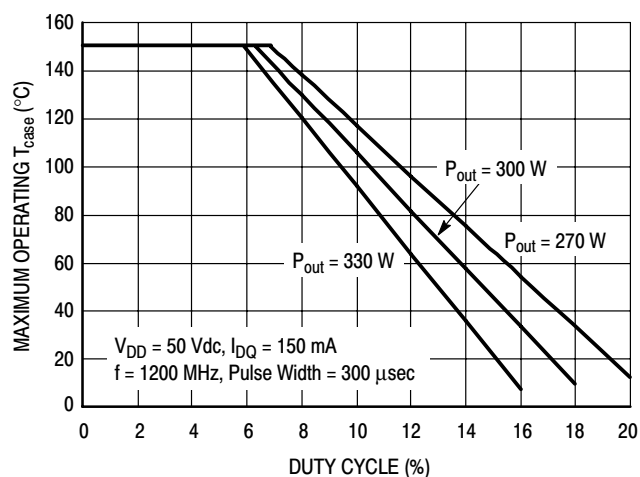


Figure 4. Safe Operating Area

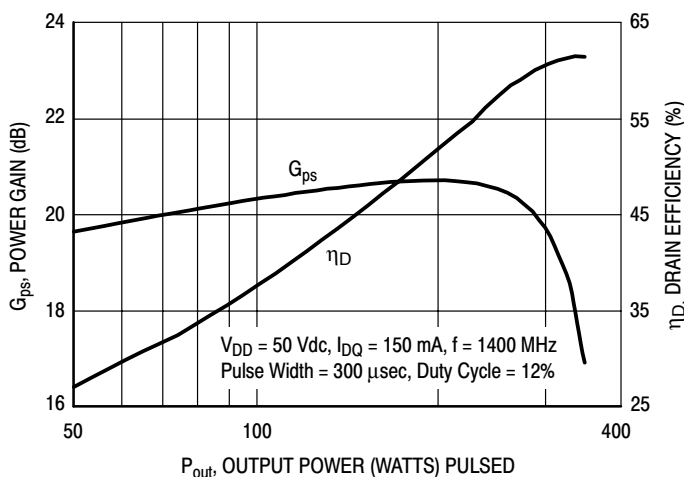


Figure 5. Pulsed Power Gain and Drain Efficiency versus Output Power

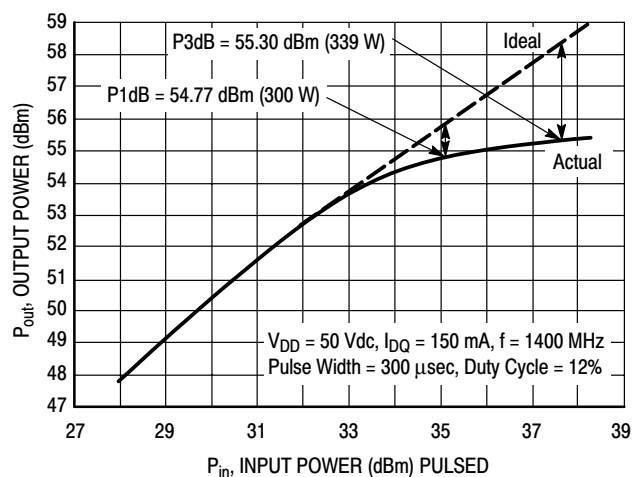


Figure 6. Pulsed Output Power versus Input Power

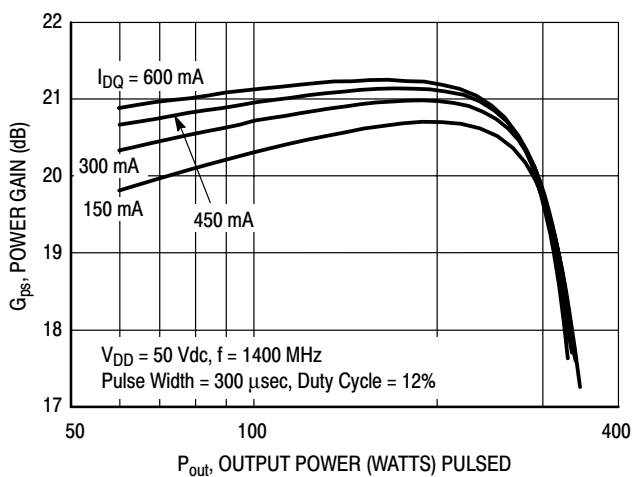


Figure 7. Pulsed Power Gain versus Output Power

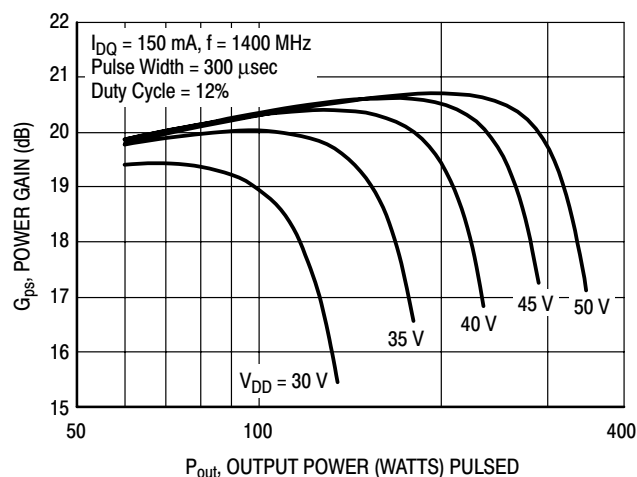


Figure 8. Pulsed Power Gain versus Output Power

TYPICAL CHARACTERISTICS

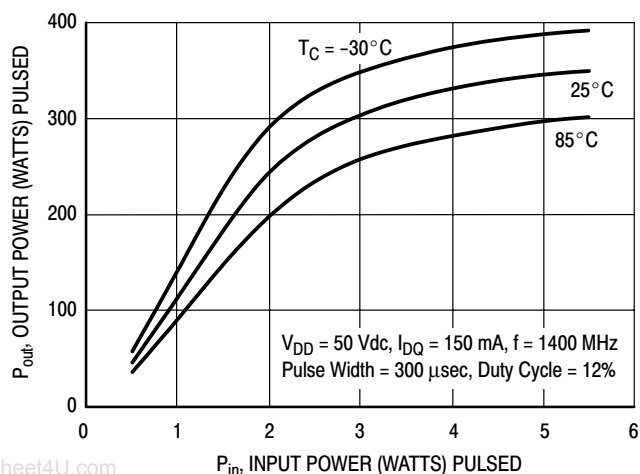


Figure 9. Pulsed Output Power versus Input Power

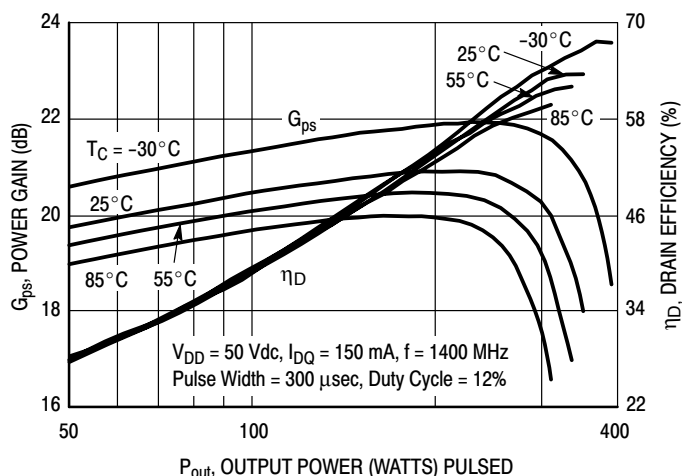


Figure 10. Pulsed Power Gain and Drain Efficiency versus Output Power

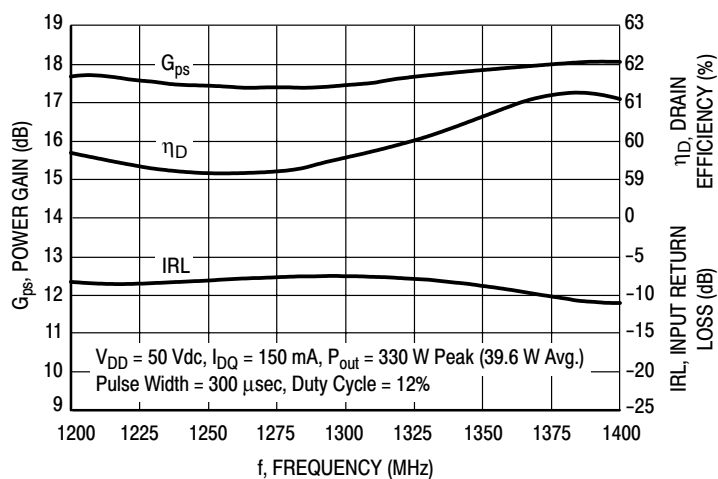
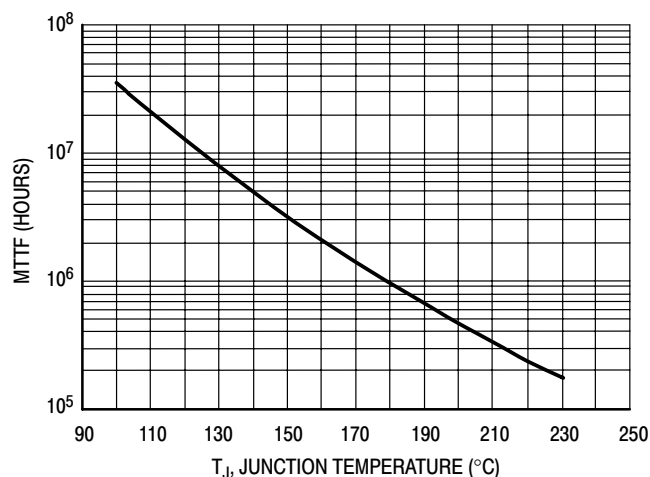


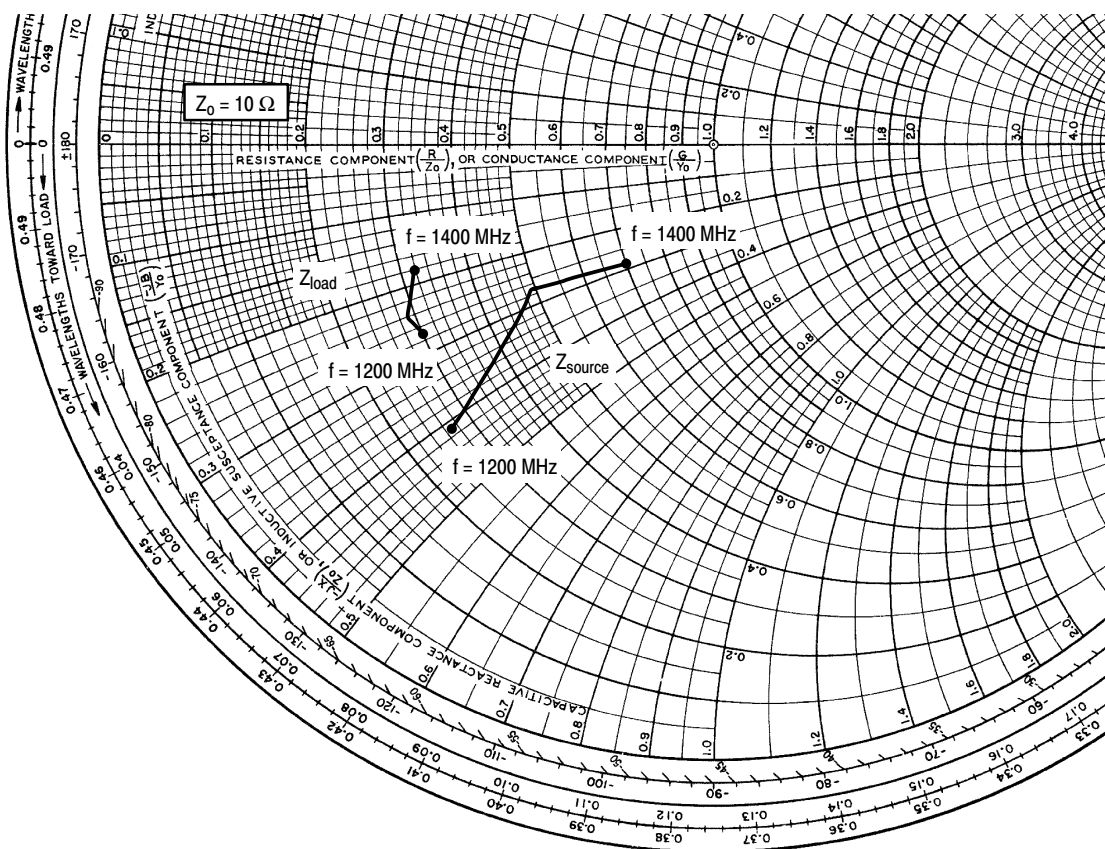
Figure 11. Broadband Performance @ $P_{out} = 330$ Watts Peak



This above graph displays calculated MTTF in hours when the device is operated at $V_{DD} = 50$ Vdc, $P_{out} = 330$ W Peak, Pulse Width = 300 μ sec, Duty Cycle = 12%, and $\eta_D = 60.5\%$.

MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 12. MTTF versus Junction Temperature



$V_{DD} = 50 \text{ Vdc}$, $I_{DQ} = 150 \text{ mA}$, $P_{out} = 330 \text{ W Peak}$

f MHz	Z_{source} Ω	Z_{load} Ω
1200	$2.70 - j4.10$	$2.97 - j2.66$
1300	$4.93 - j2.66$	$2.85 - j2.40$
1400	$7.01 - j2.87$	$3.17 - j1.78$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

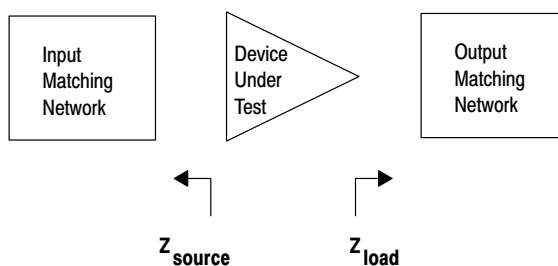
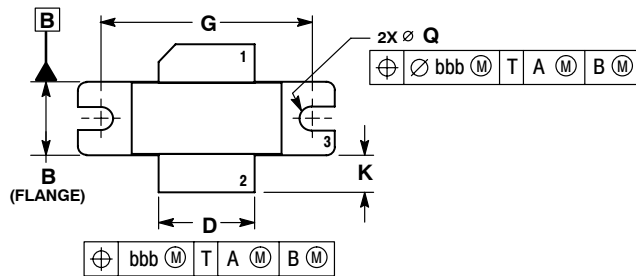


Figure 13. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS



NOTES:

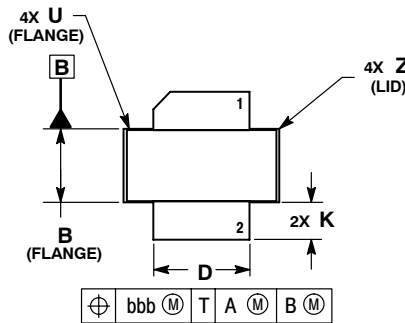
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100	BSC	27.94	BSC
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.66	19.96
N	0.772	0.788	19.60	20.00
Q	Ø 0.118	Ø 0.138	Ø 3.00	Ø 3.51
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
aaa	0.005	REF	0.127	REF
bbb	0.010	REF	0.254	REF
ccc	0.015	REF	0.381	REF

STYLE 1:

- PIN 1. DRAIN
- GATE
- SOURCE

CASE 465-06
ISSUE G
NI-780
MRF6V14300HR3



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.805	0.815	20.45	20.70
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.61	20.02
N	0.772	0.788	19.61	20.02
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
U	---	0.040	---	1.02
Z	---	0.030	---	0.76
aaa	0.005	REF	0.127	REF
bbb	0.010	REF	0.254	REF
ccc	0.015	REF	0.381	REF

STYLE 1:

- PIN 1. DRAIN
- GATE
- SOURCE

CASE 465A-06
ISSUE H
NI-780S
MRF6V14300HSR3

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Sept. 2008	• Initial Release of Data Sheet
1	Oct. 2008	• Added footnote to describe the formula used to calculate values for Min and Typ Drain Efficiency in the Functional Test table, p. 2 • Updated Fig. 4, Safe Operating Area, to show additional curves for 270 W and 300 W output power, p. 5 • Added Fig. 12, MTTF versus Junction Temperature, p. 6
2	Nov. 2008	• Changed “multiply by” symbol to “divide by” symbol in the Functional Test Drain Efficiency formula footnote, p. 2

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