Freescale Semiconductor
Technical Data

Document Number: MRF7S19080H
Rev. 0, 1/2007

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

MRF7S19080HR3
MRF7S19080HSR3

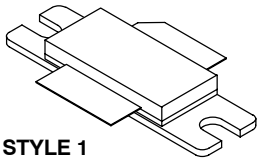
1930-1990 MHz, 24 W AVG., 28 V
SINGLE W-CDMA
LATERAL N-CHANNEL
RF POWER MOSFETs

Designed for CDMA base station applications with frequencies from 1930 to 1990 MHz. Suitable for CDMA and multicarrier amplifier applications. To be used in Class AB and Class C for TD-SCDMA and PCN-PCS/cellular radio applications.

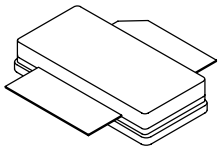
- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQ} = 750 mA, P_{out} = 24 Watts Avg., Full Frequency Band, 3GPP Test Model 1, 64 DPCH with 50% Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.
  Power Gain — 18 dB
  Drain Efficiency — 32%
  Device Output Signal PAR — 6.2 dB @ 0.01% Probability on CCDF
  ACPR @ 5 MHz Offset — -38 dBc in 3.84 MHz Channel Bandwidth
- Capable of Handling 10:1 VSWR, @ 32 Vdc, 1960 MHz, 80 Watts CW Peak Tuned Output Power
- P_{out} @ 1 dB Compression Point ≥ 80 Watts CW

Features

- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.



CASE 465-06, STYLE 1
NI-780
MRF7S19080HR3



CASE 465A-06, STYLE 1
NI-780S
MRF7S19080HSR3

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 81°C, 79 W CW Case Temperature 79°C, 24 W CW	$R_{\theta JC}$	 0.60 0.69	°C/W

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Tools/Software/Application Software/Calculators to access the MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

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Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1C (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Electrical Characteristics (T_C = 25°C unless otherwise noted)

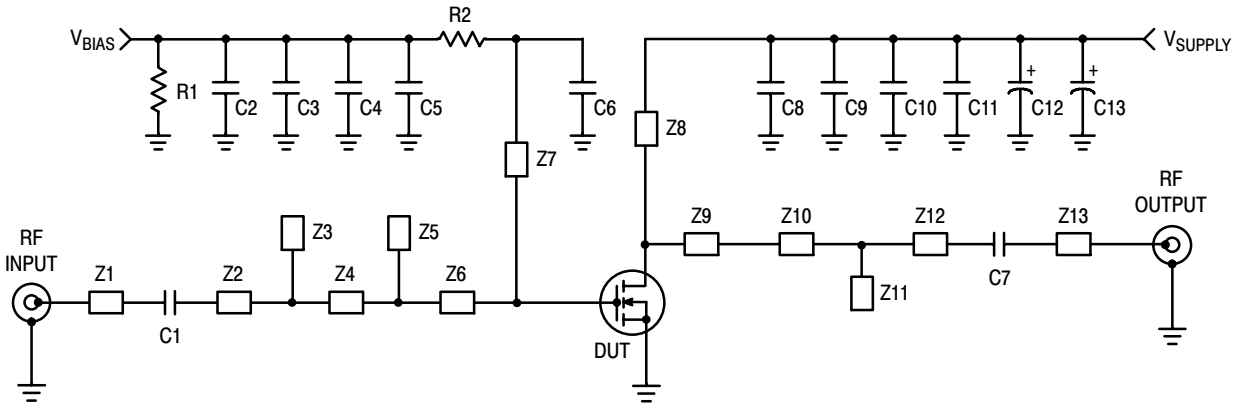
Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 174 μAdc)	$V_{GS(th)}$	1.2	2	2.7	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_D = 750 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	2	2.7	3.8	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.74 Adc)	$V_{DS(on)}$	0.1	0.21	0.3	Vdc
Dynamic Characteristics (1)					
Reverse Transfer Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	0.64	—	pF
Output Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	297	—	pF
Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 750 mA, P_{out} = 24 W Avg., f = 1932.5 MHz and f = 1987.5 MHz, Single-Carrier W-CDMA, 3GPP Test Model 1, 64 DPCH, 50% Clipping, PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	17	18	20	dB
Drain Efficiency	η_D	30	32	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	5.7	6.2	—	dB
Adjacent Channel Power Ratio	ACPR	—	-38	-35	dBc
Input Return Loss	IRL	—	-20	-9	dB

1. Part internally matched both on input and output.

(continued)

Table 4. Electrical Characteristics (T_C = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 750 mA, 1930 - 1990 MHz Bandwidth					
Video Bandwidth @ 80 W PEP P_{out} where IM3 = -30 dBc (Tone Spacing from 100 kHz to VBW) ΔIMD3 = IMD3 @ VBW frequency - IMD3 @ 100 kHz <1 dBc (both sidebands)	VBW	—	90	—	MHz
Gain Flatness in 60 MHz Bandwidth @ P_{out} = 24 W Avg.	G_F	—	0.165	—	dB
Average Deviation from Linear Phase in 60 MHz Bandwidth @ P_{out} = 80 W CW	Φ	—	1.14	—	°
Average Group Delay @ P_{out} = 80 W CW, f = 1960 MHz	Delay	—	2.25	—	ns
Part - to - Part Insertion Phase Variation @ P_{out} = 80 W CW, f = 1960 MHz, Six Sigma Window	ΔΦ	—	22.3	—	°
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.009	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	ΔP1dB	—	0.017	—	dBm/°C



Z1	0.530″ x 0.084″ Microstrip	Z8	0.306″ x 0.388″ x 0.090″ Taper
Z2	0.336″ x 0.084″ Microstrip	Z9	0.880″ x 0.201″ x 0.795″ Taper
Z3	0.211″ x 0.180″ x 0.084″ Taper	Z10	0.415″ x 0.084″ Microstrip
Z4	0.704″ x 0.216″ Microstrip	Z11	0.191″ x 0.243″ x 0.084″ Taper
Z5	0.220″ x 0.216″ x 0.084″ Taper	Z12	0.510″ x 0.084″ Microstrip
Z6	0.504″ x 0.800″ x 0.084″ Taper	Z13	0.525″ x 0.084″ Microstrip
Z7	0.265″ x 0.313″ x 0.332″ x 0.040″ Taper	PCB	Arlon, GX-0300-55-22, 0.030″, ε_r = 2.55

Figure 1. MRF7S19080HR3(HSR3) Test Circuit Schematic

Table 5. MRF7S19080HR3(HSR3) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C7	15 pF Chip Capacitors	ATC100B150JT500XT	ATC
C2, C11	13 pF Chip Capacitors	ATC100B130JT500XT	ATC
C3	10 μF Chip Capacitor	GRM31MF51A106ZA01B	TDK
C4	1000 pF Chip Capacitor	ATC100B102JT50XT	ATC
C5, C10	0.1 μF Chip Capacitors	C1206C104K5RAC	Kemet
C6	5.1 pF Chip Capacitor	ATC100B5R1CT500XT	ATC
C8	6.8 pF Chip Capacitor	ATC100B6R8CT500XT	ATC
C9	2.2 μF Chip Capacitor	C1825C225J5RAC	Kemet
C12	470 μF, 63 V Electrolytic Capacitor	MCR63V477M13X26	Multicomp
C13	100 μF, 50 V Electrolytic Capacitor	MCR50V107M8X11	Multicomp
R1	330 Ω, 1/4 W Chip Resistor	CRCW12063300FKTA	Vishay
R2	10 Ω, 1/4 W Chip Resistor	CRCW120610R0FKTA	Vishay

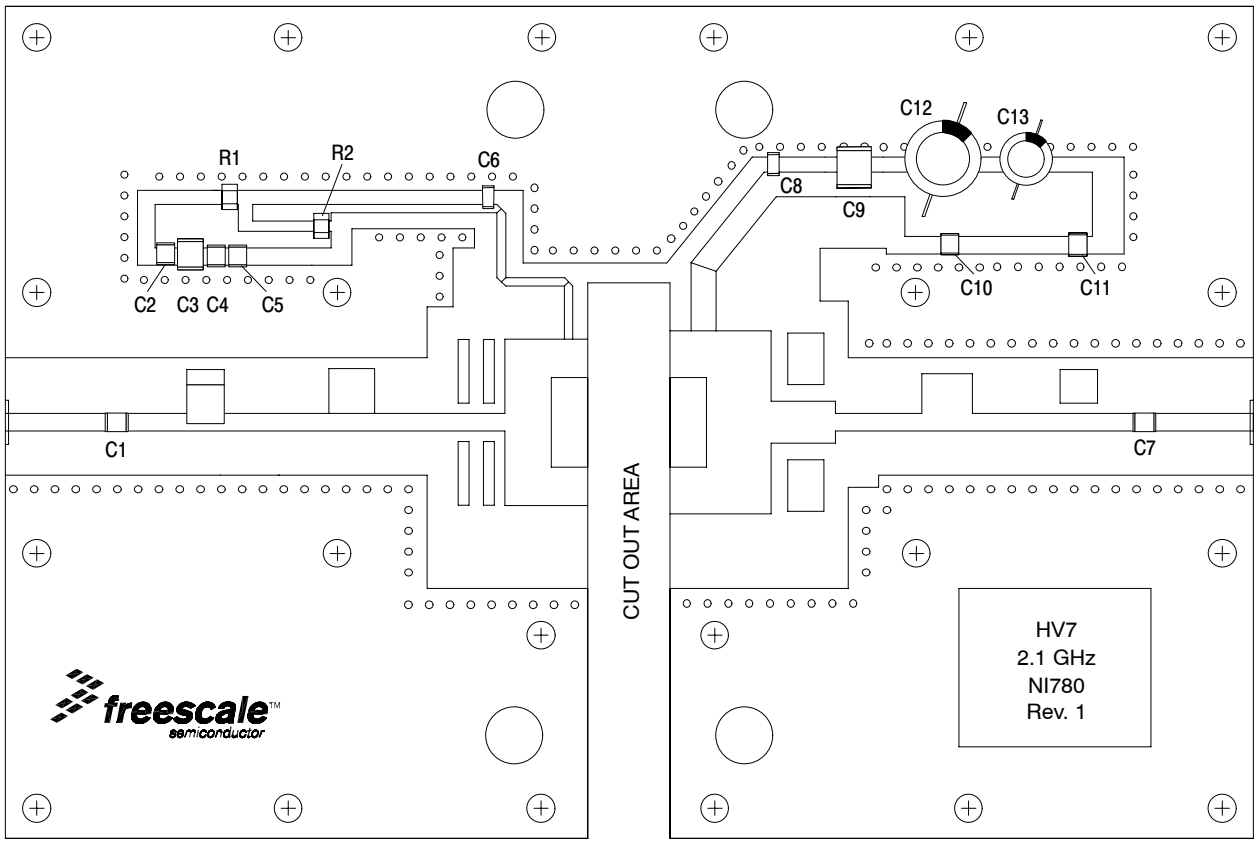


Figure 2. MRF7S19080HR3(HSR3) Test Circuit Component Layout

TYPICAL CHARACTERISTICS

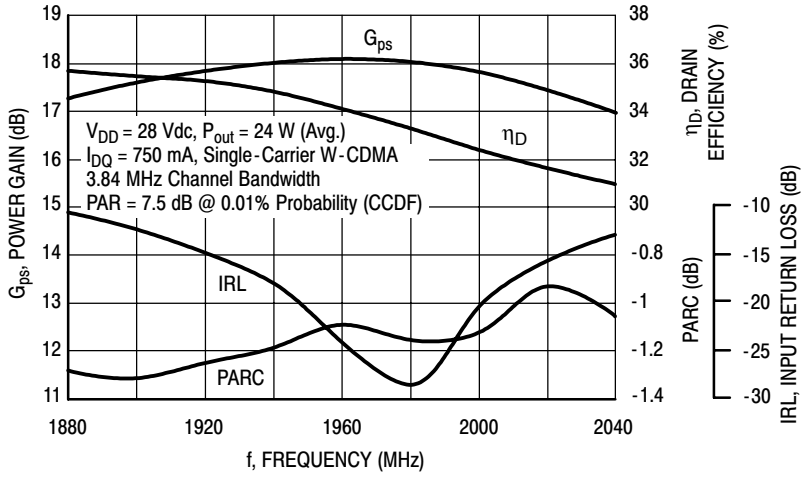


Figure 3. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 24 Watts Avg.

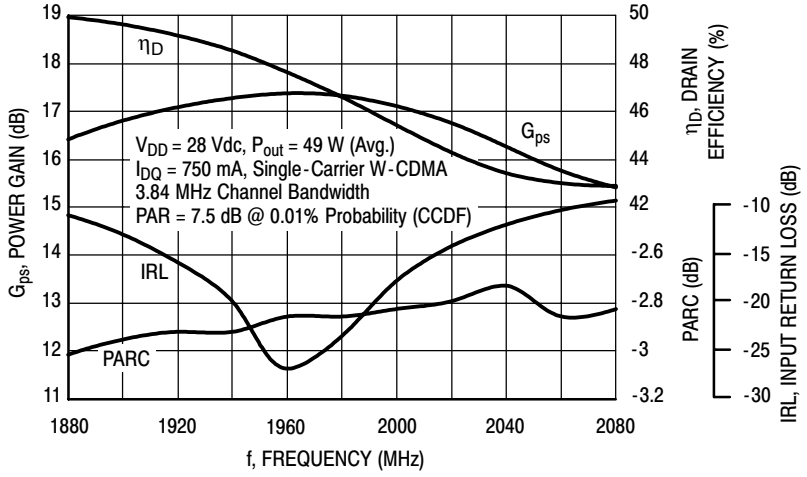


Figure 4. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 49 Watts Avg.

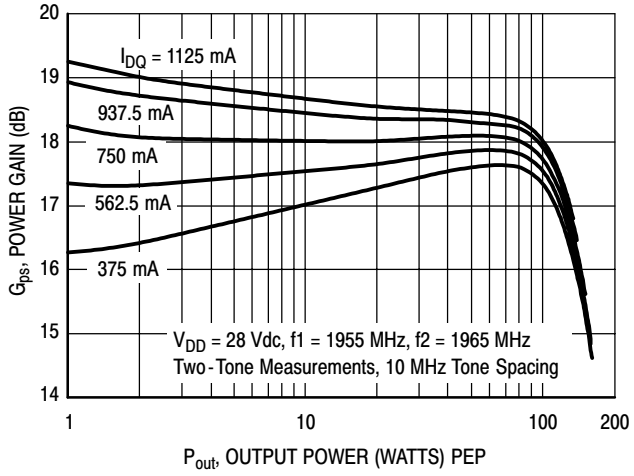


Figure 5. Two-Tone Power Gain versus Output Power

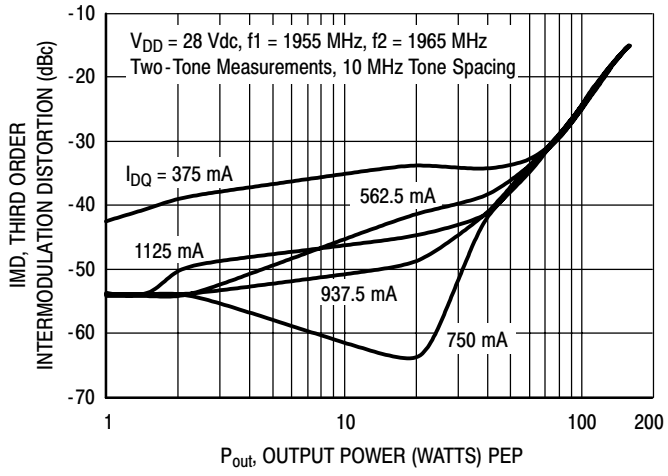


Figure 6. Third Order Intermodulation Distortion versus Output Power

TYPICAL CHARACTERISTICS

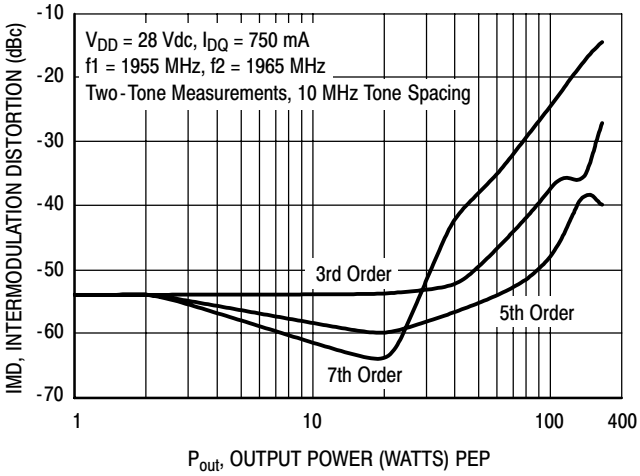


Figure 7. Intermodulation Distortion Products versus Output Power

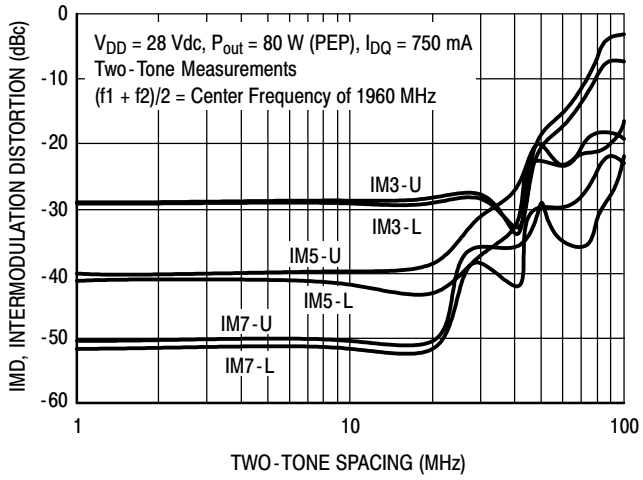


Figure 8. Intermodulation Distortion Products versus Tone Spacing

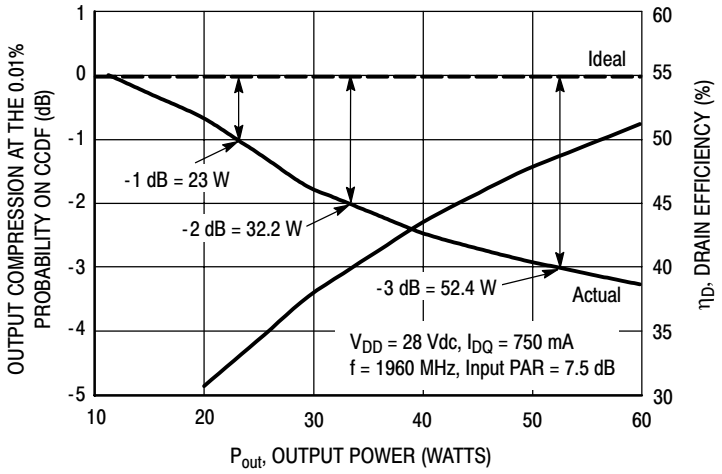


Figure 9. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

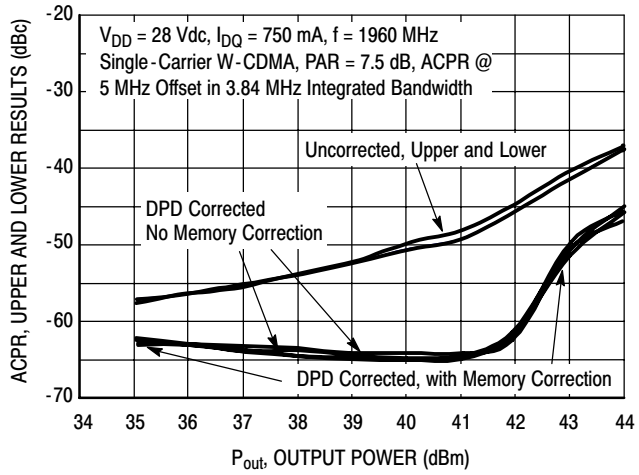


Figure 10. Digital Predistortion Correction versus ACPR and Output Power

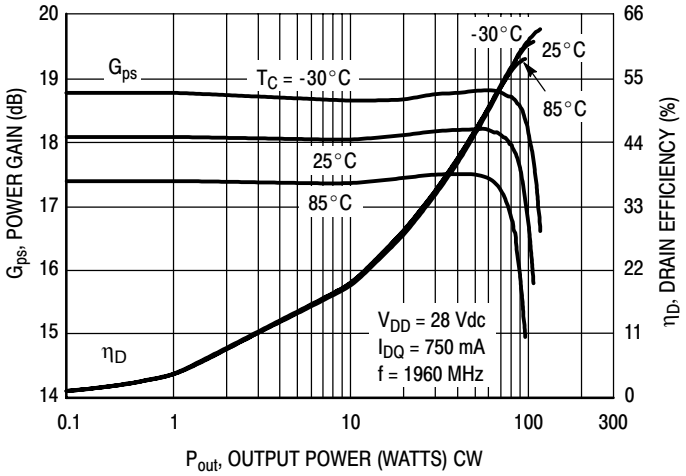


Figure 11. Power Gain and Drain Efficiency versus CW Output Power

TYPICAL CHARACTERISTICS

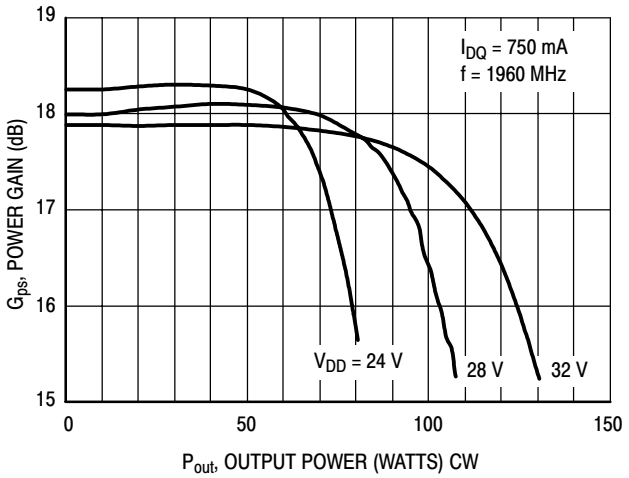
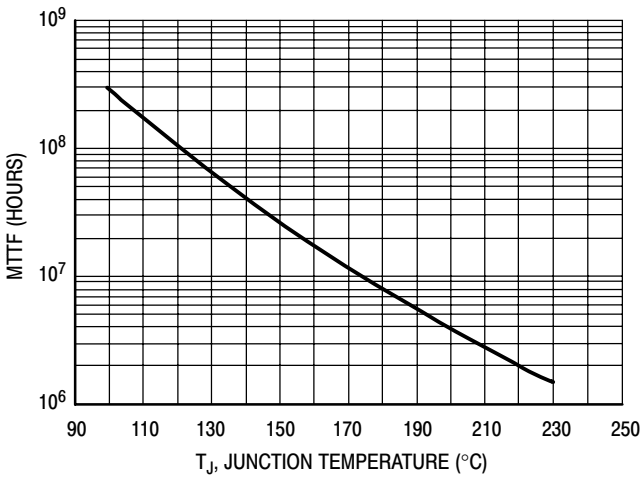


Figure 12. Power Gain versus Output Power



This above graph displays calculated MTTF in hours when the device is operated at V_{DD} = 28 Vdc, P_{out} = 24 W Avg., and η_D = 32%.

MTTF calculator available at http:/www.freescale.com/rf. Select Tools/Software/Application Software/Calculators to access the MTTF calculators by product.

Figure 13. MTTF versus Junction Temperature

W-CDMA TEST SIGNAL

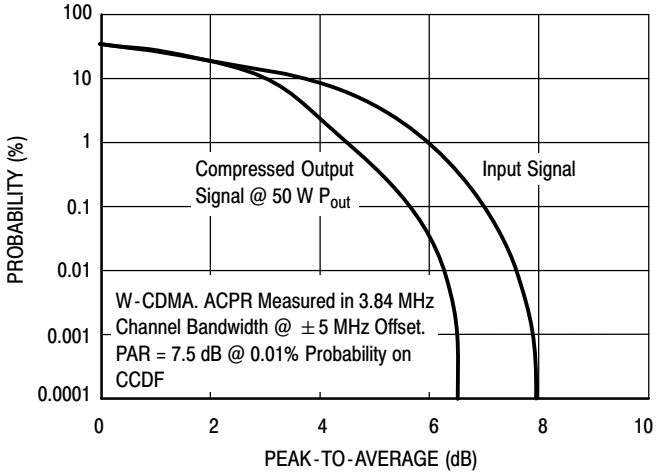


Figure 14. CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 50% Clipping, Single-Carrier Test Signal

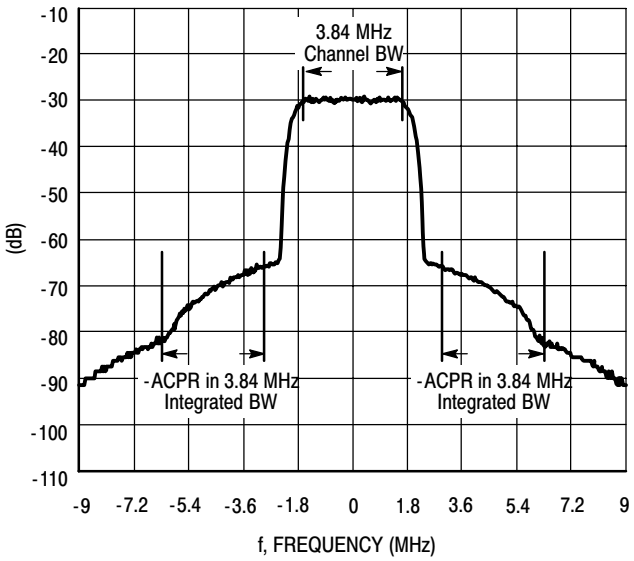
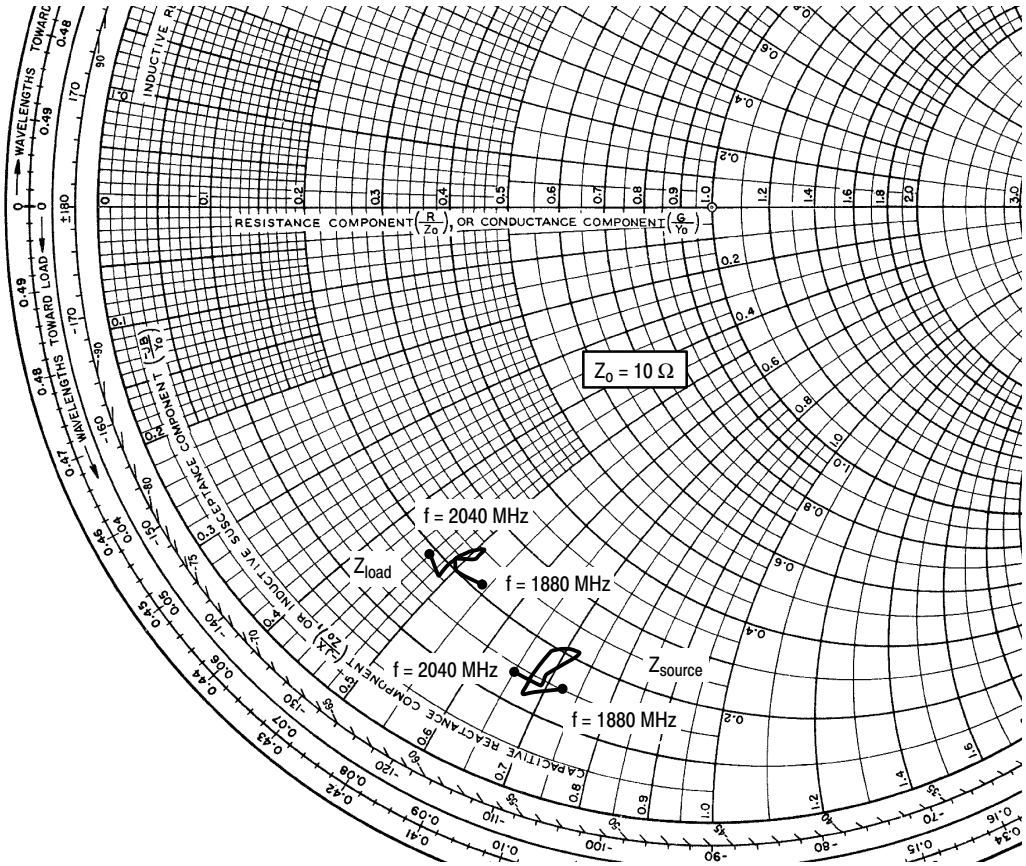


Figure 15. Single-Carrier W-CDMA Spectrum



V_{DD} = 28 Vdc, I_{DQ} = 750 mA, P_{out} = 24 W Avg.

f MHz	Z_{source} Ω	Z_{load} Ω
1880	1.47 - j7.3	2.10 - j5.4
1900	1.22 - j6.7	1.96 - j5.0
1920	1.43 - j6.7	2.06 - j4.9
1940	1.89 - j6.8	2.27 - j5.1
1960	2.10 -j7.1	2.45 - j5.1
1980	2.11 - j7.2	2.38 - j5.0
2000	1.60 - j6.9	2.08 - j4.9
2020	1.41 - j6.9	1.84 - j4.9
2040	1.43 - j6.5	1.89 - j4.6

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

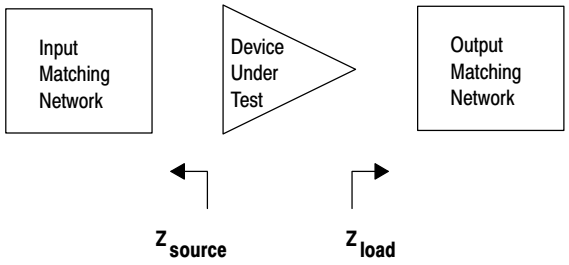
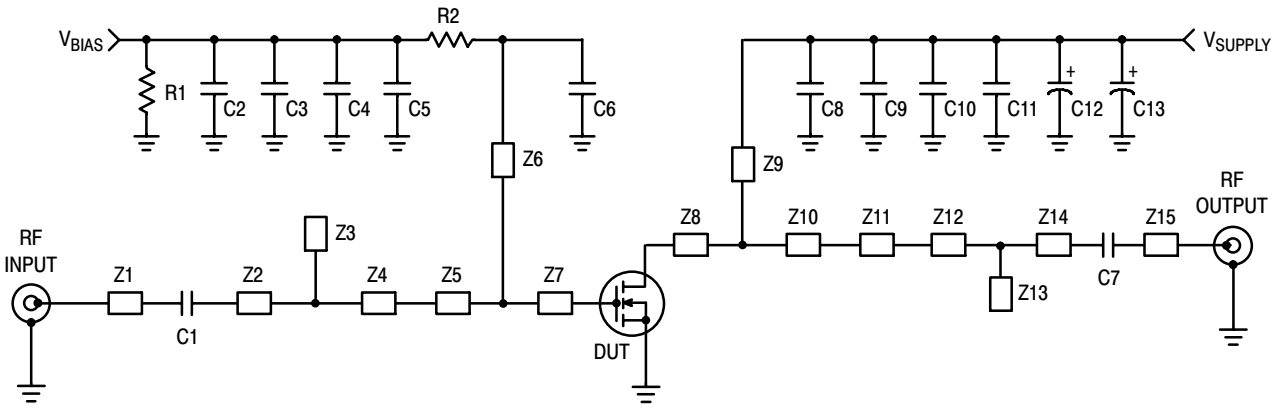


Figure 16. Series Equivalent Source and Load Impedance

TD-SCDMA CHARACTERIZATION



Z1	0.490″ x 0.084″ Microstrip	Z9	0.432″ x 0.121″ Microstrip
Z2	1.082″ x 0.084″ Microstrip	Z10	0.327″ x 0.974″ Microstrip
Z3	0.131″ x 0.220″ Microstrip	Z11	0.505″ x 0.201″ Microstrip
Z4	0.734″ x 0.084″ Microstrip	Z12	0.220″ x 0.084″ Microstrip
Z5	0.308″ x 0.800″ Microstrip	Z13	0.191″ x 0.243″ Microstrip
Z6	0.889″ x 0.040″ Microstrip	Z14	0.781″ x 0.084″ Microstrip
Z7	0.092″ x 0.800″ Microstrip	Z15	0.500″ x 0.084″ Microstrip
Z8	0.160″ x 0.880″ Microstrip	PCB	Arlon, GX-0300-55-22, 0.030″, ε_r = 2.55

Figure 17. MRF7S19080HR3(HSR3) Test Circuit Schematic — TD-SCDMA

Table 6. MRF7S19080HR3(HSR3) Test Circuit Component Designations and Values — TD-SCDMA

Part	Description	Part Number	Manufacturer
C1, C7	15 pF Chip Capacitors	ATC100B150JT500XT	ATC
C2, C11	13 pF Chip Capacitors	ATC100B130JT500XT	ATC
C3	10 μF Chip Capacitor	GRM31MF51A106ZA01B	TDK
C4	1000 pF Chip Capacitor	ATC100B102JT50XT	ATC
C5, C10	0.1 μF Chip Capacitors	C1206C104K5RAC	Kemet
C6	5.1 pF Chip Capacitor	ATC100B5R1CT500XT	ATC
C8	6.8 pF Chip Capacitor	ATC100B6R8CT500XT	ATC
C9	2.2 μF Chip Capacitor	C1825C225J5RAC	Kemet
C12	470 μF, 63 V Electrolytic Capacitor	MCR63V477M13X26	Multicomp
C13	100 μF, 50 V Electrolytic Capacitor	MCR50V107M8X11	Multicomp
R1	330 Ω, 1/4 W Chip Resistor	CRCW12063300FKTA	Vishay
R2	10 Ω, 1/4 W Chip Resistor	CRCW120610R0FKTA	Vishay

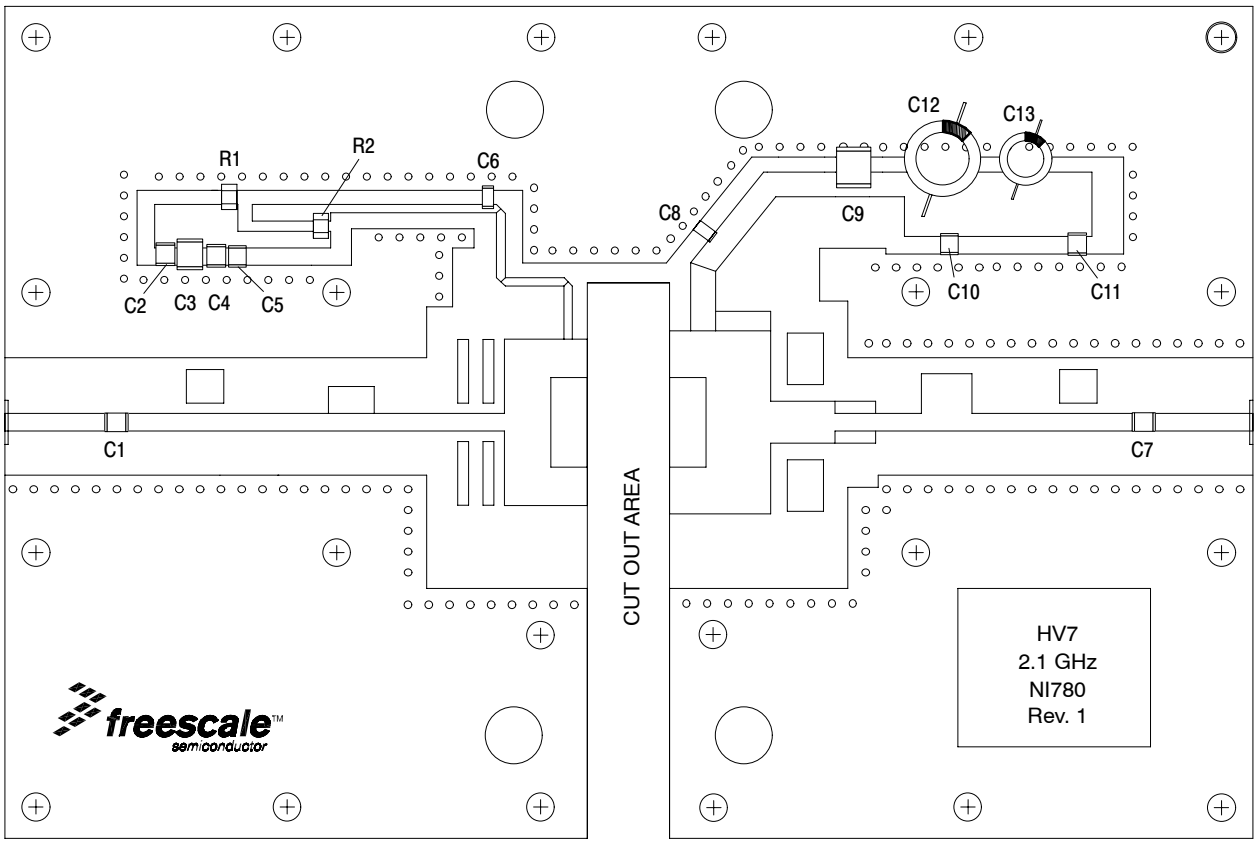


Figure 18. MRF7S19080HR3(HSR3) Test Circuit Component Layout — TD-SCDMA

TYPICAL CHARACTERISTICS

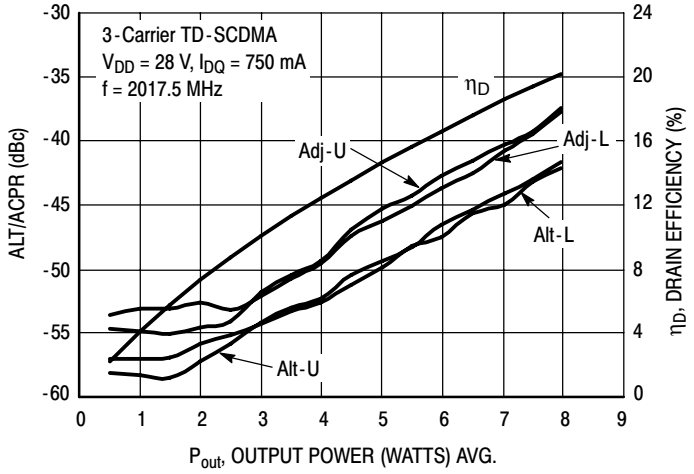


Figure 19. 3-Carrier TD-SCDMA ACPR, ALT and Drain Efficiency versus Output Power

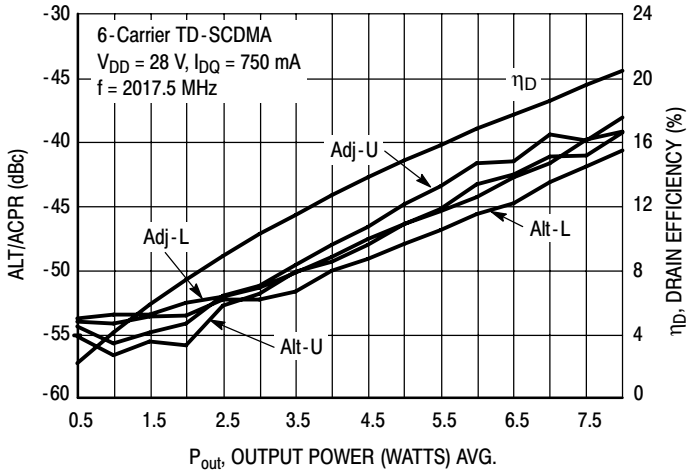


Figure 20. 6-Carrier TD-SCDMA ACPR, ALT and Drain Efficiency versus Output Power

TD-SCDMA TEST SIGNAL

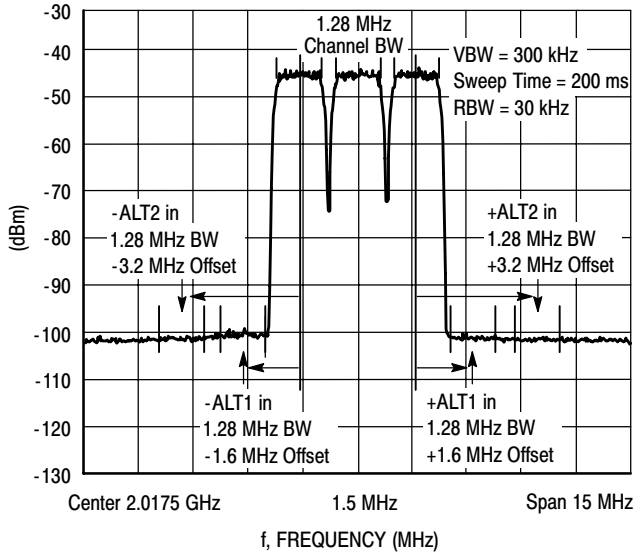


Figure 21. 3-Carrier TD-SCDMA Spectrum

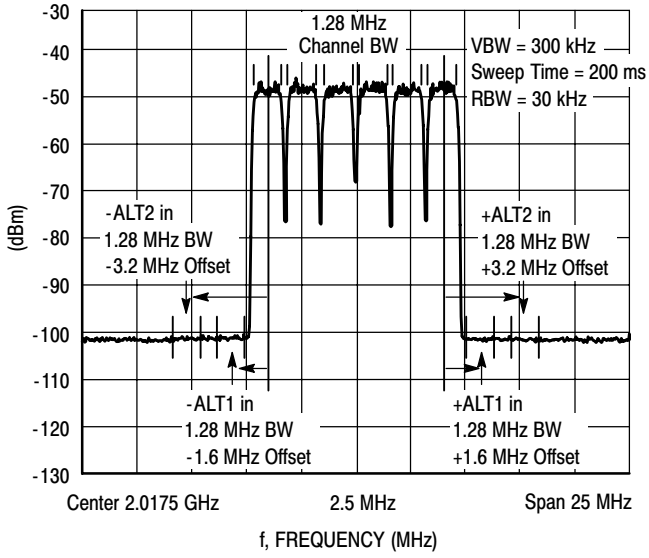
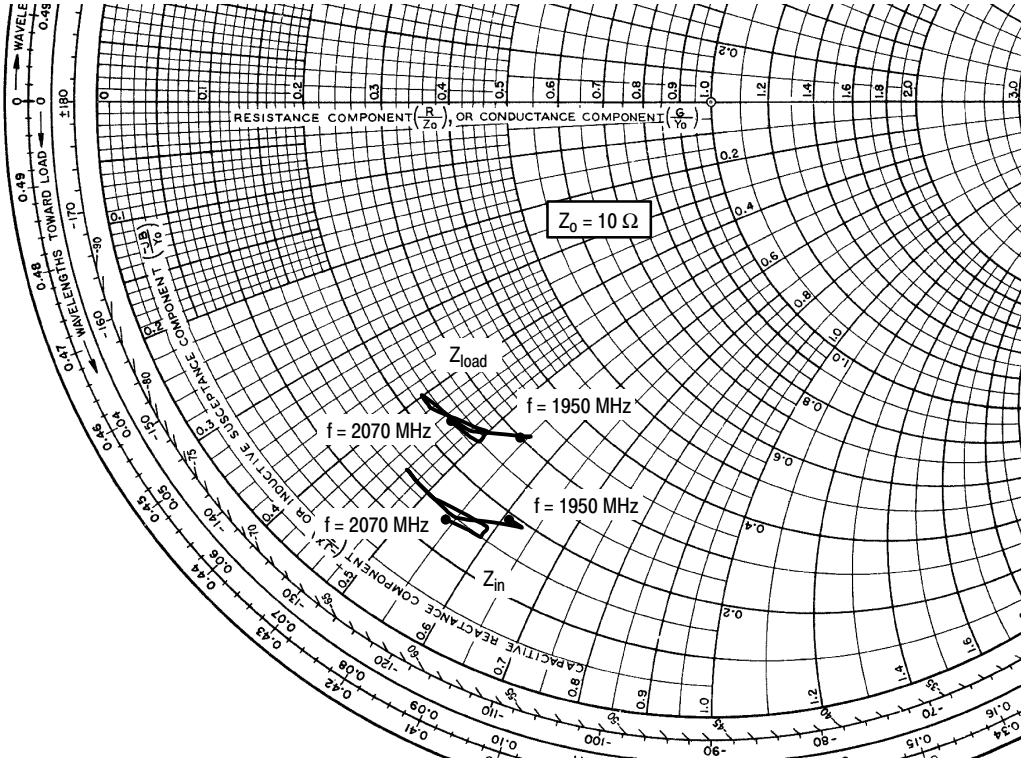


Figure 22. 6-Carrier TD-SCDMA Spectrum



V_{DD} = 28 Vdc, I_{DQ} = 750 mA

f MHz	Z_{in} Ω	Z_{load} Ω
1950	1.87 - j6.10	2.98 - j5.42
1960	1.94 - j6.25	3.07 - j5.47
1970	1.77 - j6.04	2.87 - j5.26
1980	1.52 - j5.47	2.53 - j4.77
1990	1.46 - j4.92	2.35 - j4.26
2000	1.49 - j4.62	2.30 - j3.99
2010	1.53 - j4.64	2.34 - j3.98
2020	1.50 - j4.85	2.34 - j4.20
2030	1.50 - j5.15	2.40 - j4.44
2040	1.62 - j5.56	2.59 - j4.75
2050	1.63 - j5.90	2.68 - j5.03
2060	1.47 - j5.86	2.52 - j4.98
2070	1.38 - j5.40	2.35 - j4.54

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

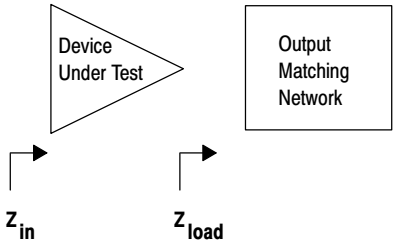
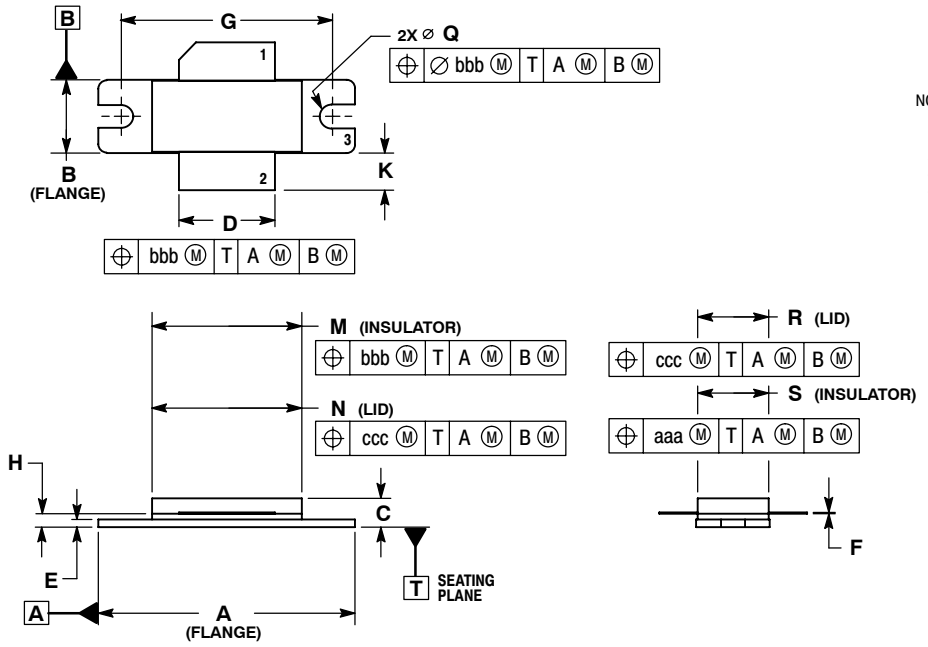


Figure 23. Series Equivalent Input and Load Impedance — TD-SCDMA

PACKAGE DIMENSIONS

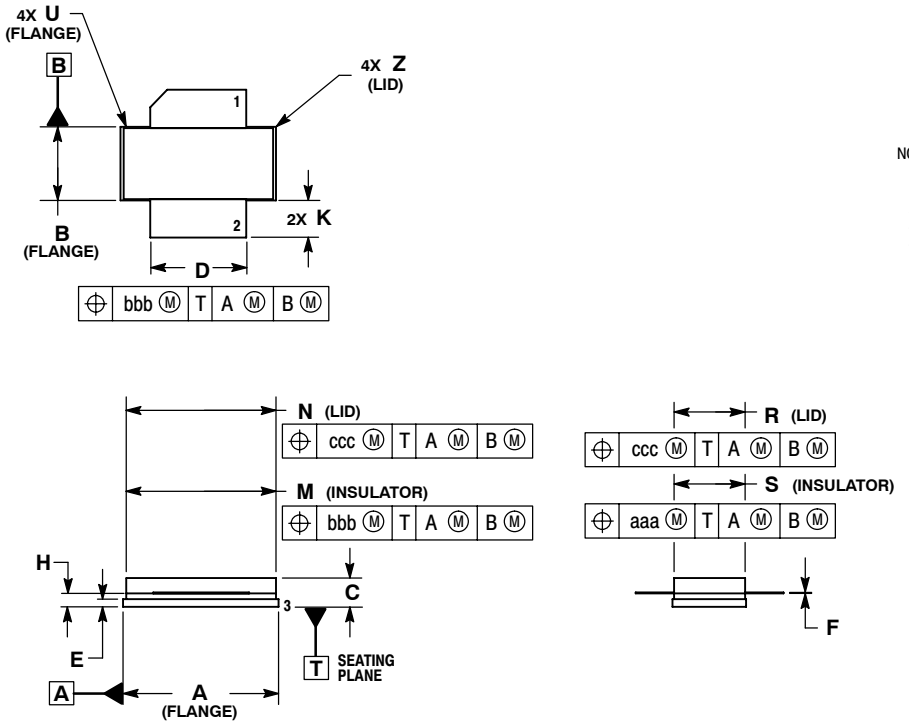


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.66	19.96
N	0.772	0.788	19.60	20.00
Q	⌀.118	⌀.138	⌀3.00	⌀3.51
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465-06
ISSUE G
NI-780
MRF7S19080HR3



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.805	0.815	20.45	20.70
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.61	20.02
N	0.772	0.788	19.61	20.02
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
U	---	0.040	---	1.02
Z	---	0.030	---	0.76
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
5. SOURCE

CASE 465A-06
ISSUE H
NI-780S
MRF7S19080HSR3

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Jan. 2007	• Initial Release of Data Sheet

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Freescale Semiconductor Japan Ltd.
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ARCO Tower 15F
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Japan
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