RF Power Field Effect Transistors

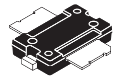
N−Channel Enhancement−Mode Lateral MOSFETs

MRF9030NR1
MRF9030NBR1
MRF9030MR1
MRF9030MBR1

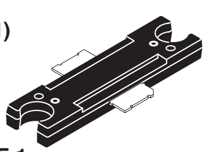
Designed for broadband commercial and industrial applications with frequencies up to 1000 MHz. The high gain and broadband performance of these devices make them ideal for large−signal, common−source amplifier applications in 26 volt base station equipment.

- Typical Performance at 945 MHz, 26 Volts
  Output Power — 30 Watts PEP
  Power Gain — 20 dB
  Efficiency — 41% (Two Tones)
  IMD — −31 dBc
- Integrated ESD Protection
- Capable of Handling 5:1 VSWR, @ 26 Vdc, 945 MHz, 30 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large−Signal Impedance Parameters
- Dual−Lead Boltdown Plastic Package Can Also Be Used As Surface Mount.
- N Suffix Indicates Lead−Free Terminations
- 200°C Capable Plastic Package
- TO−272−2 in Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.
- TO−270−2 in Tape and Reel. R1 Suffix = 500 Units per 24 mm, 13 inch Reel.

945 MHz, 30 W, 26 V
LATERAL N−CHANNEL
BROADBAND
RF POWER MOSFETs



CASE 1265−08, STYLE 1
TO−270−2
PLASTIC
MRF9030NR1(MR1)



CASE 1337−03, STYLE 1
TO−272−2
PLASTIC
MRF9030NBR1(MBR1)

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain−Source Voltage	V_{DSS}	−0.5, +65	Vdc
Gate−Source Voltage	V_{GS}	−0.5, +15	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	139 0.93	W W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature	T_J	200	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.08	°C/W

Table 3. ESD Protection Characteristics

Test Conditions		Class
Human Body Model		1 (Minimum)
Machine Model		M2 (Minimum)
Charge Device Model	MRF9030NR1(MR1) MRF9030NBR1(MBR1)	C7 (Minimum) C6 (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22−A113, IPC/JEDEC J−STD−020	3	260	°C

NOTE − **CAUTION** − MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

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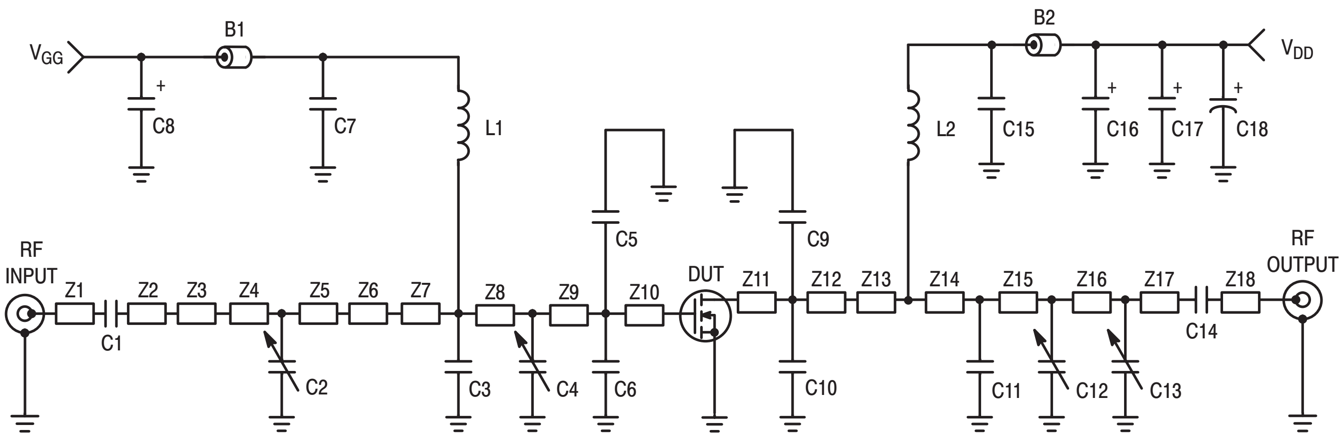
Table 5. Electrical Characteristics (T_c = 25°c Unless Otherwise Noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate−Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 100 μAdc)	$V_{GS(th)}$	2	2.9	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 250 mAdc)	$V_{GS(Q)}$	3	3.8	5	Vdc
Drain−Source On−Voltage (V_{GS} = 10 Vdc, I_D = 0.7 Adc)	$V_{DS(on)}$	—	0.23	0.4	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 2 Adc)	g_{fs}	—	2.7	—	S
Dynamic Characteristics					
Input Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{iss}	—	49	—	pF
Output Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	27	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	1.2	—	pF
Functional Tests (In Freescale Test Fixture)					
Two−Tone Common−Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	G_{ps}	18	20	—	dB
Two−Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	η	37	41	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	IMD	—	−31	−28	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	IRL	—	−13	−9	dB
Two−Tone Common−Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz)	G_{ps}	—	20	—	dB
Two−Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz)	η	—	40.5	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz)	IMD	—	−31	—	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz)	IRL	—	−12	—	dB

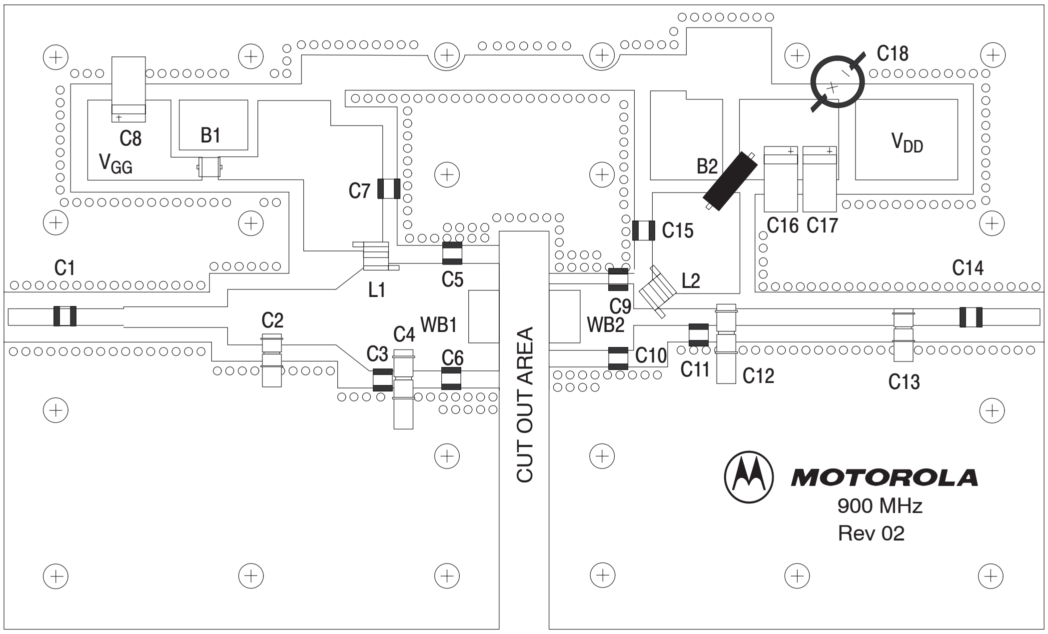


Z1	0.260″ x 0.060″ Microstrip	Z11	0.360″ x 0.270″ Microstrip
Z2	0.240″ x 0.060″ Microstrip	Z12	0.050″ x 0.270″ Microstrip
Z3	0.500″ x 0.100″ Microstrip	Z13	0.110″ x 0.060″ Microstrip
Z4	0.200″ x 0.270″ Microstrip	Z14	0.220″ x 0.060″ Microstrip
Z5	0.330″ x 0.270″ Microstrip	Z15	0.100″ x 0.060″ Microstrip
Z6	0.140″ x 0.270″ x 0.520″, Taper	Z16	0.870″ x 0.060″ Microstrip
Z7	0.040″ x 0.520″ Microstrip	Z17	0.240″ x 0.060″ Microstrip
Z8	0.090″ x 0.520″ Microstrip	Z18	0.340″ x 0.060″ Microstrip
Z9	0.370″ x 0.520″ Microstrip (MRF9030NR1/MR1) 0.290″ x 0.520″ Microstrip (MRF9030NBR1/MBR1)	Board	Taconic RF−35−0300, ε_r = 3.5
Z10	0.130″ x 0.520″ Microstrip (MRF9030NR1/MR1) 0.210″ x 0.520″ Microstrip (MRF9030NBR1/MBR1)		

Figure 1. 930−960 MHz Broadband Test Circuit Schematic

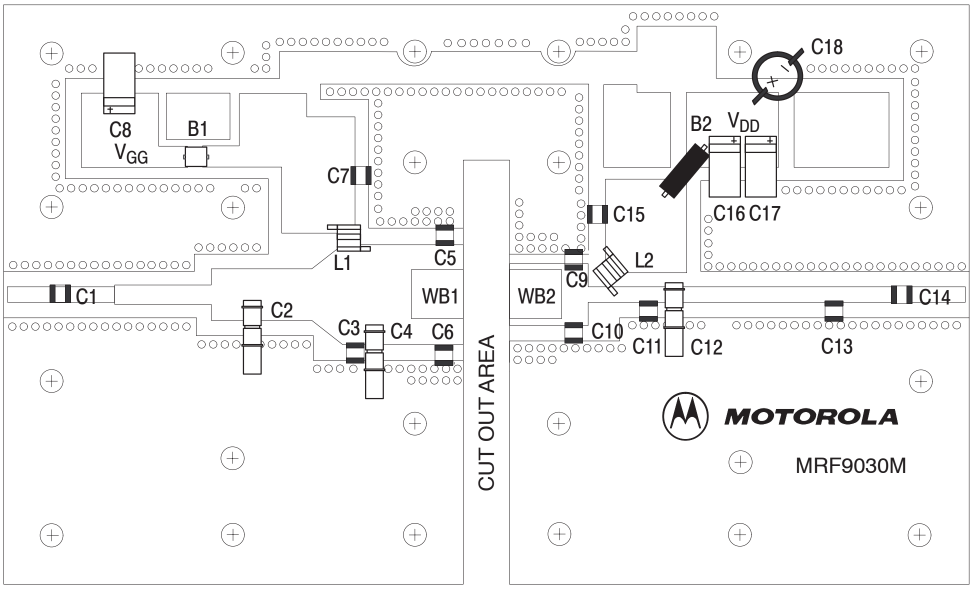
Table 6. 930 − 960 MHz Broadband Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
B1	Short Ferrite Bead, Surface Mount	95F786	Newark
B2	Long Ferrite Bead, Surface Mount	95F787	Newark
C1, C7, C14, C15	47 pF Chip Capacitors	100B470JP 500X	ATC
C2	0.6−4.5 Variable Capacitor, Gigatrim	44F3360	Newark
C3, C11	3.9 pF Chip Capacitors	100B3R6BP 500X	ATC
C4, C12	0.8−8.0 Variable Capacitors, Gigatrim	44F3360	Newark
C5, C6	6.8 pF Chip Capacitors	100B7R5JP 500X	ATC
C8, C16, C17	10 μF, 35 V Tantulum Chip Capacitors	93F2975	Newark
C9, C10	10 pF Chip Capacitors	100B100JP 500X	ATC
C13	1.8 pF Chip Capacitor (MRF9030NR1/MR1) 0.6−4.5 Variable Capacitor, Gigatrim (MRF9030NBR1/MBR1)	100B1R8BP 44F3360	ATC Newark
C18	220 μF Electrolytic Chip Capacitor	14F185	Newark
L1, L2	12.5 nH Coilcraft Inductors	A04T−5	Coilcraft
WB1, WB2	20 mil Brass Shim (0.250 x 0.250)	RF−Design Lab	RF−Design Lab
PCB	Etched Circuit Board	900 MHz μ250/Viper Rev 02	DSelectronics



Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 2. 930−960 MHz Broadband Test Circuit Component Layout (MRF9030NR1/MR1)



Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 3. 930−960 MHz Broadband Test Circuit Component Layout (MRF9030NBR1/MBR1)

TYPICAL CHARACTERISTICS

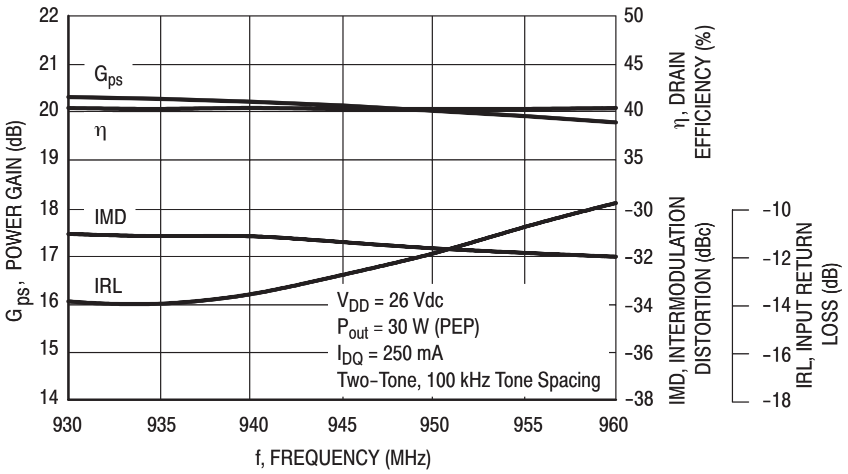


Figure 4. Class AB Broadband Circuit Performance

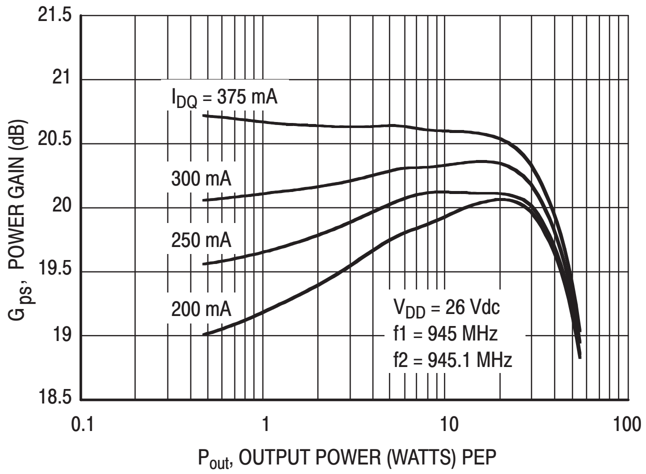


Figure 5. Power Gain versus Output Power

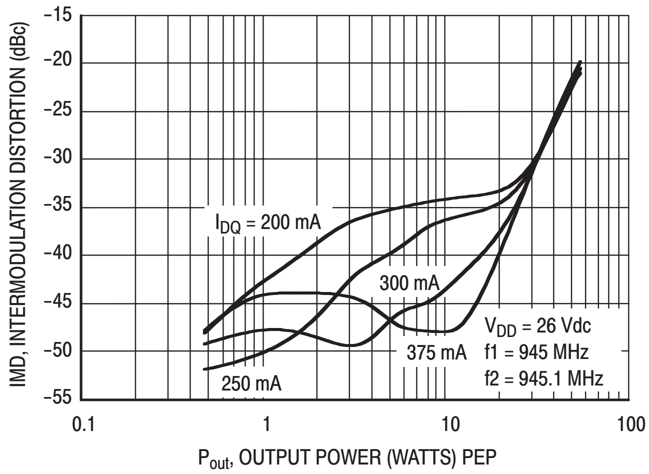


Figure 6. Intermodulation Distortion versus Output Power

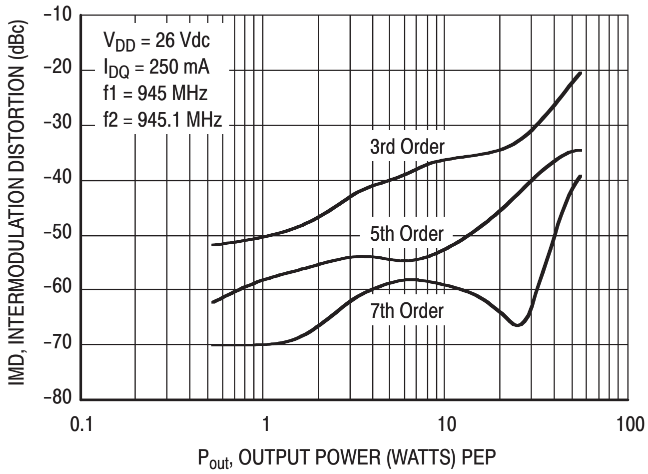


Figure 7. Intermodulation Distortion Products versus Output Power

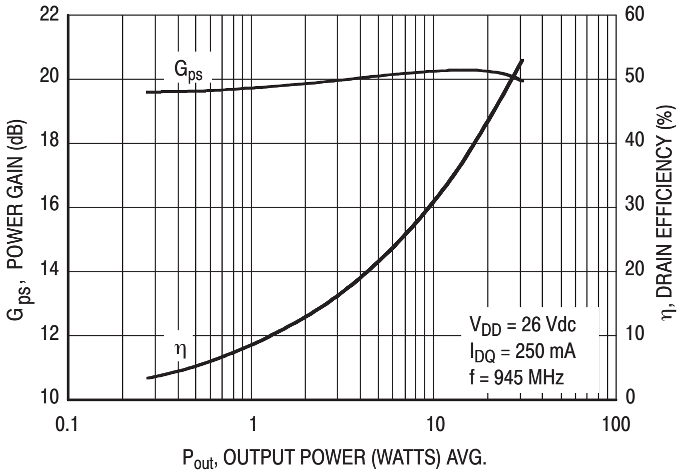


Figure 8. Power Gain and Efficiency versus Output Power

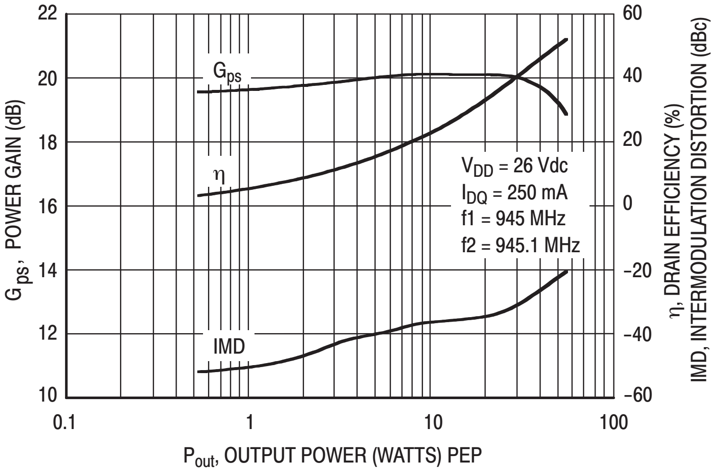
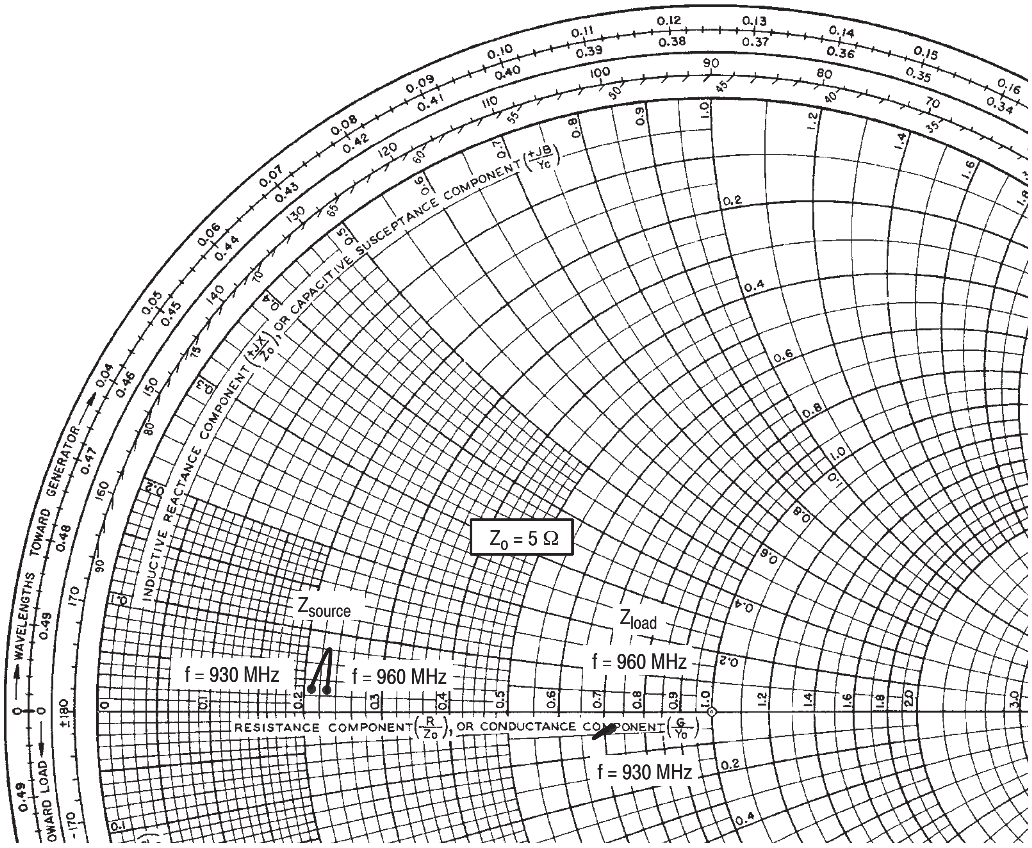


Figure 9. Power Gain, Efficiency and IMD versus Output Power



V_{DD} = 26 V, I_{DQ} = 250 mA, P_{out} = 30 Watts (PEP)

f MHz	Z_{source} Ω	Z_{load} Ω
930	1.07 + j0.160	3.53 − j0.20
945	1.14 + j0.385	3.41 − j0.24
960	1.17 + j0.170	3.60 − j0.17

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

Note: Z_{load} was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

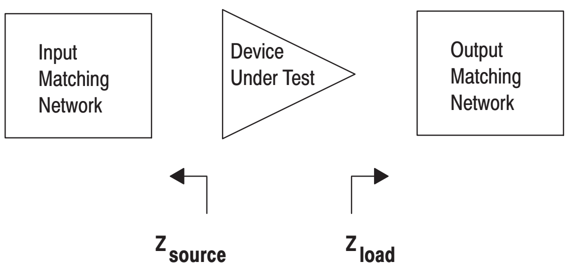
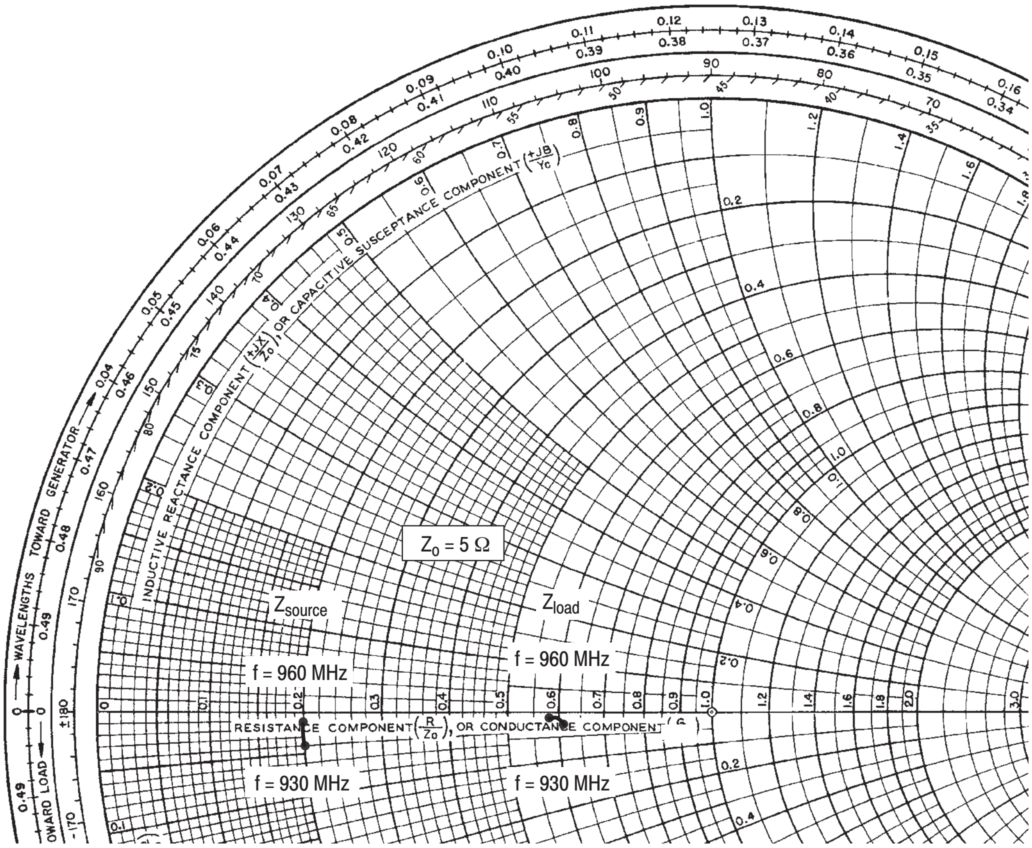


Figure 10. Series Equivalent Source and Load Impedance (MRF9030NR1/MR1)



V_{DD} = 26 V, I_{DQ} = 250 mA, P_{out} = 30 Watts (PEP)

f MHz	Z_{source} Ω	Z_{load} Ω
930	1.0 – j0.18	3.05 – j0.09
945	1.0 – j0.10	3.00 – j0.07
960	1.0 – j0.03	2.95 – j0.03

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

Note: Z_{load} was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

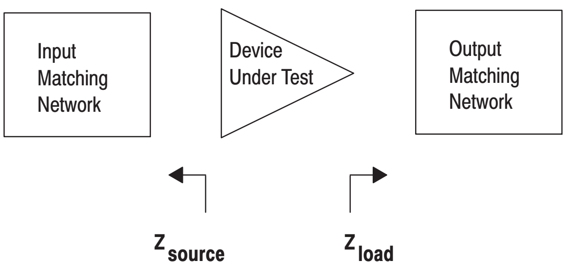
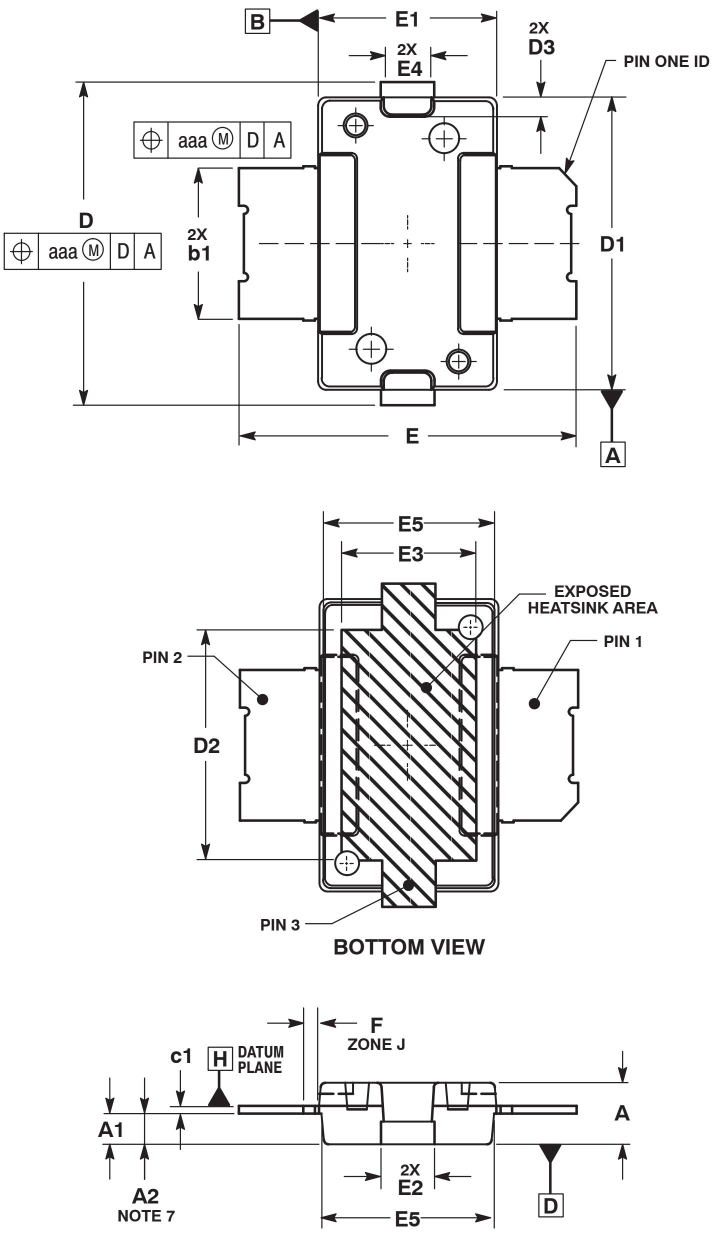


Figure 11. Series Equivalent Source and Load Impedance (MRF9030NBR1/MBR1)

NOTES

PACKAGE DIMENSIONS

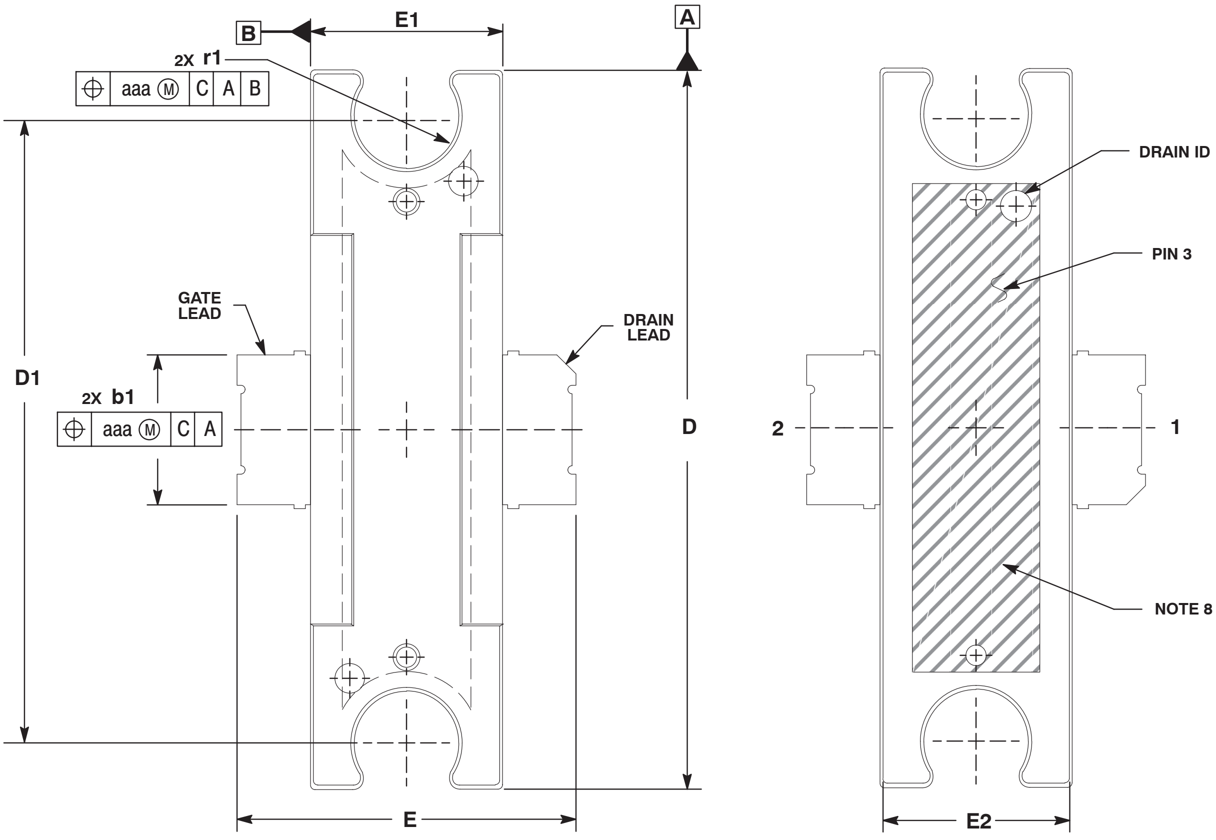


NOTES:
1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994.
3. DATUM PLANE −H− IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D1" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE −H−.
5. DIMENSION b1 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE b1 DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS −A− AND −B− TO BE DETERMINED AT DATUM PLANE −H−.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. DIMENSIONS "D" AND "E2" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .003 PER SIDE. DIMENSIONS "D" AND "E2" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE −D−.

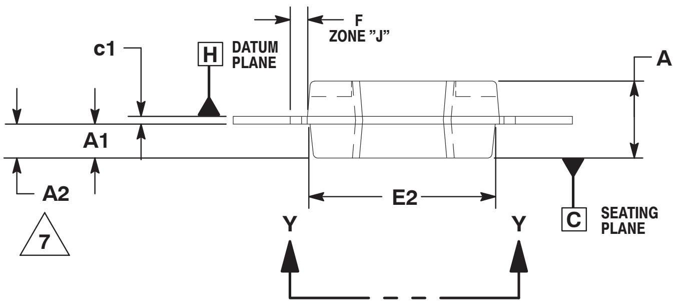
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.078	.082	1.98	2.08
A1	.039	.043	0.99	1.09
A2	.040	.042	1.02	1.07
D	.416	.424	10.57	10.77
D1	.378	.382	9.60	9.70
D2	.290	.320	7.37	8.13
D3	.016	.024	0.41	0.61
E	.436	.444	11.07	11.28
E1	.238	.242	6.04	6.15
E2	.066	.074	1.68	1.88
E3	.150	.180	3.81	4.57
E4	.058	.066	1.47	1.68
E5	.231	.235	5.87	5.97
F	.025 BSC		0.64 BSC	
b1	.193	.199	4.90	5.06
c1	.007	.011	0.18	0.28
aaa	.004		0.10	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 1265−08
ISSUE G
TO−270−2
PLASTIC
MRF9030NR1(MR1)



VIEW Y−Y



NOTES:
1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE −H− IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE −H−.
5. DIMENSION "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS −A− AND −B− TO BE DETERMINED AT DATUM PLANE −H−.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. CROSSHATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.100	.104	2.54	2.64
A1	.039	.043	0.99	1.09
A2	.040	.042	1.02	1.07
D	.928	.932	23.57	23.67
D1	.810 BSC		20.57 BSC	
E	.438	.442	11.12	11.23
E1	.248	.252	6.30	6.40
E2	.241	.245	6.12	6.22
F	.025 BSC		0.64 BSC	
b1	.193	.199	4.90	5.05
c1	.007	.011	.18	.28
r1	.063	.068	1.60	1.73
aaa	.004		.10	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 1337−03
ISSUE B
TO−272−2
PLASTIC
MRF9030NBR1(MBR1)

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