



MOTOROLA

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Integrated GPS Downconverter

This integrated circuit is intended for GPS receiver applications. The dual conversion design is implemented in Motorola's low-cost, high-performance MOSAIC 5™ silicon bipolar process and is packaged in a low-cost surface mount LQFP-48 package. In addition to the mixers, a VCO, PLL, Crystal Oscillator, A/D converter and a loop filter are integrated on-chip. Output IF is nominally 4.1 MHz.

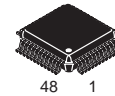
- 105 dB Typical Conversion Gain
- 2.7 V Operation
- 28 mA Typical Current Consumption
- Low-Cost, Low-Profile Plastic LQFP Package

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MRFIC1504

1.575 GHz GPS DOWNCONVERTER

SEMICONDUCTOR TECHNICAL DATA

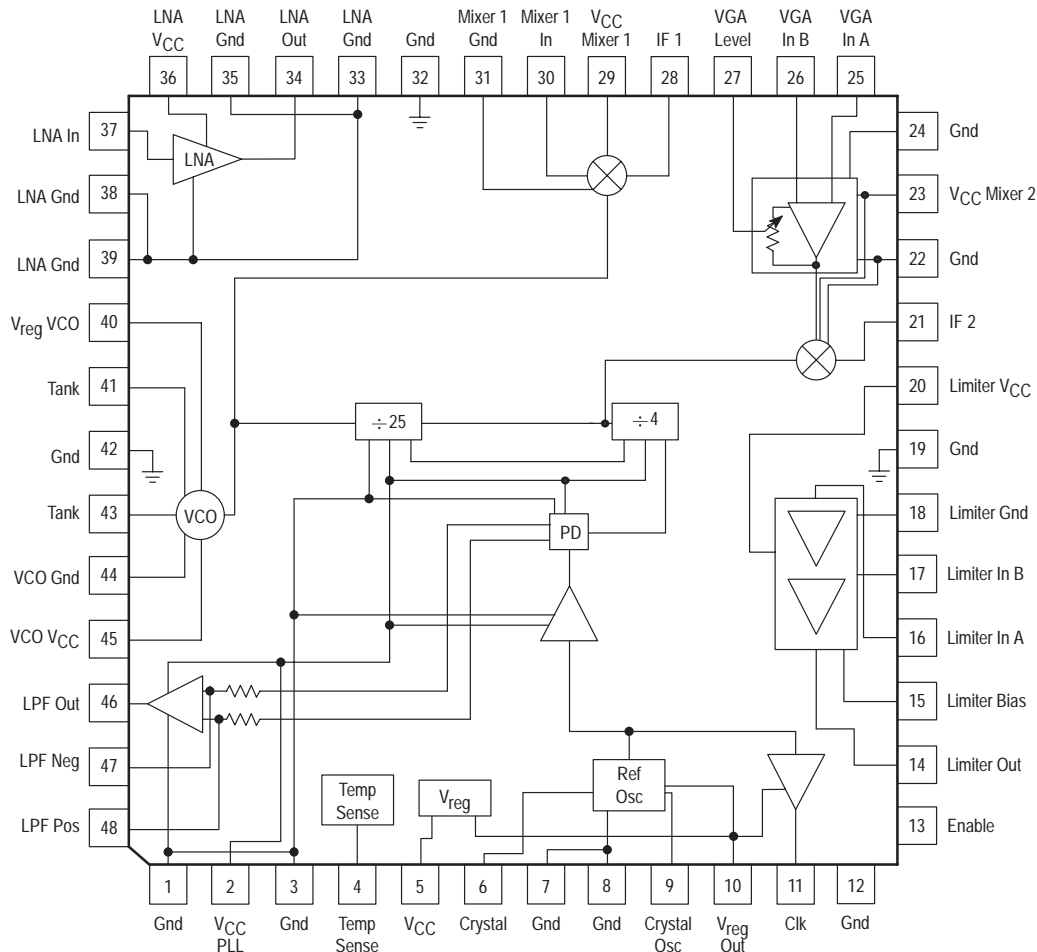


PLASTIC PACKAGE
CASE 932
(LQFP-48)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MRFIC1504R2	T _A = -40 to 85°C	LQFP-48

Pin Connections and Functional Block Diagram



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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	5.0	Vdc
DC Supply Current	I _{DD}	60	mA
Operating Ambient Temperature	T _A	-40 to 85	°C
Storage Temperature Range	T _{stg}	-65 to 150	°C
Lead Soldering Temperature Range (10 seconds)	-	260	°C

NOTE: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables.

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 3.3 V; T_A = -40 to 85°C; Enable = 2.7 V unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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TOTAL DEVICE

Supply Voltage	V _{CC}	2.7	3.0	3.3	V
Supply Current (T _A = 25°C, V _{CC} = 2.7 V, Enable = 2.7 V)	I _{CC}	-	28	36	mA
Supply Current (T _A = 25°C, V _{CC} = 2.7 V, Enable = 0 V)	I _{CC}	-	2.0	4.0	mA

RF AMPLIFIER

RF Input Frequency	f _{in}	-	1575.42	-	MHz
Input Impedance	Z _{in}	-	50	-	Ω
Input VSWR	VSWR _{in}	-	2.0	-	-
Gain	G	13	15	-	dB
Noise Figure	NF	-	2.0	-	dB
1.0 dB Compression (Measured at Output)	P _{1dB}	-	1.0	-	dBm

FIRST MIXER

Input Frequency	f _{in}	-	1575.42	-	MHz
Gain	G	10	14	-	dB
Noise Figure	NF	-	13	-	dB
1.0 dB Compression (Measured at Output)	P _{1dB}	-	-13	-	dBm
First Local Oscillator Frequency	f _{LO1}	-	1636.8	-	MHz
First Intermediate Frequency	f _{IF1}	-	61.38	-	MHz
LO Leakage at IF Port	-	-	-40	-	dBm
LO Leakage at RF Port	-	-	-50	-	dBm
Output Impedance	Z _{out}	-	50	-	Ω

FIRST IF AMPLIFIER and SECOND MIXER

Input Frequency	f _{in}	-	61.38	-	MHz
Input Impedance	Z _{in}	-	230	-	Ω
Output Impedance	Z _{out}	-	50	-	Ω
Second Local Oscillator Frequency	f _{LO2}	-	65.47	-	MHz
Second Intermediate Frequency	f _{IF2}	-	4.092	-	MHz
LO Leakage at IF Port	-	-	-40	-	dBm
Gain	G	40	43	-	dB
Cascaded Noise Figure	NF	-	9.3	-	dB
1.0 dB Compression Point (Measured at Output)	P _{1dB}	-	-13	-	dBm

ELECTRICAL CHARACTERISTICS — continued ($V_{CC} = 2.7$ to 3.3 V; $T_A = -40$ to 85°C ; Enable = 2.7 V unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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LIMITING AMPLIFIER

Second Intermediate Frequency	f_{IF2}	–	4.092	–	MHz
Input Signal Level	–	4.0	11	31	mV
Output Voltage Swing (Into 10 pF 100 k Ω)	V_{out}	800	–	–	mVpp
DC Output Level	–	–	1.4	–	V
Gain	G	–	50	–	dB

REFERENCE OSCILLATOR

Reference Frequency	f_r	–	16.368	–	MHz
Reference Frequency Input Level (Crystal Output Pin)	–	–	500	–	mVpp
Reference Oscillator Output Voltage Level (Into 15 pF 10 k Ω)	–	750	–	–	mVpp
Reference Clock Input Drive Level	–	400	800	1500	mVpp

PLL

First Local Oscillator Frequency	f_{LO1}	–	1636.8	–	MHz
Second Local Oscillator Frequency	f_{LO2}	–	65.47	–	MHz
VCO C/N (at 10 kHz Offset)	–	–	–80	–	dBc/Hz
VCO Gain (TBD Varactor)	–	–	20	–	MHz/V

ENABLE

Enable Active Level	–	$0.8 \times V_{CC}$	V_{CC}	–	V
Disable Active Level	–	–	0	$0.2 \times V_{CC}$	V

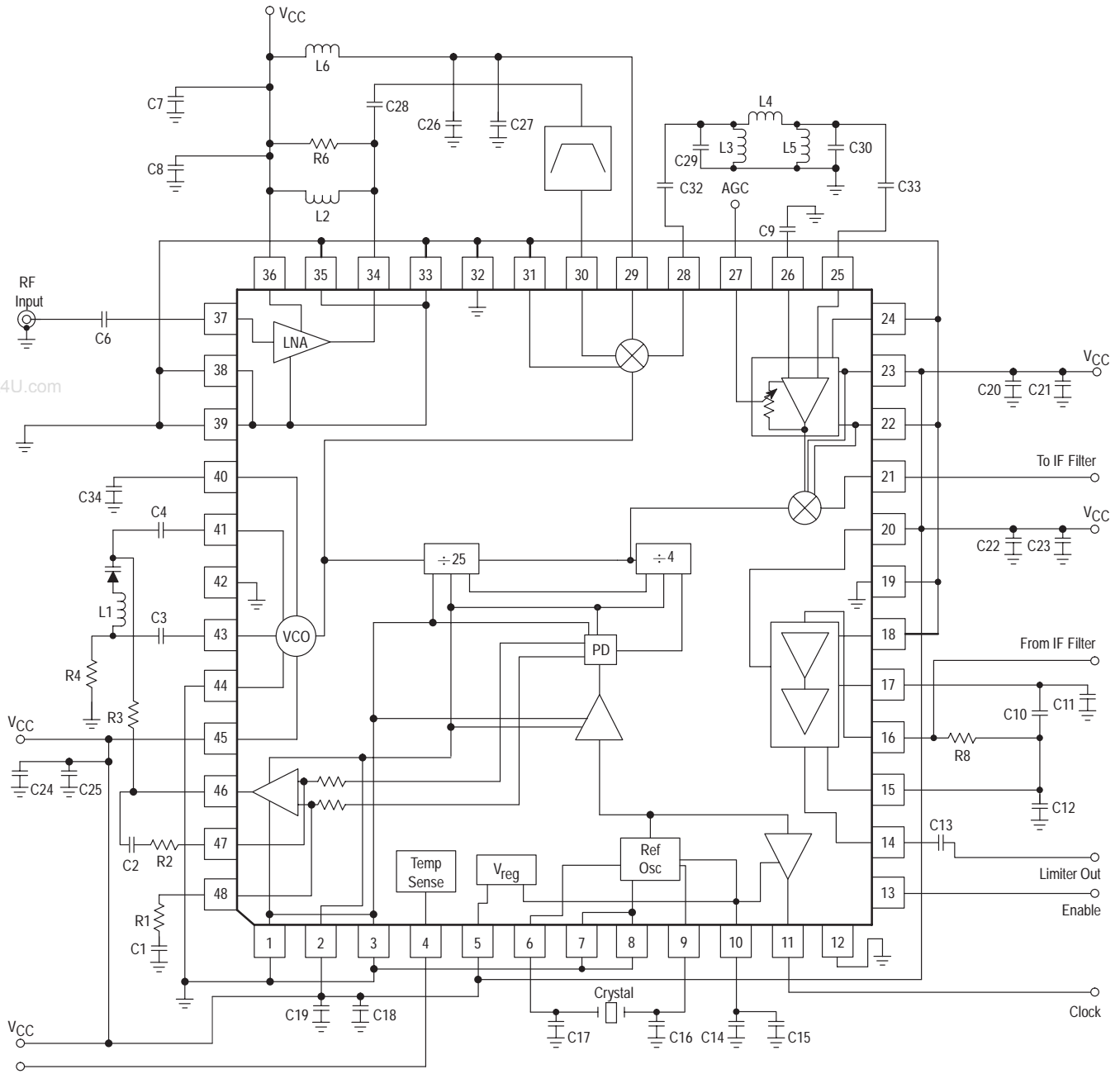
VOLTAGE REGULATOR

Regulator Output Voltage ($V_{CC} = 2.7$ to 3.3 V, $I_{out} = 3.0$ mA)	V_o	2.1	2.3	2.5	V
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TEMPERATURE SENSE SPECS

Temperature Sensor Output Voltage @ 25°C	–	1.2	1.28	1.375	V
Temperature Sensor Slope over Temperature	–	–	5.0	–	mV/ $^\circ\text{C}$

Figure 1. Applications Schematic (1636.8 MHz LO)



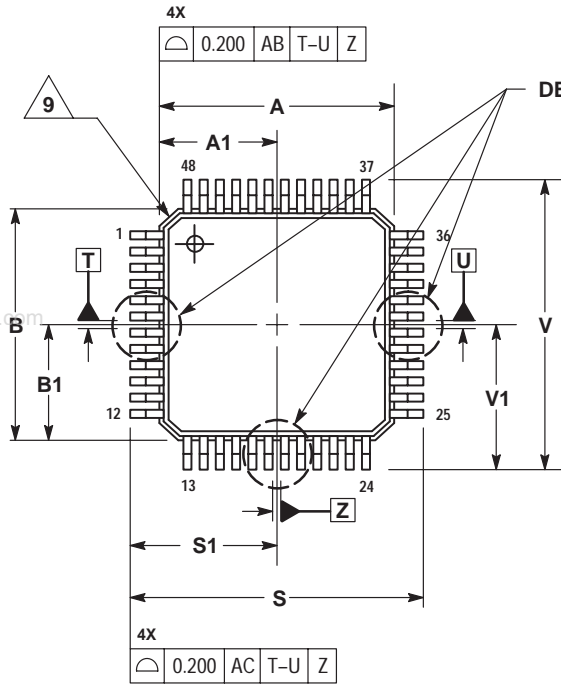
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Temp Sense	C1, C2	220 pF	C29, C30	91 pF
	C3, C4	1.7 pF	C32, C33	1.0 nF
	C6	10 pF	L1	10 nH
	C7, C14, C18, C20, C22, C24, C34	0.01 μF	L2	3.9 nH
	C8, C15, C19, C21, C23, C25, C27	1000 pF	L3, L5	82 nH
	C9	1.0 μF	L4	0.62 μH
	C10, C11, C12	1.0 nF	L6	TBD
	C13	2.7 nF	R1, R2, R4	10 k
	C16, C17	27 pF	R3	2 k
	C26	470 pF	R6	1.2 k
	C28	0.6 pF	R8	5.0 k

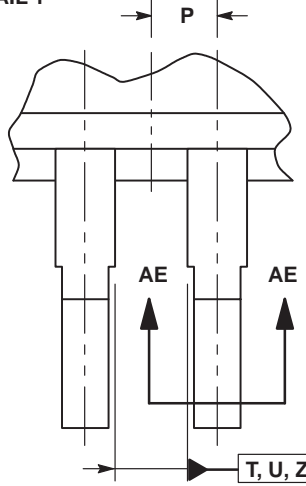
NOTES: 1. R8 must be set to match your 2nd IF filter impedance.
 2. Layout of capacitors C10, C11, C12 is critical for stability of Limiter.

OUTLINE DIMENSIONS

PLASTIC PACKAGE
CASE 932-03
(LQFP-48)
ISSUE F



DETAIL Y

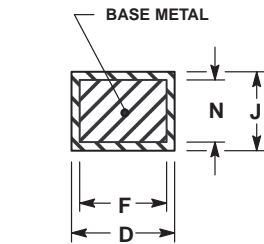
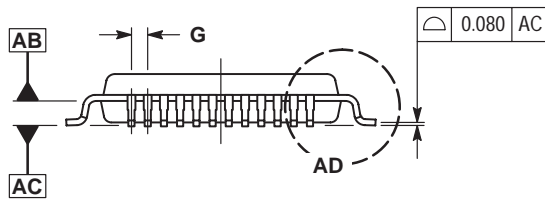


DETAIL Y

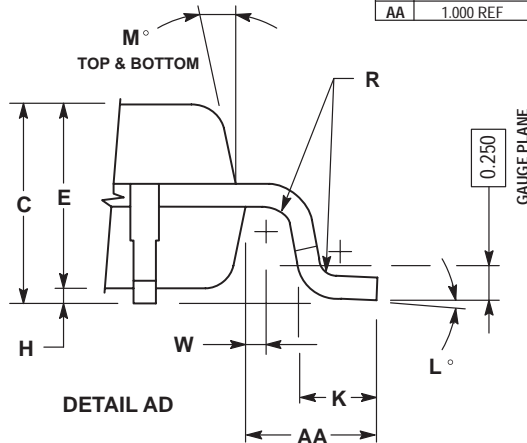
NOTES:

- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2 CONTROLLING DIMENSION: MILLIMETER.
- 3 DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
- 4 DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
- 5 DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE AC.
- 6 DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
- 7 DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350.
- 8 MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
- 9 EXACT SHAPE OF EACH CORNER IS OPTIONAL.

MILLIMETERS		
DIM	MIN	MAX
A	7.000	BSC
A1	3.500	BSC
B	7.000	BSC
B1	3.500	BSC
C	1.400	1.600
D	0.170	0.270
E	1.350	1.450
F	0.170	0.230
G	0.500	BSC
H	0.050	0.150
J	0.090	0.200
K	0.500	0.700
L	0 °	7 °
M	12 °	REF
N	0.090	0.160
P	0.250	BSC
R	0.150	0.250
S	9.000	BSC
S1	4.500	BSC
V	9.000	BSC
V1	4.500	BSC
W	0.200	REF
AA	1.000	REF



SECTION AE-AE



DETAIL AD

NOTES


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NOTES

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