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MOTOROLA

MRFIC1819

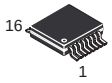
3.6 V 1800 MHz GaAs Integrated Power Amplifier

The MRFIC1819 is a single supply, RF power amplifier designed for the 1W DCS1800/PCS1900 handheld radio. The negative power supply is generated inside the chip using RF rectification, which avoids any spurious signal. A built in priority switch is provided to prevent Drain Voltage being applied on the RF lineup if not properly biased by the Negative Voltage. The device is packaged in the TSSOP–16EP package, with exposed backside pad, which allows excellent electrical and thermal performance through a solderable contact.

- Target 3.6 V Characteristics:
  RF Input Power: 6.0 dBm
  RF Output Power: 33 dBm Typical
  Efficiency: 41% Typical
- Single Positive Supply Solution
- Negative Voltage Generator
- Positive Step–Up Voltage Generator
- V_{SS} Check Switch for Gate–Drain Priority

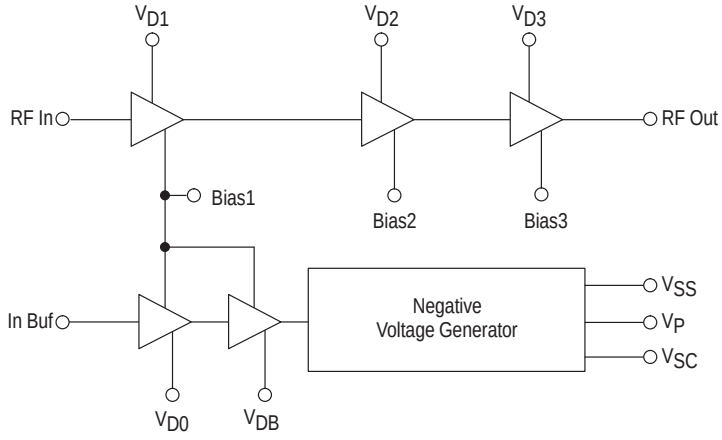
INTEGRATED RF POWER AMPLIFIER DCS1800/PCS1900

SEMICONDUCTOR TECHNICAL DATA



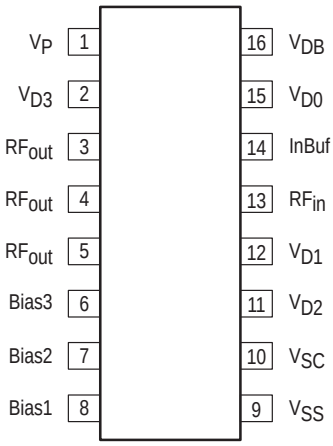
PLASTIC PACKAGE
CASE 948L
(TSSOP–16EP, Tape and Reel Only)

Simplified Block Diagram



This device contains 9 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temp Range	Package
MRFIC1819R2	T_A = –40 to 85°C	TSSOP–16EP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	$V_{D1, 2, 3}$	6.0	V
RF Input Power	P_{in}	12	dBm
RF Output Power	P_{out}	36	dBm

NOTES: 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Recommended Operating Contitions or Electrical Characteristics tables.
2. ESD (electrostatic discharge) immunity meets Human Body Model (HBM) ≤250 V and Machine Model (MM) ≤60 V. This device is rated Moisture Sensitivity Level (MSL) 4. Additional ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{D0}, V_{DB}, $V_{D1, 2, 3}$	3.0	–	5.0	Vdc
Input Power	P_{in}	5.0	–	10	dBm
Input Frequency	f_{RF}	1700	–	1900	MHz
Operating Case Temperature Range	T_C	–40	–	85	°C
Storage Temperature Range	T_{stg}	–55	–	150	°C

ELECTRICAL CHARACTERISTICS ($V_{D0} = V_{DB} = 3.6$ V, $V_{D1, 2, 3} = 3.6$ V, $P_{in} = 6.0$ dBm, Peak measurement at 12.5% duty cycle, 4.6 ms Period, $T_A = 25°C$, unless otherwise noted.)

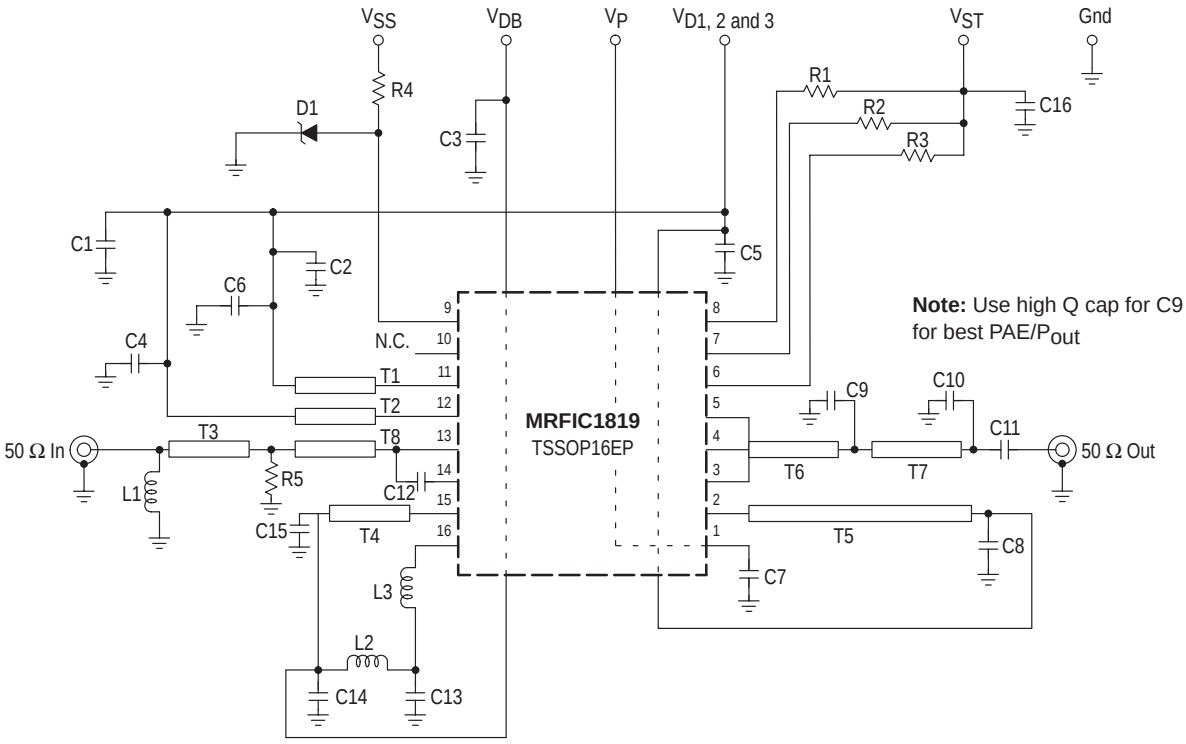
Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	1710	–	1785	MHz
Output Power	P_{out}	32	33	–	dBm
Power Added Efficiency	PAE	35	41	–	%
Output Power (Tuned for PCS Band 1850 to 1910 MHz)	P_{out}	–	33	–	dBm
Power Added Efficiency (Tuned for PCS Band 1850 to 1910 MHz)	PAE	–	41	–	%
Output Power at low voltage ($V_{D0} = V_{DB} = 3.0$ V, $V_{D1, 2, 3} = 3.0$ V)	P_{out}	30.5	31	–	dBm
Harmonic Output $2f_0$ $3f_0$	–	 – –	 –45 –35	 –40 –30	dBc
Input Return Loss	|S11|	–	12	–	dB
Output Power Isolation ($P_{in} = 10$ dBm, $V_{D0} = V_{DB} = 3.0$ V, $V_{D1, 2\&3} = 0$ V)	P_{off}	–	–30	–	dBm
Noise Power (In 100 kHz, 1805 to 1880 MHz)		–	–90	–	dBm
Negative Voltage ($P_{in} = 6.0$ dBm, $V_{D0} = V_{DB} = 3.0$ V)	V_{ss}	–4.85	–	–	V
Negative Voltage Setting Time ($P_{in} = 6.0$ dBm, VD0 = V_{DB} stepped from 0 to 3.0 V)	T_s	–	0.7	–	µs
Positive Voltage ($P_{in} = 6.0$ dBm,$V_{D0} = V_{DB} = 3.0$ V)	V_P	5.7	6.6	–	V
Stability–Spurious Output ($P_{out} = 0$ to 33 dBm, Load VSWR 6:1 all phase angles, source VSWR = 3:1, at any phase angle, Adjust $V_{D1, 2\&3}$ for specified power)	P_{spur}	–	–	–60	dBc
Load Mismatch Stress ($P_{out} = 3$ to 33 dBm, Load VSWR = 10:1 all phase angles, 5 seconds, Adjust $V_{D1, 2\&3}$ for specified power)	No Degradation in Output Power Before & After Test				

Table 1. Optimum Loads Derived from Circuit Characterization

f MHz	Z_{in} OHMS		Z_{OL}* OHMS	
	R	jX	R	jX
1710	14.51	–66.87	5.88	3.30
1720	14.67	–67.40	5.86	3.20
1730	14.82	–68.07	5.79	3.10
1740	15.08	–68.73	5.74	2.93
1750	15.30	–69.29	5.67	2.75
1760	15.55	–69.80	5.59	2.58
1770	15.80	–70.30	5.53	2.46
1780	16.00	–70.89	5.44	2.28
1790	16.16	–71.20	5.42	2.25

Z_{in} represents the input impedance of the device.
Z_{OL}* represents the conjugate of the optimum output load to present to the device.

Figure 1. Reference Circuit



C1,C2	47 nF	R4	1.0 kΩ
C3,C14	330 pF	R5	680 Ω
C4,C6,C8,C11,		L1	1.8 nH
C15,C16	22 pF	L2	33 nH
C5	10 nF	L3	2.7 nH
C7	2.7 pF	D1	Zener 5.1 V MMSZ4689T1
C9	3.9 pF AVX Accu–F	T1, T2	60 Ω Microstrip Line, L = 3.0 mm
C10	1.0 pF	T3	50 Ω Microstrip Line, L = 4.5 mm
C12	0.8 pF	T4	80 Ω Microstrip Line, L = 4.0 mm
C13	47 pF	T5	50 Ω Microstrip Line, L = 17 mm
R1,R2	15 kΩ	T6,T7	30 Ω Microstrip Line, L = 1.0 mm
R3	7.5 kΩ	T8	50 Ω Microstrip Line, L = 2.5 mm

Figure 2. 3.6 V DCS Application Circuit

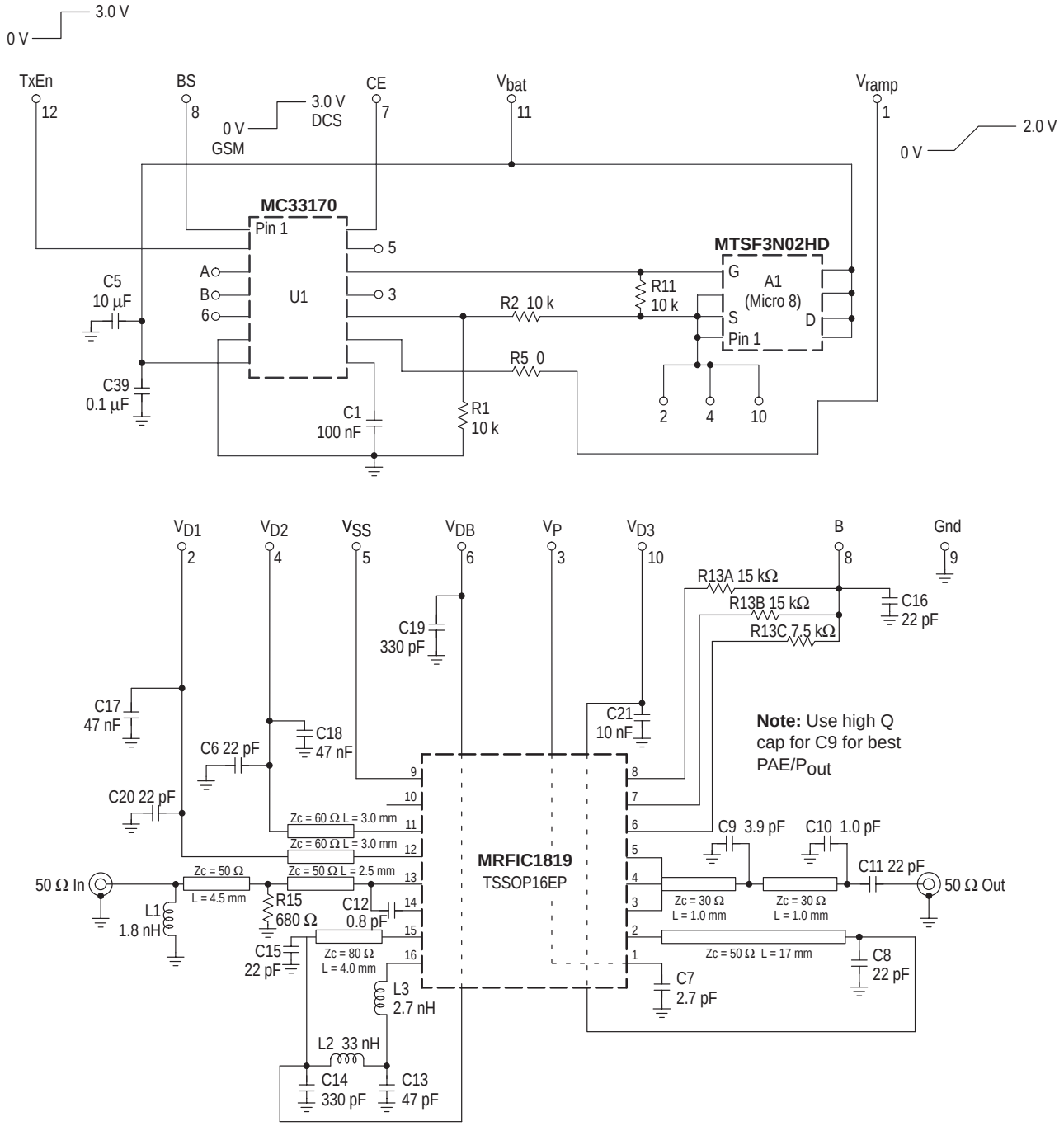


Figure 3. 3.6 V GSM & DCS IPA Dual–Band Application Circuit with Companion Chip & NMOS Switch

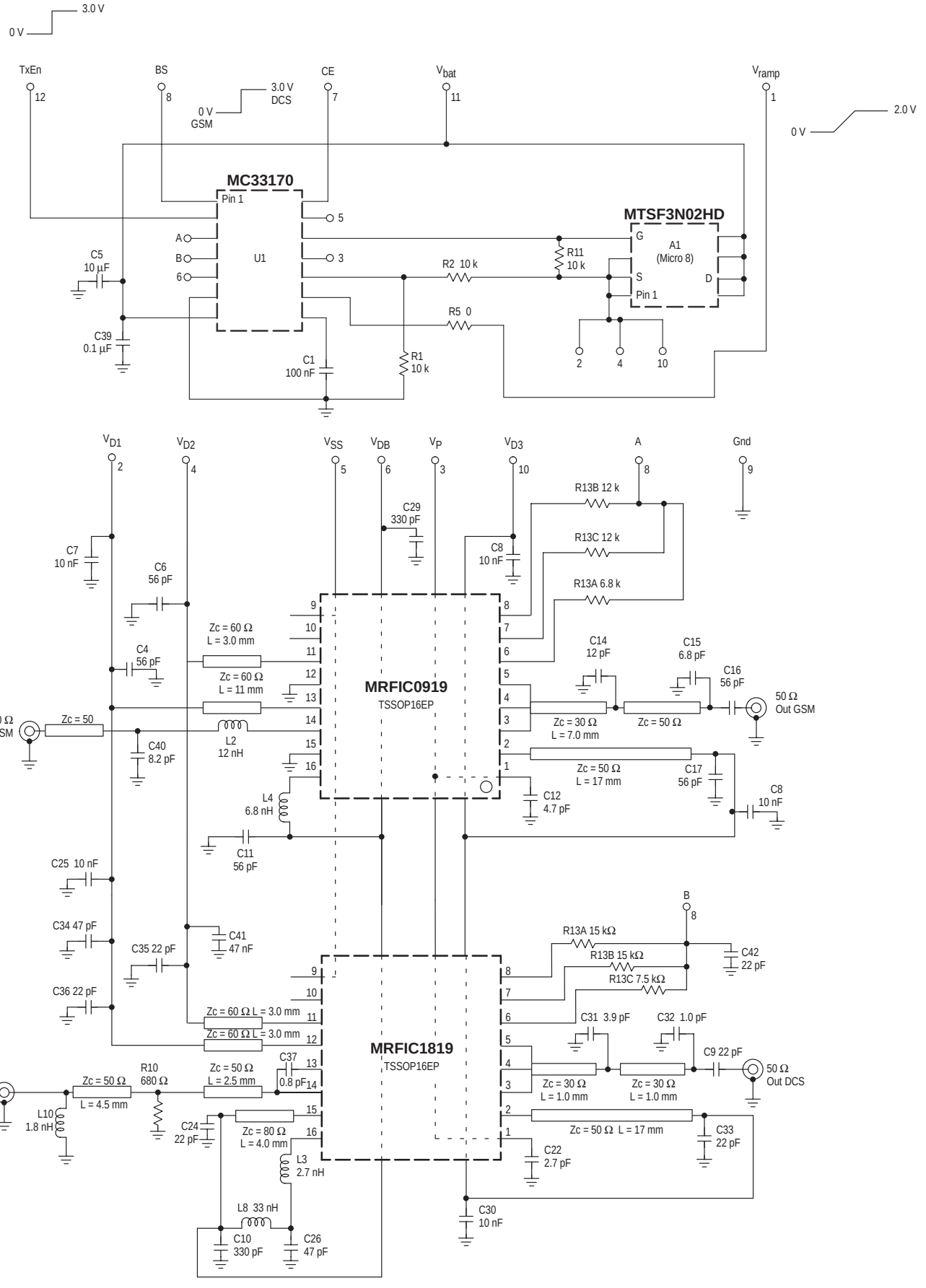


Figure 4. Output Power versus Frequency

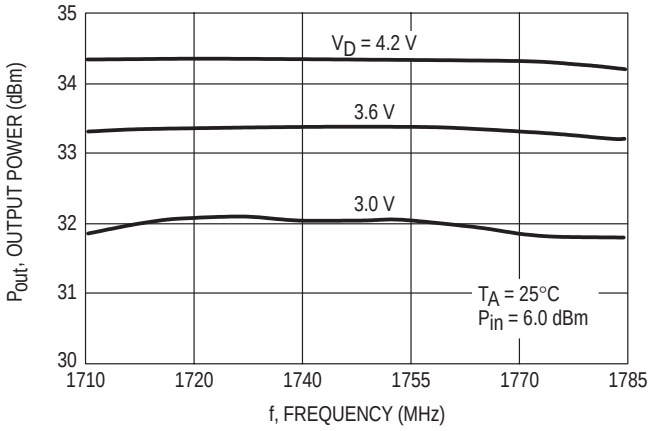


Figure 5. Power Added Efficiency versus Frequency

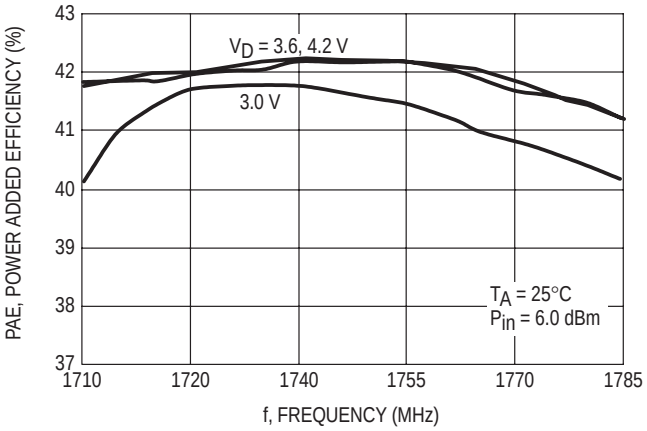


Figure 6. Output Power versus Frequency

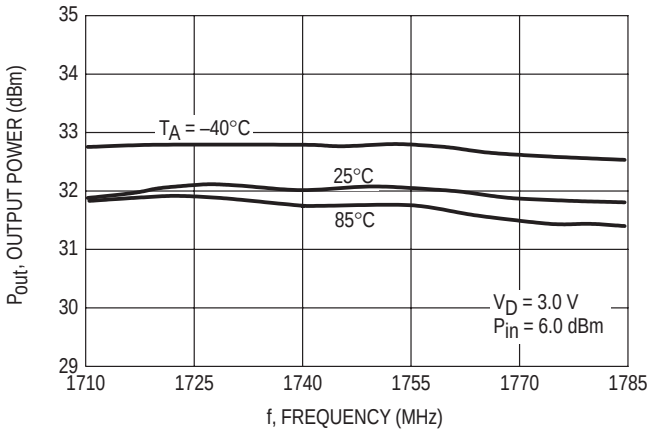


Figure 7. Output Power versus Frequency

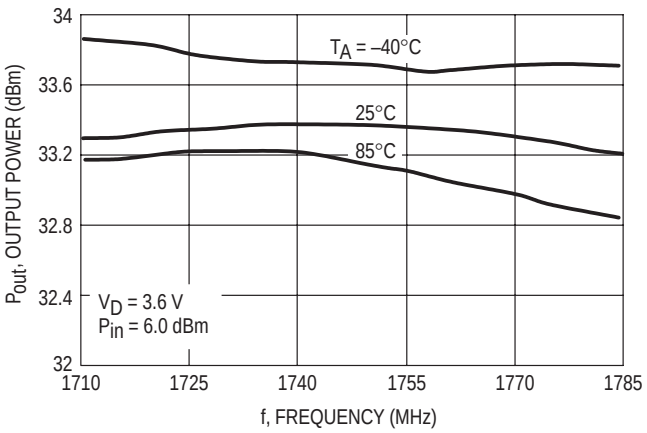


Figure 8. Output Power versus Frequency

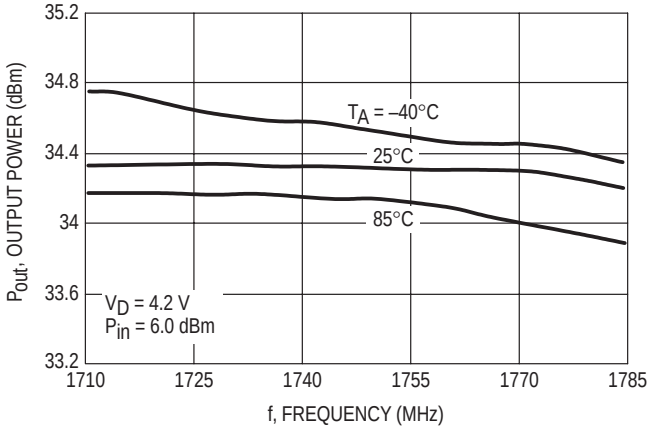


Figure 9. Power Added Efficiency versus Frequency

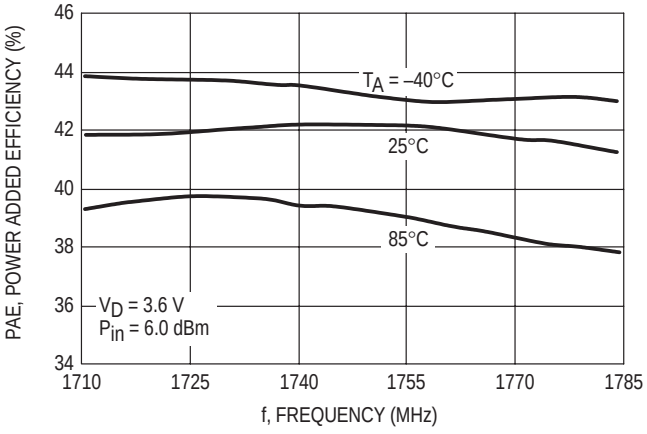


Figure 10. Output Power versus Drain Voltage

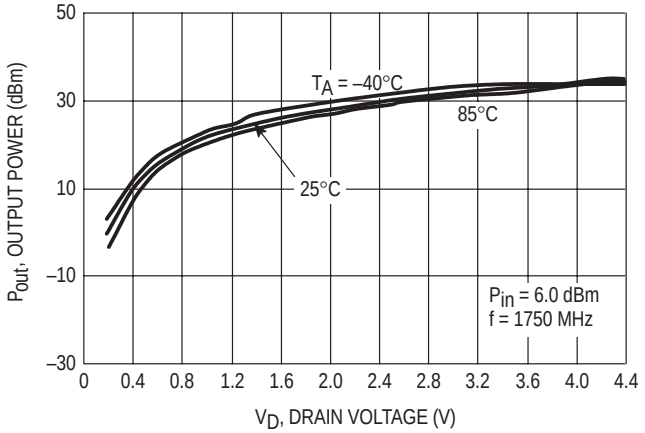


Figure 11. Power Added Efficiency versus Drain Voltage

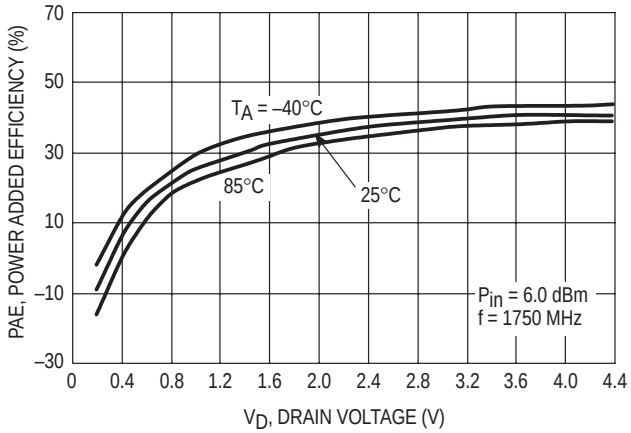


Figure 12. Positive Voltage Generator Output versus Drain Voltage

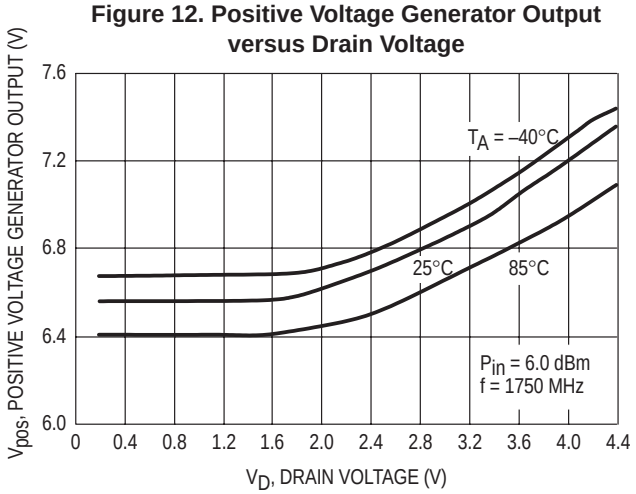
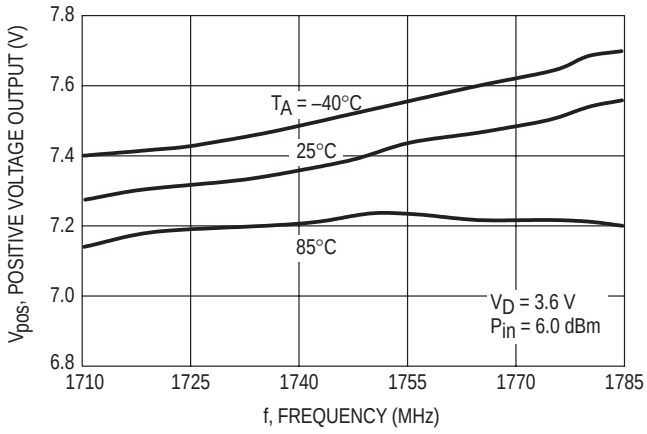


Figure 13. Positive Voltage Output versus Frequency



APPLICATIONS INFORMATION

Design Philosophy

The MRFIC1819 is a high performance three stage GaAs IPA (Integrated Power Amplifier) designed for DCS/PCS handheld radios (1710–1785 MHz DCS frequency band, 1850–1910 MHz PCS frequency band). With a 3.6 V battery supply, it delivers typically 33 dBm of Output Power with 41% Power Added Efficiency.

It features an internal Negative Voltage Generator based on RF rectification of the input carrier after its amplification by two dedicated buffer stages (see Internal Block Diagram). This method eliminates spurs found on the Output signal when using dc/dc converter type negative voltage generators, either on or off chip. The buffer also generates a step–up positive voltage which can be used to drive a N–MOS drain switch.

The RF input power is split **externally** (different from MRFIC0919) to the 3 stage RF line–up (Q1, Q2 and Q3) and the Buffer amplifier (Q0, QB). This arrangement allows separate operation of Voltage Generation and Power Amplification for maximum flexibility.

External Circuit Considerations

The MRFIC1819 can be tuned by changing the values and/or positions of the appropriate external components (see Figure 1: Reference Circuit). While tuning the RF line–up, it is recommended to apply external negative supply in order to prevent any damage to the power amplifier stages. Poor tuning on the input may not provide enough RF power to operate the negative voltage generator properly.

Input matching is a shunt–L, series–L high–pass structure and should be optimized at the rated RF Input power (e.g. 6.0 dBm). However, broadband matching is easier with a parallel 680 Ω resistor. This part can be removed to get operation to a lower input power (e.g. 5.0 dBm). Since the Input line feeds both 1st stage and buffer, Input matching should be iterated with Buffer and Q1 drain matching. Note that a dc blocking capacitor is included on chip.

RF input signal is fed to buffer amplifier using C12 capacitor (Figure 1). The value of this capacitor determines the power split between RF line–up and buffer amplifier. C12 has been tuned to get the best trade–off between RF gain and negative voltage on Pin 9.

First stage buffer amplifier is tuned with a short 80 Ω microstrip line which may be replaced by a chip inductor (T4 on Figure 1). Second stage buffer amplifier is supplied and matched through a discrete chip inductor. Those two elements are tuned to get the maximum output from voltage generator. The overall typical buffer current is about 50 mA; however, the negative generator needs a settling time of 2.0 μsec (see burst mode paragraph). During this transcient period of time, both stages are biased to IDSS which is about 200 mA each.

The step–up positive voltage available at Pin 1 is both decoupled and maximised by a small shunt capacitor. This positive voltage which is approximately twice the buffer drain voltage can be used to drive a NMOS drain switch for best performances.

Q1 drain is supplied and matched through a printed microstrip line that could be replaced by a discrete chip inductor as well. Its length (or equivalent inductor value) is tuned by sliding the RF decoupling capacitor along to get the maximum gain on the first stage.

Q2 is supplied through a printed microstrip line that contributes also to the interstage matching in order to provide optimum drive to the final stage.

The line length for Q1 and Q2 is small , so replacing it with a discrete inductor is not practical.

Q3 drain is fed via a printed line that must handle the high supply current of that stage (2.0 Amp peak) without significant voltage drop. This line can be buried in an inner layer to save PCB space or be a discrete RF choke.

Output matching is accomplished with a two stages low–pass network. Easy implementation is achieved with shunt capacitors mounted along a 2.0 mm 30 Ω microstrip transmission line. Value and position are chosen to reach a load line of 5.5 Ω while conjugating the device output parasitics. The network must also properly terminate the second and third harmonic to optimize efficiency and reduce harmonic level. Use of high Q capacitor for the first output matching capactor circuit is recommended in order to get the best Output Power and Efficiency performance.

NOTE: The choice of output matching capacitors type and supplier will affect H2 and H3 level and efficiency, because of series resonant frequency.

Biasing Considerations

The internally generated negative voltage is clamped by an external Zener diode in order to eliminate variation linked to Input power or Buffer supply. This negative voltage is used by three independent bias circuits to set the proper quiescent current of all stages. Each bias circuitry is equivalent to a current source sinking its value from the bias pin. When the bias pins are set to 3.0 V, nominal quiescent current and operating point of each RF stage are selected.

Q1 and Buffer share the Bias1 (0.25 mA) while Q2 and Q3 have dedicated Bias2 (0.25 mA) and Bias3 (0.5 mA) respectively. It is also possible to reference those bias pins to Gnd by changing series resistors R1, R2, R3 (Figure 1) that drops the 3.0 V.

If those pins are left opened, the corresponding stages are pinched–off. Thus the bias pins can be used as a mean to select the MRFIC1819 or the MRFIC0919 in a dual band configuration. The MRFIC0919 is the partner device to the MRFIC1819 and is designed for GSM900 applications.

Table 2. Pin Function Description

Pin	Symbol	Description
1	V_P	Positive voltage output
2	V_{D3}	Third stage drain supply
3	RF Out	RF output
4	RF Out	RF output
5	RF Out	RF output
6	Bias3	Third stage bias
7	Bias2	Second stage bias
8	Bias1	Buffer and first stage bias
9	V_{SS}	Negative voltage output
10	V_{SC}	Negative voltage check
11	V_{D2}	Second stage drain supply
12	V_{D1}	First stage drain supply
13	RF In	RF input
14	In Buf	Buffer RF input
15	V_{D0}	First buffer stage drain supply
16	V_{DB}	Buffer stage drain supply

V_{SC} is an open drain internal FET switch which is biased through the negative voltage. Consequently, this pin is high impedance when negative voltage is okay and low impedance (about 40 Ω) when negative voltage is missing.

Operation Procedure

The MRFIC1819 is a standard MESFET GaAs Power Amplifier, presence of a negative voltage to bias the RF line–up is essential in order to avoid any damage to the parts. Due to the fact that the negative voltage is generated through rectification of the RF input signal, a minimum input power level is needed for correct operation of the demoboard. The following procedure will guaranty safe operation for doing the RF measurements.

Note: make sure that Bias1 (Pin 8 of demoboard Figure 3) is connected 3.0 V or will have equivalent potential for nominal biasing of Buffer stage.

1. Apply RF input power (RF In) > 6.0 dBm.
2. Apply V_{DB} = 3.0 to 5.0 V.
3. Check that V_{SS} reaches approximatively –5.1 V (settling of the negative voltage) (Pin 9).
4. Apply $V_{D1,2\&3}$ = 3.0 to 5.5 V.
5. Measure RF output power and relevant parameters.

Proceed in the reverse order to switch off the Power Amplifier.

For linear operation, an external negative voltage will have to be supplied to the V_{SS} pin to maintain initial quiescent operating conditions of the FET amplifiers since the RF input will not provide sufficient voltage to operate the negative voltage generator. When using an external negative voltage supply, an input to the buffer (Pin 14) and supply voltages to V_{DB} (Pin 16) and V_{D0} (Pin 15), would no longer be required.

Control Considerations

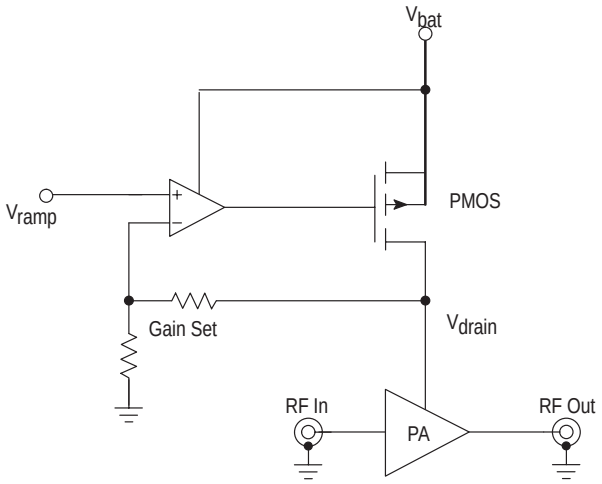
MRFIC01819 application uses the drain control technique developed for our previous range of GaAs IPAs (refer to application note AN1599). This method relies on the fact that for an RF amplifier operating in saturation mode, the RF output power is proportional to the square of the Amplifier drain voltage: Pout(Watt)=k*V_D(Volt)*V_D(Volt).

In the proposed application circuit (see Figure 2), a PMOS FET is used to switch the IPA drain and vary the drain supply voltage from 0 to battery voltage. As the PMOS FET has a non linear behavior, an OpAmp is included in the application. This OpAmp is linearizing the PMOS by sensing its drain output and gives a true linear relationship between the Control voltage and the RF output voltage.

The obtained power control transfer function is so linear and repeatable than it can be used to predict the output power within a dynamic range of 25 to 30 dB over frequency and temperature. This so called “open–loop” arrangement eliminates the need for coupler and detector required for the classical but complex closed–loop control and consequently reduces the Insertion Loss from Power Amplifier to the Antenna.

The block diagram (Figure 14) shows the principle of operation as implemented in the application circuit of Figure 2. The OpAmp is connected as an inverter to compensate the negative gain of the PMOS switch.

Figure 14. Drain Control through PMOS Switch



NOTE: The positive voltage generated by the Buffer stage can be used to supply the OpAmp and make it possible to drive a NMOS switch as a voltage follower. Doing so, the main advantage is to have a lower Rdson switch and better intrinsic linearity.

In Figure 15, the plot illustrates the “open–loop” performance regarding temperature stability. The measured datas are diplayed in a log–log scale in order to have a good representation of both the dynamic and the linearity of control. The variation of Pout accross the frequency band are also very small (less than 1.0 dB ripple) and are kept to that small amount when controlling Pout through the Drain voltage.

Figure 15. Temperature Stability of the Open Loop Control

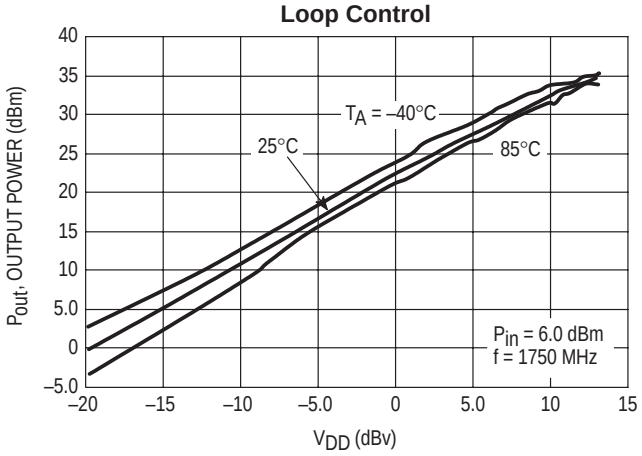
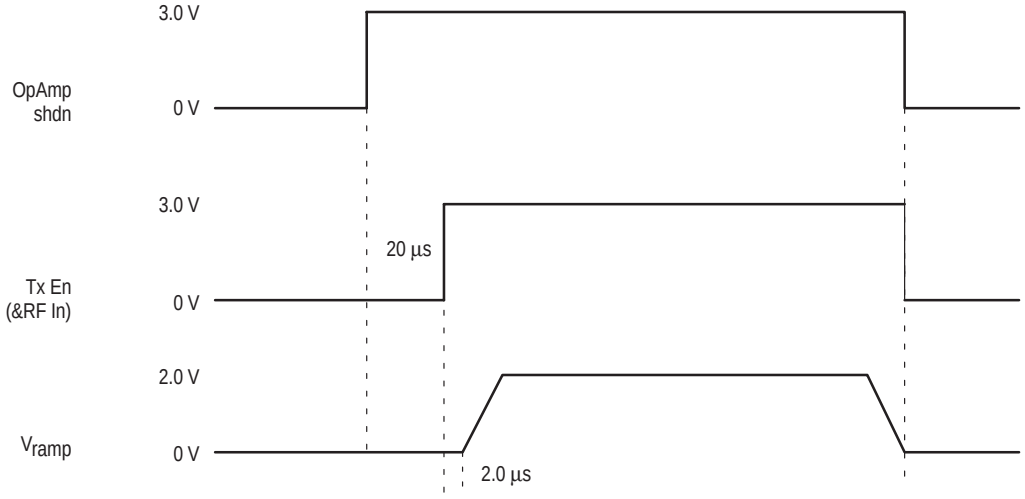


Figure 16. Timing Guide



Burst mode

Use Figure 16 as a guide line to perform burst mode measurements with the complete application circuit of Figure 2. Notice that the V_{SC} pin is connected to V_{ramp} (through a resistor) and acts as a pull down when negative voltage is missing so that drain voltage is not applied to the RF line–up.

– Bursting the OpAmp with its Pin 8 (shdn) is not mandatory during a call as the OpAmp current consumption is very small (1.0 to 2mA). This pin is mainly used for the idle mode of the radio. In any case, the wake–up time of the OpAmp is very short.

– V_{ramp} can be applied soon after Tx EN since the internal negative voltage generator settles in less than 2.0 µs.

– Tx EN signal can be used to switch the input power (using a driver or attenuator) in order to provide higher isolation for on/off burst dynamic.

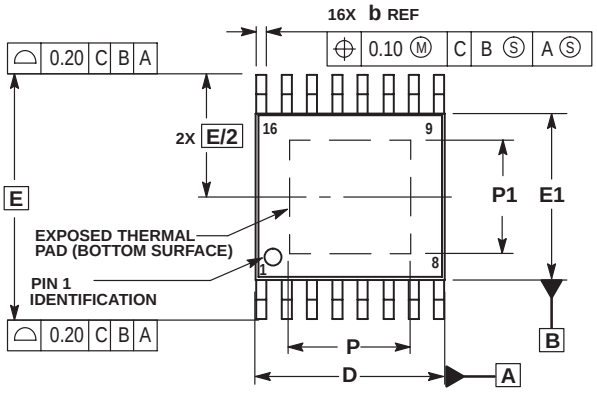
References (Motorola application notes)

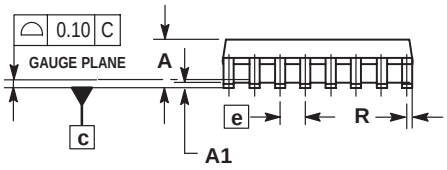
AN1599 – Power Control with the MRFIC0913 GaAs Integrated Power Amplifier and MC33169 Support IC.

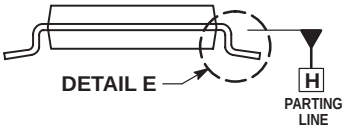
AN1602 – 3.6 V and 4.8 V GSM/DCS1800 Dual Band PA Application with DECT capability Using Standard Motorola RFIC's.

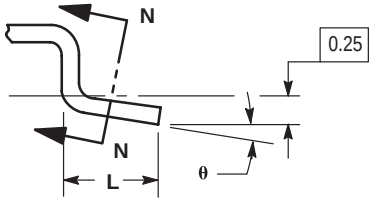
OUTLINE DIMENSIONS

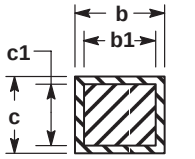
PLASTIC PACKAGE
CASE 948L–01
(TSSOP–16EP)
ISSUE O











NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
4. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE H.

	MILLIMETERS	
DIM	MIN	MAX
A	—	1.20
A1	0.00	0.10
b	0.19	0.30
b1	0.19	0.25
c	0.09	0.20
c1	0.09	0.16
D	4.90	5.10
E	6.40 BSC	
E1	4.30	4.50
e	0.65 BSC	
L	0.50	0.75
P	—	3.90
P1	—	3.00
R	0.18	0.28
θ	0°	8°

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