PLESSEY
Semiconductors

ADVANCE INFORMATION

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have '*pre-production*' status. Details given may, therefore, change without notice although we would expect this performance data to be representative of '*full production*' status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

MS2014

DIGITAL FILTER AND DETECTOR (FAD)

The MS2014 is a real time general purpose digital signal processor (DSP) which is easily programmed to perform digital filtering and level detection. The architecture of the FAD comprises a cascadable second order recursive filter and level detector using dedicated multipliers, adders and delay elements.

The data controlling the response of the MS2014 is stored in an external PROM or RAM and consists of a list of filter coefficients and comparison levels. This simple data format means that the user does not need an expensive development system at the design stage (in contrast to other DSP devices, which use microprocessor-based structures and require considerable software development effort to realise their function). The off-chip data memory allows for easy adaptive control, even when complicated algorithms are to be implemented.

The filter and detector have been designed to give maximum flexibility in use and can easily generate most of the functions required in tone detector, spectral analysis, adaptive filter and speech synthesis systems.

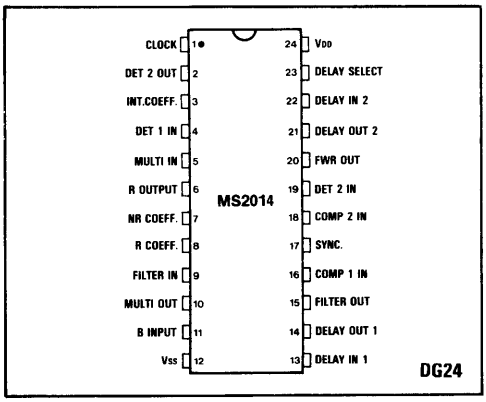

Fig.1 Pin connections - top view

FEATURES

- Linear 16-Bit Data
- 13-Bit Coefficient
- 2MHz Operating Clock Frequency
- Serial Operation
- 448 Bits of On-Chip Shift Register Data Storage for 8th Order Multiplex
- Nth Order Multiplexing (N≤8)
- TTL Compatible
- Single +5V Supply

APPLICATIONS

- Low Cost Digital Filtering
- Level Detection
- Spectral Analysis
- Tone Detectors (Multi-Frequency Receivers)
- Speech Synthesis and Analysis
- Data Modems
- Group Delay Equalisers (All-Pass Networks)

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD})	-0.5V to +7V
Input voltage	-0.5V to +7V
Maximum output voltage	+7V
Temperature: Storage	-65°C to 125°C
Operating	0°C to 70°C

NOTE
All voltages with respect to V_{SS}.

PIN NAMES

	Name	Function	I/O
1	Clock	Single phase clock input	I
2	Detect 2 Out	Output from detector 2	O
3	Int.Coeff	Integrator coefficients	I
4	DET 1 In	Detector 1 input	I
5	Mult In	Input to NR B multiplier	I
6	R Output	Output of recursive section	O
7	NR Coeff	Non-recursive (NR) coefficient input	I
8	R Coeff	Recursive coefficient input	I
9	Filter In	Data input to filter section	I
10	Mult Out	Output from B multiplier	O
11	B Input	Input from B multiplier	I
12	Vss	0V	
13	Delay In 1	Input from filter external delay	I
14	Delay Out 1	Output to filter external delay	O
15	Filter Out	Data output from filter section	O
16	Comp 1 In	Comparison level 1 input	I
17	Sync	Synchronisation pulse input	I
18	Comp 2 In	Comparison level 2 input	I
19	DET 2 In	Input for detector 2 via FWR	I
20	FWR Out	FWR output from Det 2 In data	O
21	Delay Out 2	Output from detectors 1 and 2, and connection to detector external delay	O
22	Delay In 2	Input from detector external delay	I
23	Delay Select	Internal/External delay selector	I
24	VDD	+5V supply	

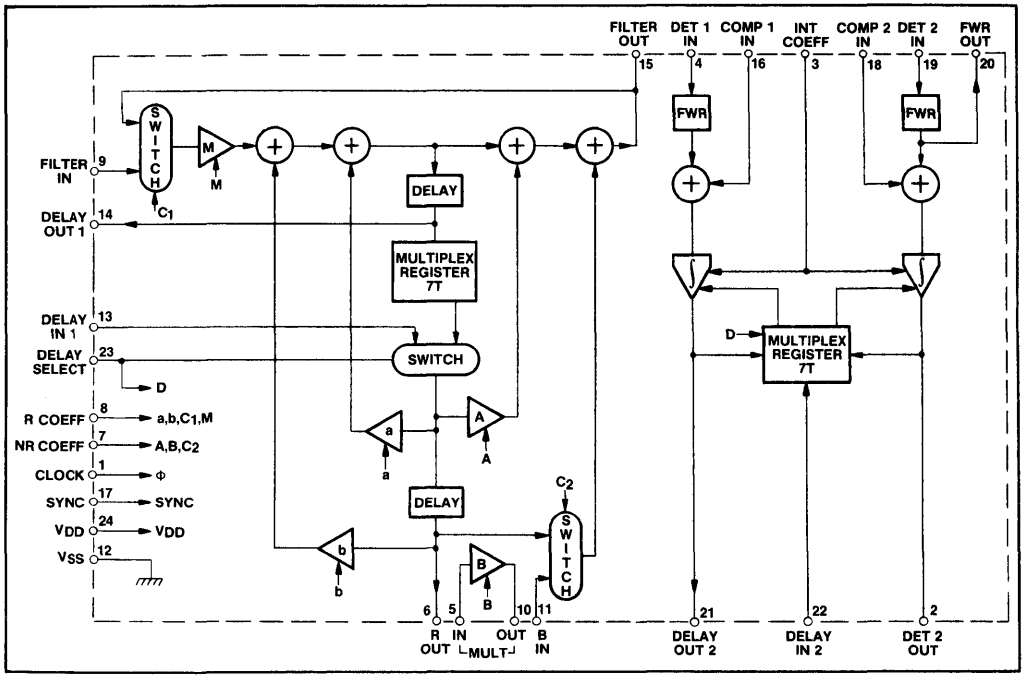

Fig.2 Block diagram

PERFORMANCE

A sample throughput of 64000 samples/s is guaranteed. Thus using a sampling period of 125μs (8000 samples/s) the following may be realised:

8 bi-quadratic 2nd-order recursive filter sections;
plus 16 full-wave rectification operations;
plus 16 1st-order leaky integrations;
plus 16 level comparisons.

Filters of more than 16th order are possible but will require a lower sampling rate or more than one MS2014.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value		Units	Conditions
		Min.	Max.		
Supply voltage	V_{DD}	4.75	5.25	V	
Input voltage (high state) except clock	V_{IH}	2.2	-	V	
Input voltage (low state) except clock	V_{IL}	-	0.7	V	
Input voltage (high state) clock	V_{IHC}	4.5	-	V	
Input voltage (low state) clock	V_{ILC}	-	0.5	V	
Clock rise and fall time	t_{cl}		30	ns	10% - 90% (Note 1)
Clock frequency	f_{cl}	0.5	2.048	MHz	
Operating temperature	T_{amb}	0	70	°C	

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD} = +5V T_{amb} = 25° C

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	I_{DD}		90	120	mA	
Output voltage, low	V_{OL}	-	-	0.5	V	I_{OL} = 0.4mA (Note 2)
Output voltage, high	V_{OH}	2.7	3.4	-	V	I_{OH} = -40μA (Note 2)
Input capacitance (except clock)	C_{in}		5	7	pF	
Input capacitance (clock)	C_{inc}		25		pF	
Input data set up time	t_{is}	50	-	-	ns	Fig.7
Input data hold time	t_{ih}	150	-	-	ns	Fig.7
Output data delay time	t_{os}	-	-	200	ns	Fig.7

NOTES
1. An operating clock frequency of 2.048MHz is guaranteed over the supply voltage range and the full operating temperature range.
2. The output stage is designed to drive a standard TTL LS gate (74LS series).

FUNCTIONAL DESCRIPTION

The Filter Section

The filter section provided in the MS2014 is a second order recursive type (see Fig.3). This structure was chosen because of its good coefficient sensitivity and predictable round-off, limit-cycle and overflow properties. Higher order filters are easily produced by cascading sections in a similar manner to analogue active filter design.

The transfer function of the section is given by:

$$H(z) = M \frac{[1 + Az^{-1} + Bz^{-2}]}{[1 - az^{-1} - bz^{-2}]} \quad \ldots (1)$$

The coefficients a and b define a pair of complex poles, whilst A and B define a pair of complex zeros. The Scaling Factor M is necessary because many filters have greater than unity gain, hence there is a danger of numeric overflow in the filter arithmetic. In the MS2014 this scaler multiplies by a factor of

$$M = (\tfrac{1}{2})^n \text{ where } 0 \leqslant n \leqslant 13$$

The multipliers in the MS2014 are serial/parallel types which require the coefficient data as a static parallel word. To minimise the number of pins on the device, this data is loaded serially and stored in a SIPO shift register. Each multiplier requires the coefficient data to be in 2s complement form with 12 bits for the fractional part of the number.

The range for the coefficients are:

$$\begin{aligned} 2 &> A \geqslant -2 \\ 2 &> a \geqslant -2 \\ 1 &\geqslant B \geqslant -1 \\ 1 &> b \geqslant -1 \end{aligned}$$

For the A,a coefficients there is an added bit ($a_S A_S$) to give the extra ± 1 range, which gives a total of 14 bits for the A,a coefficients and 13 bits for B,b.

The second-order filter is very easily multiplexed by increasing the delay function in steps of T (where T is the computation period*) and time-sharing the arithmetic elements. The limit on this process is the maximum clock rate of the MS2014. With a 32 bit computation cycle the clock rate f_{cl} is given by:

$$f_{cl} = 32 \times f_s \times Y$$

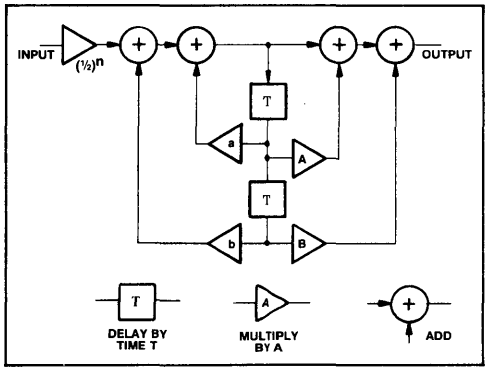

Fig.3 Basic 2nd order filter section

where Y is the number of times the filter is multiplexed and f_s is the sampling rate (the reciprocal of the sampling period T_s **). In telephony applications it is usual for f_s to be 8000 samples/s; hence at the maximum guaranteed clock rate of 2048kHz, Y must be less than or equal to 8.

By presenting an input sample during every 32-bit computation cycle, 8 separate second-order filters can be implemented. As the inputs can be independent of each other the filter is then said to be 'channel multiplexed'.

Filters of higher order can be built by feeding the output data emerging from one second-order section back to the input via an on-chip data selector, which is enabled by the control bit C_1; since the delay between the input and output of the filter section is 32 clock periods, the data arrives at the beginning of the next computation cycle. Thus by controlling the data selector two or more second-order filter sections can be cascaded. This arrangement allows any combination of filter and channel multiplexing to be achieved.

Higher orders of channel or filter multiplex require the connection of additional delay. For 8th-order multiplex, a delay of $7T$ (224 bits) is provided on chip; together with the inherent delay T (32 bits) of the computation cycle, this

*T = computation period = 32 x (1/2048k)s = 15.63µs i.e. 32 bits at 2048 kbit/s clock rate.

**T_S = sampling period = (1/8000)s = 125µs at a sampling rate of 8kHz i.e. 256 bits at 2048 kbit/s clock rate.

makes up the necessary $8T$ delay. Other orders of multiplex require the external connection of $(Y - 1) \times 32$ bits of delay.

The detector function is carried out by 'full wave rectifiers' followed by comparators and leaky integrators. By interconnecting these in different ways various absolute and relative level decisions can be made.

The 'Full Wave Rectifiers'

Data entering the 'full wave rectifiers' is inverted if the sign bit of the word is a '1' (i.e. negative). The 1LSB error generated by this is insignificant and does not materially affect operation of the detector.

The Integrators

The integrators in the MS2014 are unity gain variable-leak-factor types. Fig.4 shows the internal arrangement. The leak factor

$$1\text{-}2^{-(K + 1)}$$

controls the rise time of the integrator, the relationship is given in Table 1.

Level Detection

Both relative and absolute level detectors can be implemented in the MS2014. Fig.5 shows the arrangement for an absolute level detector. The sign bit of the data word emerging from the integrator is '1' if the mean level of the filter output is greater than the comparator input level.

Relative level detection can be achieved by using the arrangement of Fig.6. In most applications where relative level sensing is required, the filtering can be arranged such that $B = 1$ (i.e. the complex zeros are located on the unit circle in the z plane), this allows the B multiplier to be used for scaling the relative levels. In this application the B coefficient must be negative.

Leak factor	Rise time (0 to 90%)
1/2	3 Ts + T
3/4	8 Ts + T
7/8	17 Ts + T
15/16	35 Ts + T
31/32	72 Ts + T
63/64	146 Ts + T
127/128	293 Ts + T
255/256	588 Ts + T

Table 1 Integrator rise times

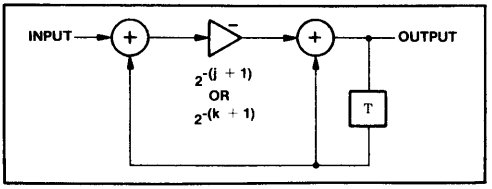

Fig.4 Leaky integrator

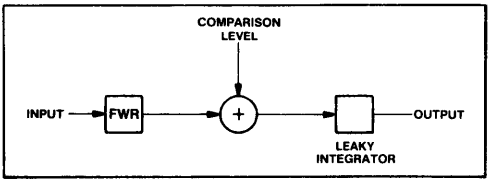

Fig.5 Simple level detector

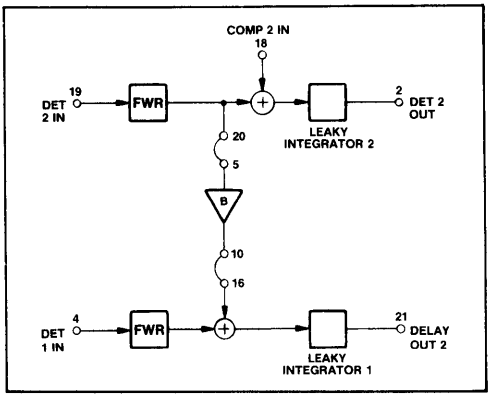

Fig.6 Relative level detection

FILTER DESIGN WITH THE MS2014

One of the commonest techniques for designing analogue filters is to factor the transfer function into blocks which can be realised by second order filter sections. Most designs of this type are done using tables which give coefficients for equations of the form:

$$H(s) = \frac{Cs^2 + Ds + K}{Es^2 + Fs + 1} \quad \ldots (2)$$

Since the MS2014 filter section is a general second-order structure, the same design technique can be employed. By using the Bilinear Transform:

$$s = \frac{2}{T}\frac{(1 - z^{-1})}{(1 + z^{-1})} \quad \ldots (3)$$

it is possible to design digital filters from analogue prototypes. By substituting equation (3) into (2) and re-arranging the result into the form of equation (1) the following relationships are derived:

$$A = \frac{2KT^2 - 8C}{4C + 2DT + T^2}$$

$$a = \frac{8E - 2T^2}{4E + 2FT + T^2}$$

$$M = \frac{4C + 2DT + KT^2}{4E + 2FT + T^2} \quad \ldots (4)$$

$$B = \frac{4C - 2DT + KT^2}{4C + 2DT + KT^2}$$

$$b = \frac{2FT - 4E - T^2}{4E + 2FT + T^2}$$

These five equations allow an analogue filter design to be transformed into digital form.

In addition to the four coefficients required by the filter section the data streams fed to the NR and R coefficient inputs include the four bits setting the Scaling Factor M (M_1 to M_4) and two selector control bits C_1 and C_2.

When $C_1 = 1$, data applied to FILTER IN (pin 9) goes to the filter section, when $C_1 = 0$ data emerging on FILTER OUT (pin 15) is fed back to the filter at the start of the next computation cycle.

When $C_2 = 0$ the B multiplier is by-passed by a direct connection, setting $B = 1$.

Table 2 shows the format of the serial data words for the NR and R coefficient inputs. The timing diagram (Fig.7) shows where this fits into the computation cycle. The synchronising pulse (SYNC) is coincident with the first clock pulse of the cycle and must be low before the rising edge of

32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Clock Pulse Number
C_1	M_1	M_2	M_3	M_4	b Coeff. msb												lsb	a_S	a Coeff. (Recursive) msb													lsb	
X	X	X	X	C_2	B Coeff. msb												lsb	A_S	A Coeff. (Non-Recursive) msb													lsb	
0.125					0													0.73217773437														
1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	0	1	1	0	1	1	1	R
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	NR

Table 2 Filter data format

the clock. The SYNC pulse is applied every *Y* clock pulses, where *Y* = CLOCK RATE/SAMPLING RATE.

Coefficient Conversion

After the coefficients have been obtained (from the Bilinear Transform or FAD Development Program) they must be assembled in the format given in Table 2. The FAD Development Program gives the multiplier coefficients in a ready-to-use binary string format, other techniques will give numerical values for the coefficients which must be converted into binary strings.

Coefficient Conversion Algorithm for '*A*'

The algorithm for converting *A* or *a* to binary is as follows:

Obtain $A = \frac{|A|}{2} \cdot 8191$

Convert *A* into a binary number (13 bits)

If *A* is positive INVERT THE MSB AND APPEND '0' AS NEW MSB.

If *A* is negative INVERT ALL BITS AND APPEND '1' AS NEW MSB, then ADD '1' LSB.

Conversion of '*B*' Coefficients

Obtain $B = B.4096$

Convert *B* into a binary number (12 bits)

If *B* is negative INVERT ALL BITS, ADD '1' LSB AND APPEND '1' AS NEW MSB.

If *B* is positive APPEND '0' AS NEW MSB.

In addition to the coefficient data streams one further input must be set up. DELAY SELECT (pin 23) is the control pin used to select the internal 7*T* delay. A '1' maintained on pin 23 selects the internal delay and a '0' the external option. The *B* multiplier is independent of the rest of the circuit and may be used for any purpose, although usually it will form part of either the filter or detect functions. In each case the appropriate connections must be made externally.

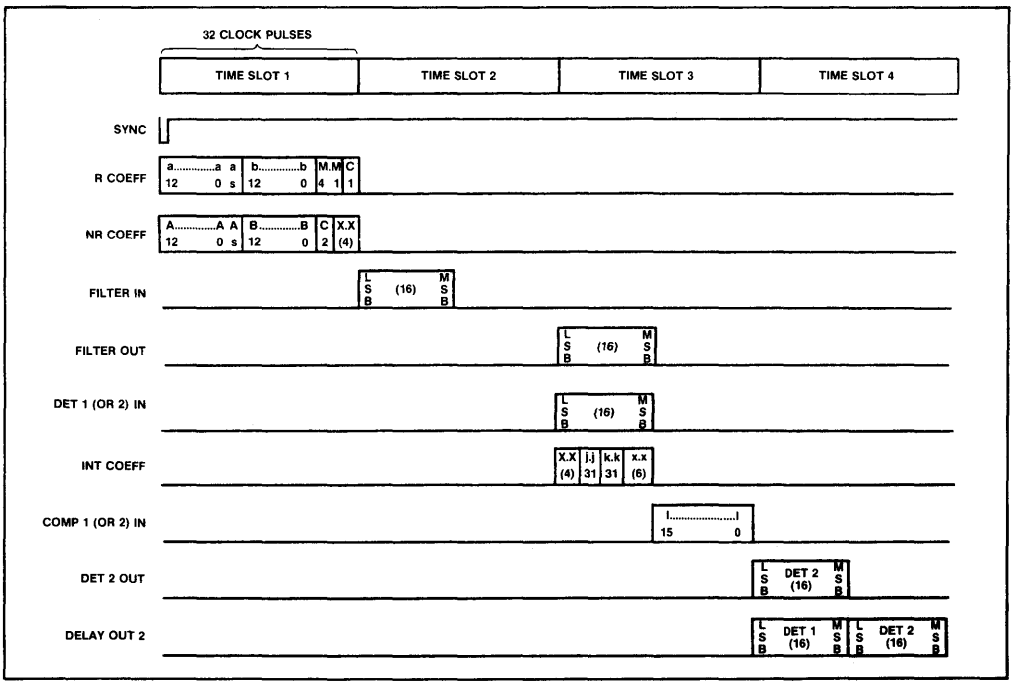

Fig.7 Timing diagram

Clock pulse number	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Integrator coefficients	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	K_1	K_2	K_3	J_1	J_2	J_3	X	X	X	X
Comparison level 1 or 2	P_0	P_1	P_2	P_3	P_4	P_5	P_6	P_7	P_8	P_9	P_{10}	P_{11}	P_{12}	P_{13}	P_{14}	P_{15}	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 3 Detector data format

Programming the Detector

Control data for the detect function is supplied by an external memory to the INT COEFF input (pin 3) and to the COMP 1 IN and COMP 2 IN inputs (pins 16 and 18) of the MS2014. The relative positions in time of the input sample data, detect function control data and output sample data are shown on the timing diagram (Fig.7).

Note that it is possible to economise on memory by strapping pin 3 either to pin 16 or to pin 18, since valid data for either combination of pins occurs at different times in the computation cycle. There are two integrator scaling factors in the INT COEFF data stream. The j_1, j_2, j_3 data bits determine the integrator coefficient for the data stream applied to DET 1 IN (pin 4) and the k_1, k_2, k_3 data bits for the DET 2 IN (pin 19) data stream; their definitions and clock pulse positions are given in Table 3.

In most applications, the comparison levels *l* and *m* applied to COMP 1 IN (pin 16) and COMP 2 IN (pin 18) will be negative quantities, and as they are coded in two's complement, each sign bit at clock pulse 32 will be a '1'. However,a positive quantity can be input by setting the sign bit to '0'. In this case, care must be taken to ensure that the addition of the DET data and the COMP data does not result in a number greater than unity and cause overflow, since no protection against overflow is provided in either detect function.

NOTE Round-off errors in the detector section may result in the integrator 'jamming' if the signal is below the 4 LSBs. Consequently, the available dynamic range is limited to the 12 MSBs.

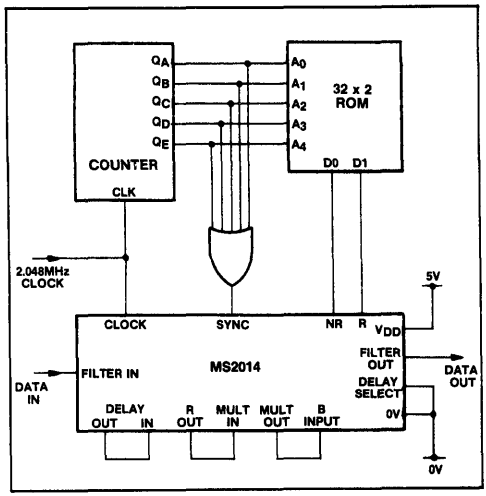

Fig.8 2nd order 32kHz bandwidth filter

TYPICAL APPLICATIONS CIRCUITS

A Second-Order High Sampling Rate Filter (Fig.8)

This is the simplest filter arrangement for the MS2014. No external delay is required so that DELAY 1 IN is connected to DELAY 1 OUT and DELAY SELECT is grounded.

A ÷32 counter generates the 5-bit wide address for the coefficient ROM. A 5-input OR gate on the address lines generates the SYNC pulse every 32 clock cycles so that at a 2.048MHz clock rate the sample rate is 64000 samples/second giving a maximum bandwidth of 32kHz.

If the desired *B* coefficient is not unity then ROUT (pin 16) must be connected to MULT IN (pin 5) and MULT OUT (pin 10) to *B* INPUT (pin 11).

A 16th Order Filter 8kHz Sample Rate Fig.9)

In this example DELAY SELECT (pin 23) is high so that the internal *7T* delay is switched in. Input data is applied during the first computation cycle (the one with the SYNC pulse in it) and coefficient data is loaded in the last computation cycle.

Channel Multiplexed Second Order Filter 8kHz Sampling

The hardware for this filter is identical to Fig.9. However, input data is provided during each computation cycle and each cycle contains a separate output. If the filter required for each channel is identical, then the coefficient memory need only be 32 x 2 bits.

Other Configurations

Sampling rates other than 64kHz and 8kHz can be achieved either by reducing the clock rate and/or by using external delays in place of the internal 0/*7T*. The use of external delay also allows different orders of multiplexing.

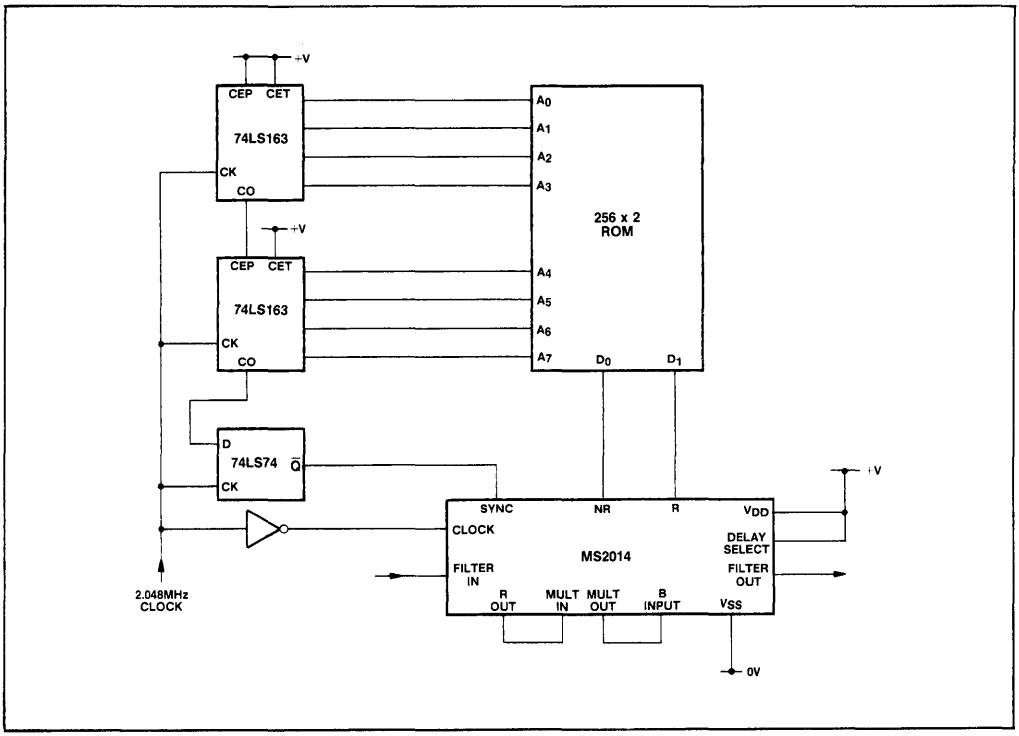

Fig.9 A 16th order 4kHz bandwidth filter

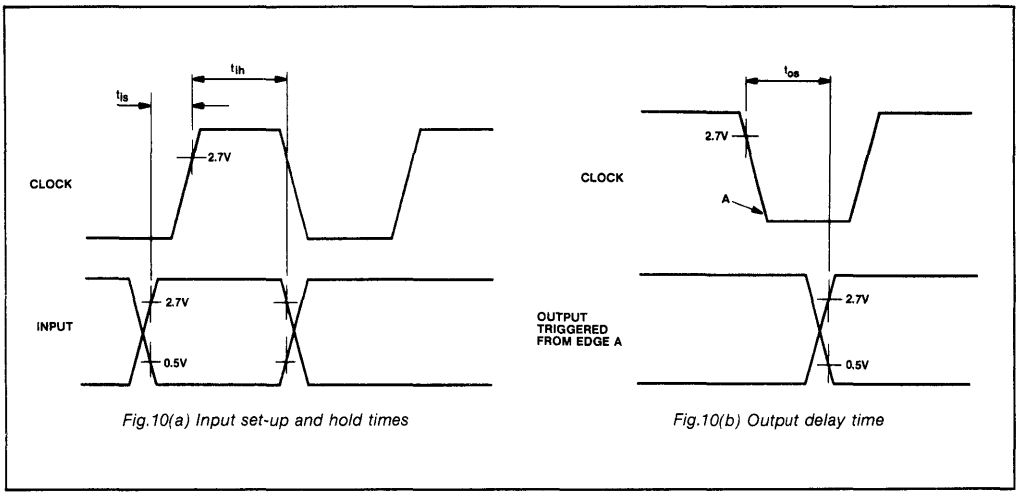

Fig.10(a) Input set-up and hold times

Fig.10(b) Output delay time

Fig.10 Input and output timing