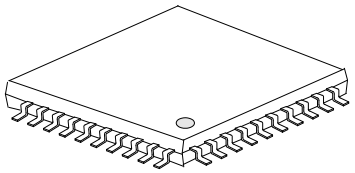
Ethernet Transceiver

PRODUCT DESCRIPTION

The MS2201 is a gigabit ethernet transceiver, which could achieve super high-speed full-duplex data transmission. The communication follows the timing requirement protocol of 10-bit interface in the IEEE 802.3 Gigabit Ethernet protocol. The MS2201 supports data transmission rate ranging from 1Gbps to 1.85Gbps.



TQFP64

FEATURES

- Power Supply : 2.5V, 3.3V
- Operating Temperature : -40°C~100°C
- Transmission Data : 1Gbps~1.85Gbps
- Low Power Dissipation : Less than 200mW at 1.25Gbps
- Compatible with LVPECL High-speed Differential I/O Interface
- Single PLL
- Support 10-bit Interface or 5-bit Interface (Double Data Rate)
- Support Receiving Minimum 200mV Differential-mode Voltage for Differential Signal
- Support 3.3V LVTTL Input
- Hot-plug Protection
- Follow IEEE 802.3 Gigabit Ethernet Protocol
- Follow IEEE 1149.1 JTAG Protocol

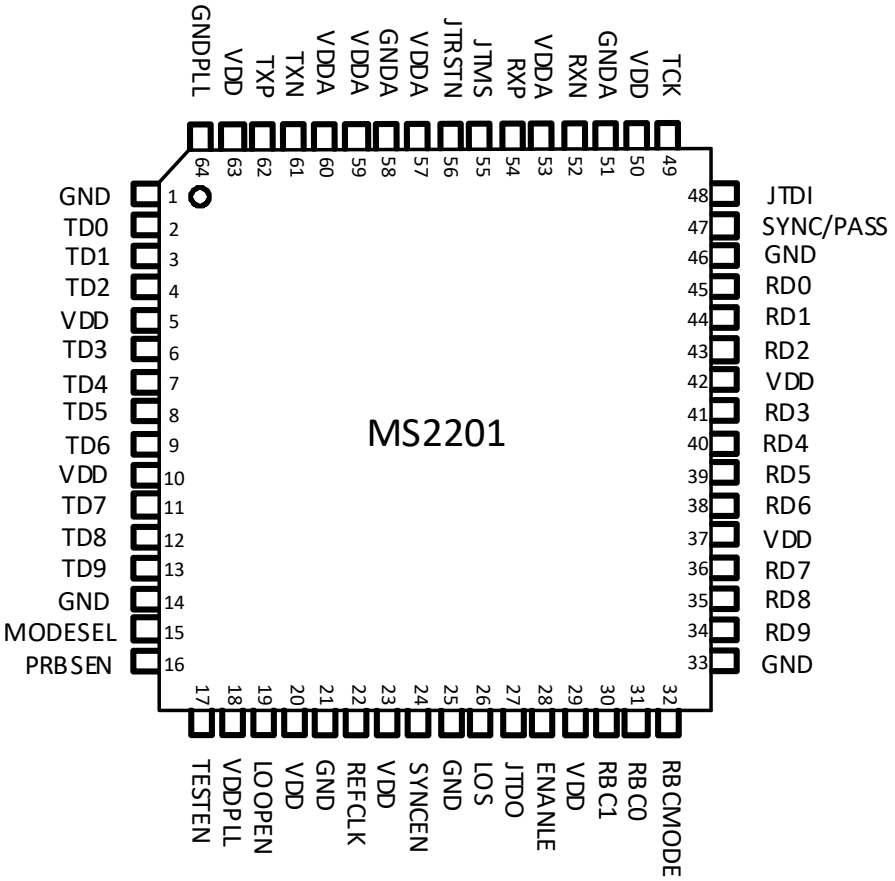
APPLICATIONS

- Optical Fibre Communication

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS2201	TQFP64	MS2201

PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
Signal			
TXP	62	PECL O	Different Output of Transmit Terminal. TXP and TXN as differential serial interfaces are connected to copper wire or optical fibre I/F unit. When LOOPEN is high-level, TXP and TXN are high0impedance state; When LOOPEN is low-level, TXP and TXN are activated.
TXN	61		
RXP	54	PECL I	Differential Input of Receive Terminal. RXP and RXN as differential serial input interfaces are connected to copper wire or optical fibre I/F unit.
RXN	52		
REFCLK	22	I	Reference Clock. REFCLK is external input clock, making receiver and transmitter synchronized (100MHz-185MHz). Transmitter uses the clock to storage input data (TD0-TD9) and then sends to serializer. In TBI mode, data is stored on REFCLK rising edge. In DDR mode, data is stored on REFCLK rising and falling edges. The data starts to combine from MSB on REFCLK rising edge.
TD0-TD9	2-4, 6-9, 11-13	I	Transmit Data. In TBI mode (MODESEL low-level), the input parallel 10-bit data is output from a protocol device to transceiver and then output serially. The 10-bit parallel data is clocked into transceiver, and TD0 is as the first bit of serial output. In DDR mode (MODESEL high-level), only TD0-TD4 are activated. 5-bit parallel data is input to transceiver on REFCLK rising and falling edges, and TD0 is as the first bit of serial output.
RD0-RD9	34,35,36, 38,39,40, 41,43,44, 45	O	Receive Data. In TBI mode (MODESEL low-level), these output parallel 10-bit data is transmitted from transceiver to protocol layer. Data output refers to clock signal on RBC0,RBC1 and is affected by selected receive clock mode. RD0 is the first bit of receive data. In DDR mode (MODESEL high-level), only RD0-RD4 are activated. RD5-RD9 remain low level. 5-bit parallel data is output on RBC0 rising edge.
RBC0	31	O	Receive Bit Clock. RBC0 and RBC1 are recovery clocks, making 10-bit output data synchronized on RD0-RD9. These two clock outputs are affected by selected receive clock mode. In half-rate mode, 10-bit output data is valid on the rising edges of RBC0 and RBC1. These two clock phases are adjusted to half-word boundary according to synchronous detection. During data recombination, clock pulse width is always extended until data recombination ends. RBC0 stores bit 1 and bit 3 of receive data. RBC1 stores bit 0 and bit 2 of receive data. In normal-rate mode, only RBC0 is activated and frequency is 1/10 of serial data rate. Data is combined on the rising edge. In DDR mode, only RBC0 is activated and frequency is 1/10 of serial data rate. Data is combined on the rising and falling edges.
RBC1	30		

Pin	Name	Type	Description
RBCMODE	32	I P/D	Receive Clock Mode Selection. When RBCMODE and MODESE are all low-level, RBC0 and RBC1 output half-rate clock. When MODESEL is low-level and RBCMODE is high-level, RBC0 outputs full-rate rate and RBC1 remains low-level. When MODESEL is high -level, RBCMODE is unaffected and RBC0 outputs full-rate clock and RBC1 remains low-level.
SYNCEN	24	I P/U	Synchronization Function Enable. When SYNCEN is high-level, internal synchronization function is activated. If required, transceiver would detect K28.5 comma character in serial data, and recombine data on bit boundary. When SYNCEN is low-level, the serial input data is unframed on RD0-RD9.
SYNC/PASS	47	O	Synchronous Detection Flag. If comma character string is detected in serial data, SYNC outputs high-level. Only when SYNCEN is valid (high-level), SYNC outputs synchronous flag pulse. In PRBS test mode (PRBSEN high-level), SYNC/PASS outputs the result state of PRBS test (high-level indicates pass).
LOS	26	O	Signal Loss Flag. Indicate the loss situations of RXP and RXN signals receiving on high-speed differential input terminals. If RXP-RXN>150mV, LOS=1, input signal is valid If RXP-RXN<150mVand >50mV, LOS level is uncertain If RXP-RXN<50mV, LOS=0, input signal is lost.
MODESEL	15	I P/D	Mode Selection. Select 10-bit or 5-bit DDR Interface. When MODESEL is low-level, select 10-bit interface(TBI). When MODESEL is high-level, select 5-bit DDR mode. When MODESEL is floating, operate in TBI mode.
Test			
LOOPEN	19	I	Loop Enable. When LOOPEN is high-level (valid), internal loop is enabled. The transmitted serial data is directly through to the input terminal of receiver. After connection with protocol device, the loop provides self-detection function. During loop test, TXP and TXN outputs remain in high-impedance state. LOOPEN must be low-level, when in the normal operating state for valid external serial input and output.
TCK	49	I	Test Clock. IEEE1149.1 (JTAG)
JTDI	48	I	Test Data Input. IEEE1149.1 (JTAG)
JTDO	27	O	Test Data Output. IEEE1149.1 (JTAG)
JTRSTN	56	I P/U	Reset Signal. IEEE1149.1 (JTAG)
JTMS	55		Test Mode Selection. IEEE1149.1 (JTAG)

Pin	Name	Type	Description
ENABLE	28	I P/U	When the terminal is low-level, enable lddq test. RD0-RD9, RBC0, RBC1, TXP and TXN are high-impedance . So the pull-up and pull-down resistors are invalid on input terminal. When ENABLE is high-level, device operates normally.
PRBSEN	16	I P/D	PRBS Enable. When PRBSEN is high-level, PRBS generation circuit starts operation. PRBS detection circuit on receive terminal also starts operation. PRBS signal is input to receiver and detected for fault, that is indicated low-level on SYNC/PASS.
TESTEN	17	I P/D	Adjust Test Terminal
Power Supply			
VDD	5,10,20, 23,29,37, 42,50,63	-	Digital Power Supply. Provide power supply for all digital circuits and digital I/O buffers.
VDDA	53,57, 59,60	-	Analog Power Supply. Provide power supply for high-speed analog circuit, receiver and transmitter.
VDDPLL	18	-	PLL Power Supply. Provide power supply for PLL circuit. The terminal needs extra filtering.
Ground			
GNDA	51,58	-	Analog Ground. Provide grounding terminal for high-speed analog circuit, RX and TX.
GND	1,14,21, 25,33,46	-	Digital Ground. Provide grounding terminal for digital logic circuit and digital I/O buffer.
GNDPLL	64	-	PLL Ground. Provide grounding terminal for PLL circuit.

ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Ratings	Unit
Power Supply	VDD	-0.3 ~ 3.6	V
TTL Pin, Input Voltage	V_I	-0.5 ~ 4	V
Other Pin, Input Voltage		-0.3 ~ VDD+0.3	V
Storage Temperature	Tstg	-65 ~ 150	°C
ESD	CDM	1	kV
	HDM	2	kV

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power Supply 1	V_{DD}, V_{DDA}		2.3	2.5	2.7	V
Operating Current 1	I_{DD}, I_{DDA}	Frequency=1.25 Gbps, PRBS Format		80		mA
		Frequency=1.6 Gbps, Worst case Format(1)			111	mA
Total Power Dissipation 1	P_D	Frequency=1.25 Gbps, PRBS Format		200		mW
		Frequency=1.6 Gbps, Worst case Format(1)			300	mW
Low Power Dissipation Current 1	I_{DD}, I_{DDA}	Enable=0 Vdda,Vdd=2.7V			50	uA
Lock Time 1	PLL	VDD,VDDA=2.5V, EN ↑ to PLL Lock			500	us
Operating Temperature 1	T_A		-40		100	°C
Power Supply 2	V_{DD}, V_{DDA}		3.0	3.3	3.6	V
Operating Current 2	I_{DD}, I_{DDA}	Frequency=1.25 Gbps, PRBS Format		100		mA
		Frequency=1.6 Gbps, Worst case Format(1)			140	mA
Total Power Dissipation 2	P_D	Frequency=1.25 Gbps, PRBS Format		330		mW
		Frequency=1.6 Gbps, Worst case Format(1)			500	mW
Low Power Dissipation Current 2	I_{DD}, I_{DDA}	Enable=0 Vdda,Vdd=3.6V			60	uA
Lock Time 2	PLL	VDD,VDDA=3.3V, EN ↑ to PLL Lock			500	us
Operating Temperature 2	T_A		-40		100	°C

(1) Worst case format is the state of the maximum transition density of serial transceiver.

ELECTRICAL CHARACTERISTICS

Reference Clock (REFCLK) Timing Requirement

Parameter	Condition	Min	Typ	Max	Unit
Frequency	Minimum Data Rate	100-0.01%	100	100+0.01%	MHz
Frequency	Maximum Data Rate	185-0.01%	185	185+0.01%	MHz
Accuracy		-100		100	ppm
Duty Cycle		40%	50%	60%	
Jitter	Random plus Deterministic			40	ps

TTL Electrical Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output High-level Voltage	V_{OH}	I_{OH}=-400uA	V_{DD}-0.2		V_{DD}	V
Output Low-level Voltage	V_{OL}	I_{OL}=1mA	GND	0.25	0.5	V
Input High-level Voltage	V_{IH}		1.7		3.6	V
Input Low-level Voltage	V_{IL}				0.8	V
Input High Current	I_{IH}	V_{IN}=2.0V			40	uA
Input Low Current	I_{IL}	V_{IN}=0.4V	-40			uA
Input Equivalent Capacitance	C_{IN}				4	pF

Transmit/Receive Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Transmit Differential Signal, Differential-mode Voltage Vod = |TxD-TxN|		Rt=50Ω	600	850	1100	mV
		Rt=75Ω	800	1050	1200	
Transmit Differential Signal, Common-mode Voltage (TxP + TxN)/2	V_{CM}	Rt=50Ω	1000	1250	1800	mV
		Rt=75Ω	1000	1250	1800	
Receive Differential Signal, Differential-mode Voltage Vid = |RxP - RxN|			200		1600	mV
Receive Differential Signal, Common-mode Voltage (RxP + RxN)/2			1000	1250	2250	mV
Receiver Leakage Current	$I_{ikg(R)}$		-350		350	uA
Receiver Input Capacitance	C_I				2	pF
Total Jitter for Serial Data	$t_{(TJ)}$	Differential Output Jitter, Random plus Deterministic, PRBS Format, R_ω=125 MHz			0.24	UI

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Deterministic Jitter for Serial Data	$t_{(DJ)}$	Differential Output Jitter, PRBS Format, R_ω=125 MHz			0.12	UI
Differential Signal Rise, Fall Time (20%-80%)	t_r, t_f	R_L=50Ω, C_L=5pF, See Figure 1 and Figure 2	100		250	ps
Minimum Jitter Tolerance for Eye Diagram Opening		Differential Input Jitter, Random plus Deterministic, R_ω=125MHz	0.25			UI
Lock Time for Receive Data after Power up					500	us
Daata Re-lock Time after synchronization loss					1024	Bit times
Transmit Delay Time	$t_{d(Tx)}$	TBI Mode, See Figure 4	19		20	UI
		DDR Mode	29		30	
Receive Delay Time	$t_{d(Rx)}$	TBI Mode, See Figure 9	21		31	UI
		DDR Mode	27		34	

LVTTL Output Switching Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Clock Rise Time	t_r(RBC)	20%-80%, C=5pF, See Figure3	0.3		1.5	ns
Clock Fall Time	t_f(RBC)		0.3		1.5	
Data Rise Time	t_r		0.3		1.5	ns
Data Fall Time	t_f		0.3		1.5	
Data Setup Time (RD0-RD9)	t_{SU} (D1)	TBI normal Mode, See Figure 6	2.5			ns
Data Hold Time (RD0-RD9)	t_h (D1)		2			
Data Setup Time (RD0-RD4)	t_{SU} (D2)	DDR Mode, R_ω=125 MHz, See Figure 7	2			ns
Data Hold Time (RD0-RD4)	t_h (D2)		0.8			
Data Setup Time (RD0-RD9)	t_{SU} (D3)	TBI Half-rate Mode, R_ω=125 MHz, See Figure 5	2.5			ns
Data Hold Time (RD0-RD9)	t_h (D3)		1.5			

Transmitter Timing Requirement

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Data Setup Time (TD0-TD9)	t_{SU} (D4)	TBI Mode	1.6			ns
Data Hold Time (TD0-TD9)	t_h (D4)		0.8			
Data Setup Time (TD0-TD9)	t_{SU} (D5)	DDR Mode	0.7			ns
Data Hold Time (TD0-TD9)	t_h (D5)		0.5			
Data Rise, Fall Time	t_r, t_f	See Figure 3			2	ns

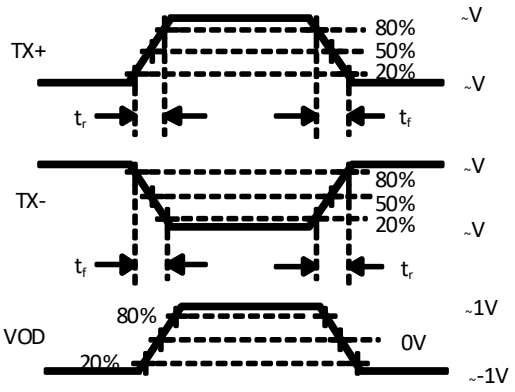


Figure 1. Definitions of Output Differential Signal and Common-mode Voltage

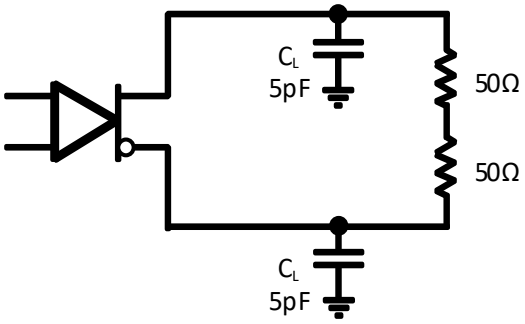


Figure 2. Setting of Transmitter Output Terminal

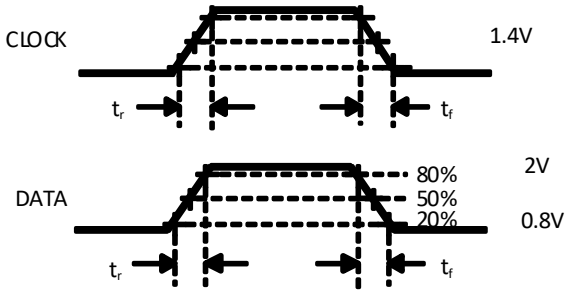


Figure 3. Valid Level of TTL I/O Data at AC Measurement

FUNCTION DESCRIPTION

Data Transmit

The MS2201 supports specified 10-bit interface (TB) and reduced 5-bit interface (DDR) using double clock. When MODESEL is low-level, select TBI mode; When MODESEL is high-level, select DDR mode.

In TBI mode, on the rising edge of REFCLK signal, the register of transmit part stores transmitted 10-bit data (8b/10b encoded data, TD0-TD9). In the following serializer, internal circuit multiplies the REFCLK frequency by 10 and makes it as clock signal of shift register. Finally, on the high-speed I/O channel, 8b/10b encoded data is serially output from bit0 to bit9.

In DDR mode, the circuit of transmit part receives 5-bit wide 8b/10b encoded data. In this mode, the MS2201 samples transmitted data on the rising and falling edges of REFCLK at the same time. Then, data is combined as 10-bit wide data and sent to serializer. Sample bit0-bit4 on REFCLK rising edge; sample bit5-bit9 on REFCLK falling edge (bit0 is the first transmitted data).

Transmission Latency

Data transmission latency is the delay time from 10-bit initial data to transmitter serial output bit9. In TBI mode, the minimum latency is 19-bit time; the maximum latency is 20-bit time. In DDR mode, the minimum latency is 29-bit time; the maximum latency is 30-bit time.

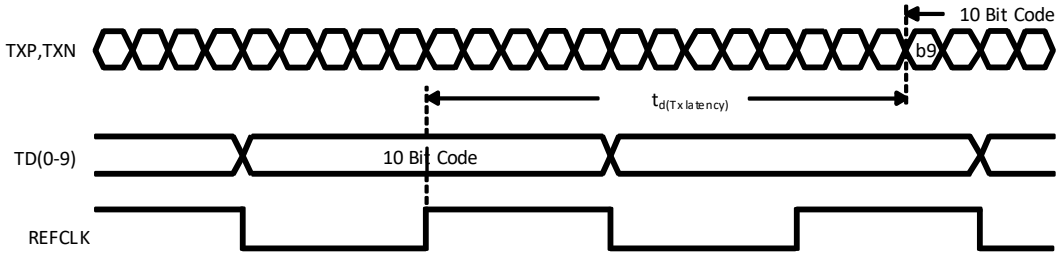


Figure 4. Transmit Latency in Full-rate Mode

Data Receive

The receive part deserializes the differential signal, where serial data is retimed bases on the clock generated by phase interpolation. Then serial data is recombined as a group of 10-bit parallel data, which is sent to the protocol controller following receive bit clock protocol (RBC0,RBC1).

Receive Clock Select Mode

The MS2201 has two parallel bus modes : 10-bit mode (TBI); 5-bit mode (DDR). In TBI mode, two optional clock modes are provided for user by RBCMODE pin : Full-rate clock output from RBC0 pin; Half-rate clock output from RBC0 and RBC1 pins. In DDR mode, only full-rate clock is output from RBC0 pin. The mode selection is shown as follows.

Table 1. Mode Selection

MODESEL	RBCMODE	MODE	Frequency
0	0	TBI Half-rate	100-125MHz
0	1	TBI Full-rate	100-185MHz
1	0	DDR	100-125MHz
1	1	DDR	100-125MHz

In half-rate mode, two receive clocks (RBC0, RBC1) have 180 degrees difference in phase and the frequencies are half of data rate. The receive clock is available by dividing recovered clock. The output data is reference for these two receive clocks, following certain protocol to clock the output data by the rising edges of RBC0 and RBC1. According to protocol, on RBC1 rising edge, byte0 of receiver output data is valid. The timing diagram is shown in figure 5.

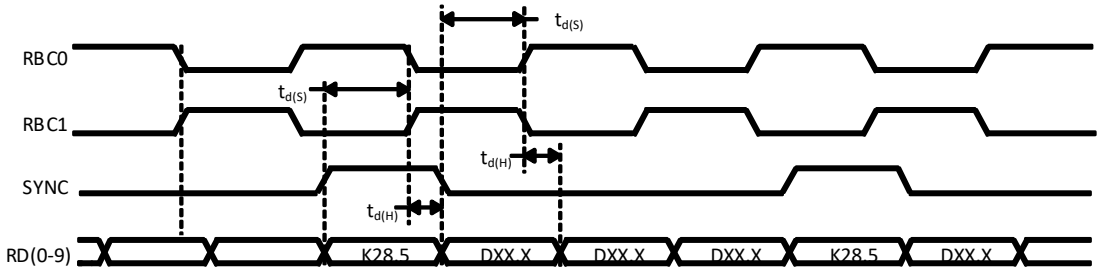


Figure 5. Synchronous Timing Characteristics Waveform (TBI half-rate mode)

In full-rate mode, only RBC0 clock is valid and operates in full-rate mode. Receive data is output by RBC0 rising edge and RBC1 is low-level. The timing diagram is shown in figure 6.

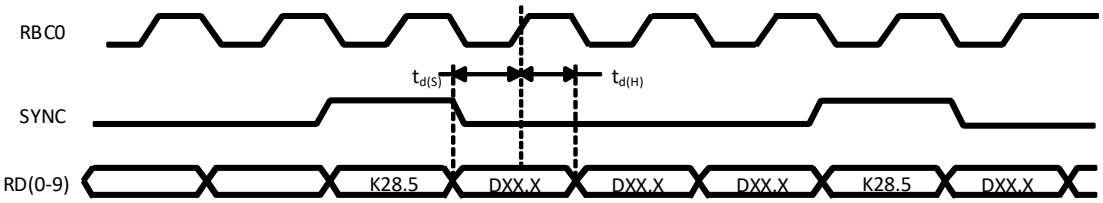


Figure 6. Synchronous Timing Characteristics Waveform (TBI full-rate mode)

In DDR mode, receiver outputs data on the rising and falling edges of RBC0 at the same time. RBC1 is low-level. Data starts output from bit0 and recombined on RBC0 rising edge. The timing diagram is shown in figure 7.

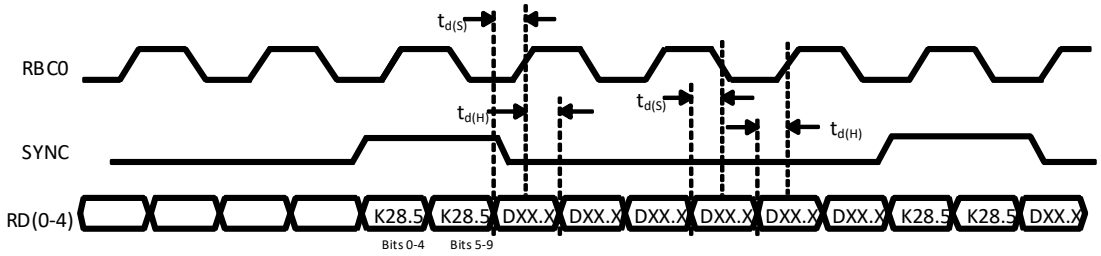


Figure 7. Synchronous Timing Characteristics Waveform (DDR mode)

In the MS2001, the receiver clock interpolation circuit could lock phase according to input data, without reference clock. The receive serial data rate (RXP, RXN) is the same as transmit, ±0.02% (200PPM) difference in the normal condition.

Receiver Word Recombination

The MS2201 defines the recombination scheme of 10-bit K28.5 (comma character) according to IEEE 802.3 Gigabit Ethernet protocol. The following contents explain how to complete the scheme and data combination.

"Comma Character" on Expected Boundary

The MS2201 integrates the recognition and word recombination functions of 10-bit K28.5 character string. Pulling SYNCEN pin high could enable 10-bit word recombination function, which checks and compares input data to 7-bit synchronous code. K28.5 character sting consists of 0011111010 defined by 8b/10b encode scheme. The high 7 bit is 0011111, comma character. K28.5 character string is used to combine data. As long as it occurs on expected 10-bit boundary, receive 10-bit data could be combined correctly and data recombination is not required. The timing characteristics waveforms of RBC0,RBC1,SYNC and RD0-RD9 are shown in figure 5. (Note : K28.5 character string is valid on RBC1 rising edge.)

Comma Character" Not on Expected Boundary

If synchronization function is enabled and K28.5 is on the both sides of expected 10-bit word boundary, the word recombination is necessary. Recombining or shifting 10-bit word boundary truncates the character string with following uncombined K28.5. Following K28.5 character string and subsequent data could be combined correctly as shown in figure 8. During the recombination process, the pulse width of RBC0 and RBC1 would extend or remain in current state. Based on the design, the maximum extension width is 20-bit time. Above this condition would occur only when K28.5 is combined on RBC1 falling edge rater than rising edge (worst case scenario). The timing characteristics waveforms of data recombination is shown in figure 8.

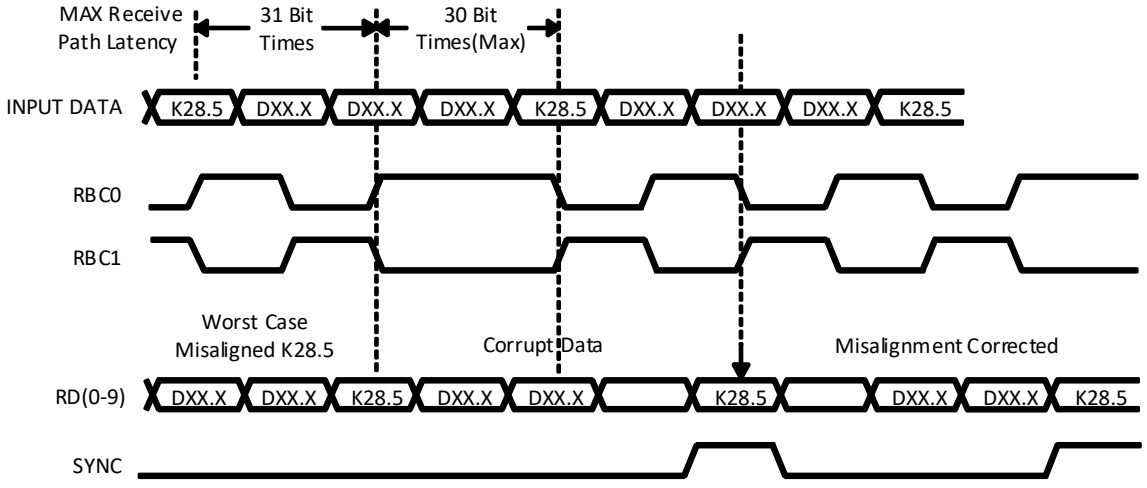


Figure 8. Timing Characteristics Waveforms of Word Recombination

If system doesn't need data package, SYNCEN pin could be pulled low to disable data combination function.

When synchronous character string is detected, SYNC signal would be pull high, and combined according to K28.5 character string. In TBI mode, SYNC pulse duration time is the same as data width. In DDR mode, SYNC pulse duration time is equal to RBC0 cycle.

Data Receive Latency

The delay time for serial data to parallel data is the time from when receiver receives the first bit until it is output with combined parallel data. And RD0 is the first received data. In TBI mode, the minimum latency is 21-bit time; the maximum latency is 31-bit time. In DDR mode, the minimum latency is 27-bit time; the maximum latency is 34-bit time.

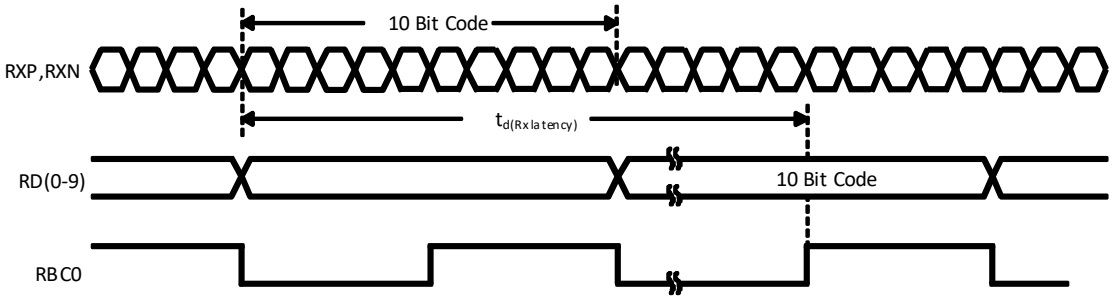


Figure 9. Receive Latency (TBI normal mode)

Signal loss Detection

The MS2201 has a signal loss detection circuit to limit the input signal, which has no enough voltage to remain stable for clock recovery circuit. LOS pin is used to indicate bad input signal, such as distant cable or no transmitted signal and is not indication of signal meeting demand. Under the condition of PRBS as serial input, when signal magnitude is more than 150mV, LOS signal is high-level; when signal magnitude is less than 50mV, LOS signal is low-level; when signal magnitude is between 50mV and 150mV, LOS signal is uncertain.

Testable

In the MS2201, LOOPBACK function provides full-speed test for transmit/receive part. In addition, ENABLE function could disable all internal circuits so as to conduct lddq test. PRBS function also provides BIST (built-in self test) test. Pulling TESTEN high enables lddq test mode. An internal pull-down resistor on TESTEN terminal, so default state is normal operation. TESTEN is just used for factory test, not for terminal user.

LOOPBACK Test

The MS2201 transceiver enables self-test function by enabling loop circuit (LOOPEN High). Once the function is activated, serial transmitted data would be directly through to receiver by internal circuit. The function verification is conducted by comparing output parallel data to input parallel data (external differential output terminal is high-impedance state in LOOPBACK test).

ENABLE Function

When ENABLE is low-level, the static power would be closed for all analog and digital circuits. It is beneficial to make the MS2201 in low power dissipation idle state when no data transmission in link.

PRBS Function

The MS2201 has built-in 2^7-1 PRBS (Pseudo Random Binary Sequence) test function. When PRBSEN control bit is placed high, PRBS test function is enabled. On transmit terminal, a PRBS is generated and sent to 10-bit transmitter input bus. In PRBS test mode, the data on parallel input terminal will be ignored in normal condition. Then PRBS is through to transmitter circuit as normal data and finally is output by transmitter. The output could be sent to BERT (bit error rate tester) test device or the receive terminal of another MS2201. Now that PRBS isn't real random but a pre-specified sequence consisting of "0", "1", data could be captured and checked by BERT. On the receive terminal of MS2201, a built-in BERT function is controlled by PRBSEN signal. It could receive PRBS data and check error by pulling SYNC/PASS low to indicate error. When PRBS function is enabled, RBCMODE makes no difference whether high-level or low-level. However, MODESEL must be low-level to make the PRBS verification function operate normally. In addition, the MS2201 operates in TBI mode, and RBC0 pin outputs a full-rate clock. PRBS test function supports two modes (normal and latched) controlled by SYNCEN. When SYNCEN is low-level, the test result of PRBS error rate would be output by SYNC/PASS terminal. When SYNCEN is high-level, the PRBS result would be latched on SYNC/PASS terminal (Once one error is detected, SYNC/PASS terminal would be latched as low-level).

JTAG

The MS2201 supports JTAG function following IEEE 1149.1protocol. If JTAG function is needed, five JTAG pins : TRSTN, TMS, TCK, TDI, TDO could act as JTAG pins with normal definition. If JTAG function is not needed, it is recommended to connect TRSTN to ground. TMS and TDI could not connection due to internal pull-up resistor. TDO could not connection as output pin. TCK could be connected to GND due to no internal pull-up resistor. When TRSTN has been pulled low, TCK can be unconnected with any signal if not used.

TYPICAL APPLICATION DIAGRAMS

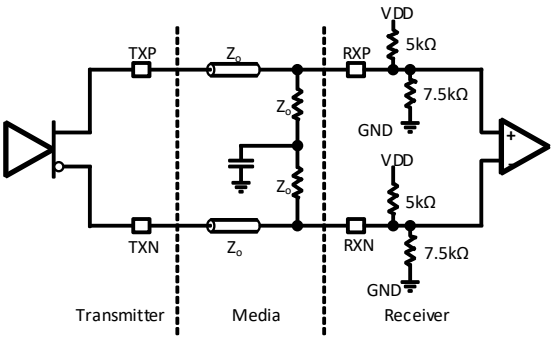


Figure 10. High-speed I/O DC Couple

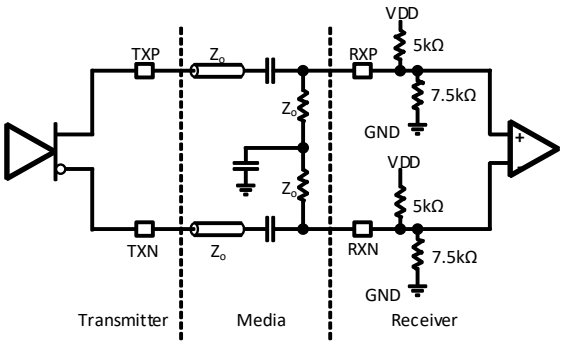


Figure 11. High-speed I/O AC Couple

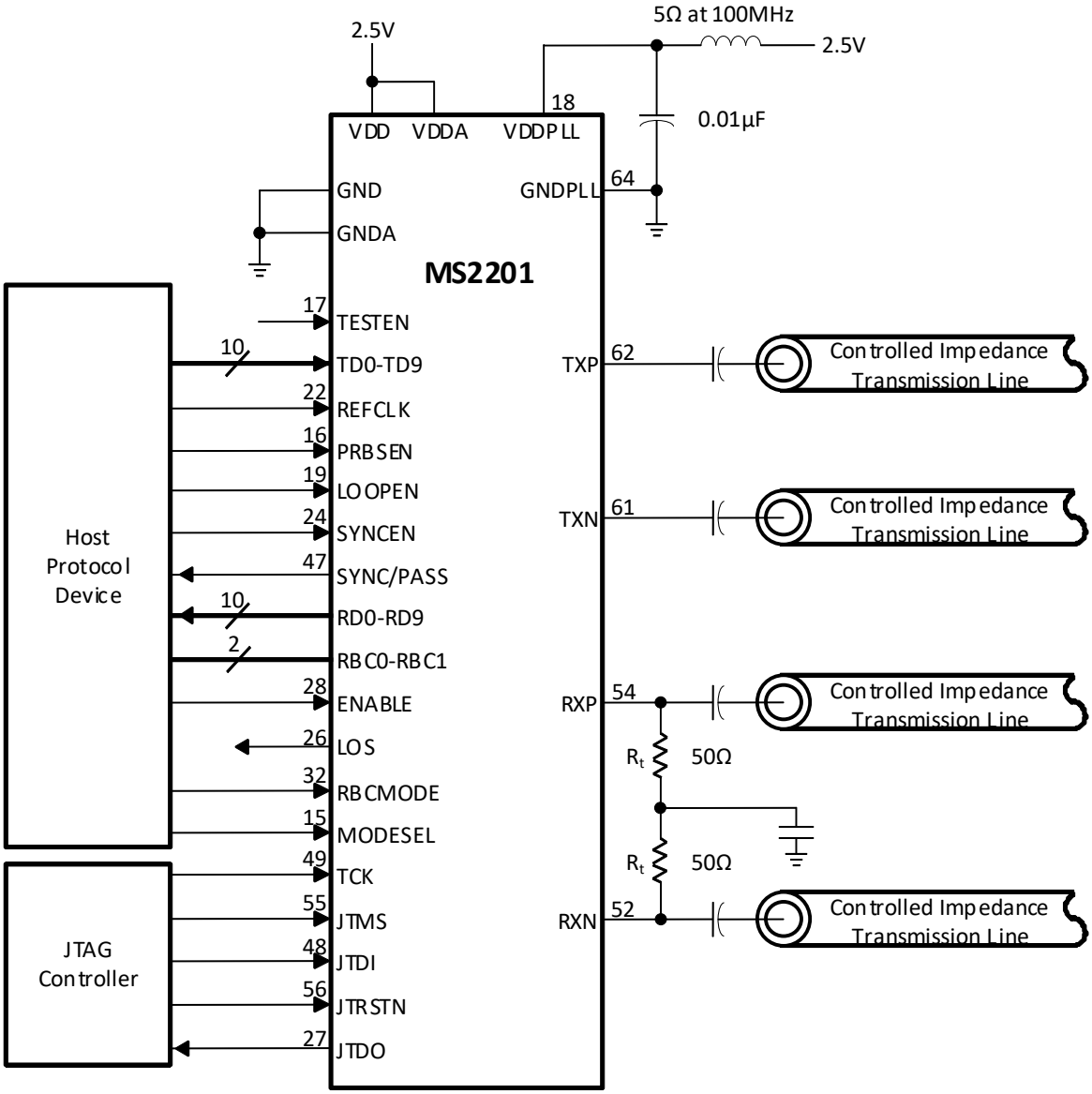
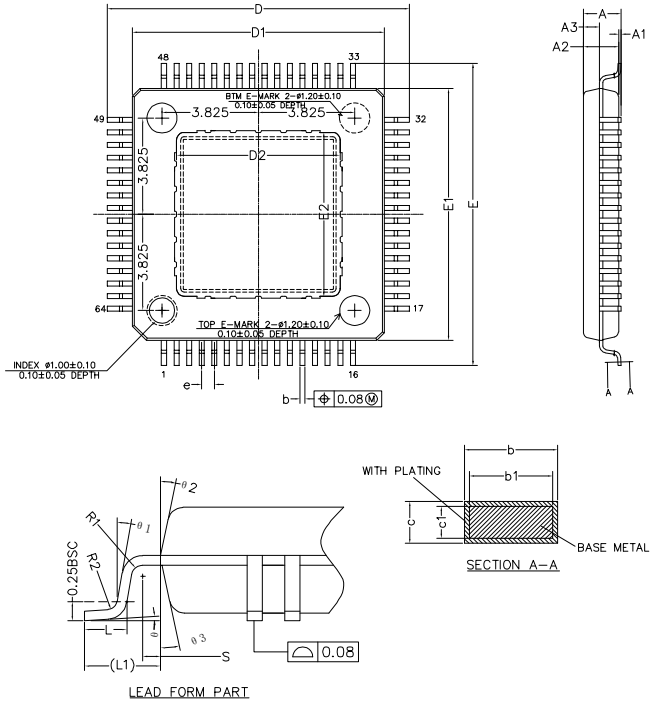


Figure 12. Typical Application Circuit (AC Couple)

PACKAGE OUTLINE DIMENSIONS

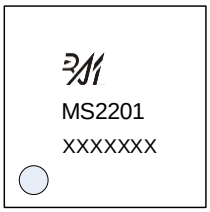
TQFP64



Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
A3	0.39	0.44	0.49
b	0.17	-	0.27
b1	0.17	0.20	0.23
c	0.09	0.13	0.18
c1	0.09	0.12	0.16
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
D2	6.50REF		
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
E2	6.50REF		
e	0.40	0.50	0.60
L	0.45	-	0.75
L1	1.00REF		
R1	0.15REF		
R2	0.13REF		
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ3	11°	12°	13°

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description



Product Name : MS2201

Product Code : XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Tray	Tray/Box	Piece /Box	Box/Carton	Piece/Carton
MS2201	TQFP64	160	10	1600	4	6400

STATEMENT

- All Revision Rights of Datasheets Reserved for Ruimeng. Don't release additional notice.

  Customer should get latest version information and verify the integrity before placing order.
- When using Ruimeng products to design and produce, purchaser has the responsibility to observe safety standard and adopt corresponding precautions, in order to avoid personal injury and property loss caused by potential failure risk.
- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

+86-571-89966911

Rm701, No.9 Building, No. 1 WeiYe Road, Puyan Street, Binjiang District, Hangzhou, Zhejiang

http:// www.relmon.com