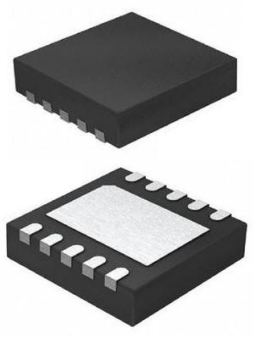
LVDS Dual Bus Driver

PRODUCT DESCRIPTION

The MS2652D is low power dissipation, high data rate, two-channel, CMOS, differential LVDS signal bus driver.

The supported data receiving rate exceeds 155.5Mbps (77.7MHz). The MS2652D converts TTL/CMOS input signal to low-voltage (425mV), differential output signal. The driver also supports tri-state output function and can be used to shut down output driving stage. According to the shutdown of output current, 11mW static power dissipation could be get. In addition, the MS2652D has power-down shutdown function. When VCC is open-circuit, LVDS output is in high-impedance state. The function can maintain the minimum load on LVDS bus at power down.



DFN10

FEATURES

- More than 155.5Mbps (77.7MHz) Switch Frequency
- LVDS Output Hi-Z at Power-down
- ±425mV Differential Output Signal
- Low Power Dissipation
- the Maximum 400ps Channel Propagation Delay Difference (5V,25°C)
- the Maximum 3.5ns Propagation Delay
- Industrial-grade Temperature Application Range
- Compatible with ANSI/TIA/EIA-644 LVDS Standard
- DFN10 Package

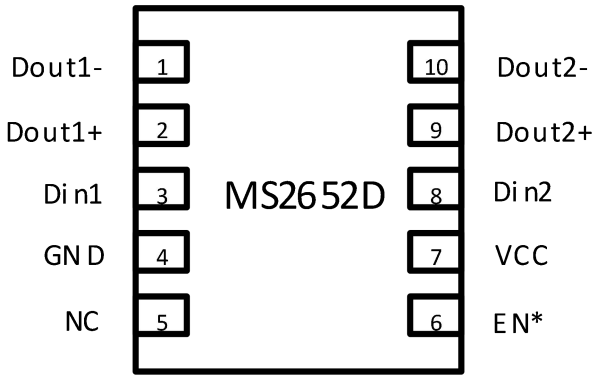
APPLICATIONS

- Flat Panel Display Interface
- High-speed Data Communication
- Monitor Camera

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS2652D	DFN10	MS2652D

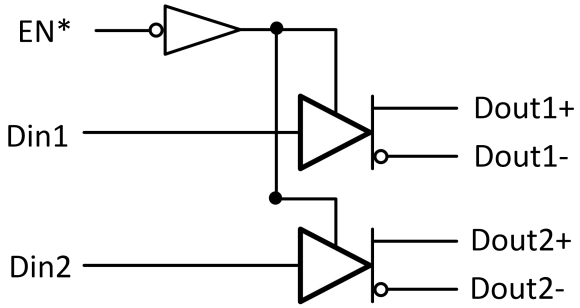
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
3, 8	Din	I	CMOS/TTL Input Signal
2, 9	Dout+	O	LVDS No-inverting Output
1, 10	Dout-	O	LVDS Inverting Output
4	GND	-	Ground
5	NC	-	Not Connection
6	EN*	I	Active Low
7	VCC	-	Power Supply, +5V ± 10%

BLOCK DIAGRAM



Function Table

Enable	Input	Output	
EN*	Din	Dout+	Dout-
H	X	Z	Z
Other Condition	L	L	H
	H	H	L

ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Power Supply	VCC	-0.3V ~ 6V	V
Input Voltage	Din	-0.3 ~ Vcc+0.3	V
Input Voltage for Enables	EN,EN*	-0.3 ~ Vcc+0.3	V
Output Voltage	Dout+, Dout-	-0.3 ~ Vcc+0.3	V
Maximum Junction Temperature	Tj	+150	°C
Storage Temperature	Tstg	-60 ~ 150	°C
ESD (HBM)	1.5 kΩ, 100 pF	≥ 3500	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Range			Unit
		Min	Typ	Max	
Power Supply	VCC	2.5	5	5.5	V
Operating Temperature		-40	25	125	°C

ELECTRICAL CHARACTERISTICS

VCC = +5.0V, TA = +25°C

Parameter	Symbol	Pin	Condition	Min	Typ	Max	Unit
Differential Output Voltage	Vod1	Dout- Dout+	RL=100Ω (Figure 1)	350	425	500	mV
Differential Output Voltage Difference (Complementary Output)	ΔVod1				5	35	mV
Common-mode Output Voltage	Vos			1.34	1.47	1.60	V
Common-mode Output Voltage Difference (Complementary Output)	ΔVos				5	25	mV
Output High Level	VOH		RL=100Ω		1.68	1.78	V
Output Low Level	VOL			0.90	1.25		V
Input High Level	VIH	Din, EN*		2.0		VCC	V
Input Low Level	VIL			GND		0.8	V
Input Current	Iin		Vin=Vcc, GND, 2.5V or 0.4V	-10	±1	+10	uA
Input Clamp Voltage	VCL		ICL=-18mA	-1.5	-0.8		V
Output Short-circuit Current	IOS	Dout- Dout+	Vout=0V (Note 4)		-4.2		mA
Output Tri-state Current	IOZ		EN=0.8V,EN*=2.0V, Vout=0 or VCC	-10	±1	+10	uA
Off Current	IOFF	VCC	Vo=0V or 2.4V Vcc=0V or Open-circuit	-10	±1	+10	uA
No Load Power Supply Current at Driver Enabled	ICC		Din=Vcc or GND		1.8	3.0	mA
			Din=2.5V or 0.4V		2.7	6.5	
Load Power Supply Current at Driver Enabled	ICCL		RL=100Ω Vin=Vcc or GND		10.4	21.0	mA
No Load Power Supply Current at Driver Disabled	ICCZ		Din=Vcc or GND EN=GND, EN*=Vcc		2.0	4.0	mA

Switch Characteristic

VCC = +5.0V, TA = +25°C (Note 1, 3, 5)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Differential Propagation Delay (High to Low)	tPHLD	RL=100Ω, CL=5pF Figure 2 and Figure 3	1.0	2.0	3.5	ns
Differential Propagation Delay (Low to High)	tPLHD		1.0	2.0	35	ns
Differential Propagation Delay Difference |tPHLD- tPLHD|	tSDK		0	80	900	ps
Channel Propagation Delay Difference (Note 2)	tSK1		0	300	1000	ps
Rise Time	tTLH			0.35	1.5	ns
Fall Time	tRHLD			0.35	1.5	ns
Delay, Output High to Hi-Z	tPHZ	RL=100Ω, CL=5PF Figure 4 and Figure 5		2.5	10	ns
Delay, Output Low to Hi-Z	tPLZ			2.5	10	ns
Delay, Output Hi-Z to High	tPZH			2.5	10	ns
Delay, Output Hi-Z to Low	tPZL			2.5	10	ns

Note:

1. All typical values are measured at VCC =+5.0V, TA=+25°C, CL=5pF.

2. Channel propagation delay difference is that the maximum propagation delay difference between the two differential channels.

3. In general test, input signal: f=1MHz, Zo=50Ω, tr, tf ≤6ns.

4. Output short-circuit current (IOS), the value is magnitude and minus is current direction.

5. Load capacitance includes probe and soldering capacitance.

Test Circuit

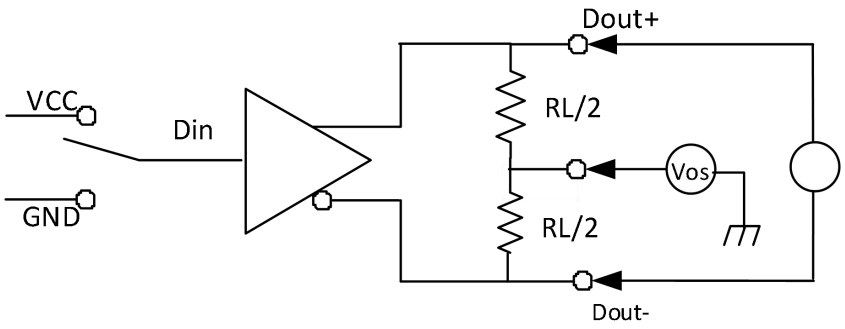


Figure 1. Vod and Vos Test Circuit

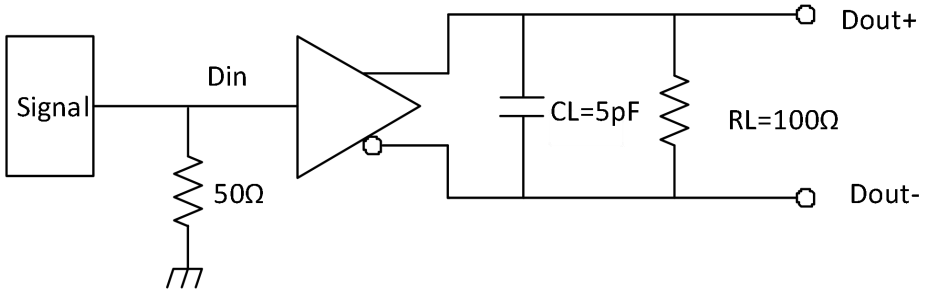


Figure 2. Propagation Delay and Edge Transition Time Test Circuit

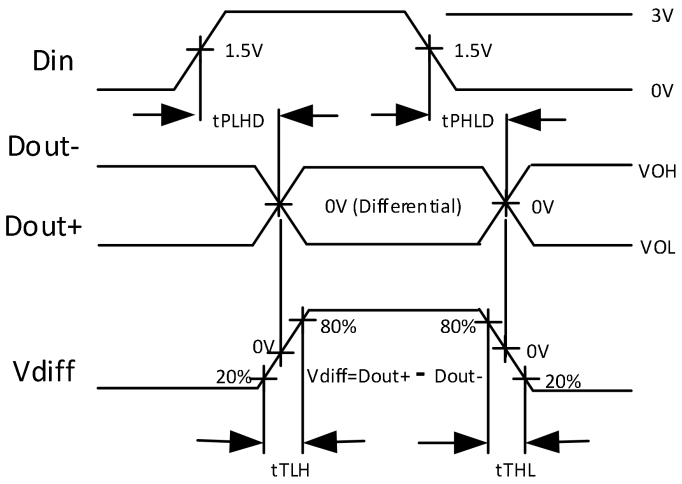


Figure 3. Propagation Delay and Edge Transition Time Waveforms

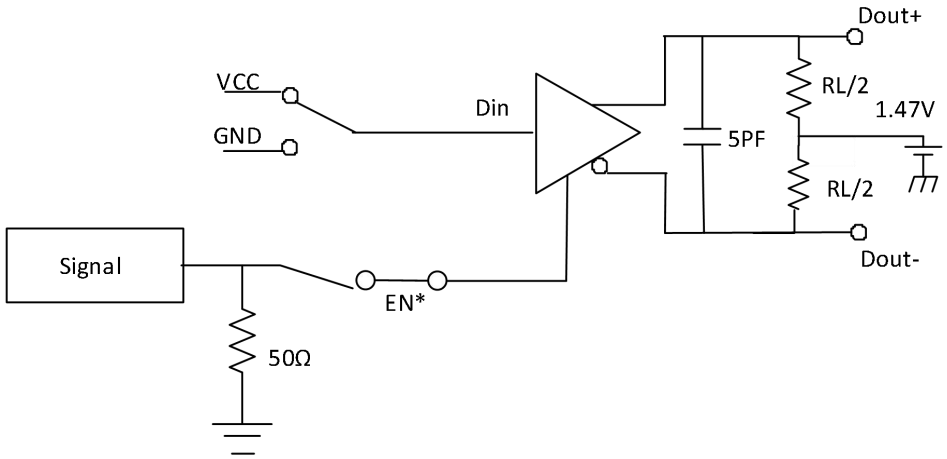


Figure 4. Tri-state Delay Test Circuit

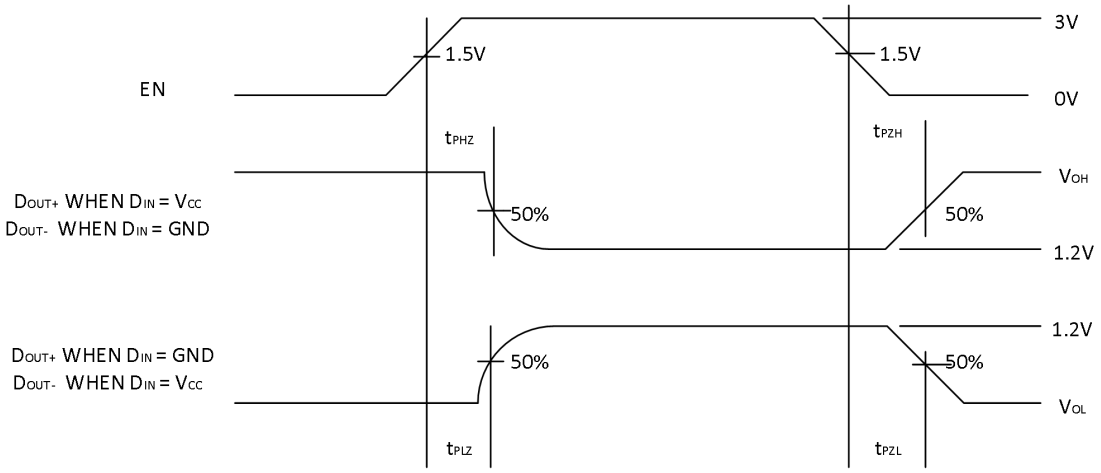


Figure 5. Tri-state Triggering Waveforms

TYPICAL DESCRIPTION

LVDS driver and receiver are mainly applied to point-to-point structure. The structure provides a clean transmission channel for high-speed data rate signal. Transmission media can be twisted-pair, cable and PCB trace. The impedance of typical transmission media is less than 100Ω. In order to match the impedance of transmission media, 100Ω terminal resistor can be connected on differential input terminals. And it should be as close to the input terminal of the device as possible. The terminal resistor converts the current signal to voltage signal, thus to provide for receiver device. For other structures, such as multi-receiver, it should be considered that the impedance match of mid connector and cable interface and noise margin.

The MS2652D, differential bus driver is designed as current mode. The driver with current mode has high output impedance and outputs constant current within load range (while the driver with voltage mode outputs constant voltage within load range). When current flows from one direction of load, logic high level is generated; When current flows from opposite direction, logic low level is generated. The scaled output current is 4.25mA, minimum 3.5mA and maximum 5mA. When system is operating, a 100Ω resistor is needed to across connected on the positive and negative terminals of the MS2652D. The common-mode point of differential LVDS signal is 1.47V(Vos) to ground. Figure 6 indicates the peak-to-peak value of steady-state voltage (Vss) is twice the differential voltage(Vod).

In operation, current-mode driver is superior to voltage-mode driver, such as RS-422. Current-mode driver could provide stable output current within wide frequency range. The output voltage like RS422 has obvious attenuation in 20MHz~40MHz range. This is caused by variation in switch current of internal gate circuit for voltage-mode driver, while the output current of current mode is fixed. This is similar to the operating modes of ECL and PECL devices, but without large current like ECL and PECL. Compare with similar PECL circuit,the required current of LVDS may less than 80%. The AC characteristics of the MS2652D are 10 times superior to RS-422 voltage-mode driver.

When input is floating, internal protection circuit ensures that outputs are logic 0 (the true output is low level, the another is high level). Tri-state output function can realize output high impedance, thus power dissipation is reduced when the driver is not operating.

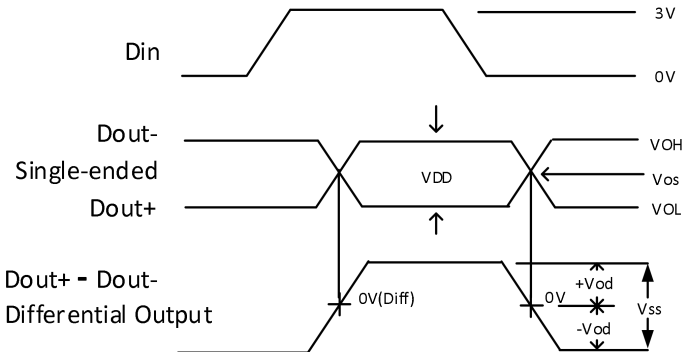
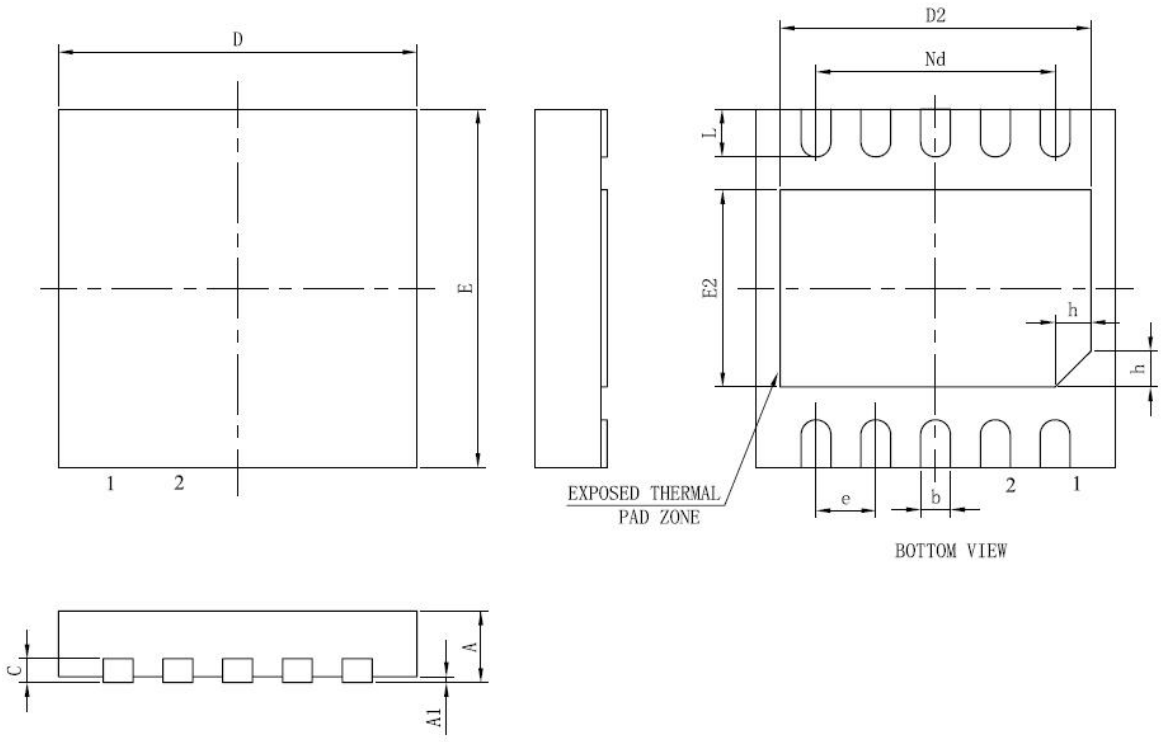


Figure 6. Driver Output Level

PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	0.70	0.75	0.80
A1	--	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
e	0.50BSC		
Nd	2.00BSC		
E	2.90	3.00	3.10
E2	1.45	1.55	1.65
L	0.30	0.40	0.50
h	0.20	0.25	0.30

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description

Product Name: MS2652D

Product Code： XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS2652D	DFN10	5000	1	5000	8	40000

STATEMENT

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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

+86-571-89966911

Rm701, No.9 Building, No. 1 WeiYe Road, Puyan Street, Binjiang District, Hangzhou, Zhejiang

http:// www.relmon.com