

MOSEL VITELIC MS621002A

256K x 4 CMOS

STATIC RAM

Features

- Fast Access Times: 20/25 ns
- High Density 400-Mil SOJ
- Low Standby Power
- TTL Compatible I/O
- 5V ± 10% Supply
- Fully Static Operation
- Three State Output
- JEDEC Standard Pinout

Description

The MS621002A is a high speed 1M-bit static RAM organized as 256K x 4. Fully static in operation, the Chip Enable (\bar{E}) reduces power to the chip when HIGH. Standby power drops to its lowest level (I_{SB1}) when \bar{E} is raised to within 0.2V of V_{CC} .

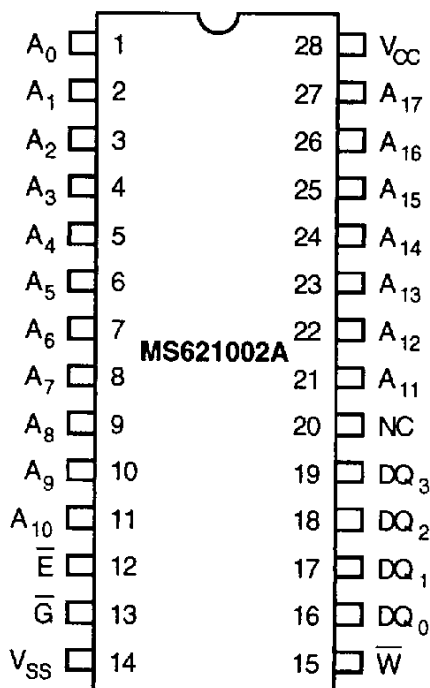
Write cycles occur when both Chip Enable (\bar{E}) and Write Enable (\bar{W}) are LOW. Data is transferred from the DQ pins to the memory location specified by the address lines.

Read cycles occur when \bar{E} is LOW and \bar{W} is HIGH.

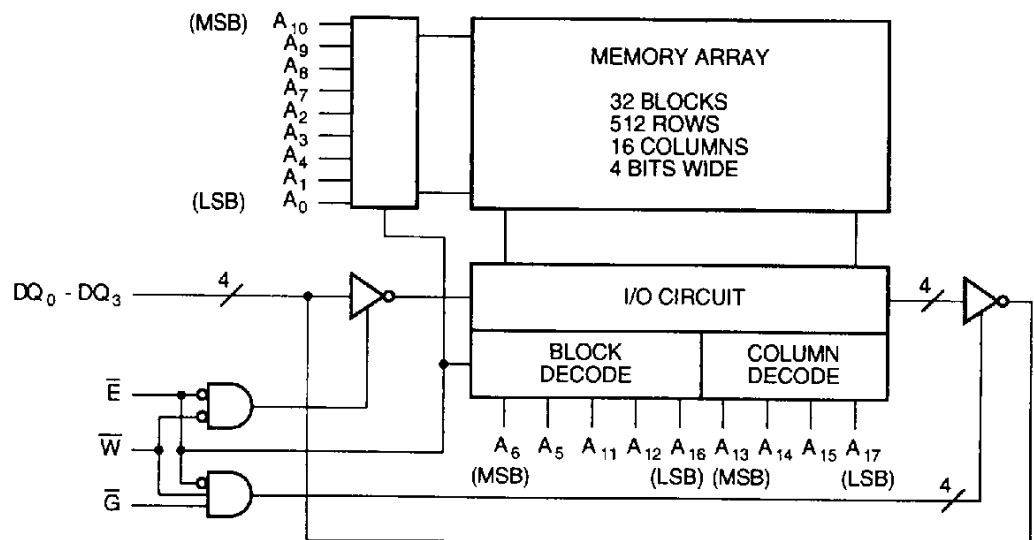
High frequency design techniques should be employed to obtain optimum performance from this device. Solid, low impedance power and ground planes, with high frequency decoupling capacitors, are desirable. Series termination of the inputs should be considered when transmission line effects occur.

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Pin Configuration



Functional Block Diagram



Pin Descriptions**A₀ - A₁₇ Address Inputs**

These 18 address inputs select one of the 256K x 4 bit segments in the RAM.

 \bar{E} Chip Enable Input

\bar{E} is active LOW. The chip enable must be active to read from or write to the device. If it is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when deselected.

 \bar{G} Output Enable Input

The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when \bar{G} is inactive.

 \bar{W} Write Enable Input

The write enable input is active LOW and controls read and write operations. With the chip enabled, when \bar{W} is HIGH and \bar{G} is LOW, output data will be present at the DQ pins; when \bar{W} is LOW, the data present on the DQ pins will be written into the selected memory locations.

DQ₀ - DQ₃ Data Input and Data Output Ports

These 4 bidirectional ports are used to read data from and write data into the RAM.

**V_{CC} Power Supply
V_{SS} Ground****Truth Table**

| Mode | \bar{E} | \bar{G} | \bar{W} | I/O Operation |
|---------|-----------|-----------|-----------|------------------|
| Standby | H | X | X | High Z |
| Read | L | L | H | D _{OUT} |
| Read | L | H | H | High Z |
| Write | L | X | L | D _{IN} |

Operating Range

| Range | Ambient Temperature | V _{CC} |
|------------|---------------------|-----------------|
| Commercial | 0°C to +70°C | 5V ± 10% |

Absolute Maximum Ratings ⁽¹⁾

| Parameter Name | Parameter | Rating | Units |
|-------------------|------------------------------|--------------------|----------------|
| V _{CC} | Supply Voltage | -0.3 to 7 | V |
| V _{IN} | Input Voltage | -0.3 to 7 | V |
| V _{DQ} | Input/Output Voltage Applied | -0.3 to 6 | V |
| T _{BIAS} | Temperature Under Bias | Plastic | -10 to +125 °C |
| T _{STG} | Storage Temperature | Plastic | -65 to +150 °C |
| P _D | Power Dissipation | 1.0 | W |
| I _{OUT} | D C Output Current | ±40 ⁽²⁾ | mA |

See Notes following "SWITCHING CHARACTERISTICS".

DC Electrical Characteristics (0°C to +70°C)

| Parameter Name | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|------------------|---|---|------|------|-----------------------|------|
| V _{CC} | Supply Voltage | | 4.5 | | 5.5 | V |
| V _{SS} | Supply Voltage | | 0 | | 0 | V |
| V _{IL} | Guaranteed Input LOW Voltage ⁽³⁾ | | -0.5 | | 0.8 | V |
| V _{IH} | Guaranteed Input HIGH Voltage | | 2.2 | | V _{CC} + 0.5 | V |
| I _{CC1} | Operating Current ⁽⁴⁾ | Output open, t _{CYCLE} = 20ns | | | 130 | mA |
| I _{CC1} | Operating Current ⁽⁴⁾ | Output open, t _{CYCLE} = 25ns | | | 120 | mA |
| I _{CC1} | Operating Current ⁽⁴⁾ | Output open, t _{CYCLE} = 35ns | | | 100 | mA |
| I _{SB1} | Standby Current | $\bar{E} \geq V_{CC} - 0.2V$ | | 0.1 | 1 | mA |
| I _{SB2} | Standby Current | $\bar{E} \geq V_{IH}$ | | | 5 | mA |
| I _{LI} | Input Leakage Current | V _{CC} = 5.5V, V _{in} = 0V to V _{CC} | -2 | | 2 | μA |
| I _{LO} | I/O Leakage Current | V _{CC} = 5.5V, V _{in} = 0V to V _{CC} | -10 | | 10 | μA |
| V _{OH} | Output High Voltage | I _{OH} = -4.0mA | 2.4 | | | V |
| V _{OL} | Output Low Voltage | I _{OL} = 8.0mA | | | 0.4 | V |

See Notes following "SWITCHING CHARACTERISTICS".

Capacitance⁽¹⁾ T_A = 25°C, f = 1.0MHz

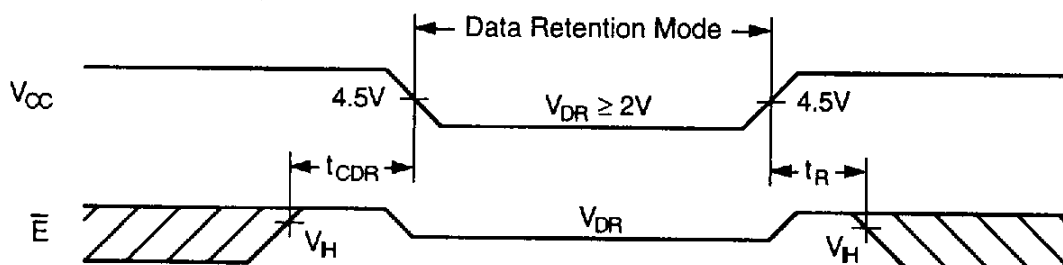
| Parameter Name | Parameter | Conditions | Max. | Unit |
|-----------------|-------------------|----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 6 | pF |
| C _{DQ} | I/O Capacitance | V _{DQ} = 0V | 8 | pF |

1. This parameter is guaranteed and not tested.

Data Retention Characteristics (over the commercial operating range)

| Parameter Name | Parameter | Test Conditions | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|-------------------|------------------------------------|---|--------------------------------|---------------------|--------------------|------|
| V _{DR} | V _{CC} for Data Retention | $\bar{E} \geq V_{CC} - 0.2V$, $\bar{G} \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V | 2.0 | - | 5.5 | V |
| I _{CCDR} | Data Retention Current | $\bar{E} \geq V_{CC} - 0.2V$, $\bar{G} \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V | - | - | 500 ⁽²⁾ | μA |
| I _{CDR} | Chip Deselected to Data | | 0 | - | - | ns |
| | Retention Time | See Retention Waveform | | | | |
| t _R | Operation Recovery Time | | t _{RC} ⁽³⁾ | - | - | ns |

NOTES:

1. V_{CC} = 2V, T_A = +25°C2. V_{CC} = 3V3. t_{RC} = Read Cycle Time**Timing Waveform Low V_{CC} Data Retention Waveform**

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AC Electrical Characteristics (over the commercial operating range) ⁽⁶⁾

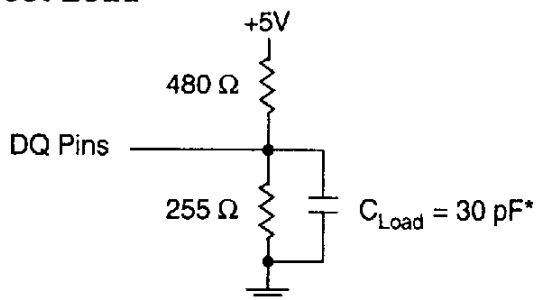
| Parameter Name | Parameter | -20 | | -25 | | Units |
|--------------------|---|------|------|------|------|-------|
| | | Min. | Max. | Min. | Max. | |
| Read Cycle | | | | | | |
| t_{RC} | Read Cycle Timing | 20 | | 25 | | ns |
| t_{AA} | Address Access Time | | 20 | | 25 | ns |
| t_{OH} | Output Hold from Address Change | 3 | | 3 | | ns |
| t_{EA} | \bar{E} Low to Valid Data | | 20 | | 25 | ns |
| t_{ELZ} | \bar{E} Low to Output Active ^{(7), (8)} | 5 | | 5 | | ns |
| t_{EHZ} | \bar{E} High to Output High-Z ^{(7), (8)} | | 8 | | 10 | ns |
| t_{GA} | \bar{G} Low to Valid Data | | 7 | | 8 | ns |
| t_{GLZ} | \bar{G} Low to Output Active ^{(7), (8)} | 0 | | 0 | | ns |
| t_{GHZ} | \bar{G} High to Output High-Z ^{(7), (8)} | | 6 | | 10 | ns |
| t_{PU} | \bar{E} Low to Power Up Time ⁽⁸⁾ | 0 | | 0 | | ns |
| t_{PD} | \bar{E} High to Power Down Time ⁽⁸⁾ | | 20 | | 25 | ns |
| Write Cycle | | | | | | |
| t_{WC} | Write Cycle Timing | 20 | | 25 | | ns |
| t_{EW} | \bar{E} Low to End of Write | 12 | | 15 | | ns |
| t_{AW} | Address Valid to End of Write | 12 | | 15 | | ns |
| t_{AS} | Address Setup | 0 | | 0 | | ns |
| t_{AH} | Address Hold | 0 | | 0 | | ns |
| t_{WP} | \bar{W} Pulse Width | 12 | | 15 | | ns |
| t_{DW} | Input Data Setup Time | 12 | | 15 | | ns |
| t_{DH} | Input Data Hold Time | 0 | | 0 | | ns |
| t_{WHZ} | \bar{W} Low to Output High-Z ^{(7), (8)} | | 8 | | 10 | ns |
| t_{WLZ} | \bar{W} High to Output Active ^{(7), (8)} | 3 | | 3 | | ns |

NOTES:

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability, and degrade performance characteristics.
- Output should not be shorted for more than 30 seconds.
- Negative undershoot of up to 3.0V is permitted once per cycle.
- I_{CC} is dependent upon output loading and cycle rates. Specified values are with output open, operating at specified cycle times.
- Capacitances are maximum values at 25°C measured at 1.0 MHz with $V_{Bias}=0V$ and $V_{CC}=5.0V$.
- Switching Characteristics measurements specified at "AC Test Conditions" levels.
- Active output to High-Z and High-Z to active output tests specified for a $\pm 200mV$ transition from steady levels into the test load.
- Sample tested only.

AC Test Conditions

| | |
|--|------------------|
| Input Pulse Levels | V_{SS} to 3V |
| Input Rise and Fall Times | 3ns |
| Input and Output Timing Reference Levels | 1.5V |
| Output Load, Timing Tests | See Figure Below |

AC Test Load

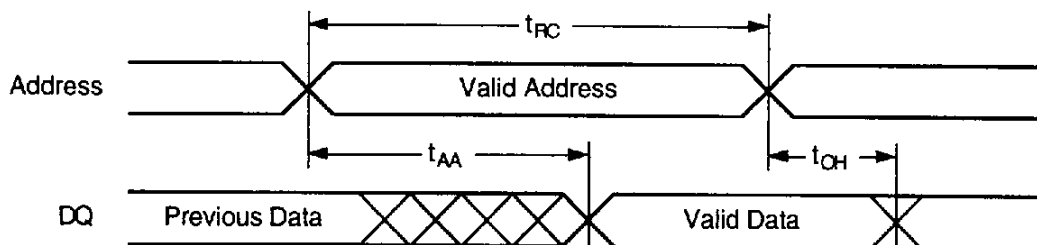
* Includes scope and jig capacitance

Key to Switching Waveforms

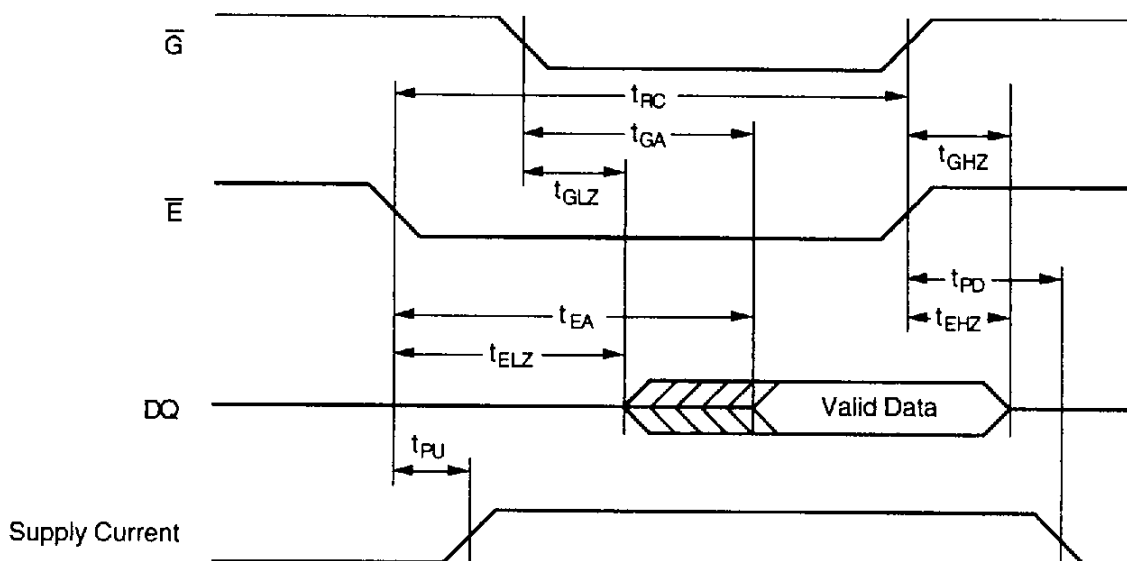
| WAVEFORM | INPUTS | OUTPUTS |
|----------|----------------------------------|---|
| | MUST BE STEADY | WILL BE STEADY |
| | MAY CHANGE FROM H TO L | WILL BE CHANGING FROM H TO L |
| | MAY CHANGE FROM L TO H | WILL BE CHANGING FROM L TO H |
| | DON'T CARE: ANY CHANGE PERMITTED | CHANGING: STATE UNKNOWN |
| | DOES NOT APPLY | CENTER LINE IS HIGH IMPEDANCE "OFF" STATE |

Switching Waveforms- Read Cycle**Read Cycle No. 1**

Chip is in Read Mode: \bar{W} is HIGH, and \bar{E} and \bar{G} are LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of DQ implies that data lines are in Low-Z state and the data may not be valid.

**Read Cycle No. 2**

Chip is in Read Mode: \bar{W} is HIGH. Timing illustrated for the case when addresses are valid before \bar{E} goes LOW. Data-out is not specified to be valid until t_{EA} , but may become valid as soon as t_{ELZ} . Outputs will transition from High-Z to Valid Data-out. Data-out is valid after both t_{EA} and t_{GA} are met.



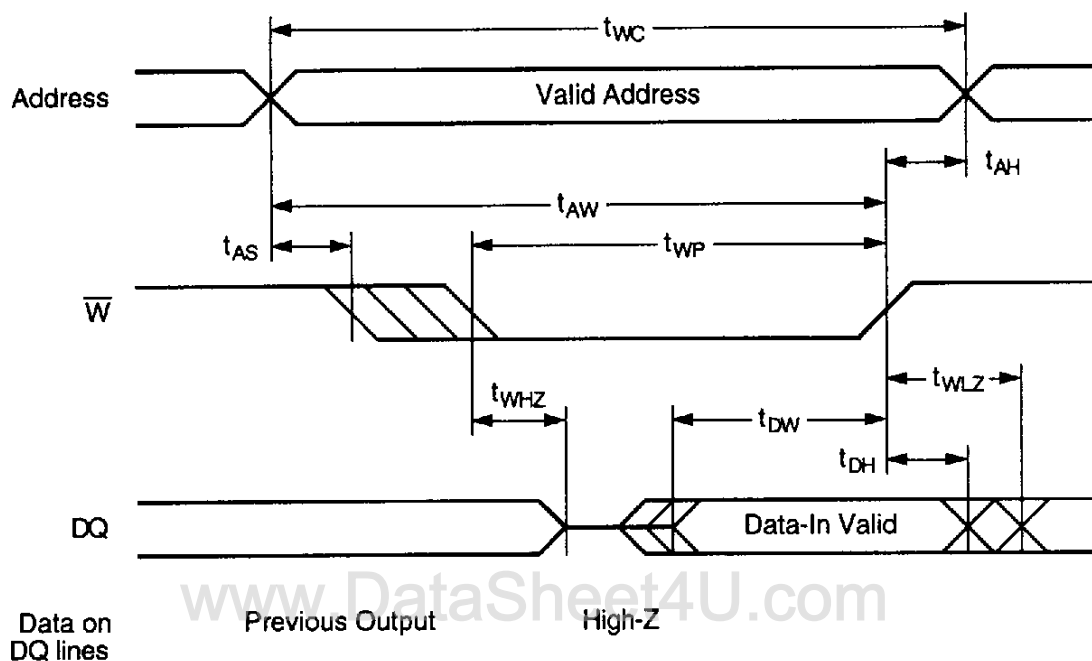
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Switching Waveform - Write Cycle

Addresses must be stable during Write Cycles. \bar{E} or \bar{W} must be HIGH during address transitions. The outputs will remain in the High-Z state if \bar{W} is LOW when \bar{E} goes LOW. Care should be taken so that the output drivers are disabled prior to placing the Input Data on the DQ lines. This will prevent bus contention, reducing system noise.

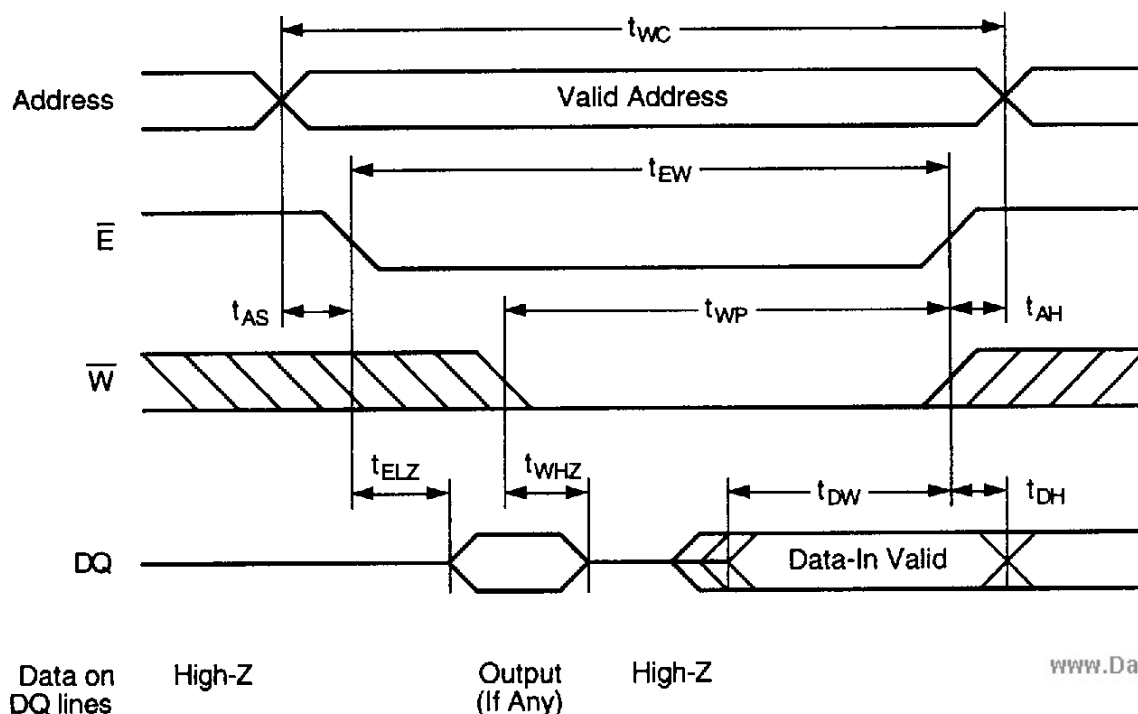
Write Cycle No. 1 (\bar{W} Controlled)

Chip is selected: \bar{E} and \bar{G} are LOW. Using only \bar{W} to control Write cycles may not offer the best device performance, since both t_{WHZ} and t_{DW} timing specifications must be met.



Write Cycle No. 2 (\bar{E} Controlled)

\bar{G} is LOW. DQ lines may transition to Low-Z if the falling edge of \bar{W} occurs after the falling edge of \bar{E} .



MOSEL VITELIC**MS621002A****Ordering Information**

| SPEED (ns) | ORDERING PART NUMBER | PACKAGE | TEMPERATURE RANGE |
|-----------------------|---------------------------------|-----------------------|------------------------------|
| 20 | MS621002-20EC | Plastic DIP - 400 mil | 0°C to +70°C |
| 20 | MS621002-20KC | 400 mil SOJ | 0°C to +70°C |
| 25 | MS621002-25EC | Plastic DIP - 400 mil | 0°C to +70°C |
| 25 | MS621002-25KC | 400 mil SOJ | 0°C to +70°C |
| 35 | MS621002-35EC | Plastic DIP - 400 mil | 0°C to +70°C |
| 35 | MS621002-35KC | 400 mil SOJ | 0°C to +70°C |

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