# *3 Stereo Inputs and 4-Channel Outputs Volume, Balance, Fader and Selectable Input Gain*

## FEATURES

- Operation range : 2.7V ~ 6.5V
- 3 stereo inputs with selectable input gain
- 4 independent speaker controls for fader and balance
- Independent mute function
- Volume control in 1.25 dB/step
- $I^2C$ interface
- Components less and good PSRR
- Housed in SSOP20 packages

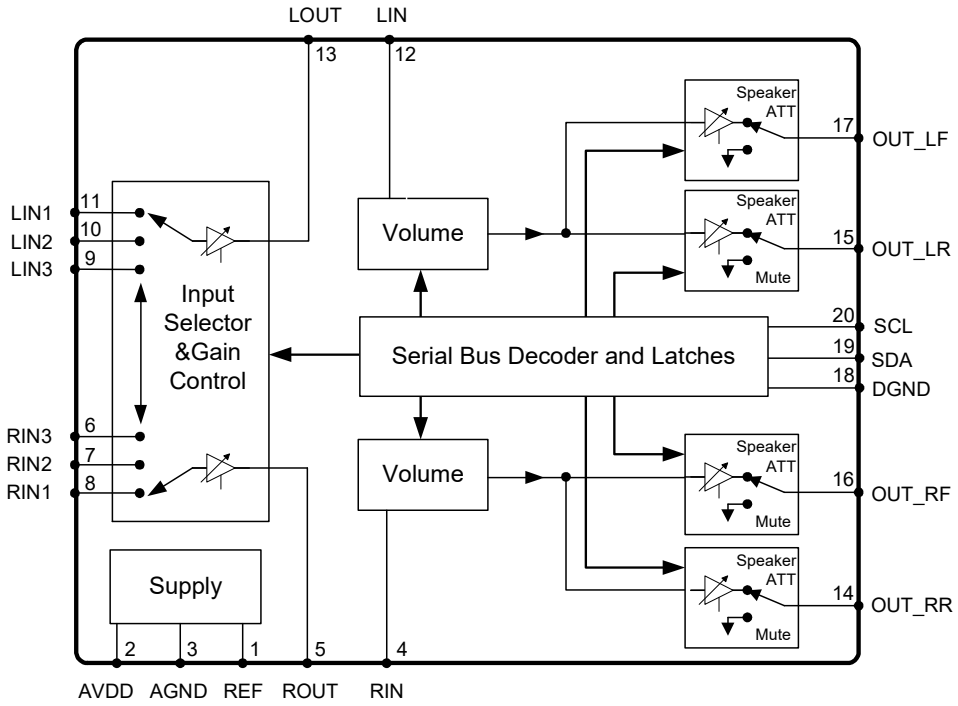
## APPLICATIONS

- Portable audio device
- Car stereo audio
- Hi-Fi audio system

## DESCRIPTION

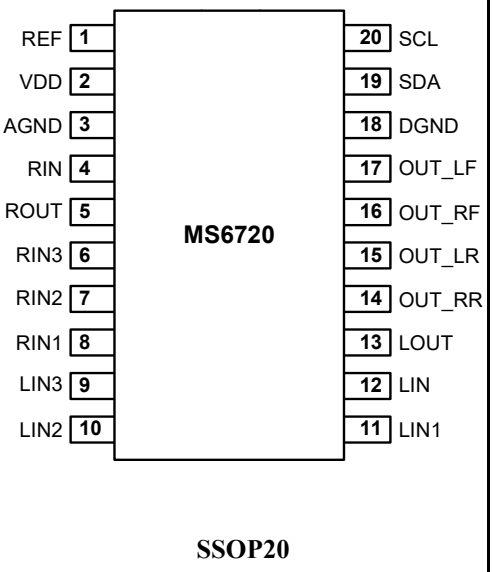
The MS6720 is a 3 stereo inputs/4-channel outputs digital control audio processor for the low voltage operation. Volume, balance (left/right), and fader (front/rear) processor are incorporated into a single chip. The MS6720 also has selectable input gain. All functions are programmable via the serial $I^2C$ bus. The default states of the chip as the power is on are: the volume is -78.75dB, the stereo 4 is selected, all the speakers are mute and the gains of the input stage are 0dB. The stereo 4 is connected internally, but not available on pins.

## BLOCK DIAGRAM



## PIN CONFIGURATION

| Symbol | Pin | Description |
|---|---|---|
| REF | 1 | Analog Reference Voltage（1/2VDD） |
| VDD | 2 | Supply Input Voltage |
| AGND | 3 | Analog Ground |
| RIN | 4 | Audio Processor Right Channel Input |
| ROUT | 5 | Gain Output and Input Selector for Right Channel |
| RIN3 | 6 | Right Channel Input 3 |
| RIN2 | 7 | Right Channel Input 2 |
| RIN1 | 8 | Right Channel Input 1 |
| LIN3 | 9 | Left Channel Input 3 |
| LIN2 | 10 | Left Channel Input 2 |
| LIN1 | 11 | Left Channel Input 1 |
| LIN | 12 | Audio Processor Left Channel Input |
| LOUT | 13 | Gain Output and Input Selector for Left Channel |
| OUT_RR | 14 | Right Rear Speaker Output |
| OUT_LR | 15 | Left Rear Speaker Output |
| OUT_RF | 16 | Right Front Speaker Output |
| OUT_LF | 17 | Left Front Speaker Output |
| DGND | 18 | Digital Ground |
| SDA | 19 | $I^2C$ Data Input |
| SCL | 20 | $I^2C$ Clock Input |




**SSOP20**

## ORDERING INFORMATION

| Package | Part number | Packaging Marking | Transport Media |
|---|---|---|---|
| 20-Pin SSOP (lead free) | MS6720SSGTR | MS6720G | 2.5k Units Tape and Reel |
| 20-Pin SSOP (lead free) | MS6720SSGU | MS6720G | 56 Units Tube |

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 6.5 | V |
| $V_{ESD}$ | Electrostatic Handling | -3000 to 3000 | V |
| $T_{STG}$ | Storage Temperature Range | -65 to 150 | ℃ |
| $T_A$ | Operating Ambient Temperature Range | -40 to 85 | ℃ |
| $T_J$ | Maximum Junction Temperature | 150 | ℃ |
| $T_S$ | Soldering Temperature, 10 seconds | 260 | ℃ |
| $R_{THJA}$ | Thermal Resistance from Junction to Ambient in Free Air SSOP20 | 210 | ℃/W |

## OPERATING RATINGS

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 2.7 | - | 6.5 | V |

## 5V ELECTRICAL CHARACTERISTICS

(Ta=25℃, All stages 0dB, f=1kHz, $C_{REF}$ =22uF, refer to the application circuit; unless otherwise specified)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply** | | | | | | |
| $I_Q$ | Quiescent Current | $V_{IN}$=0V | - | 12.2 | 12.5 | mA |
| PSRR | Power Supply Rejection Ratio | $C_{REF}$ = 22uF, f = 100Hz | 55 | 60 | - | dB |
| **Input Selectors** | | | | | | |
| $R_{IN}$ | Input Resistance | Input 1,2,3 | 35 | 50 | 70 | kΩ |
| $G_{IN}$ | Input Gain Range | Gain | 0 | - | 11.25 | dB |
| $G_{STEP}$ | Step Resolution | | - | 3.75 | - | dB |
| $ERR_G$ | Gain Setting error | | -0.2 | 0 | 0.2 | dB |
| **Volume control** | | | | | | |
| $CR_{VOL}$ | Volume Control Range | Attenuation | -78.75 | - | 0 | dB |
| $RES_{VOL}$ | Volume Step Resolution | | - | 1.25 | - | dB |
| $ERR_{VOL}$ | Volume Setting Error | Av = 0 to -40dB | -0.5 | 0 | 1 | dB |
| | | Av = -40 to -60dB | -1 | 0 | 5 | dB |
| **Speaker Attenuators** | | | | | | |
| $CR_{SPK}$ | Speaker Control Range | Attenuation | -37.5 | - | 0 | dB |
| $RES_{SPK}$ | Speaker Step Resolution | | - | 1.25 | - | dB |
| $ERR_{SPK}$ | Speaker Setting Error | | -0.2 | 0 | 0.1 | dB |
| MUTE | Output Mute Attenuation | | - | -65 | -60 | dB |
| **General** | | | | | | |
| $VO_{MAX}$ | Maximum Output Voltage Swing | (THD+N)/S <0.3% | - | 4.5 | - | Vpp |
| THD+N | Total Harmonic Distortion Plus Noise | $V_{OUT}$=2Vpp | - | -75 | - | dB |
| | | | - | 0.0177 | - | % |
| S/N | Signal-to-Noise Ratio | $V_{OUT}$=4Vpp | - | 97 | - | dB |
| CS | Channel Separation Left/Right | | 93 | 97 | - | dB |
| **Bus Input** | | | | | | |
| $V_{IH}$ | Bus High Input Level | | 2 | - | - | V |
| $V_{IL}$ | Bus Low Input Level | | - | - | 0.8 | V |

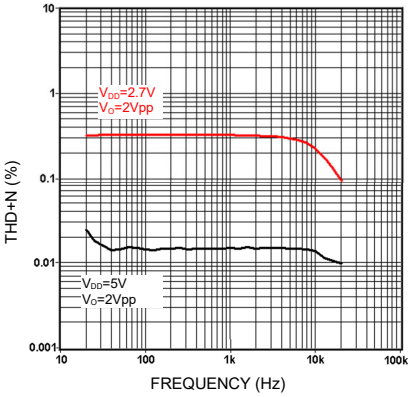
## 2.7V ELECTRICAL CHARACTERISTICS

(Ta=25℃, All stages 0dB, f=1kHz, $C_{REF}$ =22uF, refer to the application circuit; unless otherwise specified)

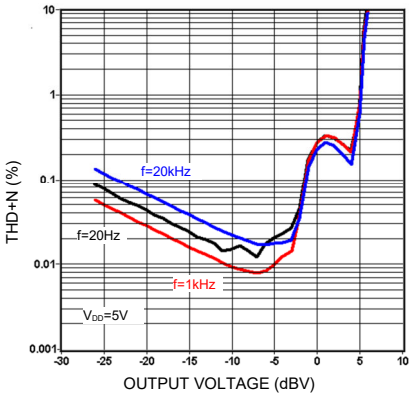
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply** | | | | | | |
| $I_Q$ | Quiescent Current | $V_{IN}$=0V | - | 8.7 | 9 | mA |
| PSRR | Power Supply Rejection Ratio | $C_{REF}$ = 22uF, f = 100Hz | 53 | 58 | - | dB |
| **General** | | | | | | |
| $VO_{MAX}$ | Maximum Output Voltage Swing | (THD+N)/S <0.3% | - | 2.5 | - | Vpp |
| THD+N | Total Harmonic Distortion Plus Noise | $V_{OUT}$=2Vpp | - | -50 | - | dB |
| | | | - | 0.3 | - | % |
| S/N | Signal-to-Noise Ratio | $V_{OUT}$=2.5Vpp | 90 | 94 | - | dB |
| CS | Channel Separation Left/Right | | 90 | 94 | - | dB |

## TYPICAL PERFORMANCE CHARACTERISTICS

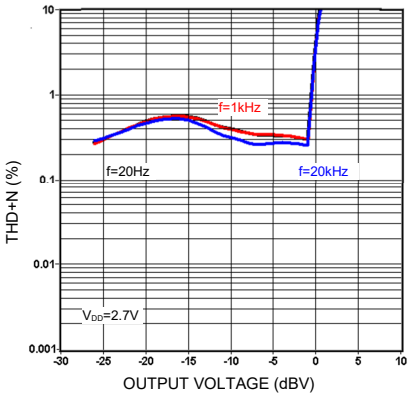
(Ta=25℃, All stages 0dB, f=1kHz, $C_{REF}$ =22uF, refer to the application circuit; unless otherwise specified)



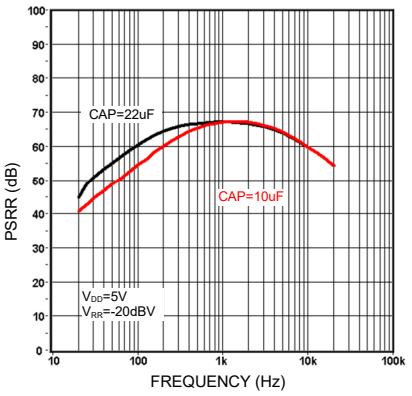

**THD+N vs. Frequency**



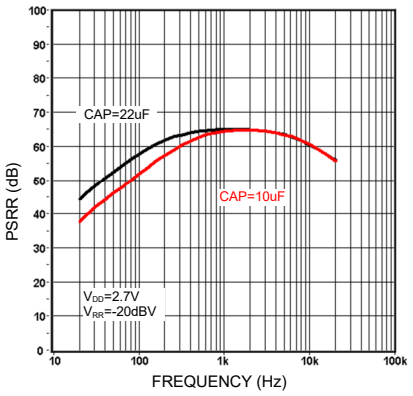

**THD+N vs. Output Voltage**



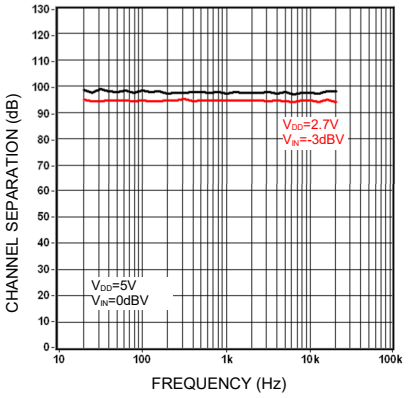

**THD+N vs. Output Voltage**



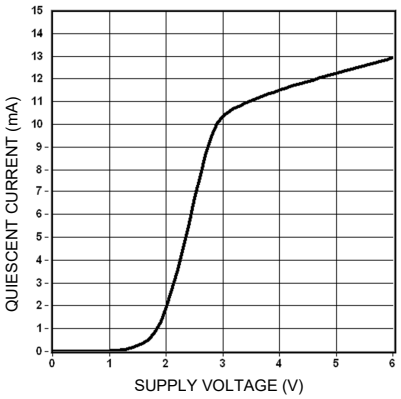

**PSRR vs. Frequency**




**PSRR vs. Frequency**




**Channel Separation vs. Frequency**

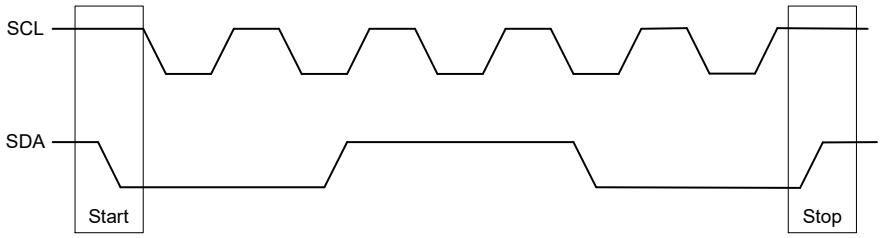



**Quiescent Current vs. Supply Voltage**

# I²C BUS DESCRIPTION

### Start and Stop Conditions

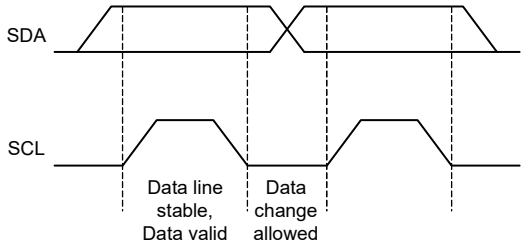
A start condition is activated when the SCL is set to HIGH and SDA shifts from HIGH to LOW state. The stop condition is activated when SCL is set to HIGH and SDA shifts from LOW to HIGH state. Please refer to the timing diagram below.




SCL : Serial Clock Line, SDA : Serial Data Line

### Data Validity

A data on the SDA line is considered valid and stable only when the SCL signal is in HIGH state. The HIGH and LOW states of the SDA line can only change when the SCL signal is LOW. Please refer to the figure below.

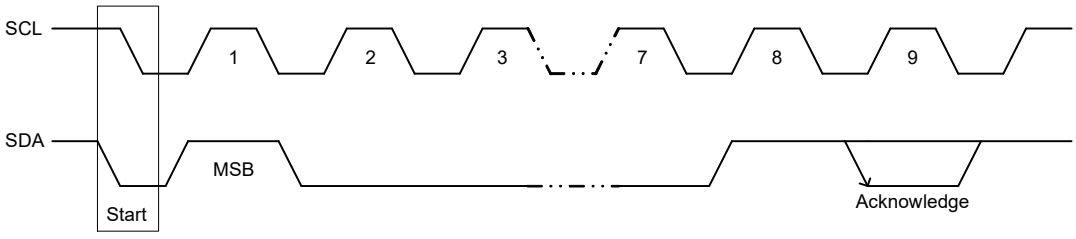



### Byte Format

Every byte transmitted to the SDA line consists of 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transmitted first.

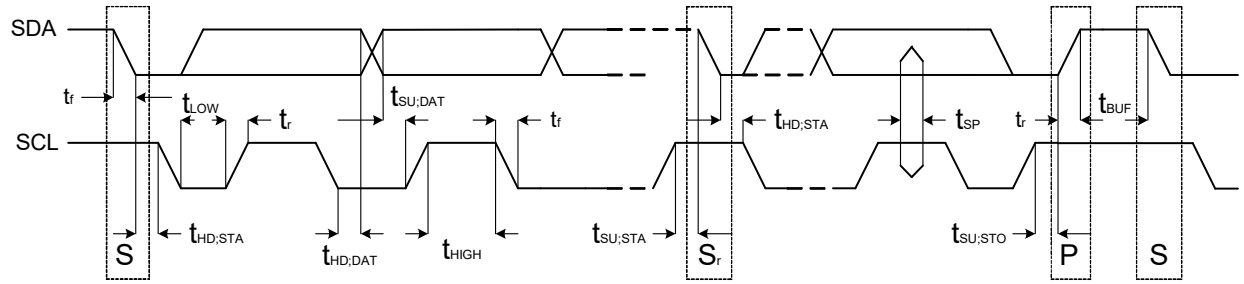
### Acknowledge

During the Acknowledge clock pulse, the master (up) put a resistive HIGH level on the SDA line. The peripheral (audio processor) that acknowledges has to pull-down (LOW) the SDA line during the Acknowledge clock pulse so that the SDA line is in a stable LOW state during this clock pulse. Please refer to the diagram below.




The audio processor that has been addressed has to generate an Acknowledge after receiving each byte, otherwise, the SDA line will remain at the HIGH level during the ninth (9th) clock pulse. In this case, the master transmitter can generate the STOP information in order to abort the transfer.

**Timing of SDA and SCL Bus Lines**

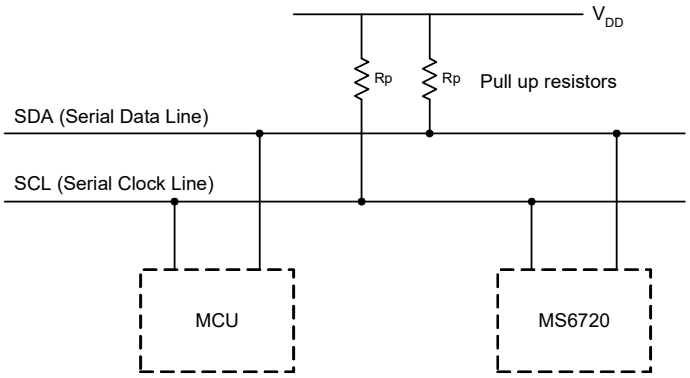



**Standard Mode**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | 0 | 100 | kHz |
| $t_{HD:STA}$ | Hold time (repeated) START condition. After this period, the first clock pulse is generated | 4.0 | - | us |
| $t_{LOW}$ | LOW period of the SCL clock | 4.7 | - | us |
| $t_{HIGH}$ | HIGH period of the SCL clock | 4.0 | - | us |
| $t_{SU:STA}$ | Set-up time for a repeated START condition | 4.7 | - | us |
| $t_{HD:DAT}$ | Data hold time: For $I^2C$-bus devices | 0 | 3.45 | us |
| $t_{SU:DAT}$ | Data-set-up time | 250 | - | ns |
| $t_r$ | Rise time of both SDA and SCL signals | - | 1000 | ns |
| $t_f$ | Fall time of both SDA and SCL signals | - | 300 | ns |
| $t_{SU:STO}$ | Set-up time for STOP condition | 4.0 | - | us |
| $t_{BUF}$ | Bus free time between a STOP and START condition | 4.7 | - | us |
| $C_b$ | Capacitive load for each bus line | - | 400 | pF |
| $V_{nL}$ | Noise margin at the LOW level for each connected device (including hysteresis) | $0.1V_{DD}$ | - | V |
| $V_{nH}$ | Noise margin at the HIGH level for each connected device (including hysteresis) | $0.2V_{DD}$ | - | V |

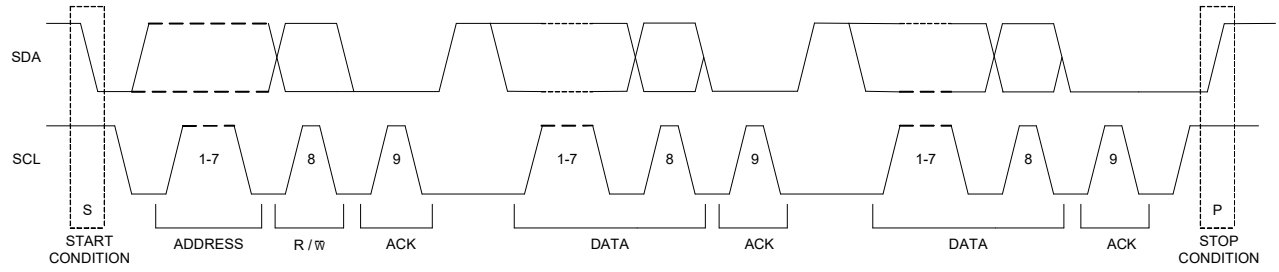
## BUS INTERFACE

Data are transmitted to and from the MCU to the MS6720 via the SDA and SCL. The SDA and SCL make up the BUS interface. It should be noted that pull-up resistors must be connected to the positive supply voltage.



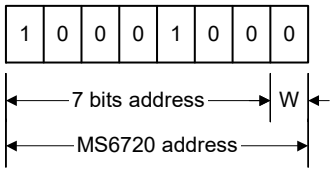
**Interface Protocol**

The format consists of the following
- A START condition
- A chip address byte including the MS6720 address. (7bits)
- The 8th bit of the byte must be "0".(write)
- MS6720 must always acknowledge the end of each transmitted byte.
- A data sequence (N-bytes + Acknowledge)
- A STOP condition




**Address Code**

The chip address of the MS6720 is 88H.




**Data Bytes Description**

The default states of the chip as the power is on are: the volume is -78.75dB, the stereo 4 is selected, all the speakers are mute and the gains of the input stage are 0dB.

| MSB | | | | | | | LSB | Function |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | B2 | B1 | B0 | A2 | A1 | A0 | Volume Control |
| 1 | 1 | 0 | B1 | B0 | A2 | A1 | A0 | Speaker ATT LR |
| 1 | 1 | 1 | B1 | B0 | A2 | A1 | A0 | Speaker ATT RR |
| 1 | 0 | 0 | B1 | B0 | A2 | A1 | A0 | Speaker ATT LF |
| 1 | 0 | 1 | B1 | B0 | A2 | A1 | A0 | Speaker ATT RF |
| 0 | 1 | 0 | G1 | G0 | 1 | S1 | S0 | Audio Switch |

Where Ax = 1.25dB/step; Bx = 10dB/step; Cx = 2dB/step; Gx = 3.75dB/step

**Volume**

| MSB | | | | | | | LSB | Function |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **B2** | **B1** | **B0** | **A2** | **A1** | **A0** | **Volume 1.25 dB steps** |
| | | | | | 0 | 0 | 0 | 0 |
| | | | | | 0 | 0 | 1 | -1.25 |
| | | | | | 0 | 1 | 0 | -2.5 |
| | | | | | 0 | 1 | 1 | -3.75 |
| | | | | | 1 | 0 | 0 | -5 |
| | | | | | 1 | 0 | 1 | -6.25 |
| | | | | | 1 | 1 | 0 | -7.5 |
| | | | | | 1 | 1 | 1 | -8.75 |
| **0** | **0** | **B2** | **B1** | **B0** | **A2** | **A1** | **A0** | **Volume 10dB steps** |
| | | 0 | 0 | 0 | | | | 0 |
| | | 0 | 0 | 1 | | | | -10 |
| | | 0 | 1 | 0 | | | | -20 |
| | | 0 | 1 | 1 | | | | -30 |
| | | 1 | 0 | 0 | | | | -40 |
| | | 1 | 0 | 1 | | | | -50 |
| | | 1 | 1 | 0 | | | | -60 |
| | | 1 | 1 | 1 | | | | -70 |

The default volume is –78.75dB.

**Speaker Attenuator**

| MSB | | | | | | | LSB | Function（dB） |
|---|---|---|---|---|---|---|---|---|
| **1** | **0** | **0** | **B1** | **B0** | **A2** | **A1** | **A0** | **Speaker LF** |
| **1** | **0** | **1** | **B1** | **B0** | **A2** | **A1** | **A0** | **Speaker RF** |
| **1** | **1** | **0** | **B1** | **B0** | **A2** | **A1** | **A0** | **Speaker LR** |
| **1** | **1** | **1** | **B1** | **B0** | **A2** | **A1** | **A0** | **Speaker RR** |
| | | | | | 0 | 0 | 0 | 0 |
| | | | | | 0 | 0 | 1 | -1.25 |
| | | | | | 0 | 1 | 0 | -2.5 |
| | | | | | 0 | 1 | 1 | -3.75 |
| | | | | | 1 | 0 | 0 | -5 |
| | | | | | 1 | 0 | 1 | -6.25 |
| | | | | | 1 | 1 | 0 | -7.5 |
| | | | | | 1 | 1 | 1 | -8.75 |
| | | | 0 | 0 | | | | 0 |
| | | | 0 | 1 | | | | -10 |
| | | | 1 | 0 | | | | -20 |
| | | | 1 | 1 | | | | -30 |
| | | | 1 | 1 | 1 | 1 | 1 | Mute |

LF: Left Front, RF: Right Front, LR: Left Rear, RR: Right Rear
The default state is mute.

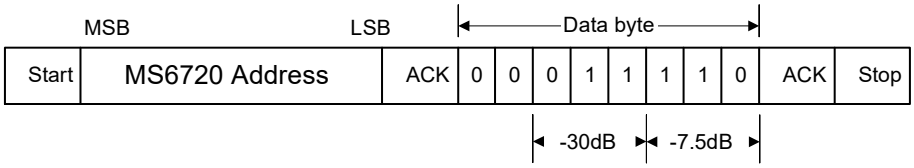
**Audio Switch**

| MSB | | | | | | | LSB | Function |
|---|---|---|---|---|---|---|---|---|
| **0** | **1** | **0** | **G1** | **G0** | **1** | **S1** | **S0** | **Audio Switch** |
| | | | | | | 0 | 0 | Stereo 1 |
| | | | | | | 0 | 1 | Stereo 2 |
| | | | | | | 1 | 0 | Stereo 3 |
| | | | | | | 1 | 1 | *Stereo 4 |
| | | | 0 | 0 | | | | +11.25dB |
| | | | 0 | 1 | | | | +7.5dB |
| | | | 1 | 0 | | | | +3.75dB |
| | | | 1 | 1 | | | | 0dB |

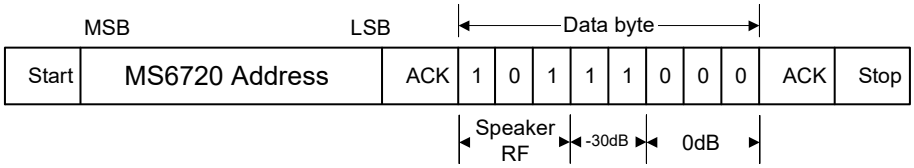
* The stereo 4 is connected internally, but not available on pins.
The default state is stereo 4 and gain 0dB.

**Examples**

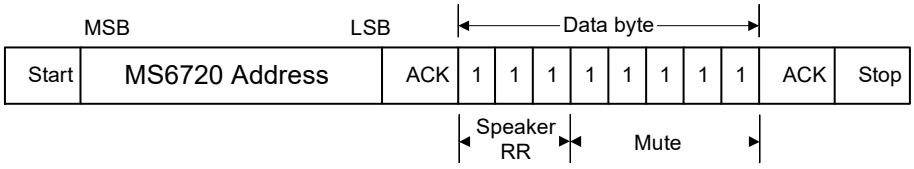
Set Volume at –37.5dB.



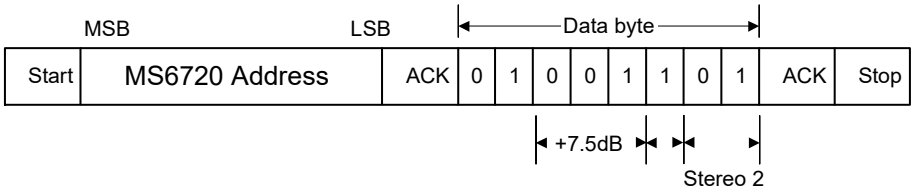

Set Speaker RF at –30dB.




Set Speaker RR in mute-on.

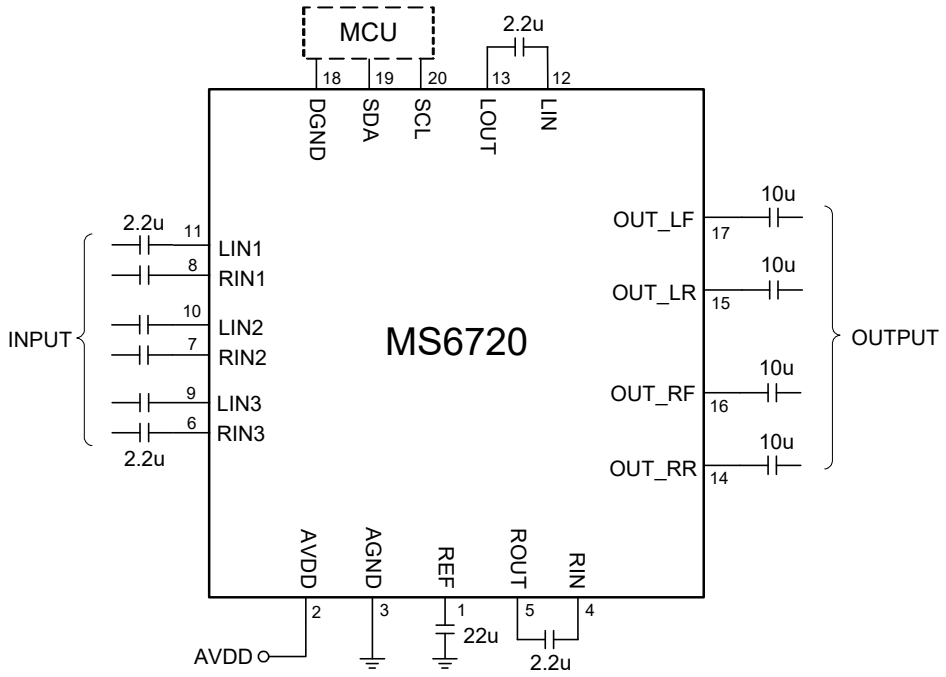



Set Stereo 2 Input with gain of +7.5dB



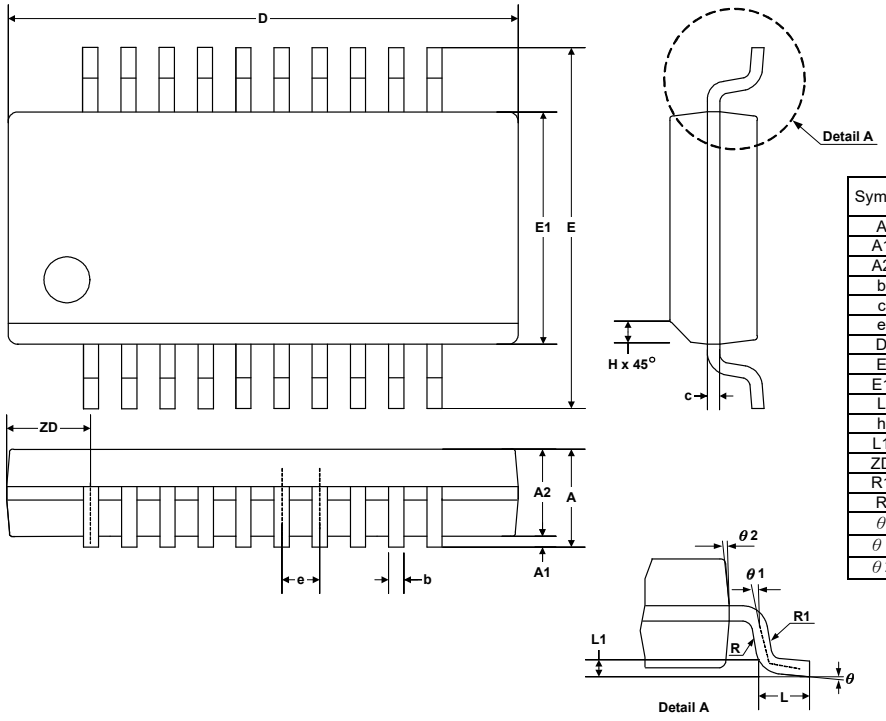
## APPLICATION INFORMATION

### Basic Application Example




## EXTERNAL DIMENSIONS

### SSOP20




| Symbol | Dimension in mm | | Dimension in inch | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.35 | 1.75 | 0.053 | 0.069 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A2 | | 1.50 | | 0.059 |
| b | 0.20 | 0.30 | 0.008 | 0.012 |
| c | 0.18 | 0.25 | 0.007 | 0.010 |
| e | 0.635 BASIC | | 0.025 BASIC | |
| D | 8.56 | 8.74 | 0.337 | 0.344 |
| E | 5.79 | 6.20 | 0.228 | 0.244 |
| E1 | 3.81 | 3.99 | 0.150 | 0.157 |
| L | 0.41 | 1.27 | 0.016 | 0.050 |
| h | 0.25 | 0.50 | 0.010 | 0.020 |
| L1 | 0.254 BASIC | | 0.010 BASIC | |
| ZD | 1.4732 REF | | 0.058 REF | |
| R1 | 0.20 | 0.33 | 0.008 | 0.013 |
| R | 0.20 | | 0.008 | |
| $\theta$ | 0° | 8° | 0° | 8° |
| $\theta$1 | 0° | | 0° | |
| $\theta$2 | 5° | 15° | 5° | 15° |