4 Stereo Inputs, 2W BTL Stereo Output 16-bit Stereo DAC and Volume Control

FEATURES

- Operation range: 2.4V ~ 6.5V
- Volume control range
  Gain: 0 to 21dB, 3dB/step
  Attenuation: 0 to –77.5dB, 1.25dB/step
- 4 stereo inputs (mixed with an audio DAC)
- Output mode : Speaker(BTL)/Headphone(SE)
- BTL Output power, THD+N=1%, Stereo Input
  R_L=4Ω, 2W at 5V, 0.8W at 3.3V, 360mW at 2.4V
  R_L=8Ω, 1.3W at 5V, 0.53W at 3.3V, 250mW at 2.4V
- BTL Output power, DAC Input
  R_L=4Ω, 1.6W at 5V, 0.70W at 3.3V, 340mW at 2.4V
  R_L=8Ω, 0.83W at 5V, 0.35W at 3.3V, 170mW at 2.4V
- Built-in 16-bit Audio DAC
- Audio format : I^2S, Right justified, Left justified
- Control interface : I^2C
- Excellent Power Supply Rejection Ratio(PSRR)
- Flexibility power management
- Component less
- Reduce pop noise circuit
- Housed in TSSOP28 package, enhanced thermal PAD

APPLICATIONS

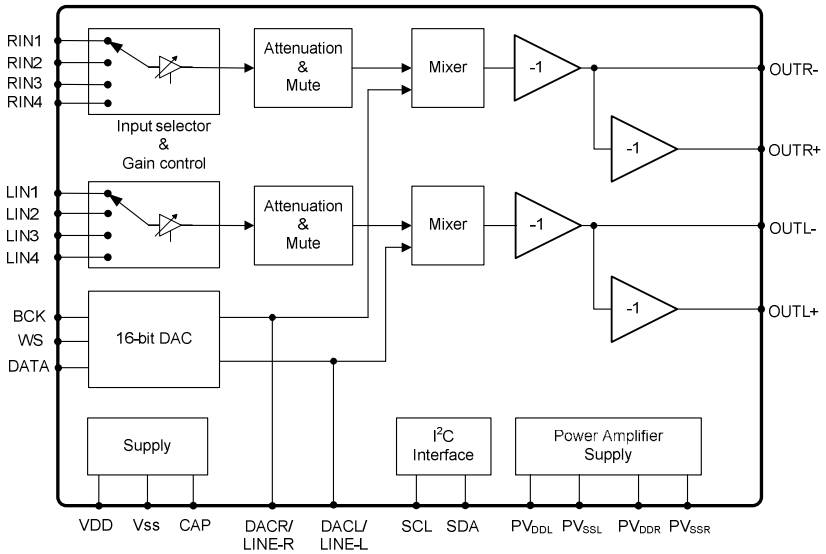
Multimedia system, Portable Digital Audio.

DESCRIPTION

The MS6821 is a 16-bits voltage-output Digital-to-Analog Converter (DAC) integrated class AB stereo headphone driver and stereo speaker power amplifier. It can drive 2W of continuous average power into a dual 4Ω bridged-tied (BTL) speaker or 2 * 90mW into stereo 32Ω single ended (SE) headphone. The 16-bit DAC supports general and popular formats as I2S, Right justified. The volume control offers wide range of gain and attenuation for 4-set stereo input. All of the functions are set by I2C interface.

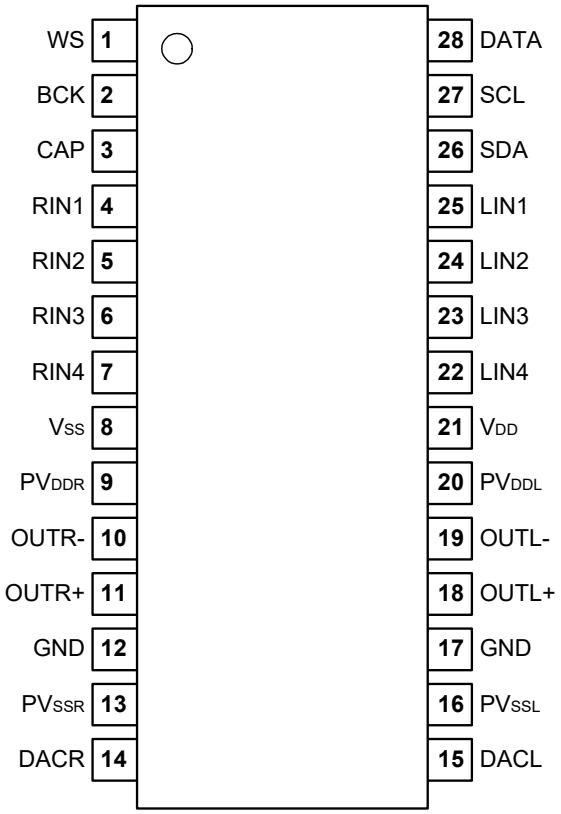
The MS6821 has good feature for portable equipment, including wide voltage operation 2.4V ~ 6.5V, low power consumption, flexible power management, component less and small package TSSOP28, make the MS6821 ideally suitable for use in the portable digital audio equipments.

BLOCK DIAGRAM



PIN CONFIGURATION

Symbol	Pin	Description
WS	1	Audio word select input
BCK	2	Audio bit clock input
CAP	3	Capacitor connected
RIN1	4	Right channel input 1
RIN2	5	Right channel input 2
RIN3	6	Right channel input 3
RIN4	7	Right channel input 4
V_{SS}	8	Negative supply voltage
PV_{DDR}	9	Positive supply voltage for right channel of power amplifier
OUTR-	10	SE right channel output or negative output of BTL right channel
OUTR+	11	Positive output of BTL right channel
GND	12	Connected to ground
PV_{SSR}	13	Negative supply voltage for right channel of power amplifier
DACR	14	DAC right channel output
DACL	15	DAC Left channel output
PV_{SSL}	16	Negative supply voltage for left channel of power amplifier
GND	17	Connected to ground
OUTL+	18	Positive output of BTL left channel
OUTL-	19	SE left channel output or negative output of BTL left channel
PV_{DDL}	20	Positive supply voltage for left channel of power amplifier
V_{DD}	21	Positive supply voltage
LIN4	22	Left channel input 4
LIN3	23	Left channel input 3
LIN2	24	Left channel input 2
LIN1	25	Left channel input 1
SDA	26	I^2C data input
SCL	27	I^2C clock input
DATA	28	Audio data input



Note: 1. SE: Single Ended. BTL: Bridged-Tied Load

ORDERING INFORMATION

Package	Part number	Packaging Marking	Transport Media
28Pin TSSOP (lead free)	MS6821TGTR	MS6821G	2.5k Units Tape and Reel
28Pin TSSOP (lead free)	MS6821TGU	MS6821G	50 Units Tube

RoHS Compliance

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
V_{DD}	Supply voltage	6.5	V
V_{ESD}	Electrostatic handling	2000	V
T_{STG}	Storage temperature range	-65 to 150	℃
T_A	Operating ambient temperature range	-40 to 85	℃
T_J	Maximum junction temperature	150	℃
T_S	Soldering temperature, 10 seconds	260	℃
R_{THJA}	Thermal resistance from junction to ambient in free air TSSOP28 (enhance thermal pad)	51	℃/W

OPERATING RATINGS

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	2.4	5	6.5	V

5V ELECTRICAL CHARACTERISTICS

(Ta=25℃, V_{DD}=5V, V_{SS}=0V, f=1kHz; unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DC Characteristics						
V_{CAP}	Voltage at CAP		$0.5V_{DD}$ -0.05	$0.5V_{DD}$	$0.5V_{DD}$ +0.05	V
V_{DC}	Output DC level		$0.5V_{DD}$ -0.05	$0.5V_{DD}$	$0.5V_{DD}$ +0.05	V
I_Q	Quiescent current	All devices are active, BTL	-	13.0	-	mA
		All devices are active, SE	-	9.8	-	
		DAC PD, BTL	-	9.9	-	
		DAC PD, SE	-	6.7	-	
		L-ch (R-ch) PD, BTL DAC active	-	8.2	-	
		L-ch (R-ch) PD, SE DAC active	-	6.6	-	
		Only DAC is active	-	3.2	-	
I_{PD}	Power down current	All devices power down	-	-	0.3	uA
		All devices power down, except CAP=1/2 VDD		12		
ATT	Mute attenuation				-90	dB
GA_{RAN}	Gain/Attenuation range	Gain	0	-	21	dB
		Attenuation	-77.5		0	dB
G_{STEP}	Gain step		-	3	-	dB
A_{STEP}	Attenuation step		-	1.25	-	dB
E_{GA}	Gain/Attenuation step error		-	0.3	-	dB
V_{I2CH}	Serial interface high input level		2			V
V_{I2CL}	Serial interface low input level				0.8	V
AC Characteristics (Stereo input)						
PSRR	Power supply rejection ratio	BTL Mode , R_L=8Ω CAP=1uF, f=200Hz	-	61	-	dB
		SE Mode , R_L=32Ω CAP=1uF, f=200Hz	-	65	-	dB
CS	Channel separation	BTL Mode, R_L=8Ω Po=1W	-	78	-	dB
		SE Mode, R_L=32Ω Po=60mW	-	81	-	dB
THD+N	Total harmonic distortion plus Noise	SE mode, R_L=32Ω, 60mW	-	-65	-	dB
			-	0.0562	-	%
S/N	Signal-to-noise ratio	SE mode, A-weighting, 75mW	-	93	-	dB
Po	Maximum output power	BTL Mode, R_L = 4Ω THD+N = 1%	-	2	-	W
		BTL Mode, R_L = 8Ω THD+N = 1%	-	1.3	-	W
		SE Mode, R_L = 32Ω THD+N = 0.1%	-	93m	-	W

PD: Power Down

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Audio DAC Characteristics (sampling rate=4fs, fs= 44.1kHz, f=1kHz)						
Res	Resolution		-	-	16	bits
V_{FSDAC}	Full scale output voltage of DAC	V_{FS}=0.72 * V_{DD}	V_{FS}-1.5%	V_{FS}	V_{FS}+1.5%	V
PSRR	Power supply rejection ratio	CAP=1uF (200Hz)		66	-	dB
		CAP=10uF (200Hz)		67	-	
CS	Channel separation			88		dB
THD+N	Total harmonic distortion plus noise	DAC output, R_L=1kΩ, V_{FS}	-	-67	-62	dB
			-	0.0447	0.079	%
S/N	Signal-to-noise ratio	DAC output, R_L=1kΩ, V_{FS} A-weighting	86	90	-	dB
DACPo	Maximum output power using DAC	BTL Mode, R_L = 4Ω THD+N = 0.33%	1.44	1.6	-	W
		BTL Mode, R_L = 8Ω THD+N = 0.15 %	0.75	0.83	-	W
		SE Mode, R_L = 32Ω THD+N = 0.042%	41.4m	46m	-	W

3.3V ELECTRICAL CHARACTERISTICS

(Ta=25℃, V_{DD}=3.3V, V_{SS}=0V, f=1kHz; unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DC Characteristics						
I_Q	Quiescent current	All devices are active, BTL	-	11.5	-	mA
		All devices are active, SE	-	8.5	-	
		DAC PD, BTL	-	9	-	
		DAC PD, SE	-	6	-	
		L-ch (R-ch) PD, BTL DAC active	-	7.1	-	
		L-ch (R-ch) PD, SE DAC active	-	5.6	-	
		Only DAC is active	-	2.6	-	
AC Characteristics (Stereo input)						
THD+N	Total harmonic distortion plus Noise	SE mode, R_L=32Ω, 35mW	-	-67	60	dB
			-	0.0447	0.1	%
Po	Maximum output power	BTL Mode, R_L = 4Ω THD+N = 1%	-	0.8	-	W
		BTL Mode, R_L = 8Ω THD+N = 1%	-	0.53	-	W
		SE Mode, R_L = 32Ω THD+N = 0.1%	-	35m	-	W
Audio DAC Characteristics (sampling rate=4fs, fs= 44.1kHz, f=1kHz)						
THD+N	Total harmonic distortion plus noise	DAC output, R_L=1kΩ, V_{FS}	-	-66	60	dB
			-	0.05	0.1	%
DACPo	Maximum output power using DAC	BTL Mode, R_L = 4Ω THD+N = 0.25%	0.63	0.70	-	W
		BTL Mode, R_L = 8Ω THD+N = 0.14 %	0.32	0.35	-	W
		SE Mode, R_L = 32Ω THD+N = 0.052%	18m	20m	-	W

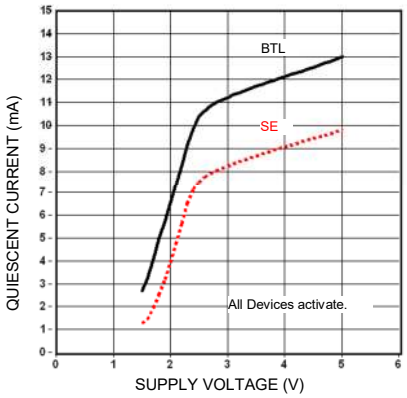
2.4V ELECTRICAL CHARACTERISTICS

(Ta=25℃, V_{DD}=2.4V, V_{SS}=0V, f=1kHz; unless otherwise specified)

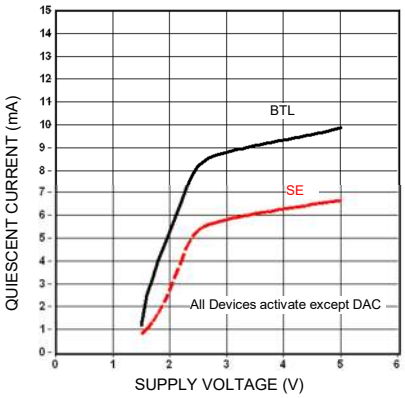
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DC Characteristics						
I_Q	Quiescent current	All devices are active, BTL	-	9.9	-	mA
		All devices are active, SE	-	7.1	-	
		DAC PD, BTL	-	7.8	-	
		DAC PD, SE	-	5.1	-	
		L-ch (R-ch) PD, BTL DAC active	-	6	-	
		L-ch (R-ch) PD, SE DAC active	-	4.7	-	
		Only DAC is active	-	2.2	-	
AC Characteristics (Stereo input)						
THD+N	Total harmonic distortion plus Noise	SE mode, R_L=32Ω, 15mW	-	-65	-60	dB
			-	0.0562	0.1	%
Po	Maximum output power	BTL Mode, R_L = 4Ω THD+N = 1%	-	0.36	-	W
		BTL Mode, R_L = 8Ω THD+N = 1%	-	0.25	-	W
		SE Mode, R_L = 32Ω THD+N = 0.1%	-	15m	-	W
Audio DAC Characteristics (sampling rate=4fs, fs= 44.1kHz, f=1kHz)						
THD+N	Total harmonic distortion plus noise	DAC output, R_L=1kΩ, V_{FS}	-	-63	-58	dB
			-	0.071	0.126	%
DACPo	Maximum output power using DAC	BTL Mode, R_L = 4Ω THD+N = 0.85%	0.31	0.34	-	W
		BTL Mode, R_L = 8Ω THD+N = 0.17 %	0.15	0.17	-	W
		SE Mode, R_L = 32Ω THD+N = 0.07%	9m	10m	-	W

TYPICAL PERFORMANCE CHARACTERISTICS

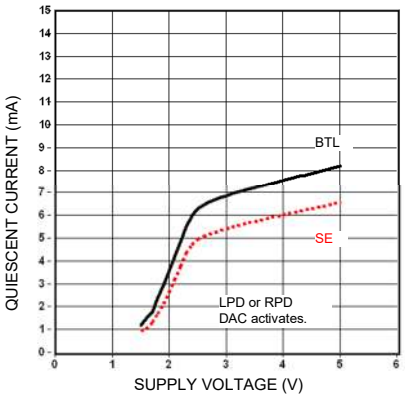
(Ta=25℃; unless otherwise specified)



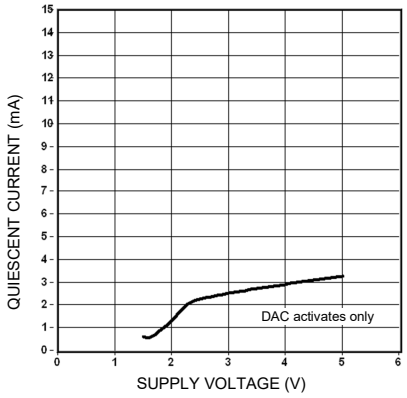
Quiescent current vs. supply voltage



Quiescent current vs. supply voltage



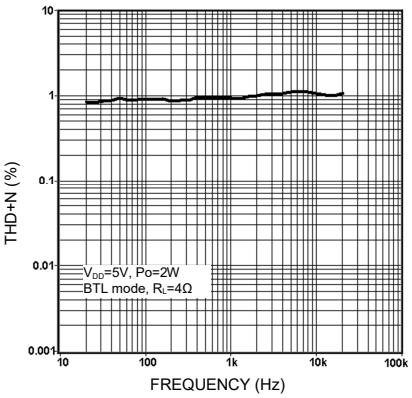
Quiescent current vs. supply voltage



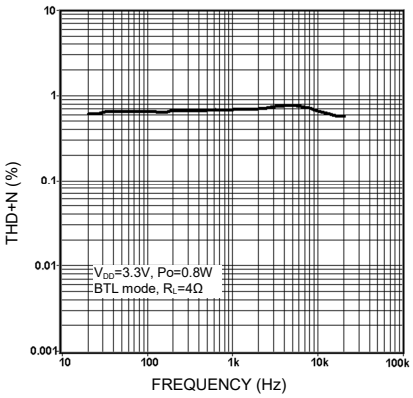
Quiescent current vs. supply voltage

Stereo inputs signal

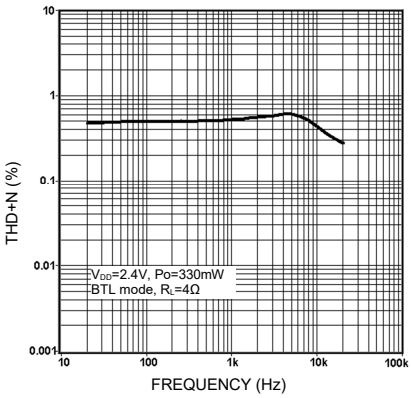
(Ta=25℃, stereo inputs signal, f=1kHz, DAC is Power Down mode; unless otherwise specified)



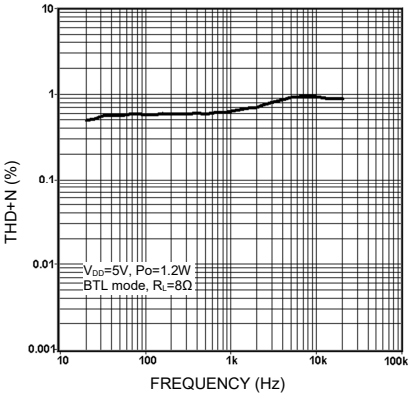
THD+N vs. frequency



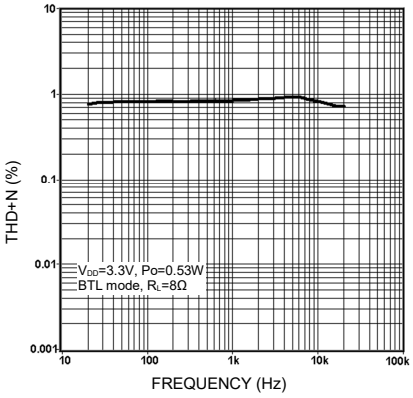
THD+N vs. frequency



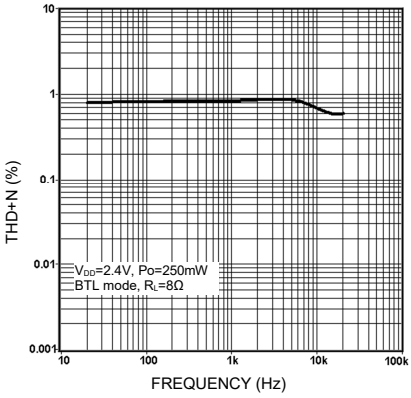
THD+N vs. frequency



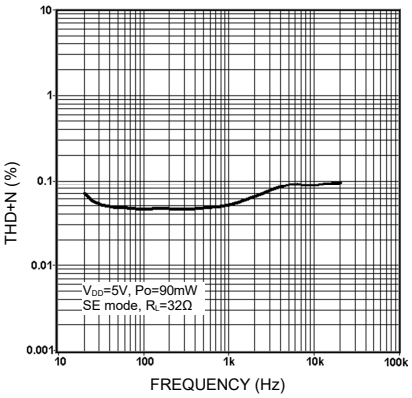
THD+N vs. frequency



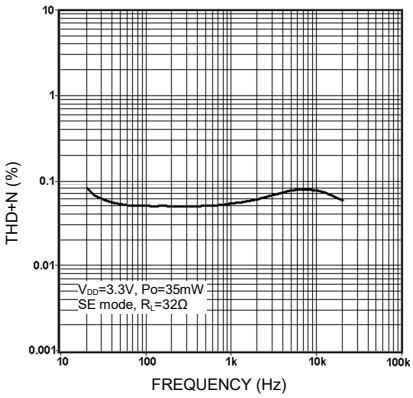
THD+N vs. frequency



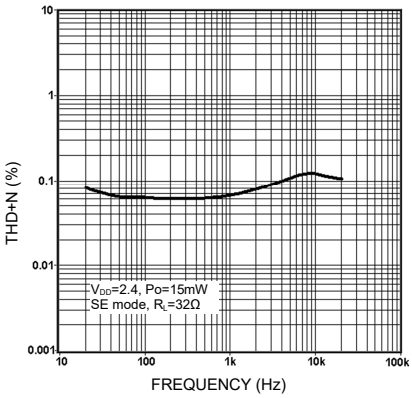
THD+N vs. frequency



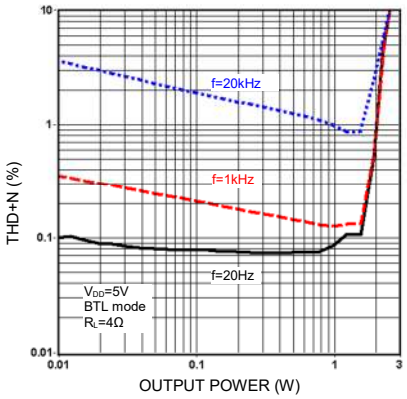
THD+N vs. frequency



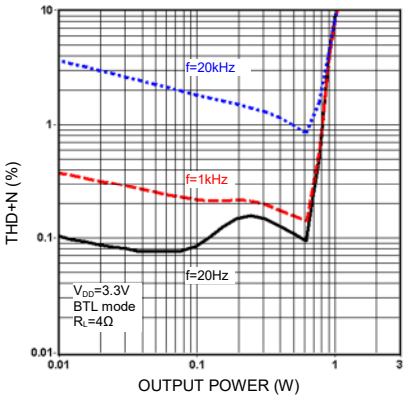
THD+N vs. frequency



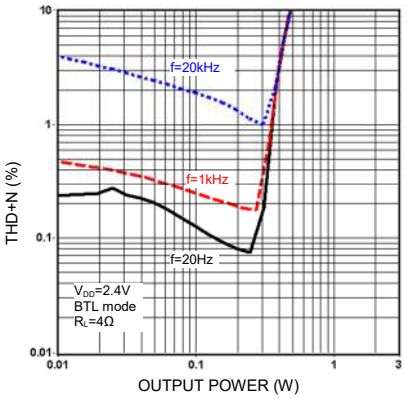
THD+N vs. frequency



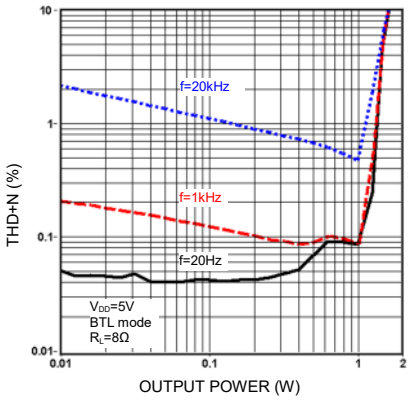
THD+N vs. output power



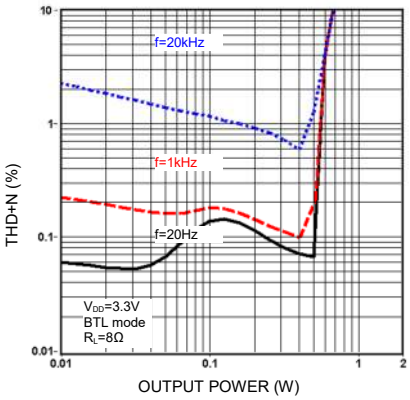
THD+N vs. output power



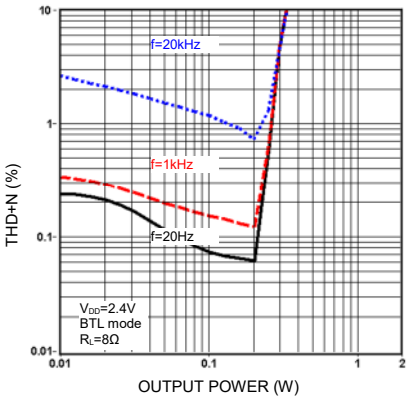
THD+N vs. output power



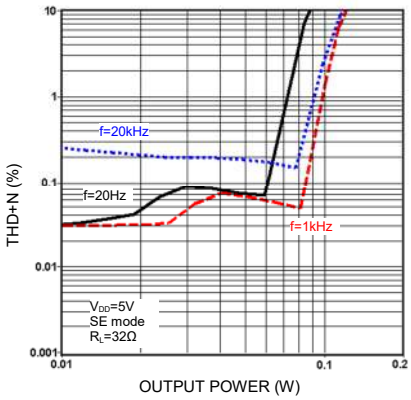
THD+N vs. output power



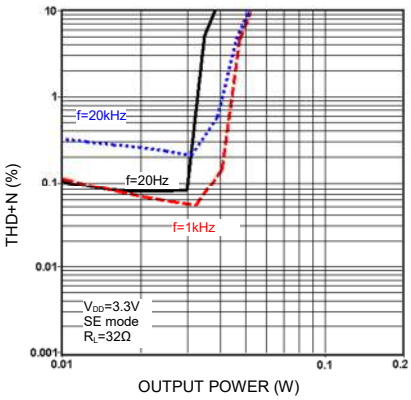
THD+N vs. output power



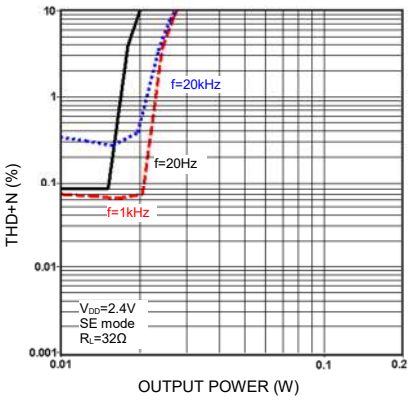
THD+N vs. output power



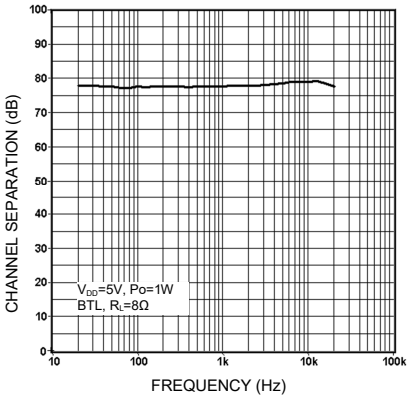
THD+N vs. output power



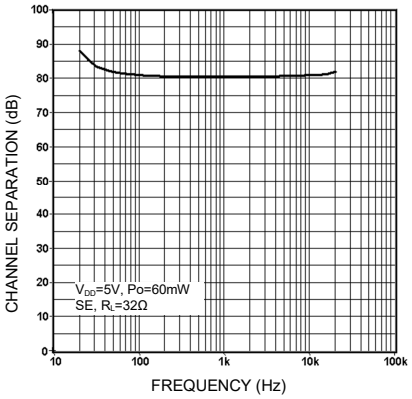
THD+N vs. output power



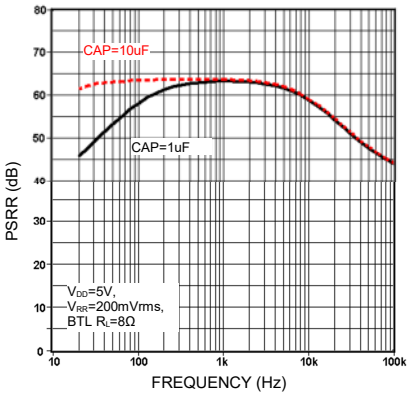
THD+N vs. output power



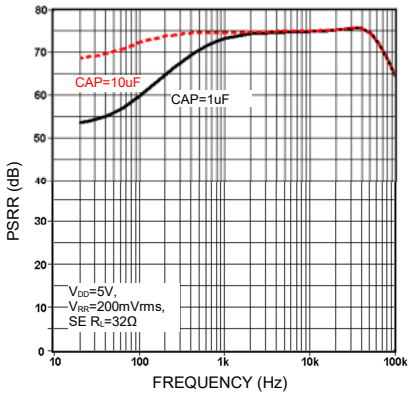
Channel separation vs. frequency



Channel separation vs. frequency



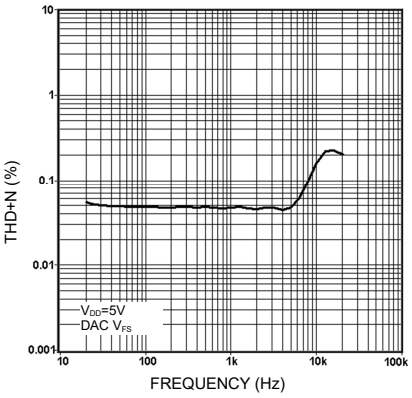
PSRR vs. frequency



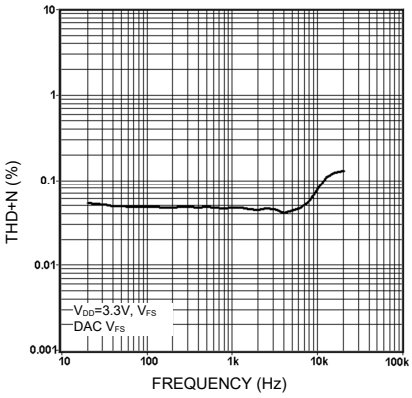
PSRR vs. frequency

DAC inputs signal

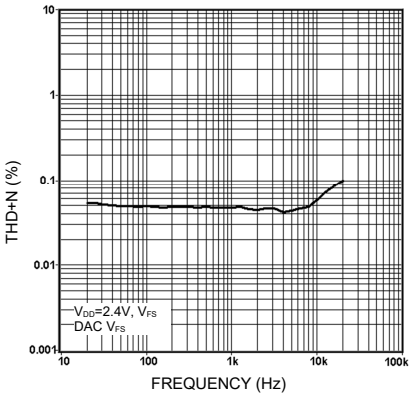
(Ta=25℃, sampling rate=4fs, fs= 44.1kHz, f=1kHz, PA is Power Down mode; unless otherwise specified)



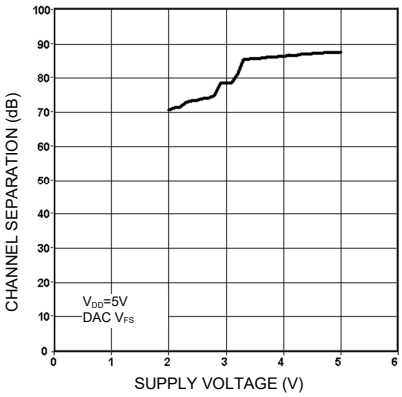
THD+N vs. frequency



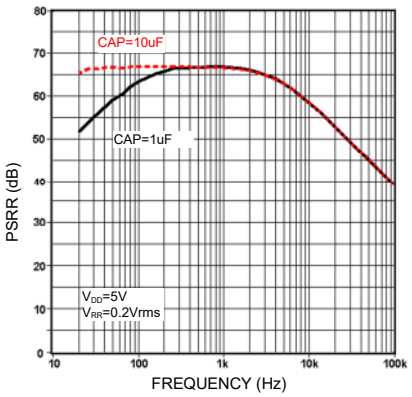
THD+N vs. frequency



THD+N vs. frequency



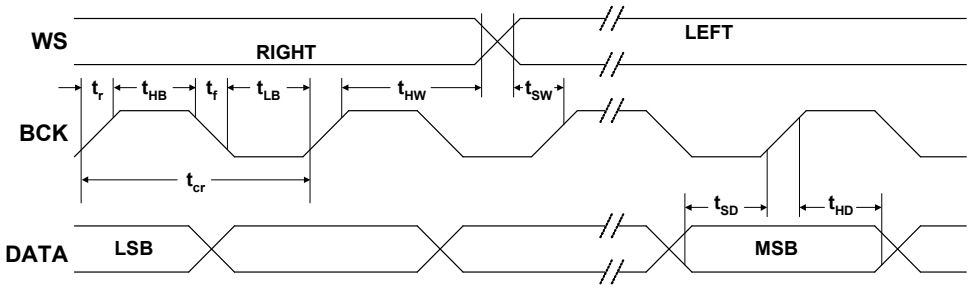
Channel separation vs. supply voltage



PSRR vs. frequency

AUDIO TIMING AND FORMAT

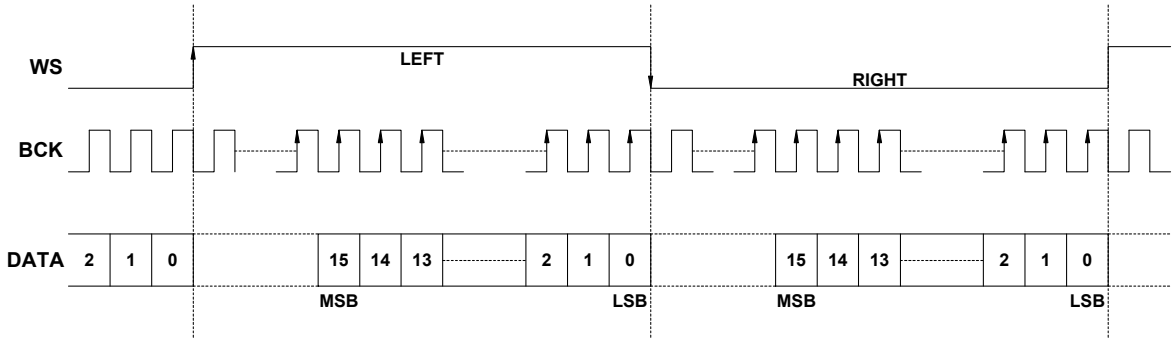
The MS6821 accepts input serial data formats of 16-bit word length. Left and right data words are time multiplexed. The MSB must always be first.



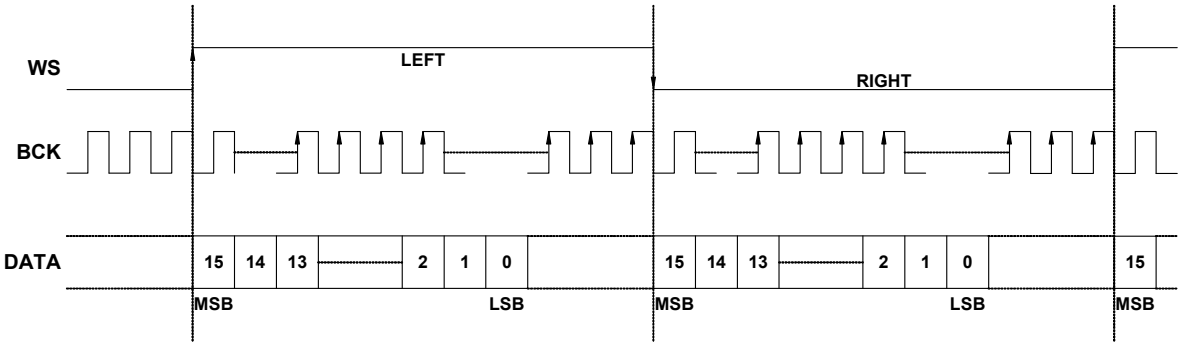
Audio data format (BCK, WS, DATA)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input LOW level		2	-	-	V
V_{IH}	Input HIGH level		-	-	0.8	V
f_{BCK}	Input Clock Frequency		-	-	18.4	MHz
BR	Bit Rate Data Input		-	-	18.4	Mbits/s
f_{ws}	Word Select Input		-	-	384	kHz
t_r	Rise Time		-	-	12	ns
t_f	Fall Time		-	-	12	ns
t_{Cr}	Bit Clock Cycle Time		54	-	-	ns
t_{HB}	Bit Clock High Time		15	-	-	ns
t_{LB}	Bit Clock Low Time		15	-	-	ns
t_{SD}	Data Set-up Time		12	-	-	ns
t_{HD}	Data Hold Time to Bit Clock		2	-	-	ns
t_{HW}	Word Select Hold Time		2	-	-	ns
t_{SW}	Word Select Set-up Time		12	-	-	ns

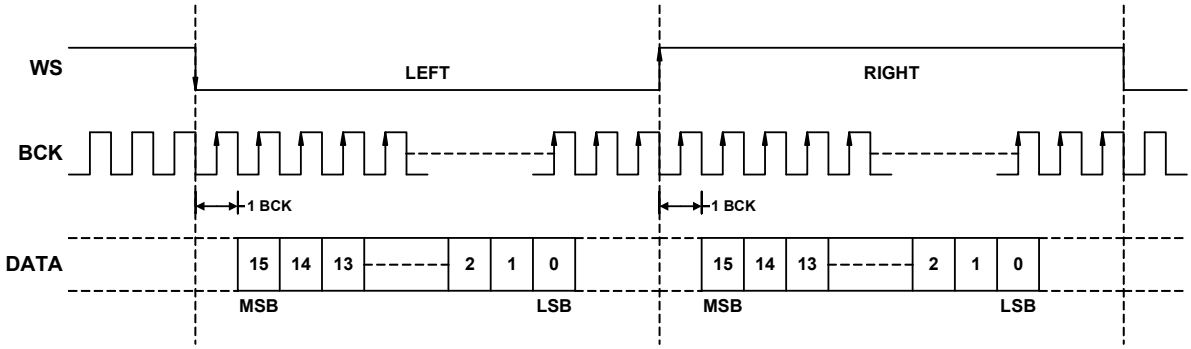
Right justified format



Left justified format



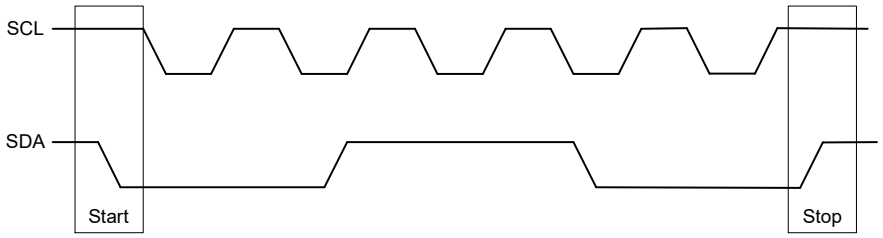
I2S format



I²C BUS DESCRIPTION

Start and Stop Conditions

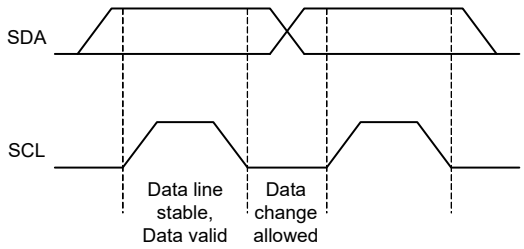
A start condition is activated when the SCL is set to HIGH and SDA shifts from HIGH to LOW state. The stop condition is activated when SCL is set to HIGH and SDA shifts from LOW to HIGH state. Please refer to the timing diagram below.



SCL : Serial Clock Line, SDA : Serial Data Line

Data Validity

A data on the SDA line is considered valid and stable only when the SCL signal is in HIGH state. The HIGH and LOW states of the SDA line can only change when the SCL signal is LOW. Please refer to the figure below.

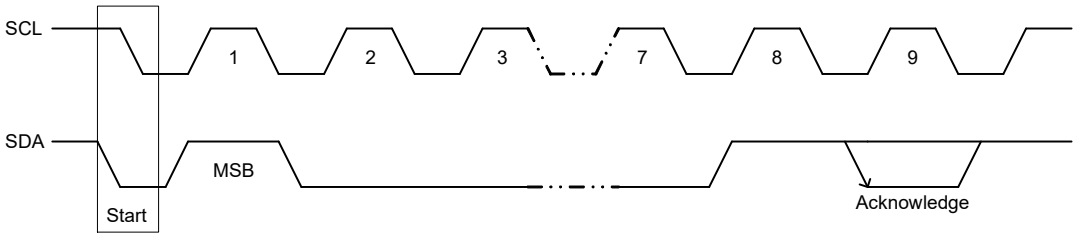


Byte Format

Every byte transmitted to the SDA line consists of 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transmitted first.

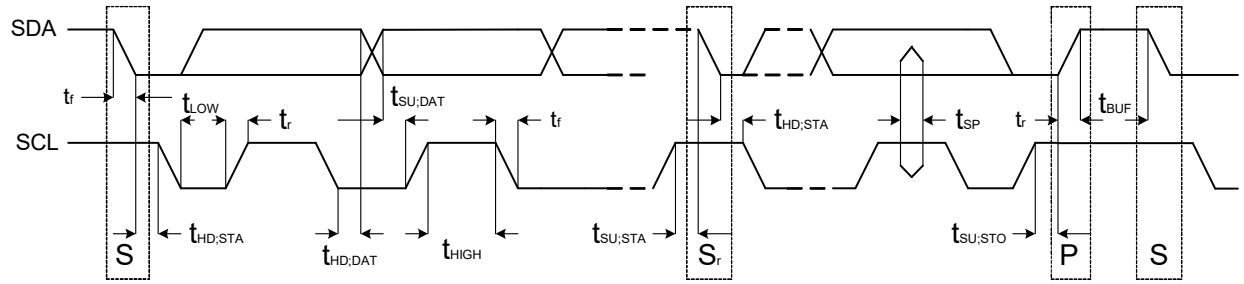
Acknowledge

During the Acknowledge clock pulse, the master (up) put a resistive HIGH level on the SDA line. The peripheral (audio processor) that acknowledges has to pull-down (LOW) the SDA line during the Acknowledge clock pulse so that the SDA line is in a stable LOW state during this clock pulse. Please refer to the diagram below.



The audio processor that has been addressed has to generate an Acknowledge after receiving each byte, otherwise, the SDA line will remain at the HIGH level during the ninth (9th) clock pulse. In this case, the master transmitter can generate the STOP information in order to abort the transfer.

Timing of SDA and SCL Bus Lines

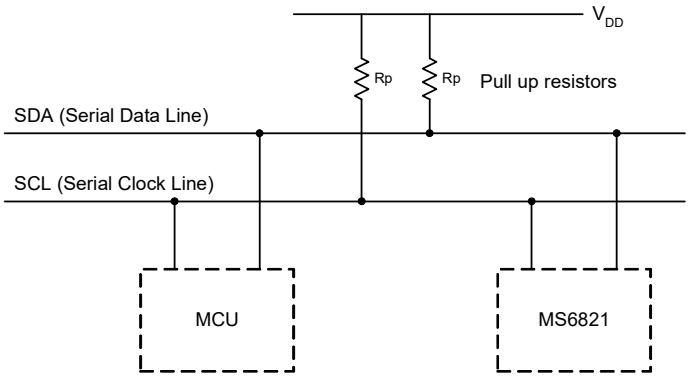


Standard Mode

Symbol	Parameter	Min	Max	Unit
f_{SCL}	SCL clock frequency	0	100	kHz
$t_{HD:STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	-	us
t_{LOW}	LOW period of the SCL clock	4.7	-	us
t_{HIGH}	HIGH period of the SCL clock	4.0	-	us
$t_{SU:STA}$	Set-up time for a repeated START condition	4.7	-	us
$t_{HD:DAT}$	Data hold time: For I^2C-bus devices	0	3.45	us
$t_{SU:DAT}$	Data-set-up time	250	-	ns
t_r	Rise time of both SDA and SCL signals	-	1000	ns
t_f	Fall time of both SDA and SCL signals	-	300	ns
$t_{SU:STO}$	Set-up time for STOP condition	4.0	-	us
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	us
C_b	Capacitive load for each bus line	-	400	pF
V_{nL}	Noise margin at the LOW level for each connected device (including hysteresis)	$0.1V_{DD}$	-	V
V_{nH}	Noise margin at the HIGH level for each connected device (including hysteresis)	$0.2V_{DD}$	-	V

BUS INTERFACE

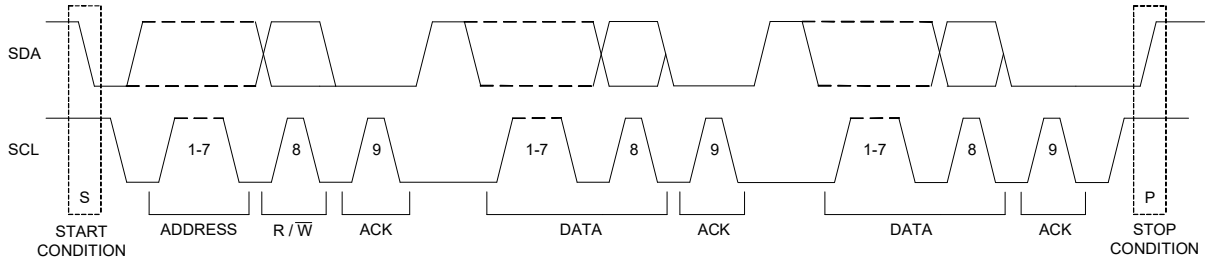
Data are transmitted to and from the MCU to the MS6821 via the SDA and SCL. The SDA and SCL make up the BUS interface. It should be noted that pull-up resistors must be connected to the positive supply voltage.



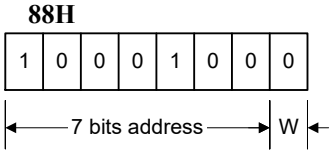
I²C interface protocol

The format consists of the following:

- A START condition
- A chip address byte including the chip address. (7bits)
- The 8th bit of the byte must be "0".(write=0, read=1)
- The chip must always acknowledge the end of each transmitted byte.
- A data sequence (N-bytes + Acknowledge)
- A STOP condition



I²C chip address



I²C data bytes description

MSB							LSB	Function
0	0	B2	B1	B0	A2	A1	A0	L-ch, Attenuation and Mute
0	1	B2	B1	B0	A2	A1	A0	R-ch, Attenuation and Mute
1	0	0	G2	G1	G0	S1	S0	L-ch, Input Gain and line Selection
1	0	1	G2	G1	G0	S1	S0	R-ch, Input Gain and line Selection
1	1	0	DAC PD	RPD	LPD	PDPR	CAP PD	Power Down Mode
1	1	1	S/B	MixL	MixR	AF1	AF0	Output mode (SE/BTL), Mixer control and Audio format

Where Ax = 1.25dB/step; Bx = 10dB/step; Gx = 3dB/step

Attenuation and Mute								
MSB							**LSB**	**Function**
0	0	**B2**	**B1**	**B0**	**A2**	**A1**	**A0**	L-ch, Attenuation and Mute
0	1							R-ch, Attenuation and Mute
					0	0	0	0 dB
					0	0	1	-1.25 dB
					0	1	0	-2.5 dB
					0	1	1	-3.75 dB
					1	0	0	-5 dB
					1	0	1	-6.25 dB
					1	1	0	-7.5 dB
					1	1	1	-8.75 dB
		0	0	0				0 dB
		0	0	1				-10 dB
		0	1	0				-20 dB
		0	1	1				-30 dB
		1	0	0				-40 dB
		1	0	1				-50 dB
		1	1	0				-60 dB
		1	1	1				-70 dB
		1	1	1	1	1	1	Mute

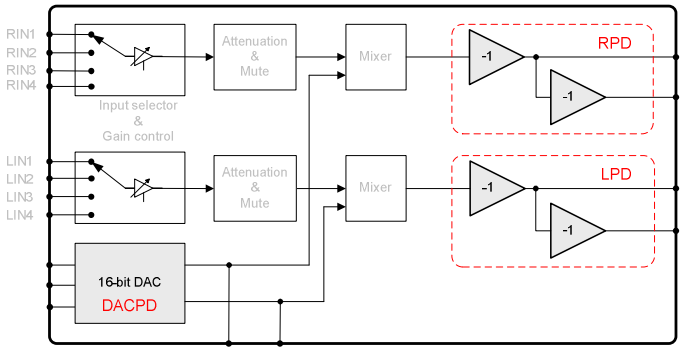
Initial state: Both L-ch and R-ch are mute-on.

Input Selector and Input Gain								
MSB							**LSB**	**Function**
1	0	0	**G2**	**G1**	**G0**	**S1**	**S0**	L-ch, Input Gain and line Selection
1	0	1						R-ch, Input Gain and line Selection
						0	0	Line 1 (L-ch or R-ch)
						0	1	Line 2 (L-ch or R-ch)
						1	0	Line 3 (L-ch or R-ch)
						1	1	Line 4 (L-ch or R-ch)
			0	0	0			0 dB
			0	0	1			3 dB
			0	1	0			6 dB
			0	1	1			9 dB
			1	0	0			12 dB
			1	0	1			15 dB
			1	1	0			18 dB
			1	1	1			21 dB

Initial state: L-ch1, R-ch1, Input gain is 0dB.

Power Down Mode								
MSB							**LSB**	**Function**
1	1	0	**DAC PD**	**RPD**	**LPD**	**PDPR**	**CAP PD**	Power mode selection and power management
			0					DAC is active mode
			1					DAC is power down mode
				0				R-ch PA output is active mode
				1				R-ch PA output is power down mode
					0			L-ch PA output is active mode
					1			L-ch PA output is power down mode
						0		Disable preparation for power off
						1		Enable preparation for power off
							0	Set the voltage of CAP to middle of supply voltage
							1	Pull down CAP pin to ground

Initial state: All are the power down modes.
Enable the power down preparation before the chip will be shut down.



Output mode (SE/BTL), Mixer control and Audio format								
MSB							**LSB**	**Function**
1	1	1	**S/B**	**MixL**	**MixR**	**AF1**	**AF0**	Output mode, mixer control and audio format
			0					Output mode is BTL
			1					Output mode is SE
				0				L-ch of input selector is the only signal
				1				Mix L-ch of input selector and L-ch of DAC
					0			R-ch of input selector is the only signal
					1			Mix R-ch of input selector and R-ch of DAC
						0	0	Right justified format
						1	0	Left justified format
						0	1	I^2S format
						1	1	

Initial state: Output mode is BTL mode, unmixed mode and Right justified format

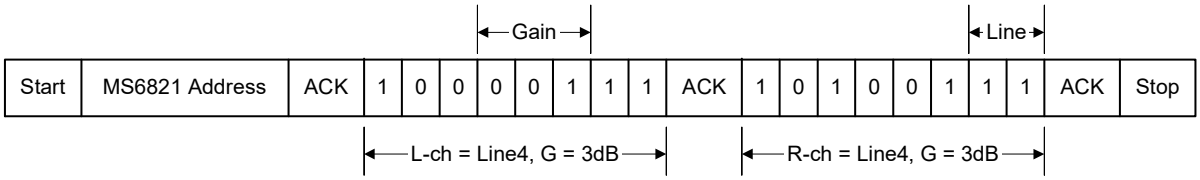
I^2C Initial code and status

MSB							**LSB**	**Function**	**Initial status**
0	0	**1**	**1**	**1**	**1**	**1**	**1**	L-ch, Attenuation and Mute	Mute On
0	1	**1**	**1**	**1**	**1**	**1**	**1**	R-ch, Attenuation and Mute	Mute On
1	0	0	**0**	**0**	**0**	**0**	**0**	L-ch, Input Gain and line Selection	Line1, 0dB
1	0	1	**0**	**0**	**0**	**0**	**0**	R-ch, Input Gain and line Selection	Line1, 0dB
1	1	0	**1**	**1**	**1**	**1**	**1**	Power Down Mode	All devices power down
1	1	1	**0**	**0**	**0**	**0**	**0**	Output mode (SE/BTL), Mixer control and Audio format	BTL, Unmixed, Right justified

I²C CODE EXAMPLE

Input selector and input gain

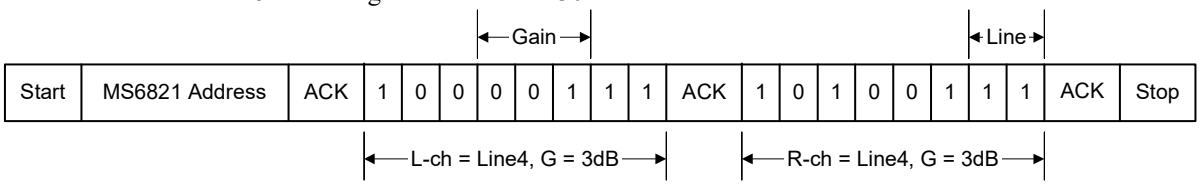
Set left channel to be line-4 and input gain to be 3dB. Set right channel to be line-4 and input gain to be 3dB.



The left and right input channel are independent.

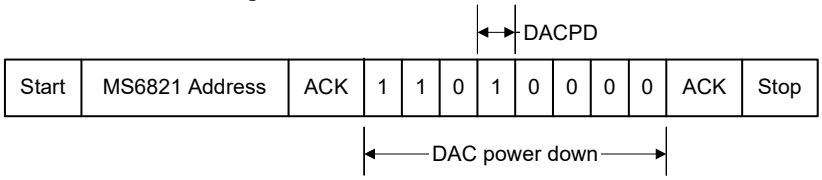
Volume control

Set left channel to be -15dB and right channel to be 30dB.



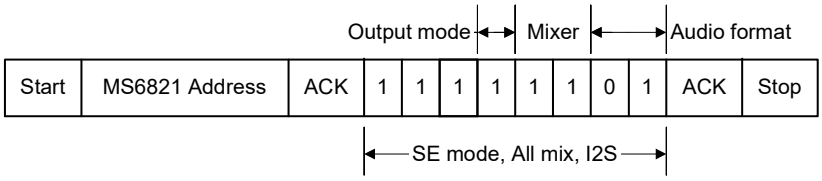
Power down mode

Set built-in DAC to be power down mode.



Output mode, mixer control and audio format

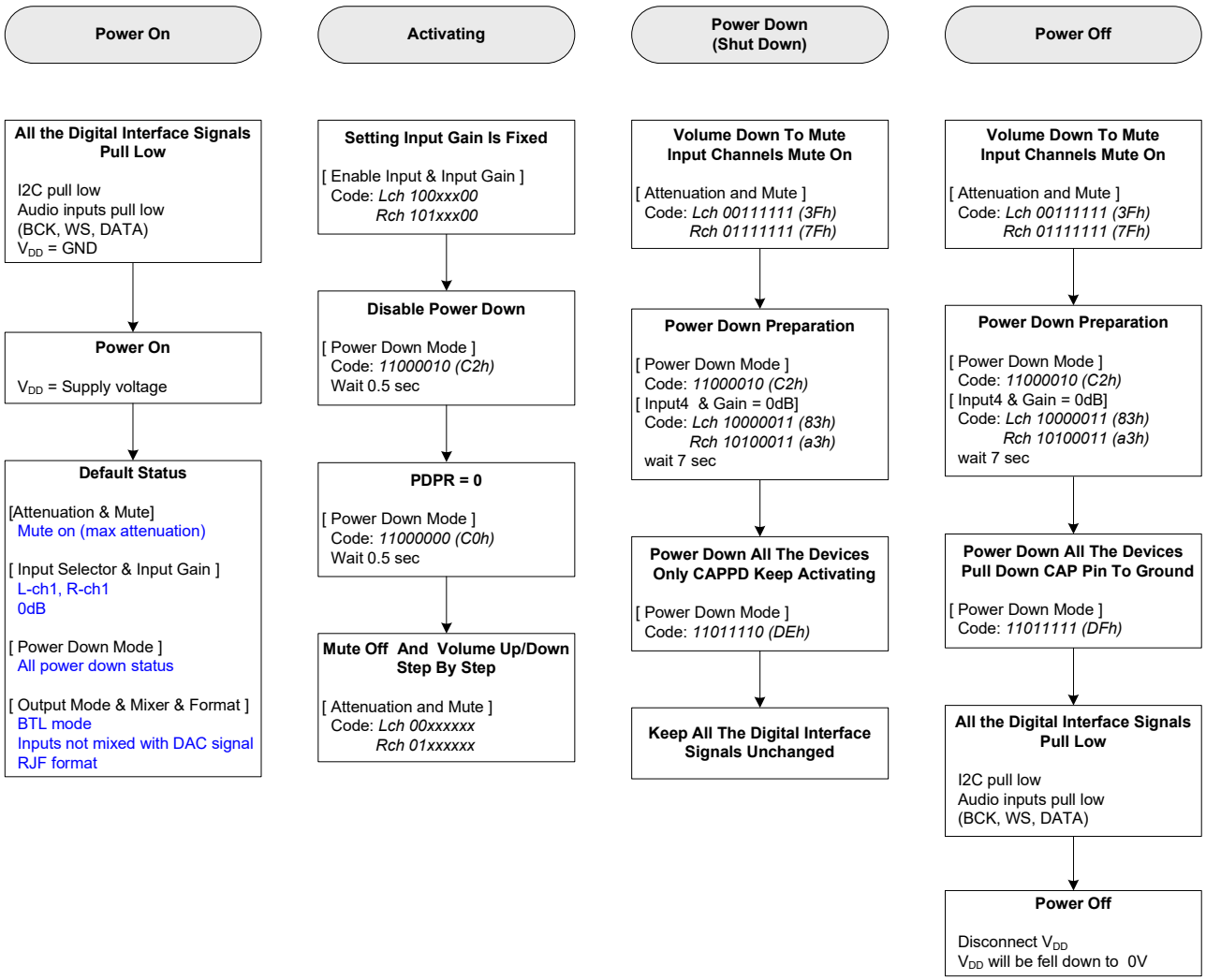
Set output mode to be SE mode, audio format is I2S, and both input channel to be mixed.



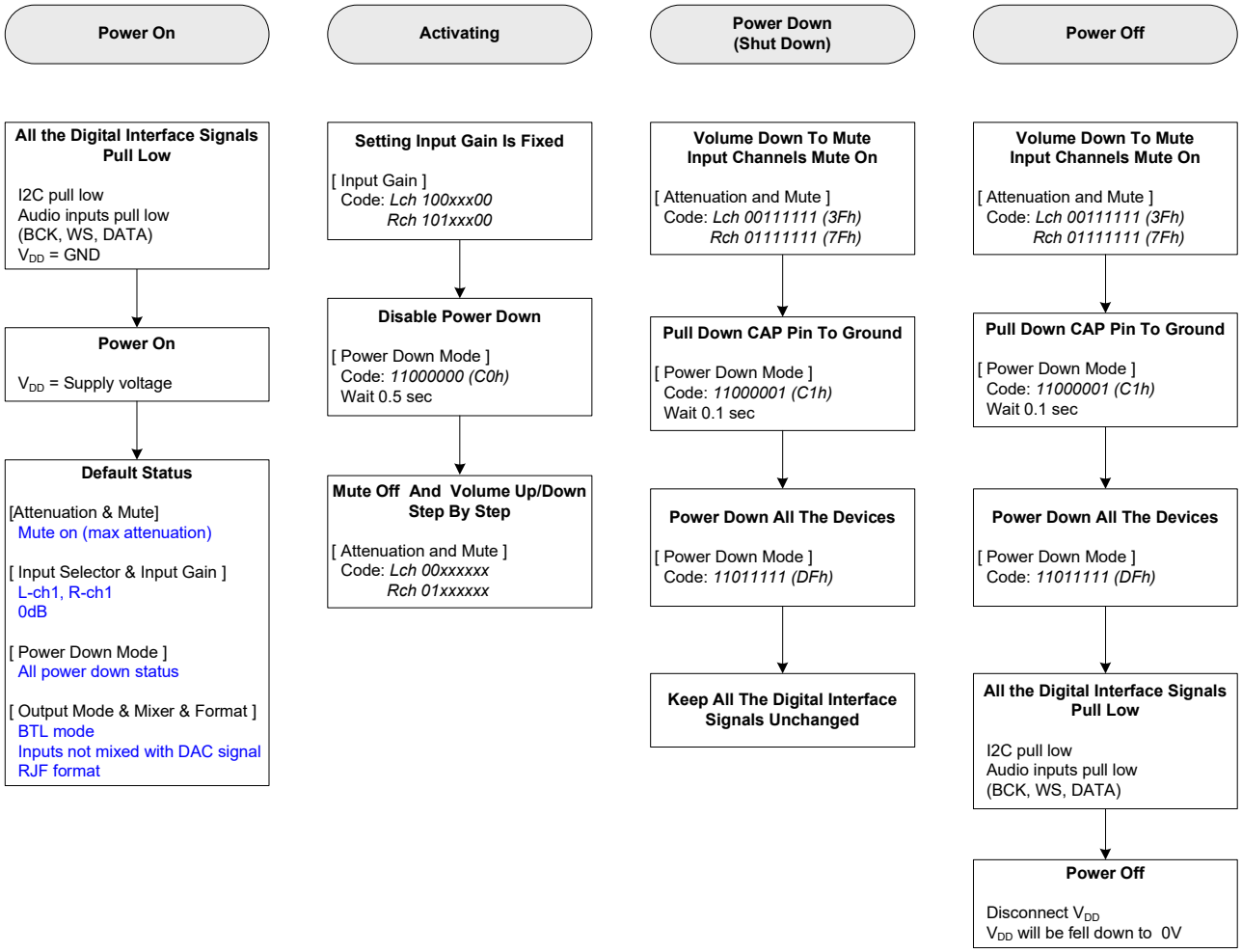
OPERATION PROCEDURE

The sequence of operation: power on→ activating → power down → activating → power off. The basic flowcharts are as follows:

For HP mode and HP/BTL mode

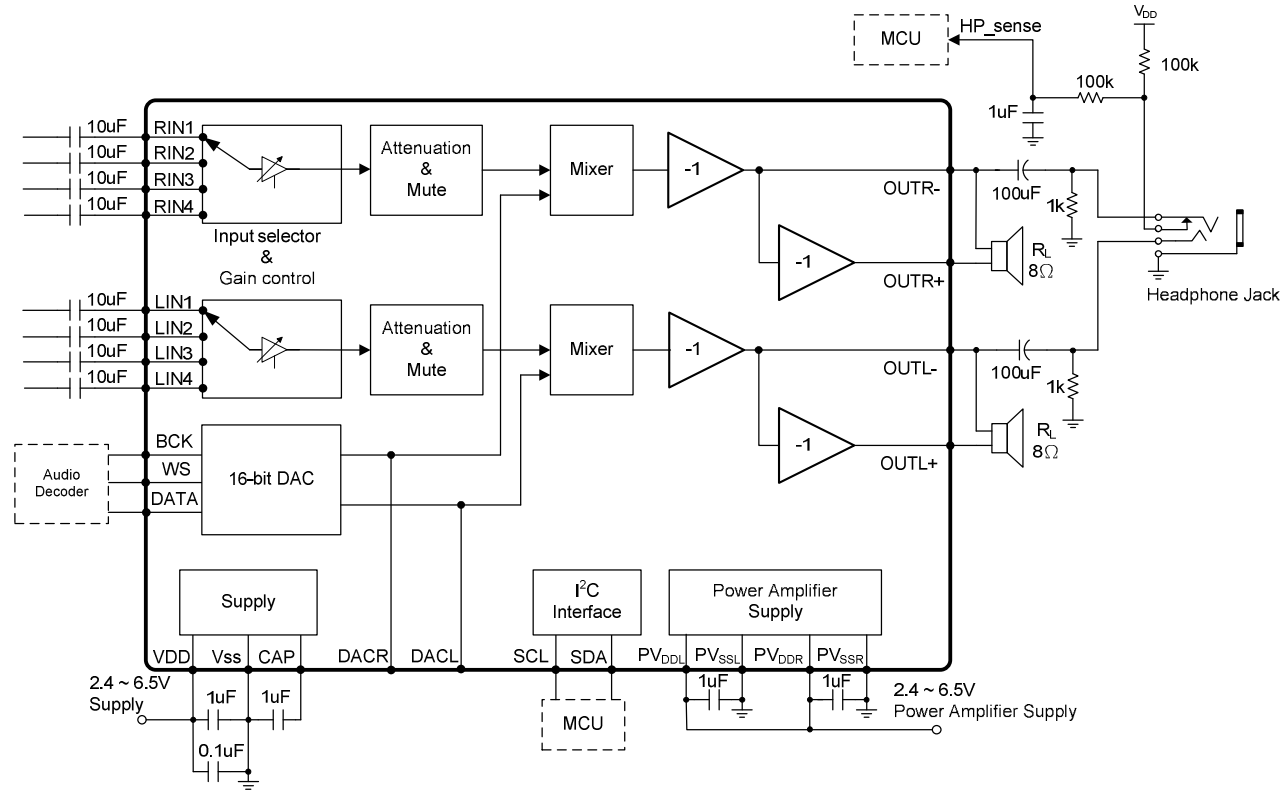


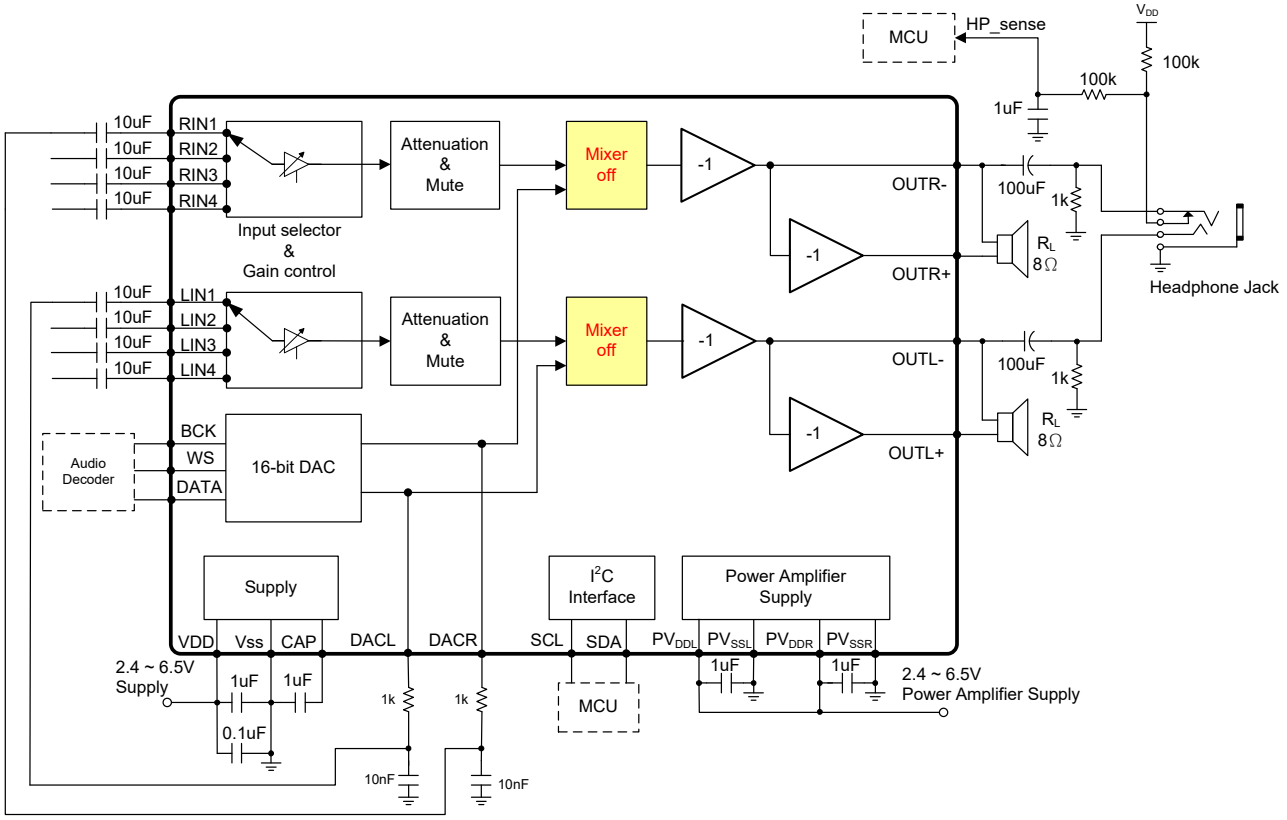
For BTL mode only



APPLICATION INFORMATION

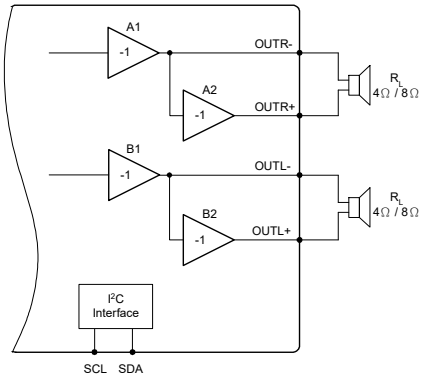
A base application circuit



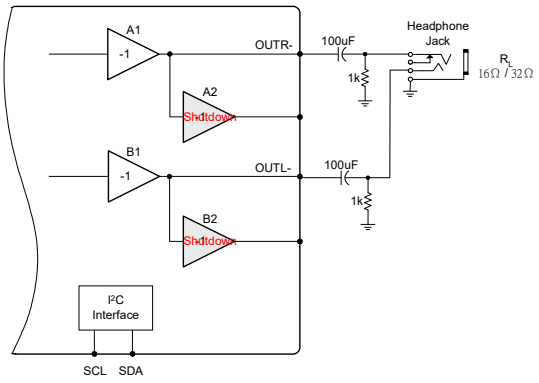


Output mode operation -- SE mode and BTL mode

The output mode has two modes, SE mode and BTL mode. The mode is selected by I2C code via a MCU.
In BTL mode, the outputs of A1(B1) and A2(B2) are then used to drive the bridged-tied load

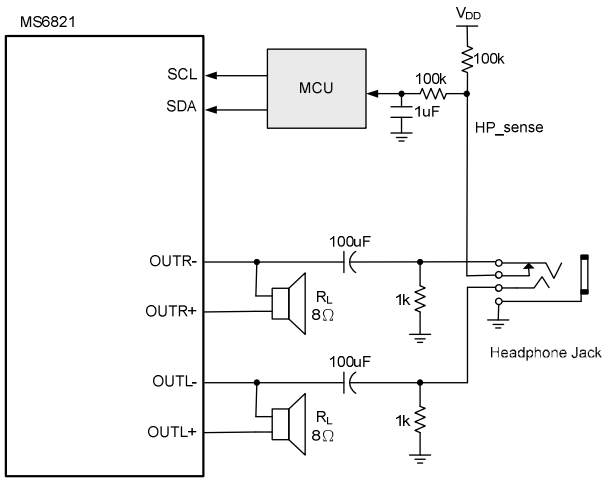


In the SE mode, the amplifiers A2 and B2 are shutdown, and then the amplifiers will be a high output impedance state.



Headphone sense

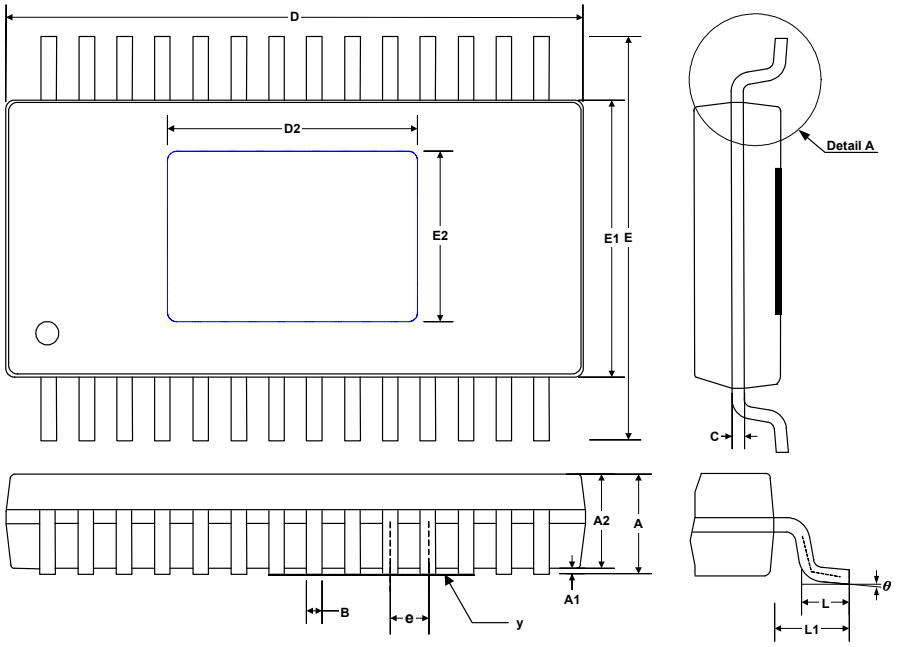
The output mode is SE or BTL that is decided by a headphone. It has to be set SE mode when a headphone is plug-in status. The output mode is selected by I2C command code by a MCU. Please note that the MS6821 don't detect a headphone automatically. Thus a detect function is executed via a MCU. An operation diagram is as follows:



The HP_sense pin is high when a headphone is plug-in.
The HP_sense pin is low when a headphone is not plug-in.

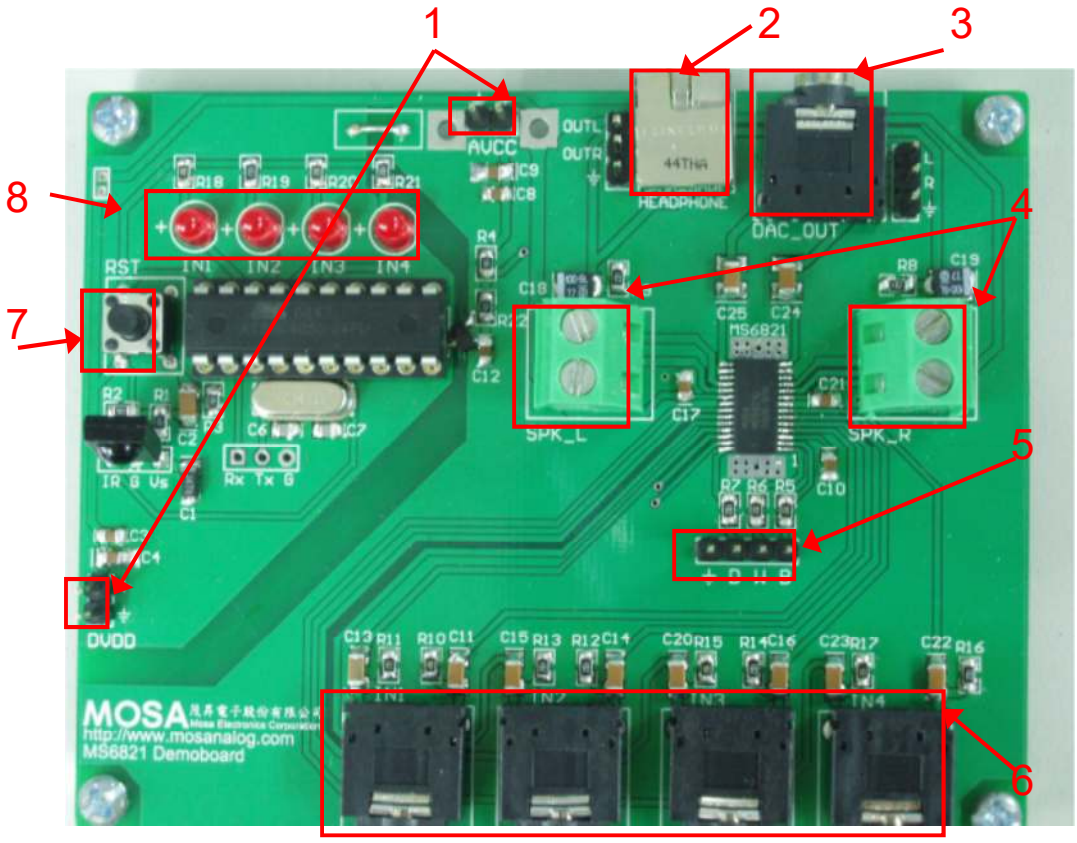
EXTERNAL DIMENSIONS

TSSOP28 (Thermal Pad)



Symbol	Dimension in mm			Dimension in inches		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.15	-	-	0.045
A1	0.00	-	0.10	0.000	-	0.004
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	-	0.30	0.007	-	0.012
C	0.09	-	0.20	0.004	-	0.008
D	9.60	9.70	9.80	0.378	0.382	0.386
D2	3.70	3.80	3.90	0.146	0.150	0.154
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
E2	2.70	2.80	2.90	0.106	0.110	0.114
e	-	0.65	-	-	0.026	-
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	0.90	1.00	1.10	0.035	0.039	0.043
θ	0°	-	8°	0°	-	8°
y	-	-	0.10	-	-	0.004

DEMO BOARD



Function description

Label 1: Supply Input
Supply voltage range is 2.4V to 6.5V.

Label 2: Headphone Jack
Used 3.5mm diameter of headphone with 32ohm

Label 3: DAC output
Connected to a post-power-amplifier, as active speaker.
In addition, using volume control for DAC, this output can connected to input section (label 6) as feedback.

Label 4: Speaker Output
Connected to speaker with 8ohm or 4 ohm

Label 5: Digital Signal Input
Connected to digital audio formats as I2S, Right Justified and Left Justified.

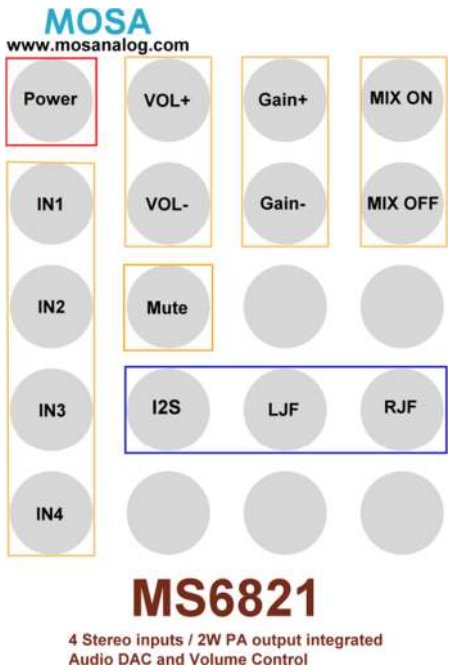
Label 6: Signal Input
There are four stereo inputs in the section. Please input stereo audio signal, as music or sine wave.

Label 7: Reset
All I/O pins are reset to default values.

Label 8: LED Indicator
The LEDs indicate the chip status and IR received status. It keeps on a light state when the MS6821 is active. The other hand, keeps on a dark state when the MS6821 is power-off. It is red-dark blink once when the MCU has received the function code correctly.

SE mode and BTL mode operation
The headphone controls operational mode. System enters SE mode when headphone jack is empty. When a set of headphone plugged into the jack, the system switched to BTL mode.

IR Controller



Power ON/OFF : The power key.
Press the key once to set power-on or power-off for MS6821.

IN1~IN4 : Analog input channel.
Press the key once to select input channel.
The default state is IN1.

VOL+, VOL- : The volume control keys.
The volume control in 1.25dB/step as the switch is pressed once, the range is –77.5dB to 0dB.
The default value is -20dB.

Gain+, Gain- : The gain control keys.
The gain control in 3dB/step as the switch is pressed once, the range is 0dB to 21dB.
The initial value is 0dB.

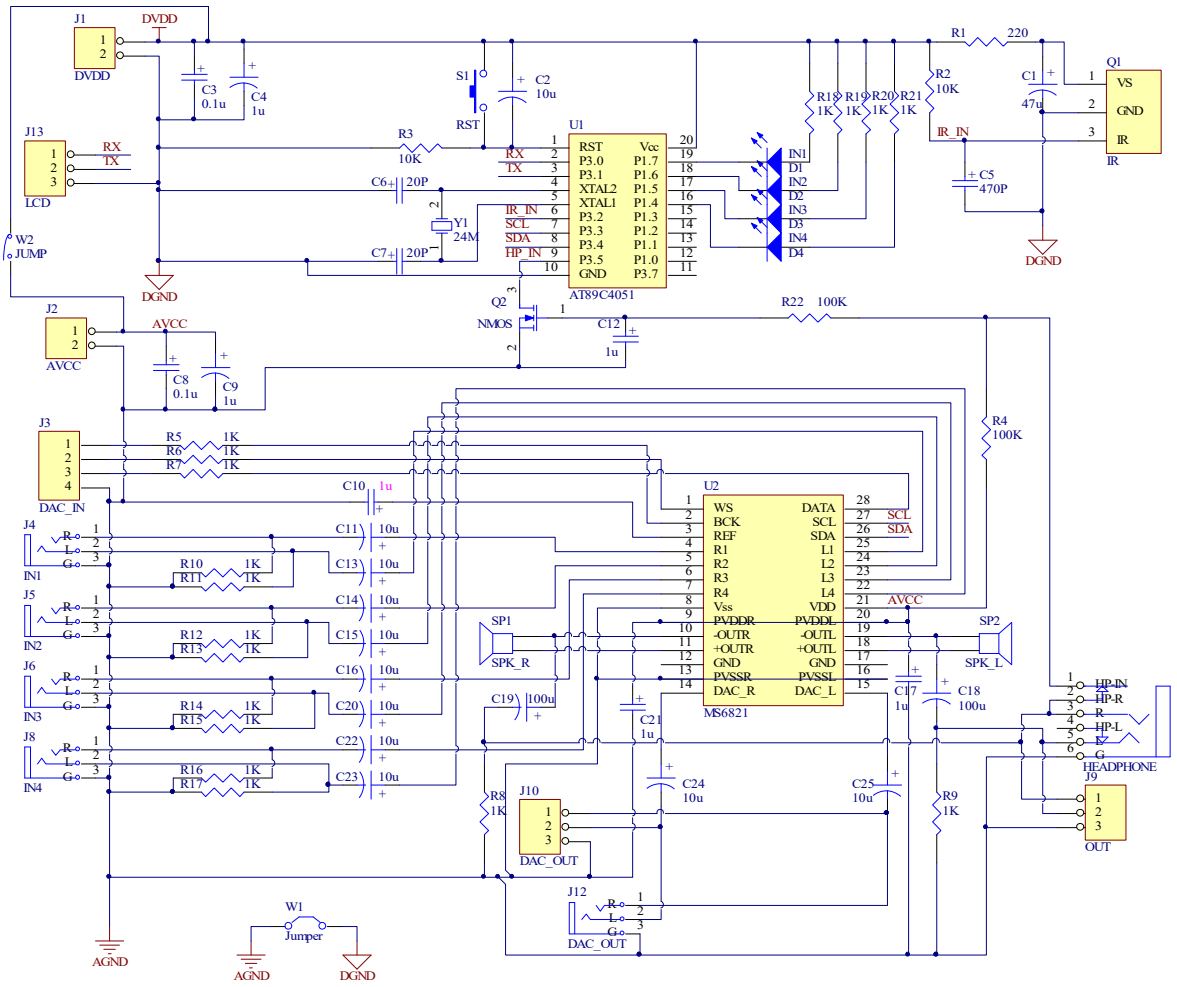
Mute : The mute key
Press the key once to set mute-on or mute-off.
The default state is mute-off.

PD/Active : The power down key.
Press the key once to set power-down or activation for MS6821.

Mix_LR ON/OFF : The mixing DAC signal keys.
Mix_L ON, mixed the left channel of DAC with the left channel of input signal.
Mix_R OFF, unmixed the right channel of DAC with the right channel of input signal.

I2S, LJF, RJF: The digital input format keys.
There are three formats can be selected that is I2S, Left justified and Right justified.

Circuit


J1
DVDD
C3
0.1u
C4
1u
S1
RST
C2
10u
R1
220
R2
10K
C1
47u
Q1
VS
GND
IR
IR_IN
C5
470P
R18 R19 R20 R21
1K
J13
RX
TX
LCD
R3
10K
C6 20P
C7 20P
Y1
24M
U1
RST
P3.0
P3.1
XTAL2
XTAL1
P3.2
P3.3
P3.4
P3.5
GND
Vcc
P1.7
P1.6
P1.5
P1.4
P1.3
P1.2
P1.1
P1.0
P3.7
AT89C4051
IN1
IN2
IN3
IN4
D1
D2
D3
D4
W2
JUMP
DGND
J2
AVCC
C8
0.1u
C9
1u
Q2
NMOS
C12
1u
R22 100K
R4
100K
J3
DAC_IN
R5 R6 R7
1K
C10 1u
J4
IN1
J5
IN2
J6
IN3
J8
IN4
R10 R11
R12 R13
R14 R15
R16 R17
C11 C13 C14 C15 C16 C20 C22 C23
10u
U2
WS
BCK
REF
R1
R2
R3
R4
Vss
PVDDR
-OUTR
+OUTR
GND
DAC_R
DATA
SCL
SDA
L1
L2
L3
L4
VDD
PVDDL
-OUTL
+OUTL
GND
PVSSL
DAC_L
MS6821
SP1
SPK_R
SP2
SPK_L
C19 100u
C21 1u
C17 1u
C18 100u
C24 10u
C25 10u
R8 1K
R9 1K
J10
DAC_OUT
J12
DAC_OUT
J9
OUT
HP-IN
HP-R
HP-L
HEADPHONE
W1
Jumper
AGND
DGND