Integrates CVBS And FHD Filter Driver

-----MS7372/MS7372M

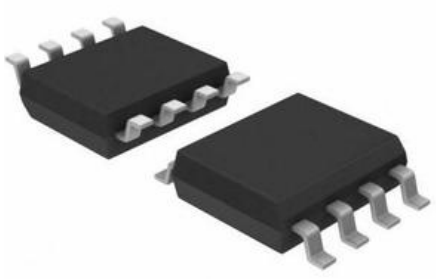
PRODUCT DESCRIPTION

The MS7372/MS7372M is a video buffer which integrated single CVBS channel and single FHD channel video amplifier .The video amplifiers integrated single 6dB Gain rail-to-rail output driver and 3rd output reconstruction filter. Operating from single supplies ranging from +2.7V to +5V and sinking an ultra-low 28.5mA quiescent current, the MS7372/MS7372M is ideally suited for battery powered applications.

The MS7372/MS7372M features two low-power shutdown pin that is activated by driving DIS_FHD/DIS_CVBS low. The MS7372 has lead SOP-8 package, the MS7372M has lead MSOP-8 package, and ESD (HBM) reaches 8KV.

FEATURES

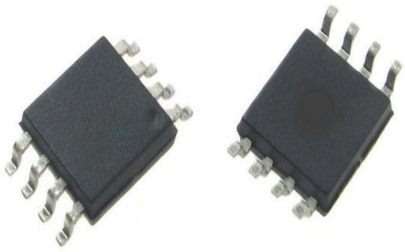
- Sixth-order 72MHz (FHD) Filter
- Sixth-order 10MHz (CVBS) Filter
- Transparent input clamping
- 6dB output driver Gain and drive dual video load
- Rail-to-Rail Output
- Input Voltage Range Includes Ground
- AC or DC Coupled Inputs
- AC or DC Coupled Outputs
- Operates from 2.7V to 5V Single power supply
- Low Power 28.5mA Supply Current
- Lead SOP-8/MSOP-8 package



SOP-8

APPLICATIONS

- Video On Demand (VOD)
- Communications device
- Portable and handheld product
- PVR/DVDR Output Buffering



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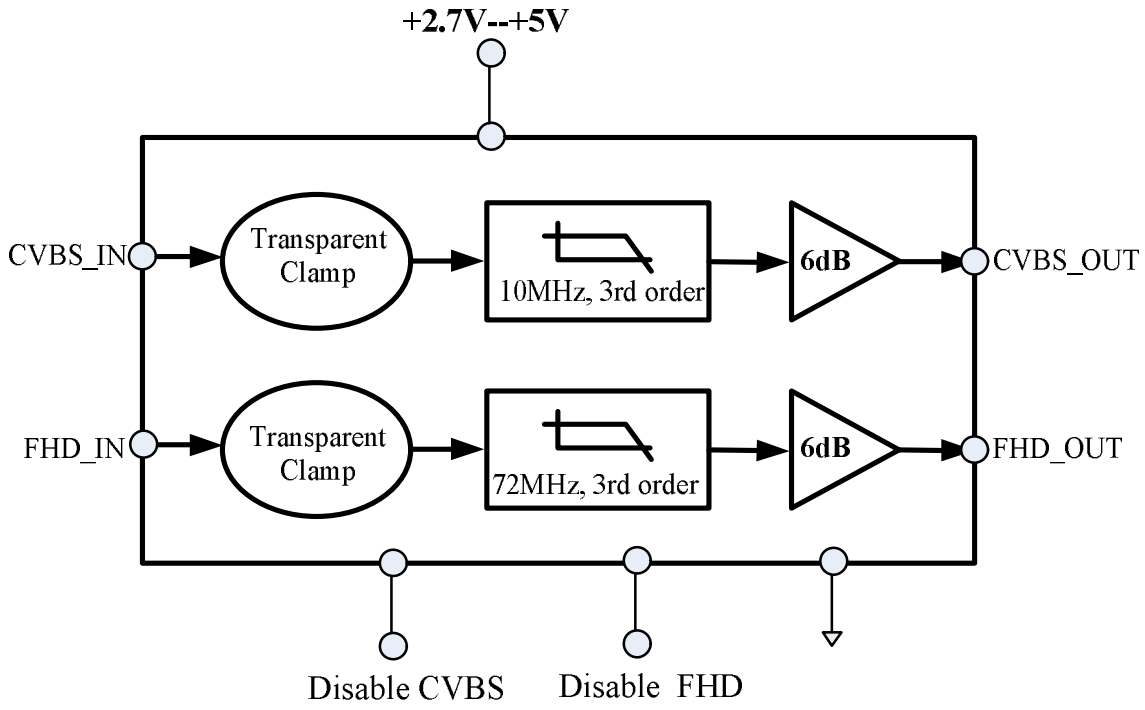
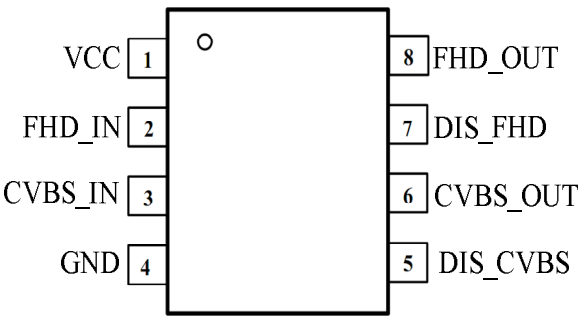
BLOCK DIAGRAM



PIN CONFIGURATIONS

MS7372/MS7372M



SOP-8/MSOP-8

Pin Description

Pin	Name	Function
1	VCC	Power supply
2	FHD_IN	FHD video input
3	CVBS_IN	CVBS input
4	GND	Ground
5	DIS_CVBS	CVBS Shutdown Mode (active low)
6	CVBS_OUT	Ground
7	DIS_FHD	FHD Shutdown Mode (active low)
8	FHD_OUT	FHD output

PACKAGE/ORDERING INFORMATION

Part Number	Package	Marking
MS7372	SOP-8	MS7372
MS7372M	MSOP-8	MS7372M

ELECTRICAL CHARACTERISTICS

(At RL = 150Ω connected to GND, Vin=1Vpp， and CIN = 0.1μF, all outputs AC coupled with 220μF， unless otherwise noted).

PARAMETER	CONDITION	TYP	MIN	MAX	UNITS
DYNAMIC PERFORMANCE：SD(CVBS) channel					
±0.1dB Bandwidth	Rl=150Ω	3.4			MHz
-3dB Bandwidth	Rl=150Ω	10			MHz
Gain		6			dB
Slew Rate	Vin=1V step，20%--80%	40			V/us
Differential Gain (DG)	NTSC & PAL DC NTSC & PAL AC	0.02 0.3			% %
Differential Phase (DP)	NTSC & PAL DC NTSC & PAL AC	0.02 0.36			
Group Delay Variation (D/DT)	f = 400KHz, 26.5MHz	1.2			ns
Crosstalk (channel to channel)	at 1MHz	-64			dB
Rise Time	2.0V step，80%--20%	30			ns
Fall Time	2.0V step，80%--20%	30.5			ns
DYNAMIC PERFORMANCE：FHD channel					
±0.1dB Bandwidth	Rl=150Ω	17			MHz
-3dB Bandwidth	Rl=150Ω	72			MHz
Gain		6			dB
Slew Rate	Vin=1V step，20%--80%	270			V/us
Differential Gain (DG)	NTSC & PAL DC NTSC & PAL AC	0.02 0.3			% %
Differential Phase (DP)	NTSC & PAL DC NTSC & PAL AC	0.02 0.36			
Group Delay Variation (D/DT)	f = 400KHz, 26.5MHz	1.2			ns
Crosstalk (channel to channel)	at 1MHz	-64			dB
Rise Time	2.0V step，80%--20%	4.5			ns

Fall Time	2.0V step，80%--20%	5.5			ns
INPUT CHARACTERISTICS					
Output Level Shift Voltage (VOLS)	Vin=0V， CVBS channel	235	230	370	mv
	Vin=0V， FHD channel	235	230	370	mv
Input Bias Current (Ib)					pA
Input Voltage Clamp (VCLAMP)	Iin= -1mA	-4.5	-4	-22	mV
Clamp Charge Current	Vin=Vclp-100mV	-5		-7.2	mA
Voltage Gain（Av）	RL=150	2	1.90	2.1	V/V
OUTPUT CHARACTERISTICS					
Output Voltage High Swing	Vin=3V，RL=150Ω	4.5	4.2	4.5	V
Output Short-Circuit Current (ISC)	Vin=0.1V, out short to VDD through 10Ω	103		115	mA
POWER SUPPLY					
Operating Voltage Range			2.7	5.5	V
Quiescent Current	no load	11			mA
Operating Current	Vin=0V，double channel operating	30			mA
	Vin=0V，CVBS channel operating	14.5			mA
	Vin=0V，FHD channel operating	14.5			mA

CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PARAMETER	MAXIMUM
Supply Voltage, V+ to V-	7.5V
Input Voltage	GND-0.3V to (+VS)+0.3V
Storage Temperature Range	-65℃ to +150℃
Junction Temperature	160℃
Operating Temperature Range	-40℃ to +125℃
Power Dissipation, PD @ TA = 25℃	0.8W
Package Thermal Resistance，θJA	128℃/W
Lead Temperature Range (Soldering 10 sec)	260℃
ESD Susceptibility：	
HBM	8000V
MM	400V

APPLICATIONS INFORMATION

Functional Description

MS7372/MS7372M operates from a single +2.7V to +5V supply. In application, MS7372/MS7372M is a fully integrated solution for filtering and buffering HDTV signals and CVBS signals in front of video decoder or behind video encoder. MS7372/MS7372M's solution can help you save PCB size and production cost, it also improves video signal performance comparing with traditional design using discrete components. MS7372/MS7372M features a DC-coupled input buffer, 3-pole low-pass filter to eliminate out-of-band noise of video encoder, and a gain of +6dB in the output amplifier to drive 75Ω load. The AC or DC-coupled input buffer eliminates sync crush, droop, and field tilt. The output of MS7372/MS7372M also can be DC-coupled or AC-coupled.

Shutdown Mode

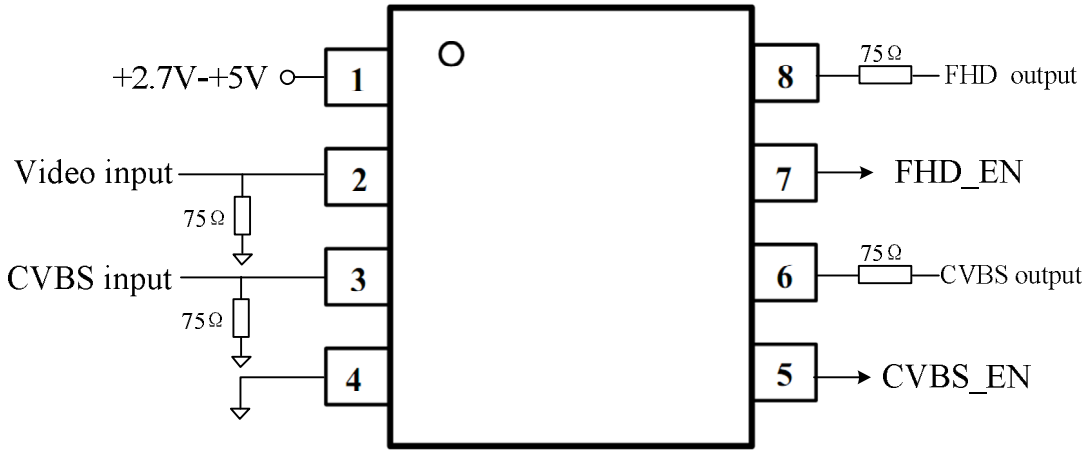
The MS7372/MS7372M features low-power shutdown pin that is activated by driving DIS_CVBS or DIS_FHD low. In shutdown mode, the output is in a high impedance state, supply current is reduced. Driving DIS_CVBS low will turn the CVBS channel shutdown, driving DIS_FHD low will turn the FHD channel shutdown. When The DIS_CVBS/DIS_FHD pin left unconnected, the DIS_CVBS/DIS_FHD input will be at high voltage.

Power-Supply Bypassing and Layout

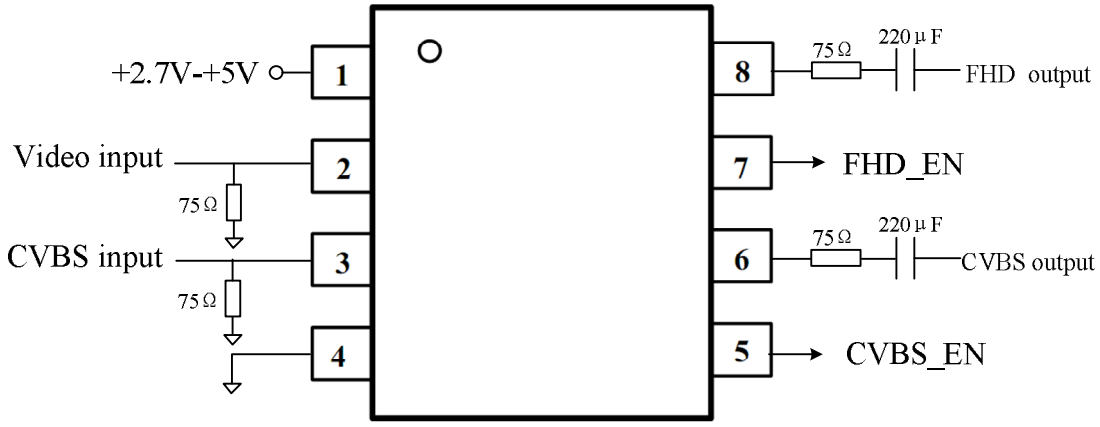
Correct power supply bypassing is very important for optimizing video performance in design. One 0.1μF and one 10μF capacitors are always used to Bypass VCC pin of MS7372/MS7372M, please place these two capacitors as close to the MS7372/MS7372M output pin as possible, a large ground plane is also needed to ensure optimum performance. The input and output termination resistors should be placed as close to the related pin of MS7372/MS7372M as possible to avoid performance degradation. The PCB traces at the output side should have 75Ω characteristic impedance in order to match the 75Ω characteristic impedance cable connecting external load. In design, please keep the board trace at the inputs and outputs of the MS7372/MS7372M as short as possible to minimize the parasitic stray capacitance and noise pickup.

Typical Application Diagram

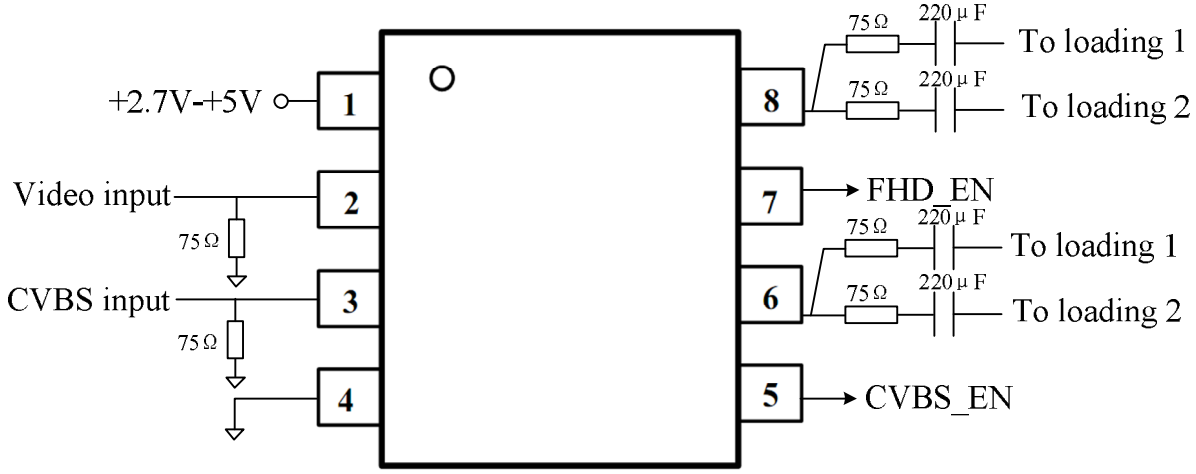
The following schematic is normally used.



DC Coupling Application Schematic



Input DC Coupling and Output AC Coupling Application Schematic



The DC Coupling Circuit Schematic is recommended in applications of STB

PACKAGE OUTLINE DIMENSIONS

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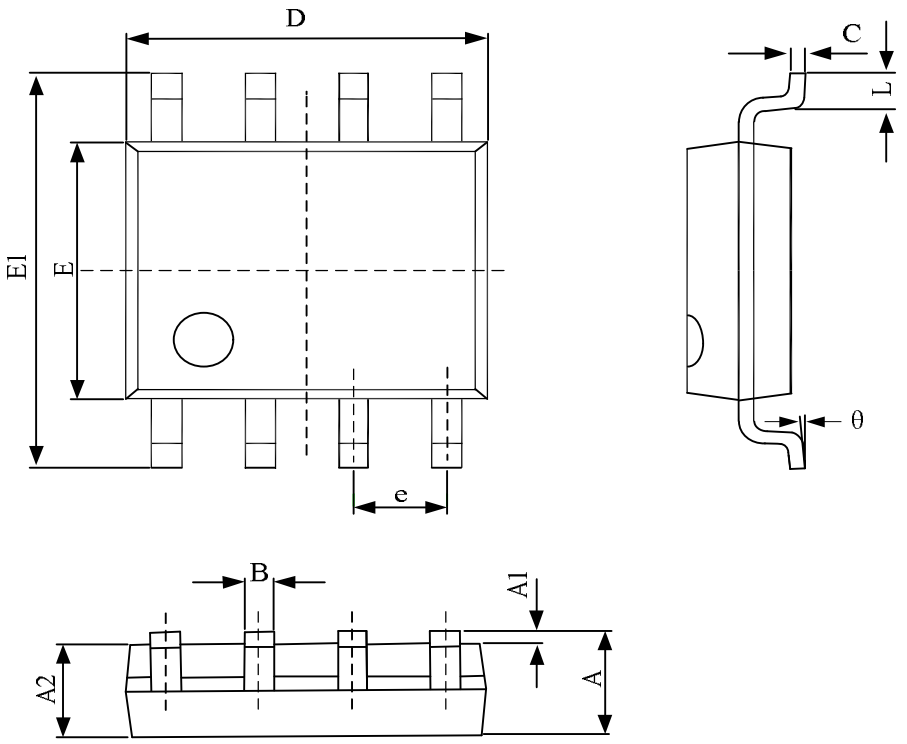

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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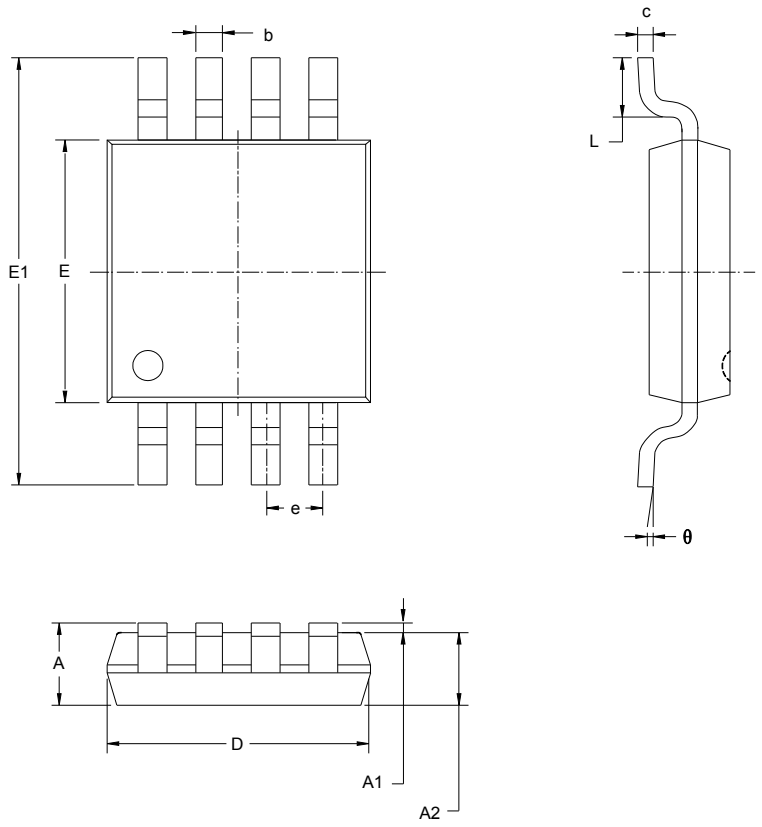

Symbol	Dimensions In Millimeters		Dimensions in Inches	
	MIN	MAX	MIN	MAX
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
e	0.650BSC		0.026BSC	
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°