FEDS8104160A-01
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OKI Semiconductor

MS8104160A

Dual FIFO (262,214 Words × 8 Bits) × 2

GENERAL DESCRIPTION

The MS8104160A is a single-chip 4Mb FIFO functionally composed of two OKI 2Mb FIFO (First-In First-Out) memories which were designed for 262,214 x 8-bit high-speed asynchronous read/write operation.
The read clocks and the write clocks of each of the 2Mb FIFO memories are connected in common. The MS8104160A, functionally compatible with Oki's 2Mb FIFO memory (MSM518222A), can be used as a x16 configuration FIFO.

The MS8104160A is a field memory for wide or low end use in general commodity TVs and VTRs exclusively and is not designed for high end use in professional graphics systems, which require long term picture storage, data storage, medical use and other storage systems.

The MS8104160A provides independent control clocks to support asynchronous read and write operations. Different clock rates are also supported, which allow alternate data rates between write and read data streams.

The MS8104160A provides high speed FIFO (First-in First-out) operation without external refreshing: MS8104160A refreshes its DRAM storage cells automatically, so that it appears fully static to the users.

Moreover, fully static type memory cells and decoders for serial access enable the refresh free serial access operation, so that serial read and/or write control clock can be halted high or low for any duration as long as the power is on. Internal conflicts of memory access and refreshing operations are prevented by special arbitration logic.

The MS8104160A's function is simple, and similar to a digital delay device whose delay-bit- length is easily set by reset timing. The delay length and the number of read delay clocks between write and read, is determined by externally controlled write and read reset timings.

Additional SRAM serial registers, or line buffers for the initial access of 71 x 16-bit enable high speed first-bit-access with no clock delay just after the write or read reset timings.

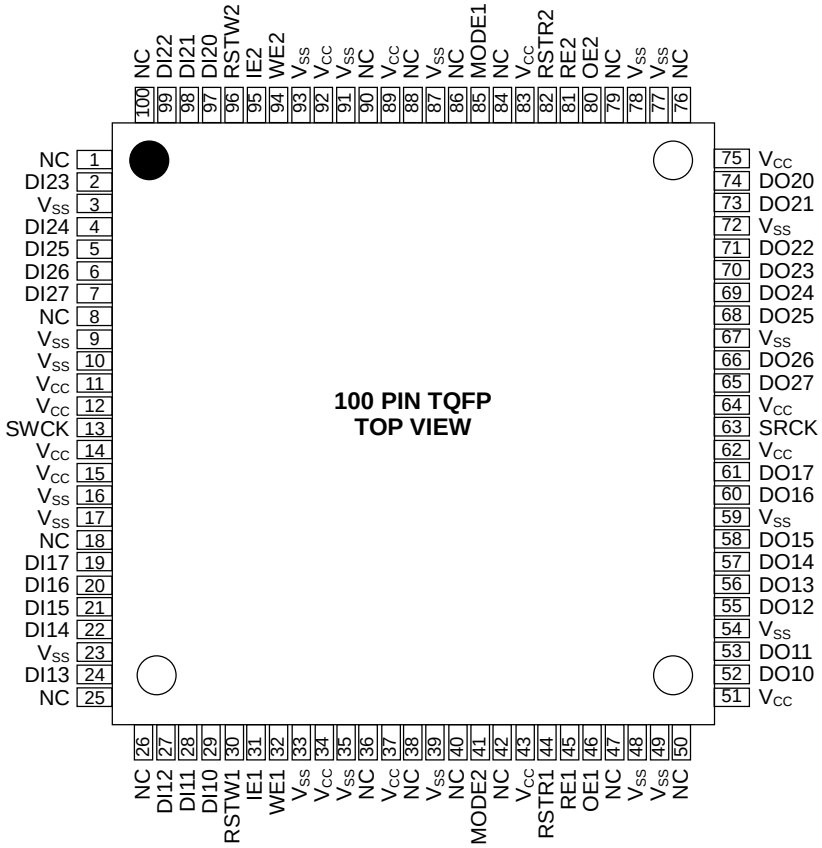
Additionally, the MS8104160A has a write mask function or input enable function (IE), and read- data skipping function or output enable function (OE). The differences between write enable (WE) and input enable (IE), and between read enable (RE) and output enable (OE) are that WE and RE can stop serial write/read address increments, but IE and OE cannot stop the increment, when write/read clocking is continuously applied to MS8104160A. The input enable (IE) function allows the user to write into selected locations of the memory only, leaving the rest of the memory contents unchanged. This facilitates data processing to display a "picture in picture" on a TV screen.

FEATURES

- 262,214 words × 8 bits × 2
- Fast FIFO (First-In First-Out) Operation: 25 ns cycle time
- Self refresh (No refresh control is required)
- High speed asynchronous serial access
  Read/Write Cycle Time 20 ns/25 ns
  Access Time 18 ns/22 ns
- Variable length delay bit (150 to 262214)
- Write mask function (Output enable control)
- Cascading capability by mode setting
- Single power supply: 5.0 V ± 0.5V
- Package:
  100-Pin plastic TQFP (TQFP 100-P-1414-0.50-k) (Product: MS8104160A-xxTB)
  xx indicates speed rank.

Parameter	Symbol	MS8104160A-xxTB	
		–20	–25
Access Time	t_{AC}	18 ns	22 ns
Read/Write Cycle Time	t_{SWC} t_{SRC}	20 ns	25 ns
Operation current	I_{CC1}	170 mA	170 mA
Standby current	I_{CC2}	5 mA	5 mA

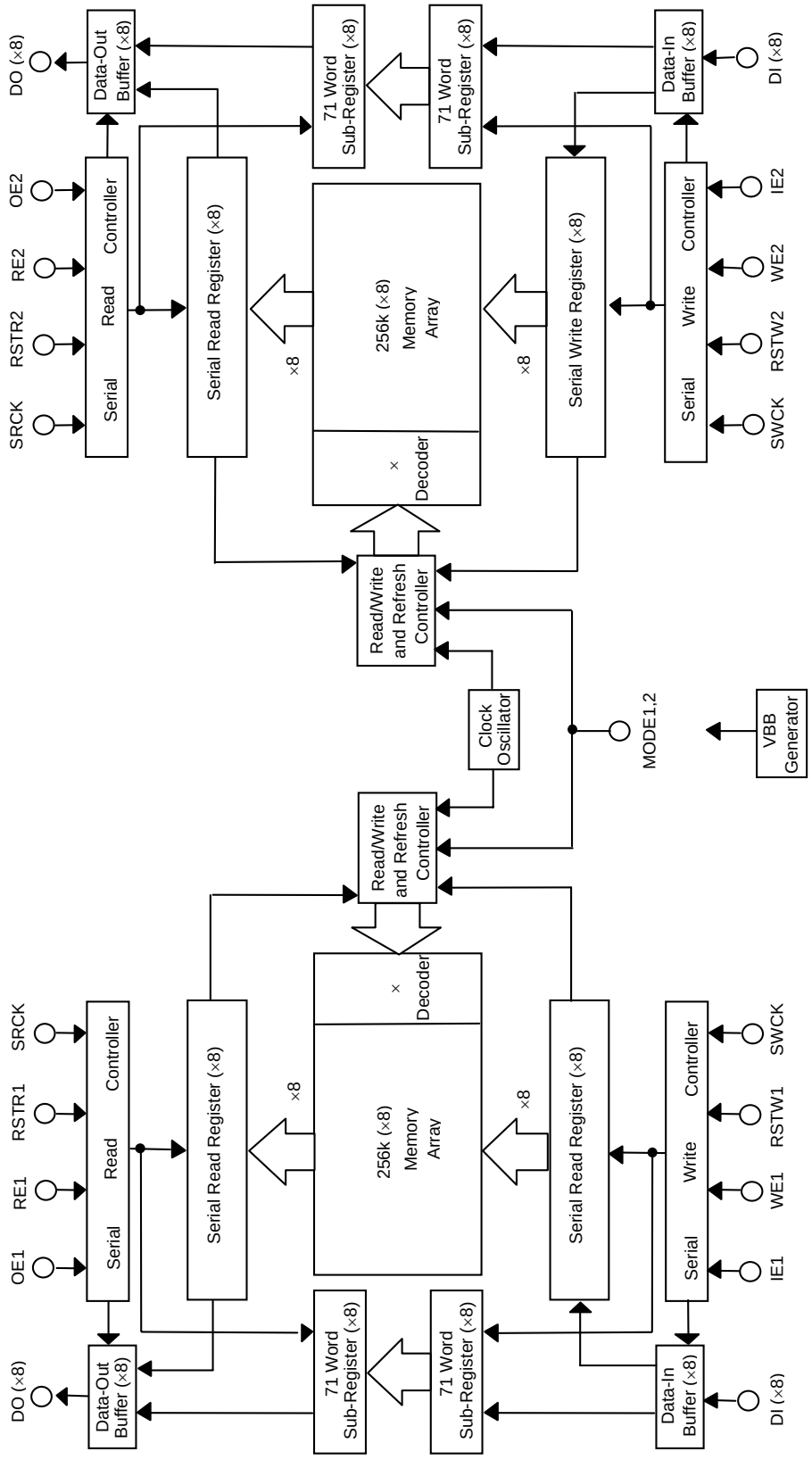
PIN CONFIGURATION (TOP VIEW)



Pin Name	Function	Pin Name	Function
SWCK	Serial Write clock	SRCK	Serial Read Clock
WE1	Port1 Write Enable	WE2	Port2 Write Enable
RE1	Port1 Read Enable	RE2	Port2 Read Enable
IE1	Port1 Input Enable	IE2	Port2 Input Enable
OE1	Port1 Output Enable	OE2	Port2 Output Enable
RSTW1	Port1 Reset Write	RSTW2	Port2 Reset Write
RSTR1	Port1 Reset Read	RSTR2	Port2 Reset Read
DI10 to 17	Port1 Data Input	DI20 to 27	Port2 Data Input
DO10 to 17	Port1 Data Output	DO20 to 27	Port2 Data Output
MODE1,2	Mode Input	NC	No Connection
V_{CC}	Power Supply (5.0 V)	V_{SS}	Ground (0 V)

Note: The same power supply voltage must be provided to every V_{CC} pin, and the same GND voltage level must be provided to every V_{SS} pin.

BLOCK DIAGRAM



PIN DESCRIPTION

Data Inputs: (DIN10 to 17)
These pins are used for serial data inputs.

Write Reset: RSTW1
The first positive transition of SWCK after RSTW becomes high resets the write address pointers to zero. RSTW1 setup and hold times are referenced to the rising edge of SWCK. Because the write reset function is solely controlled by the SWCK rising edge after the high level of RSTW1, the states of WE1 and IE1 are ignored in the write reset cycle. Before RSTW1 may be brought high again for a further reset operation, it must be low for at least two SWCK cycles.

Write Enable: WE1
WE1 is used for data write enable/disable control. WE1 high level enables the input, and WE1 low level disables the input and holds the internal write address pointer. There are no WE1 disable time (low) and WE1 enable time (high) restrictions, because the MS8104160A is in fully static operation as long as the power is on. Note that WE1 setup and hold times are referenced to the rising edge of SWCK.

Input Enable: IE1
IE1 is used to enable/disable writing into memory. IE1 high level enables writing. The internal write address pointer is always incremented by cycling SWCK regardless of the IE1 level. Note that IE1 setup and hold times are referenced to the rising edge of SWCK.

Data Out: (DOUT0 to 11)
These pins are used for serial data outputs.

Read Reset: RSTR1
The first positive transition of SRCK after RSTR1 becomes high resets the read address pointers to zero. RSTR1 setup and hold times are referenced to the rising edge of SRCK. Because the read reset function is solely controlled by the SRCK rising edge after the high level of RSTR, the states of RE1 and OE1 are ignored in the read reset cycle. Before RSTR may be brought high again for a further reset operation, it must be low for at least *two SRCK cycles.

Read Enable: RE1
The function of RE1 is to gate of the SRCK clock for incrementing the read pointer. When RE1 is high before the rising edge of SRCK, the read pointer is incremented. When RE1 is low, the read pointer is not incremented. RE1 setup times (t_{RENS} and t_{RDSS}) and RE1 hold times (t_{RENH} and t_{RDSH}) are referenced to the rising edge of the SRCK clock.

Output Enable: OE1
OE1 is used to enable/disable the outputs. OE1 high level enables the outputs. The internal read address pointer is always incremented by cycling SRCK regardless of the OE1 level. Note that OE1 setup and hold times are referenced to the rising edge of SRCK.

Serial Write: Clock SWCK
The SWCK latches the input data on chip when WE1,2 and IE1,2 are high, and also increments the internal write address pointer when WE1,2 is high. Data-in setup time t_{DS}, and hold time t_{DH} are referenced to the rising edge of SWCK.

Serial Read Clock: SRCK
Data is shifted out of the data registers. It is triggered by the rising edge of SRCK when RE1, 2 is high during a read operation. The SRCK input increments the internal read address pointer when RE1, 2 is high.
The three-state output buffer provides direct TTL compatibility (no pullup resistor required). Data out is the same polarity as data in. The output becomes valid after the access time interval t_{AC} that begins with the rising edge of SRCK.

Data Input: (DIN20 to 27)
These pins are used for serial data inputs.

Write Reset: RSTW2
The first positive transition of SWCK after RSTW becomes high resets the write address pointers to zero. RSTW2 setup and hold times are referenced to the rising edge of SWCK. Because the write reset function is solely controlled by the SWCK rising edge after the high level of RSTW2, the states of WE2 and IE2 are ignored in the write reset cycle. Before RSTW2 may be brought high again for a further reset operation, it must be low for at least two SWCK cycles.

Write Enable: WE2
WE is used for data write enable/disable control. WE2 high level enables the input, and WE2 low level disables the input and holds the internal write address pointer. There are no WE2 disable time (low) and WE2 enable time (high) restrictions, because the MS8104160A is in fully static operation as long as the power is on. Note that WE2 setup and hold times are referenced to the rising edge of SWCK.

Input Enable: IE2
IE2 is used to enable/disable writing into memory. IE2 high level enables writing. The internal write address pointer is always incremented by cycling SWCK regardless of the IE2 level. Note that IE2 setup and hold times are referenced to the rising edge of SWCK.

Data Out: (DOUT20 to 27)
These pins are used for serial data outputs.

Read Reset: RSTR2
The first positive transition of SRCK after RSTR2 becomes high resets the read address pointers to zero. RSTR2 setup and hold times are referenced to the rising edge of SRCK. Because the read reset function is solely controlled by the SRCK rising edge after the high level of RSTR2, the states of RE2 and OE2 are ignored in the read reset cycle. Before RSTR2 may be brought high again for a further reset operation, it must be low for at least *two SRCK cycles.

Output Enable: OE2
OE2 is used to enable/disable the outputs. OE2 high level enables the outputs. The internal read address pointer is always incremented by cycling SRCK regardless of the OE2 level. Note that OE2 setup and hold times are referenced to the rising edge of SRCK.

Mode Setting1: MODE1
The Cascade/Non cascade select pin. Setting the MODE1 pin to the V_{CC} level configures this memory device as cascade type and setting the pin to the V_{SS} level configures this memory device as non cascade. During memory operation, the pin must be permanently connected to V_{CC} or V_{SS}. If a MODE1 level is changed during memory operation, memory data is not guaranteed.

Mode Setting2: MODE2
MODE2 selects whether the control input signals are enabled at a high level or a low level. Setting MODE2 to the Vcc level enables the control input signals at a low level and setting MODE2 to the Vss level enables the control input signals at a high level.

Note: Cascade/Non cascade
When MODE1 is set to the V_{SS} level, memory accessing starts in the cycle in which the control signals are input (Non cascade type). When MODE1 is set to the V_{CC} level, memory accessing starts in the cycle subsequent to the cycle in which the control signals are input (Cascade type). This type is used for consecutive memory accessing.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Input Output Voltage	V_T	at Ta = 25°C, V_{SS}	–1.0 to +7.0	V
Output Current	I_{OS}	Ta = 25°C	50	mA
Power Dissipation	P_D	Ta = 25°C	1	W
Operating Temperature	T_{OPR}	—	0 to 70	°C
Storage Temperature	T_{STG}	—	–55 to +150	°C

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Power Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	V_{CC}	V_{CC} +0.5	V
Input Low Voltage	V_{IL}	–0.3	0	+0.8	V

DC Characteristics

Parameter	Symbol	Condition	Min.	Max.	Unit
Input Leakage Current	I_{LI}	$0<V_I<V_{CC}$, Other input pins at V = 0 V	–10	+10	μA
Output Leakage Current	I_{LO}	$0<V_O<V_{CC}$	–10	+10	μA
Output “H” Level Voltage	V_{OH}	I_{OH} = –1 mA	2.4	—	V
Output “L” Level Voltage	V_{OL}	I_{OL} = 2 mA	—	0.4	V
Operating Current	I_{CC1}	Minimum Cycle Time, Output Open	—	170	mA
Standby Current	I_{CC2}	Input Pin = V_{IH}/V_{IL}	—	5	mA

Capacitance

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Max.	Unit
Input Capacitance (D_I, SWCK, SRCK, RSTW, RSTR, WE, RE, IE, OE)	C_I	7	pF
Output Capacitance (D_O)	C_O	7	pF

AC Characteristics

(V_{CC} = 5.0 V ±0.5 V, Ta = 0 to 70°C)

Parameter	Symbol	MS8104160A-20		MS8104160A-25		Unit
		Min.	Max.	Min.	Max.	
Access Time from SRCK	t_{AC}	—	18	—	22	ns
D_{OUT} Hold Time from SRCK	t_{DDCK}	6	—	6	—	ns
D_{OUT} Enable Time from SRCK	t_{DECK}	6	20	6	25	ns
SWCK “H” Pulse Width	t_{WSWH}	9	—	12	—	ns
SWCK “L” Pulse Width	t_{WSWL}	9	—	12	—	ns
Input Data Setup Time	t_{DS}	3	—	3	—	ns
Input Data Hold Time	t_{DH}	5	—	5	—	ns
WE Enable Setup Time	t_{WENS}	5	—	5	—	ns
WE Enable Hold Time	t_{WENH}	5	—	5	—	ns
WE Disable Setup Time	t_{WDSS}	5	—	5	—	ns
WE Disable Hold Time	t_{WDSH}	5	—	5	—	ns
IE Enable Setup Time	t_{IENS}	5	—	5	—	ns
IE Enable Hold Time	t_{IENH}	5	—	5	—	ns
IE Disable Setup Time	t_{IDSS}	5	—	5	—	ns
IE Disable Hold Time	t_{IDSH}	5	—	5	—	ns
WE “H” Pulse Width	t_{WWEH}	5	—	5	—	ns
WE “L” Pulse Width	t_{WWEL}	5	—	5	—	ns
IE “H” Pulse Width	t_{WIEH}	5	—	5	—	ns
IE “L” Pulse Width	t_{WIEL}	5	—	5	—	ns
RSTW Setup Time	t_{RSTWS}	3	—	3	—	ns
RSTW Hold Time	t_{RSTWH}	10	—	10	—	ns
SRCK “H” Pulse Width	t_{WSRH}	9	—	12	—	ns
SRCK “L” Pulse Width	t_{WSRL}	9	—	12	—	ns
RE Enable Setup Time	t_{RENS}	5	—	5	—	ns
RE Enable Hold Time	t_{RENH}	5	—	5	—	ns
RE Disable Setup Time	t_{RDSS}	5	—	5	—	ns
RE Disable Hold Time	t_{RDSH}	5	—	5	—	ns
OE Enable Setup Time	t_{OENS}	5	—	5	—	ns
OE Enable Hold Time	t_{OENH}	5	—	5	—	ns
OE Disable Setup Time	t_{ODSS}	5	—	5	—	ns
OE Disable Hold Time	t_{ODSH}	5	—	5	—	ns
RE “H” Pulse Width	t_{WREH}	5	—	5	—	ns
RE “L” Pulse Width	t_{WREL}	5	—	5	—	ns
OE “H” Pulse Width	t_{WOEH}	5	—	5	—	ns
OE “L” Pulse Width	t_{WOEL}	5	—	5	—	ns
RSTR Setup Time	t_{RSTRS}	3	—	3	—	ns
RSTR Hold Time	t_{RSTRH}	10	—	10	—	ns
SWCK Cycle Time	t_{SWC}	20	—	25	—	ns
SRCK Cycle Time	t_{SRC}	20	—	25	—	ns
Transition Time (Rise and Fall)	t_T	3	30	3	30	ns

AC Characteristics Measuring Conditions

Output Compare Level	1.5 V / 1.5 V
Output Load	1 TTL + 30 pF
Input Signal Level	3.0 V / 0.0 V
Input Signal Rise/Fall Time	3 ns
Input Signal Measuring Reference Level	1.5 V

1. Input voltage levels for the AC characteristic measurement are V_{IH} = 3.0 V and V_{IL}= 0 V. The transition time t_T is defined to be a transition time that signal transfers between V_{IH} = 3.0 V and V_{IL} = 0 V.

2. AC measurements assume t_T = 3 ns.

3. Read address must have more than a 150 address delay than write address in every cycle when asynchronous read/write is performed.

4. Read must have more than a 150 address delay than write in order to read the data written in a current series of write cycles which has been started at last write reset cycle: this is called “new data read”. When read has less than a 20 address delay than write, the read data are the data written in a previous series of write cycles which had been written before at last write reset cycle: this is called “old data read”.

5. When the read address delay is between more than 21 and less than 149 or more than 262,214, read data will be undetermined. However, normal write is achieved in this address condition.

OPERATION MODE

Write Operation Cycle (MODE2 = V_{SS})

The write operation is controlled by seven control signals, SWCK, RSTW1, RSTW2, WE1, WE2 and IE1, IE2. Port1 write operation is accomplished by cycling SWCK, and holding WE1 and IE1 high after the write address pointer reset operation or RSTW1. RSTW1 must be preformed for internal circuit initialization before Write operation.

Each write operation, which begins after RSTW1, must contain at least 140 active write cycles, i.e. SWCK cycles while WE1 and IE1 are high. To transfer the last data to the DRAM array, which at that time is stored in the serial data registers attached to the DRAM array, an RSTW1 operation is required after the last SWCK cycle.

Note that every write timing of MS8104160A is delayed by one clock compared with read timings for easy cascading without any interface delay devices.

Setting MODE1 to the V_{SS} level starts write data accessing in the cycle in which RSTW1, WE1, and IE1 control signals are input.

Setting MODE1 to the V_{CC} level starts write data accessing in the cycle subsequent to the cycle in which RSTW1, WE1, and IE1 control signals are input.

These operation are the same for Port1 and Port2.

Settings of WE1, 2 and IE1, 2 to the operation mode of Write address pointer and Data input.

WE1, 2	IE1, 2	Internal Write address pointer	Data input
H	H	Incremented	Input
H	L		Not input
L	X	Halted	

X indicates “don’t care”

Write Operation Cycle (MODE2=V_{CC})

The write operation is controlled by seven control signals, SWCK, RSTW1, RSTW2, WE1, WE2, and IE1, IE2. Port1 write operation is accomplished by cycling SWCK and holding WE1 and IE1 low after the write address pointer reset operation or RSTW1. RSTW1 must be performed for internal circuit initialization before write operation.

Each write operation, which begins after RSTW1, must contain at least 140 active write cycle, i.e. SWCK cycles while WE1 and IE1 are high. To transfer the last data to the DRAM array, which at that time is stored in the serial data registers attached to the DRAM array, an RSTW1 operation is required after the last SWCK cycle.

Note that every write timing of MS8104160A is delayed by one clock compared with read timings for easy cascading without any interface delay devices.

Setting MODE1 to the V_{SS} level starts write data accessing in the cycle in which RSTW1.WE1, and IE1 control signals are input.

Setting MODE1 to the V_{CC} level starts write data accessing in the cycle in which RSTW1, WE1, and IE1 control signals are input.

Setting MODE1 to the V_{CC} level starts write data accessing in the cycle subsequent to the cycle in which RSTW1, WE1, and IE1 control signals are input.

These operations are the same for port1 and Port2.

Read Operation Cycle (MODE2=V_{SS})

The read operation is controlled by seven control signals, SRCK, RSTR1, RSTR2, RE1, RE2, and OE1, OE2. Port1 read operation is accomplished by cycling SRCK, and holding RE1 and OE1 high after the read address pointer reset operation or RSTR1.
Each read operation, which begins after RSTR1, must contain at least 140 active read cycles, i.e. SRCK cycles while RE1 and OE1 are high.
These operations are the same for Port1 and Port2.

Settings of RE1, 2 and OE1, 2 to the operation mode of read address pointer and Data output.

WE1, 2	IE1, 2	Internal Write address pointer	Data output
H	H	Incremented	Output
H	L		High impedance
L	X	Halted	Output
L	L		High impedance

Read Operation Cycle (MODE2=V_{CC})
The read operation is controlled by seven control signals, SRCK, RSTR1, RSTR2, RE1, RE2, and OE1, OE2. Port1 read operation is accomplished by cycling SRCK, and holding RE1 and OE1 low after the read address pointer reset operation or RSTR1.
Each read operation, which begins after RSTR1, must contain at least 140 active read cycles, i.e. SRCK cycles while RE1 and OE1 are low.
These operations are the same for Port1 and Port2.

Settings of RE1, 2 and OE1, 2 to the operation mode of read address pointer and Data output.

RE1,2	OE1,2	Internal Write address pointer	Data output
L	L	Incremented	Output
L	H		High impedance
H	L	Halted	Output
H	H		High impedance

Power-up and Initialization

On power-up, the device is designed to begin proper operation after at least 100 μs after V_{CC} has stabilized to a value within the range of recommended operating conditions. After this 100 μs stabilization interval, the following initialization sequence must be performed.

Because the read and write address pointers are undefined after power-up, a minimum of 80 dummy write operations (SWCK cycles) and read operations (SRCK cycles) must be performed, followed by an RSTW1, 2 operation and an RSTR1, 2 operation, to properly initialize the write and the read address pointer. Dummy write cycles/RSTW1, 2 and dummy read cycles/RSTR1, 2 may occur simultaneously.

If these dummy read and write operations start while V_{CC} and/or the substrate voltage has not stabilized, it is necessary to perform an RSTR1, 2 operation plus a minimum of 80 SRCK cycles plus another RSTR1, 2 operation, and an RSTW1, 2 operation plus a minimum of 80 SWCK cycles plus another RSTW1, 2 operation to properly initialize read and write address pointers.

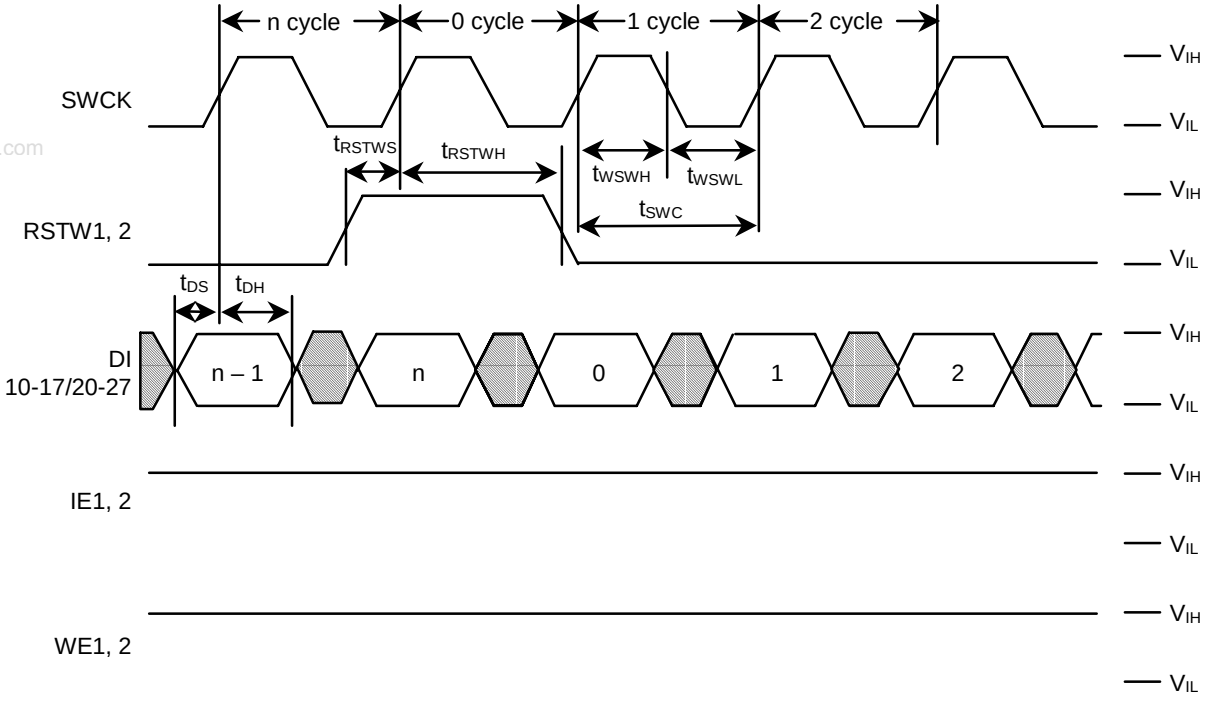
Old/New Data Access

There must be a minimum delay of 150 SWCK cycles between writing into memory and reading out from memory. If reading from the first field starts with an RSTR1, 2 operation, before the start of writing the second field (before the next RSTW1, 2 operation), then the data just written will be read out.

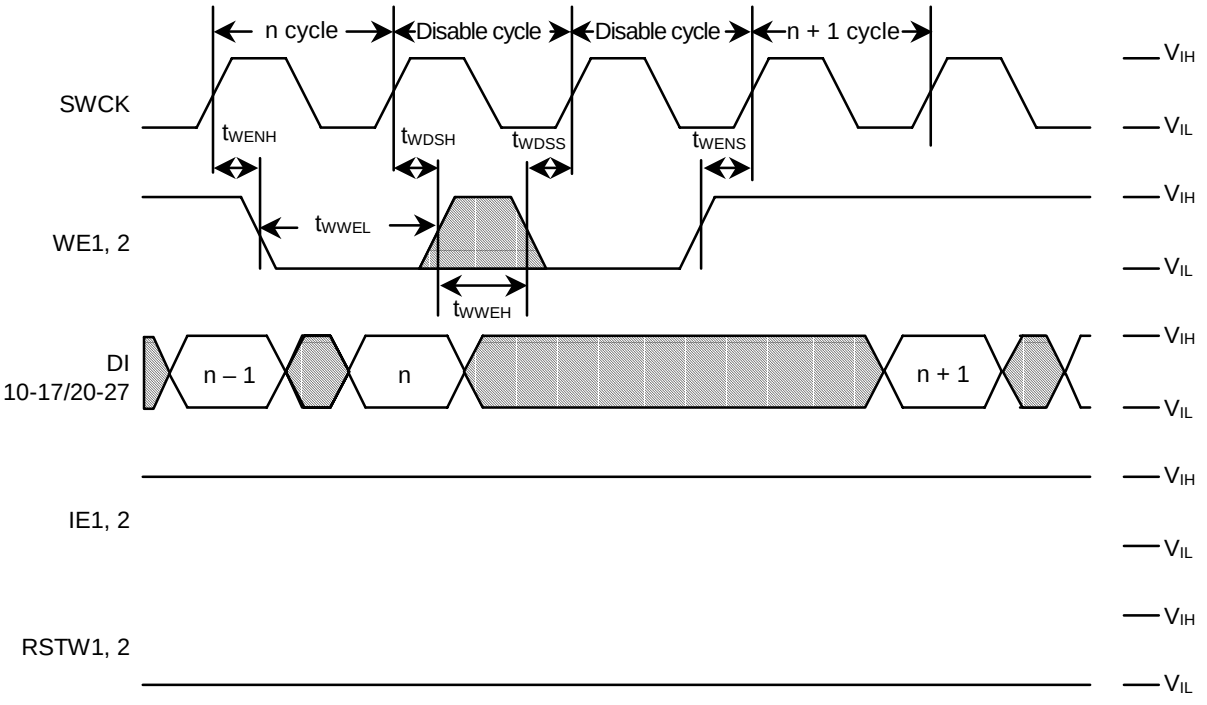
The start of reading out the first field of data may be delayed past the beginning of writing in the second field of data for as many as 20 SWCK cycles. If the RSTR1, 2 operation for the first field read-out occurs less than 20 SWCK cycles after the RSTW1, 2 operation for the second field write-in, then the internal buffering of the device assures that the first field will still be read out. The first field of data that is read out while the second field of data is written is called “old data”. In order to read out “new data”, i.e., the second field written in, the delay between an RSTW1, 2 operation and an RSTR1, 2 operation must be at least 150 SRCK cycles. If the delay between RSTW1, 2 and RSTR1, 2 operations is more than 21 but less than 149 cycles, then the data read out will be undetermined. It may be “old data” or “new data”, or a combination of old and new data. Such a timing should be avoided.

TIMING WAVEFORM

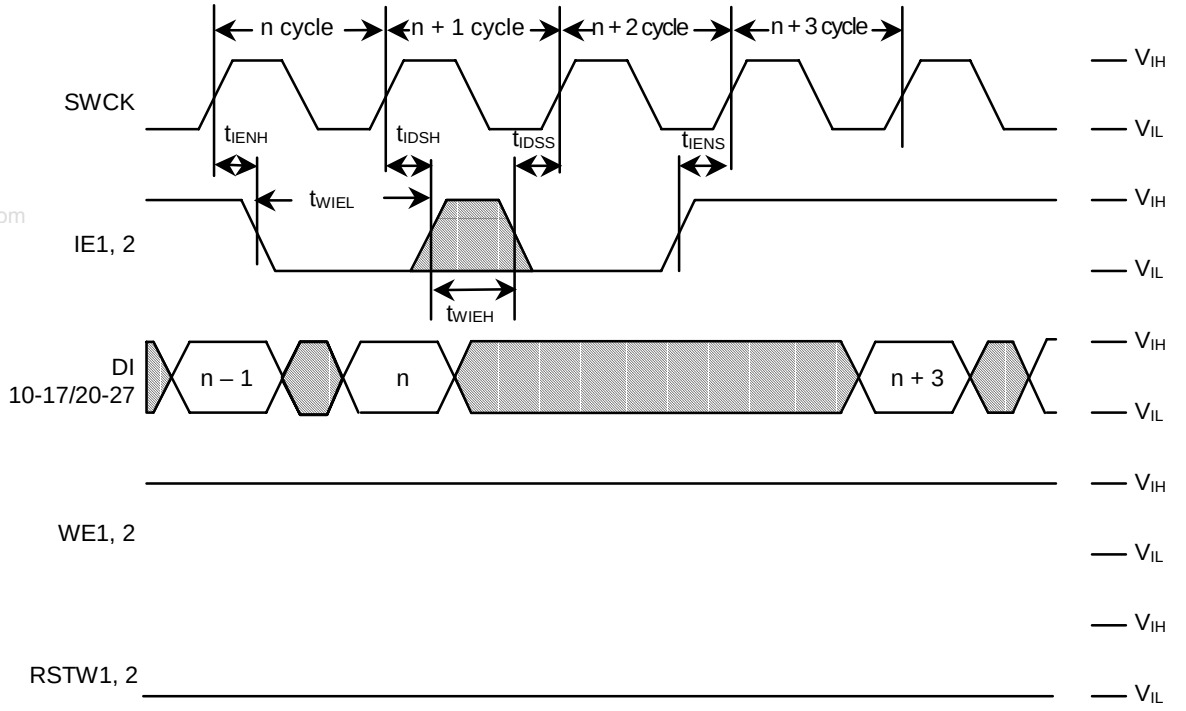
Write Cycle Timing (Write Reset): MODE1 = V_{CC}, MODE2 =V_{SS}



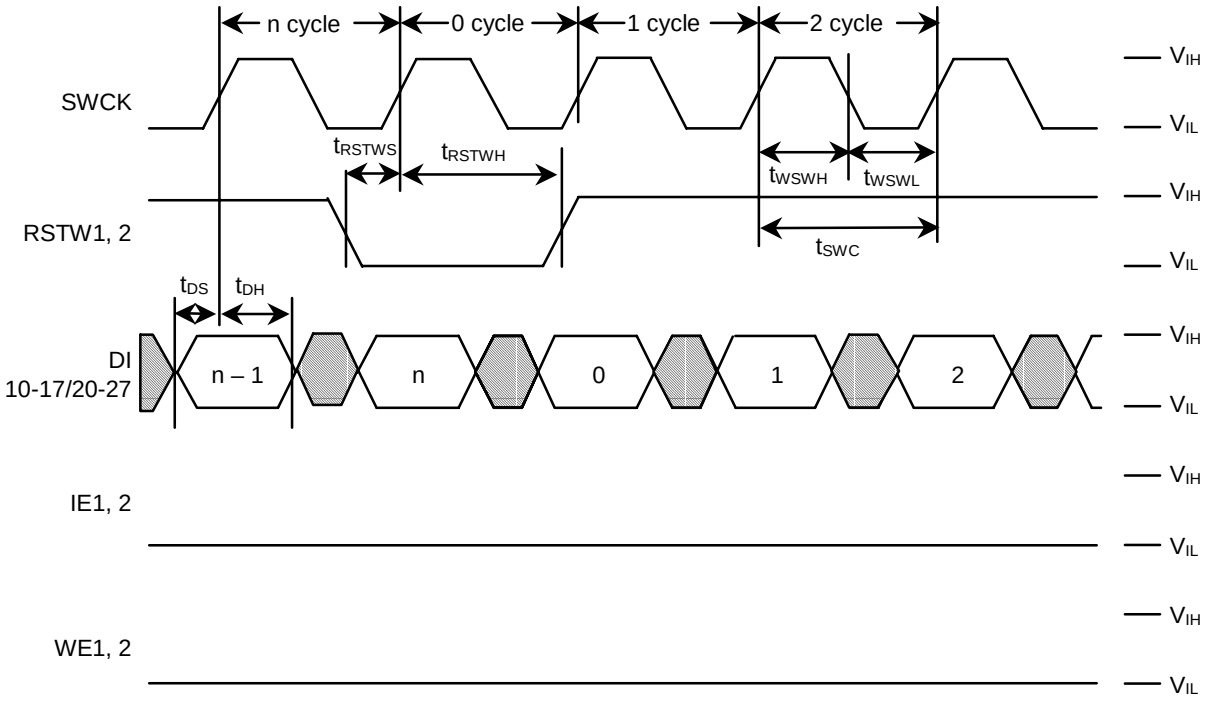
Write Cycle Timing (Write Enable): MODE1 = V_{CC}, MODE2 =V_{SS}



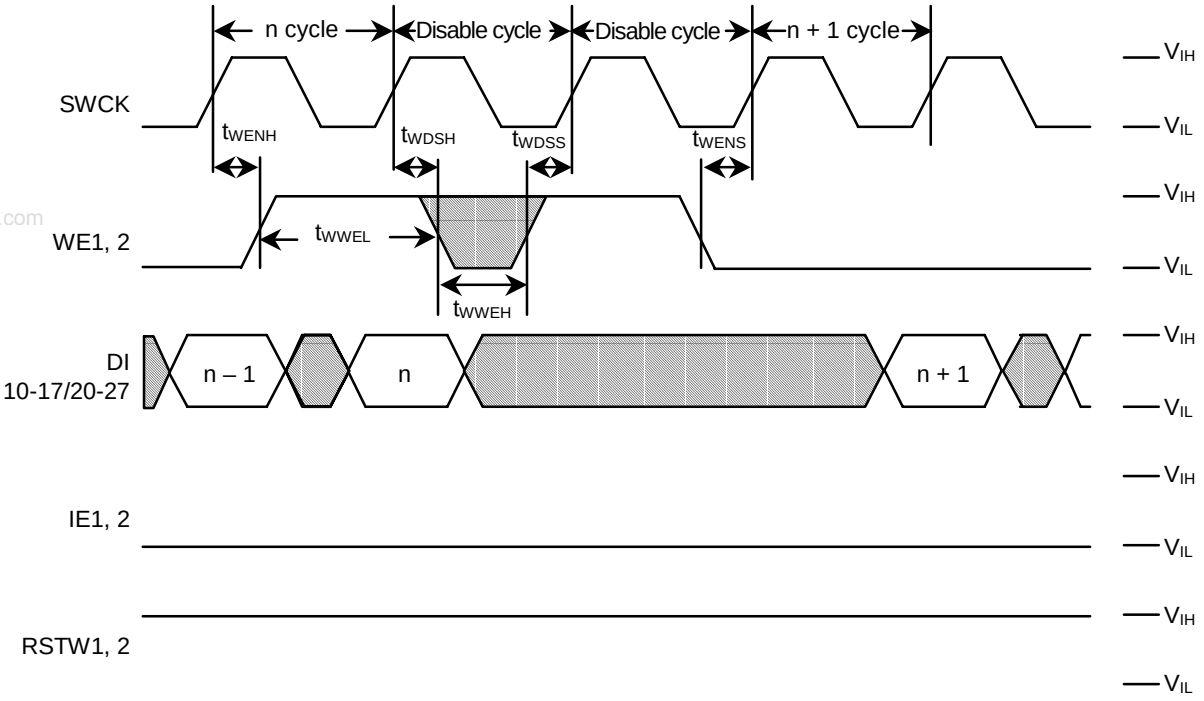
Write Cycle Timing (Input Enable): MODE1 = V_{CC}, MODE2 =V_{SS}



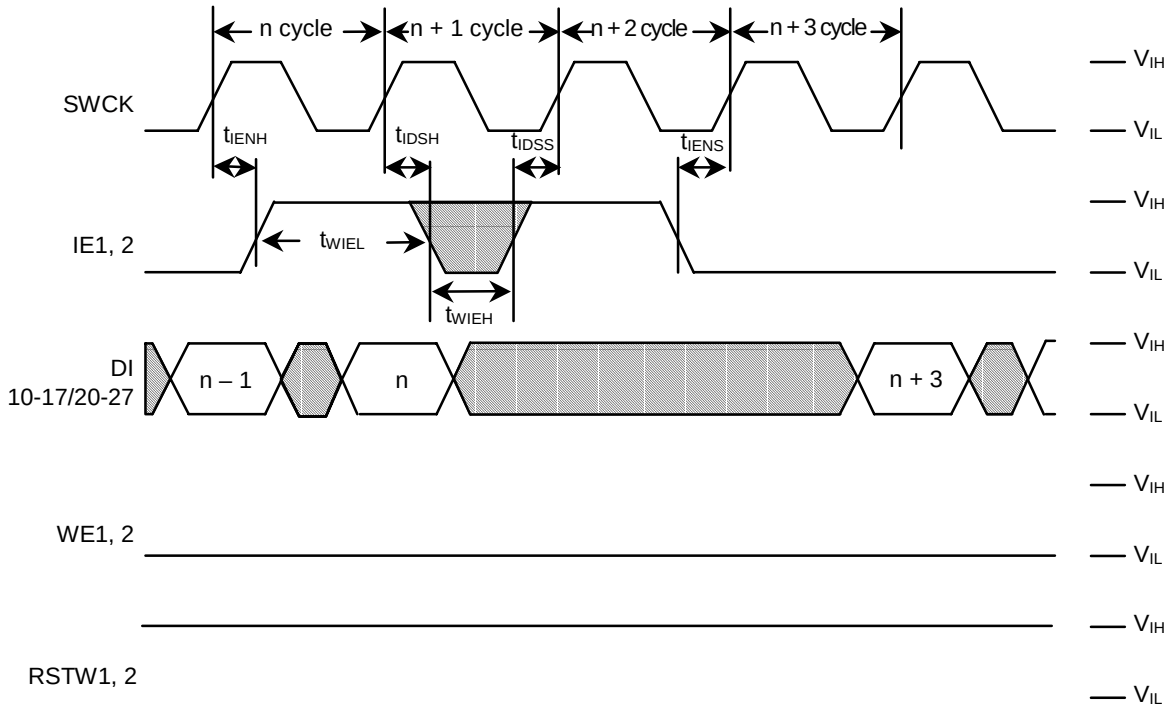
Write Cycle Timing (Write Reset): MODE1 = V_{CC}, MODE2 =V_{CC}



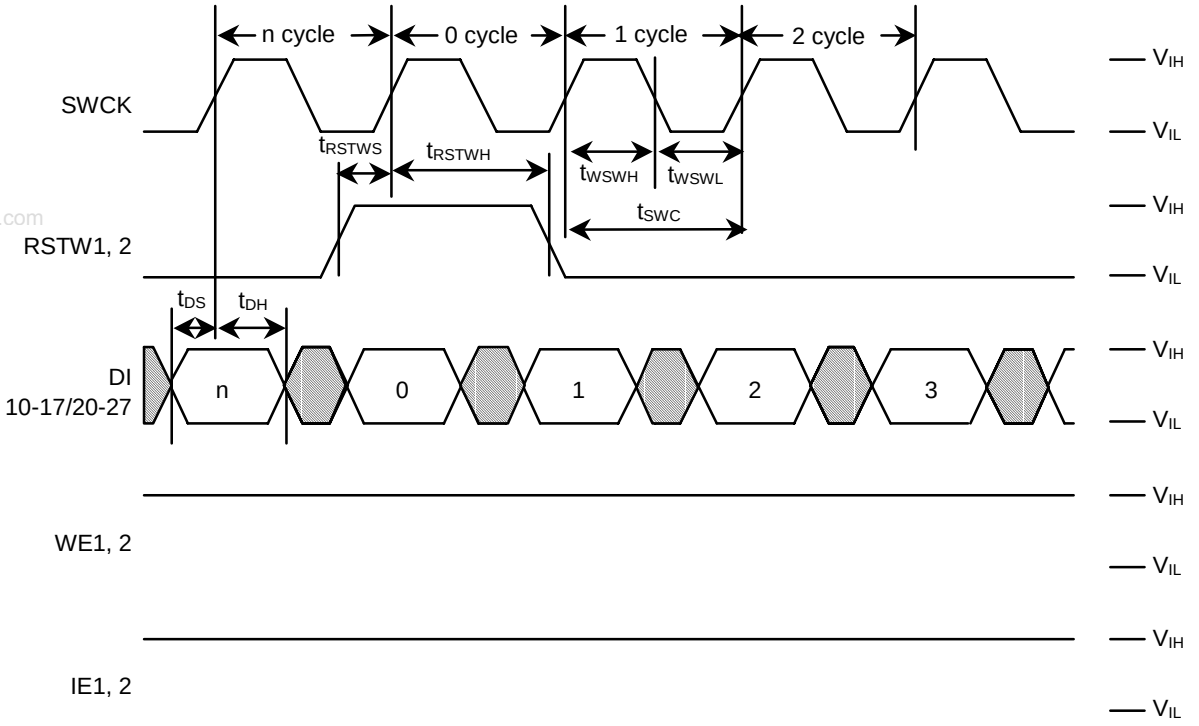
Write Cycle Timing (Write Enable): MODE1 = V_{CC}, MODE2 =V_{CC}



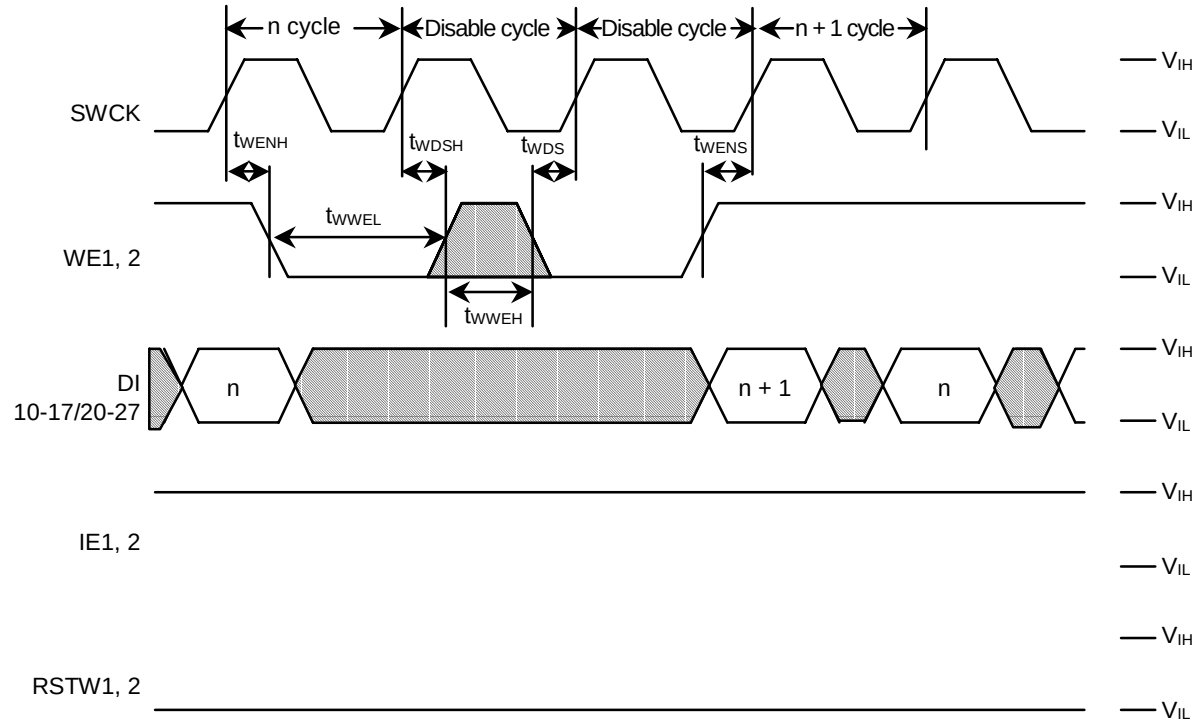
Write Cycle Timing (Input Enable): MODE1 = V_{CC}, MODE2 =V_{CC}



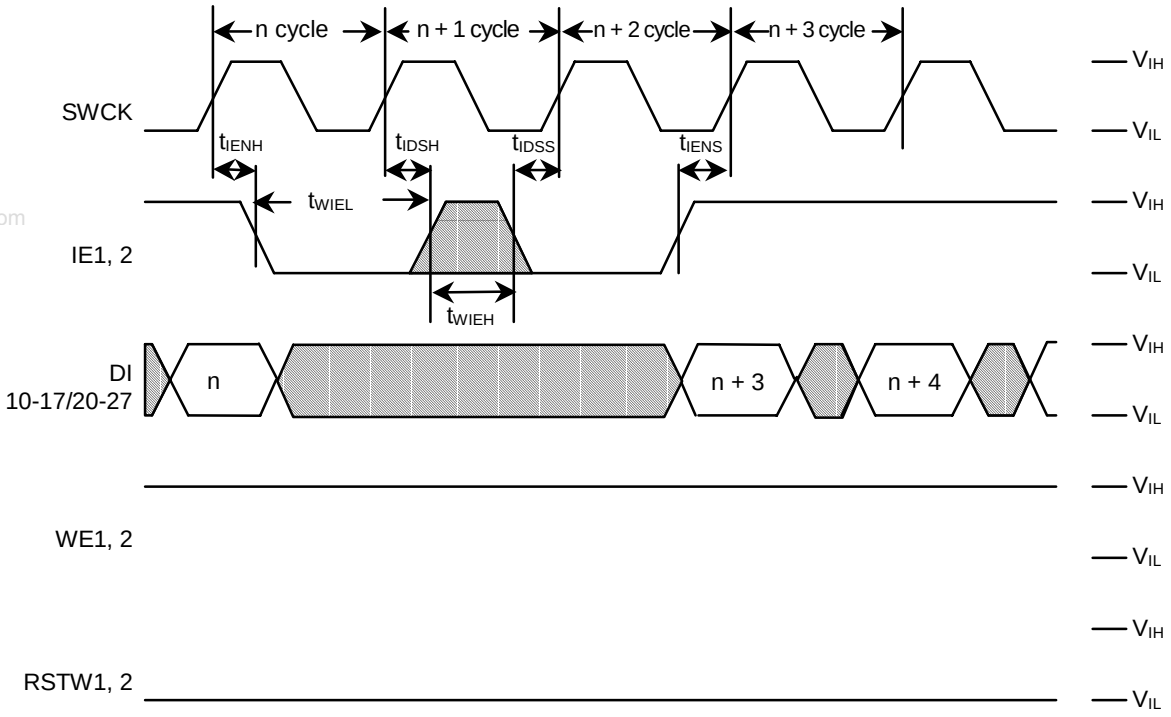
Write Cycle Timing (Write Reset): MODE1 = V_{SS}, MODE2 =V_{SS}



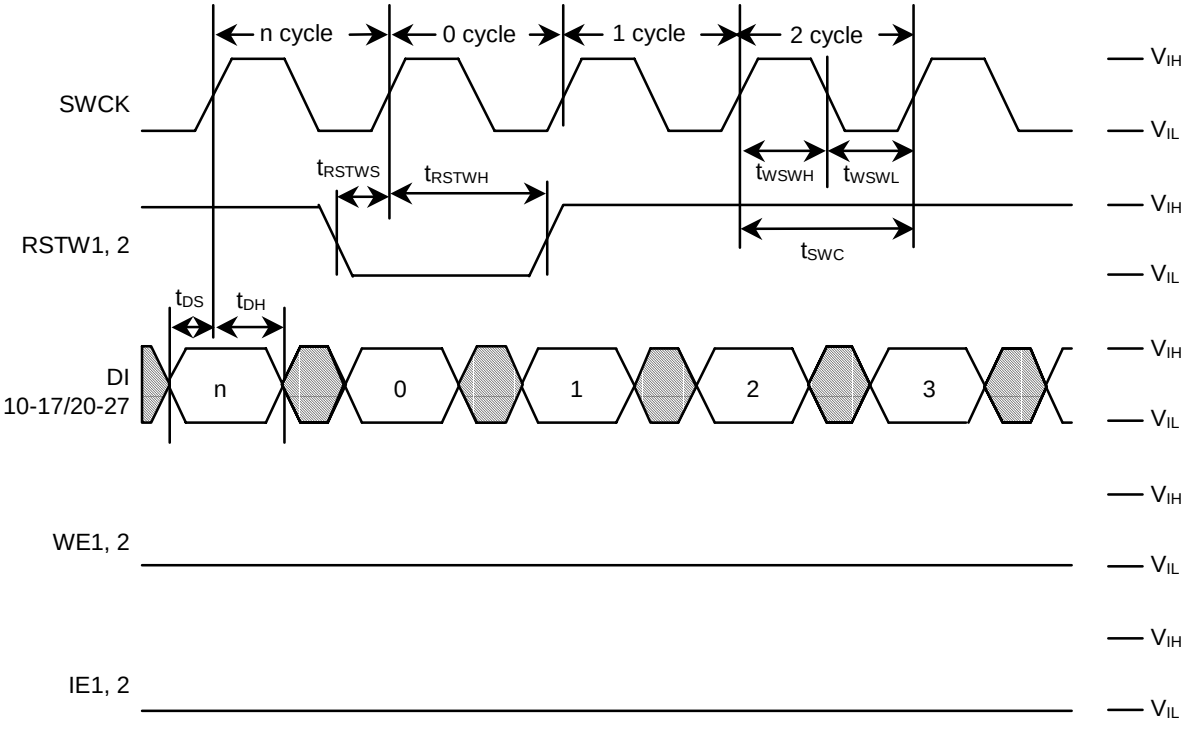
Write Cycle Timing (Write Enable): MODE1 = V_{SS}, MODE2 =V_{SS}



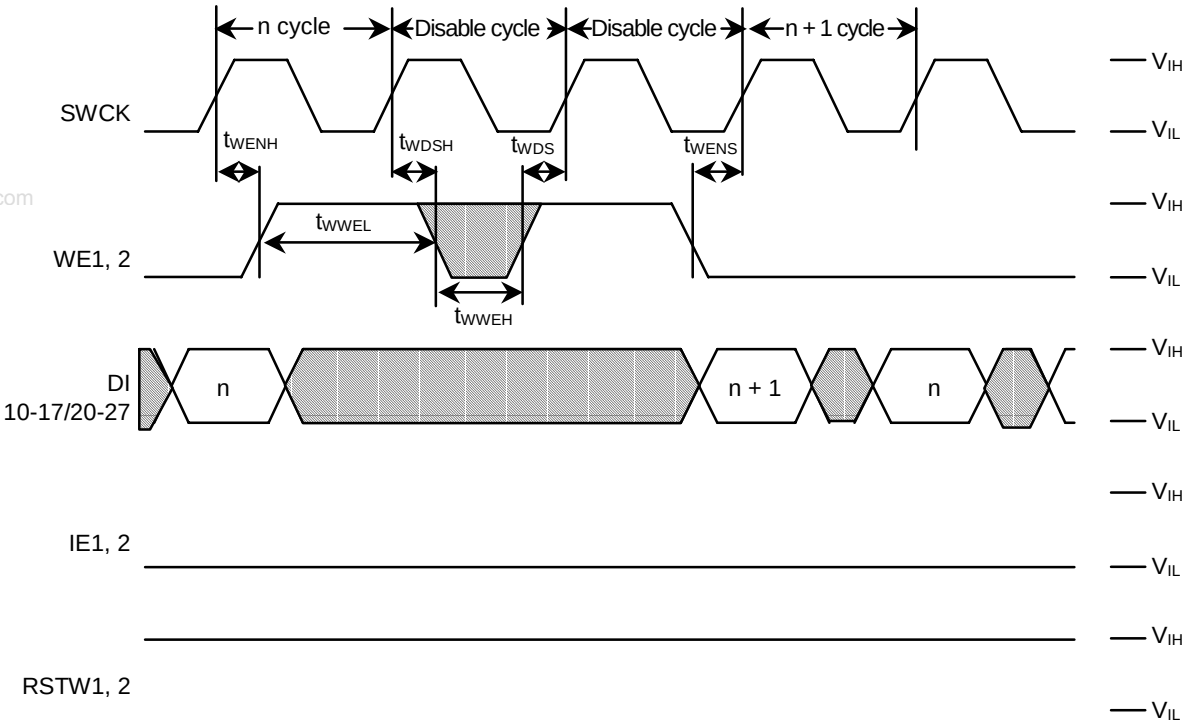
Write Cycle Timing (Input Enable): MODE1 = V_{SS}, MODE2 =V_{SS}



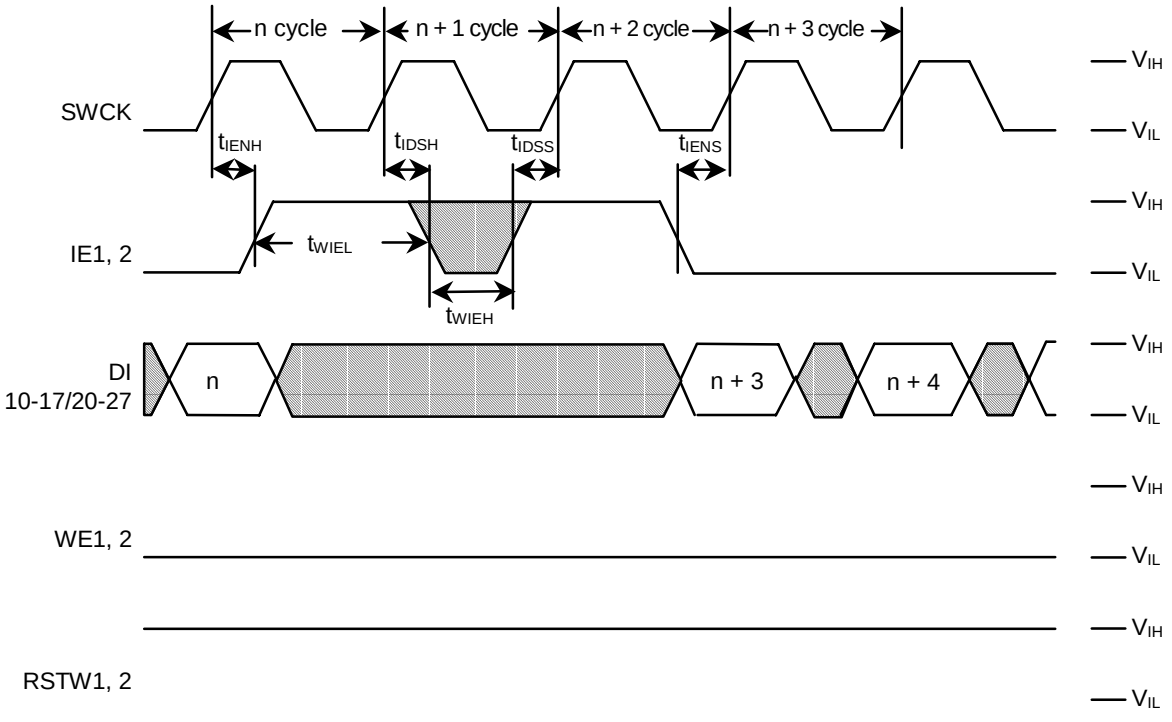
Write Cycle Timing (Write Reset): MODE1 = V_{SS}, MODE2 =V_{CC}



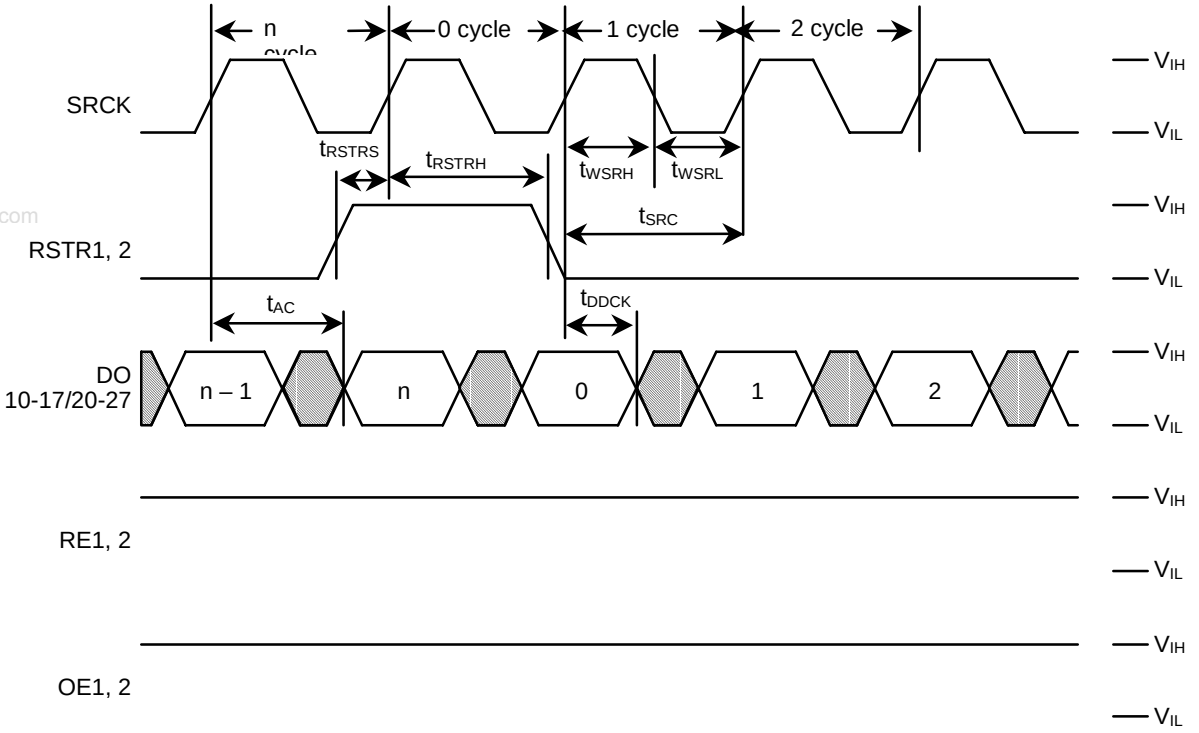
Write Cycle Timing (Write Enable): MODE1 = V_{SS}, MODE2 =V_{CC}



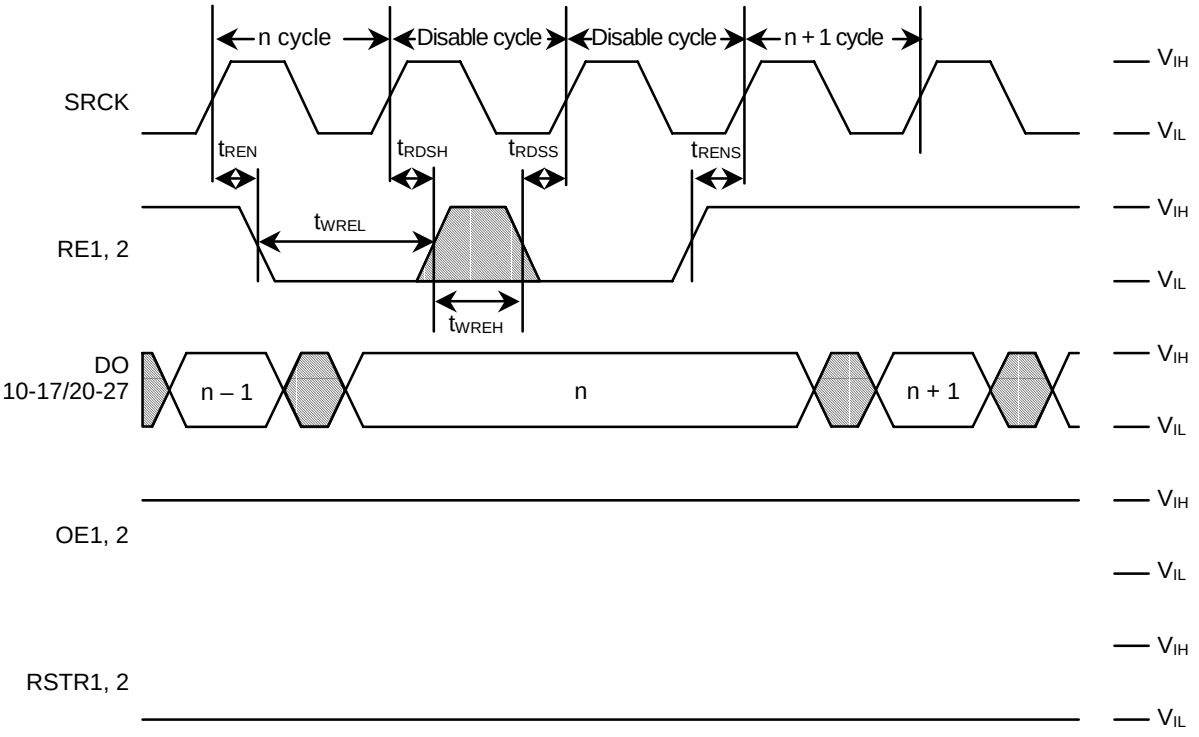
Write Cycle Timing (Input Enable): MODE1 = V_{SS}, MODE2 =V_{CC}



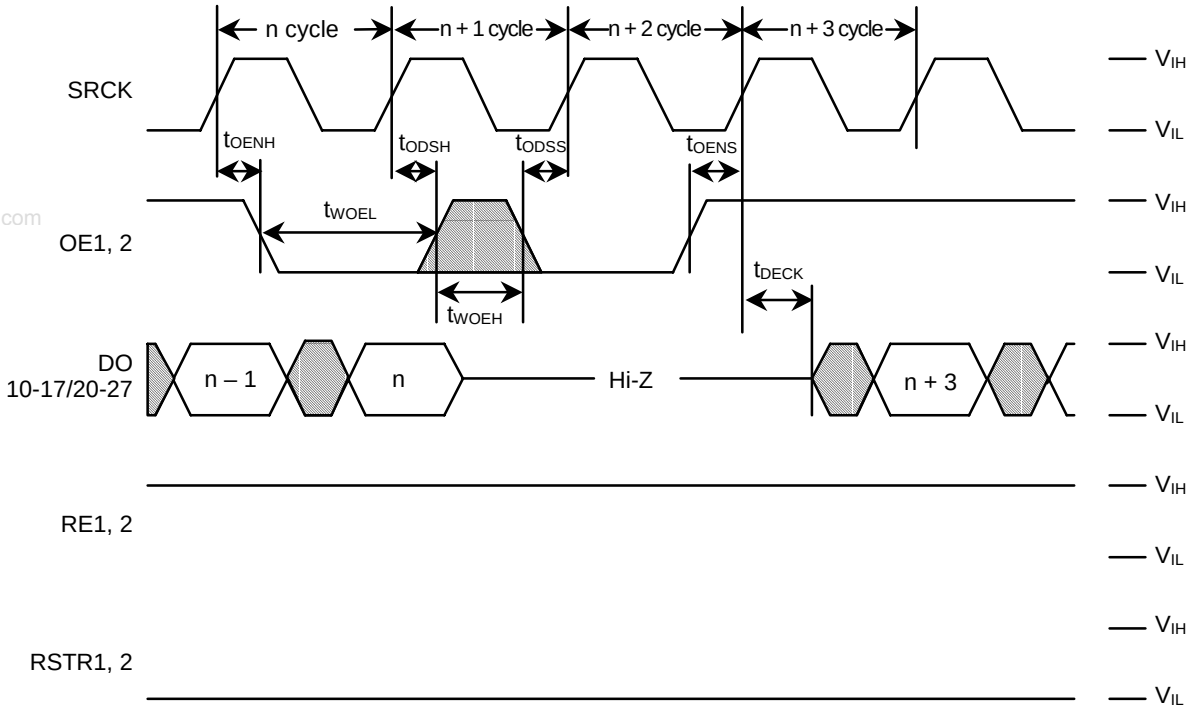
Read Cycle Timing (Read Reset): MODE1 = V_{CC}/V_{SS}, MODE2 =V_{SS}



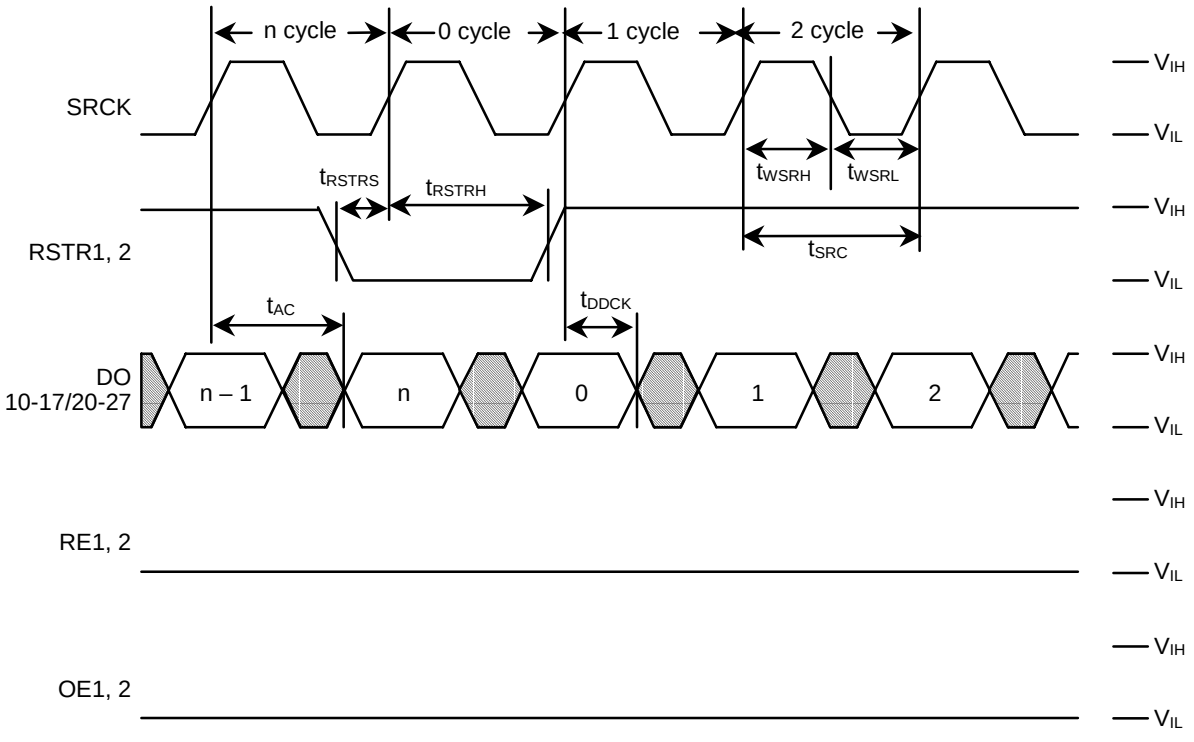
Read Cycle Timing (Read Enable): MODE1 = V_{CC}/V_{SS}, MODE2 =V_{SS}



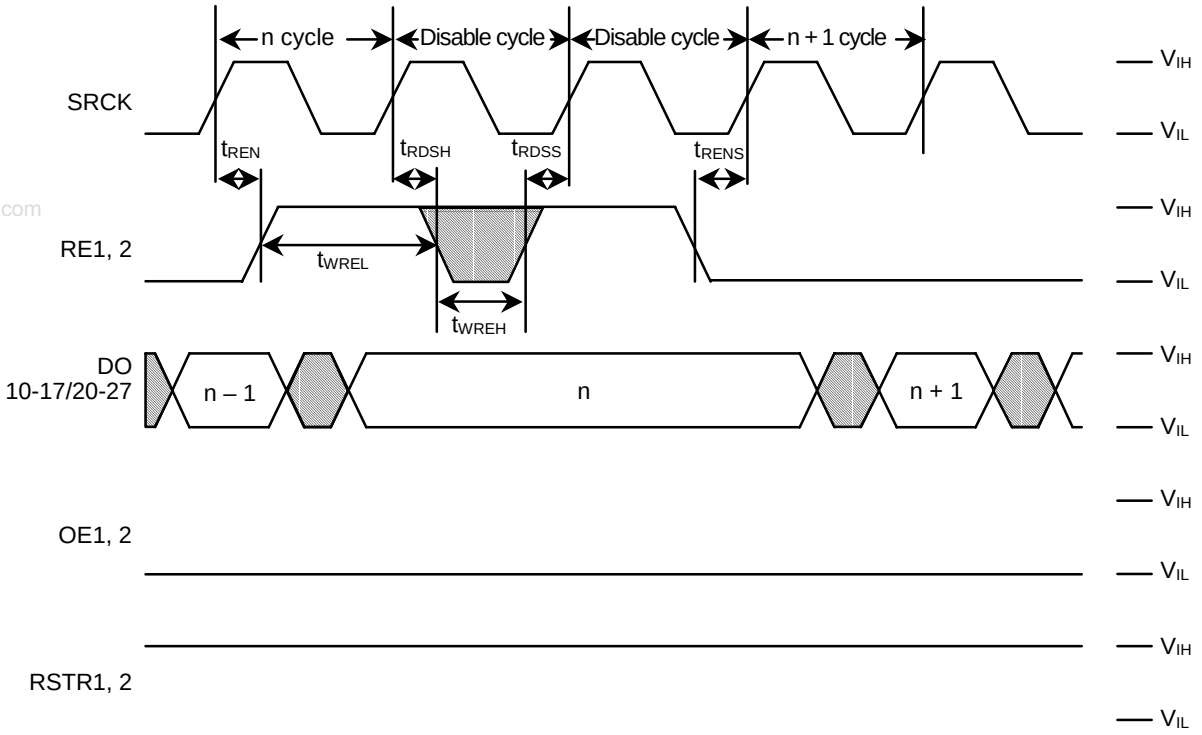
Read Cycle Timing (Output Enable): MODE1 = V_{CC}/V_{SS}, MODE2 =V_{SS}



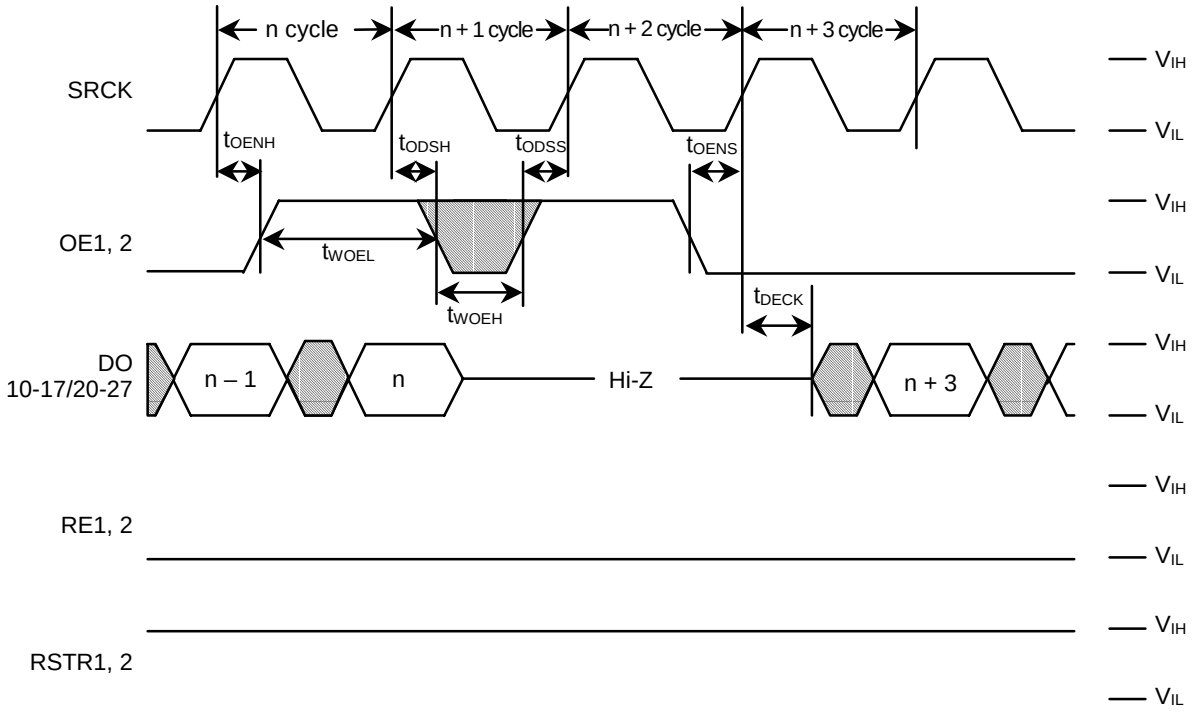
Read Cycle Timing (Read Reset): MODE1 = V_{CC}/V_{SS}, MODE2 =V_{CC}



Read Cycle Timing (Read Enable): MODE1 = V_{CC}/V_{SS}, MODE2 =V_{CC}



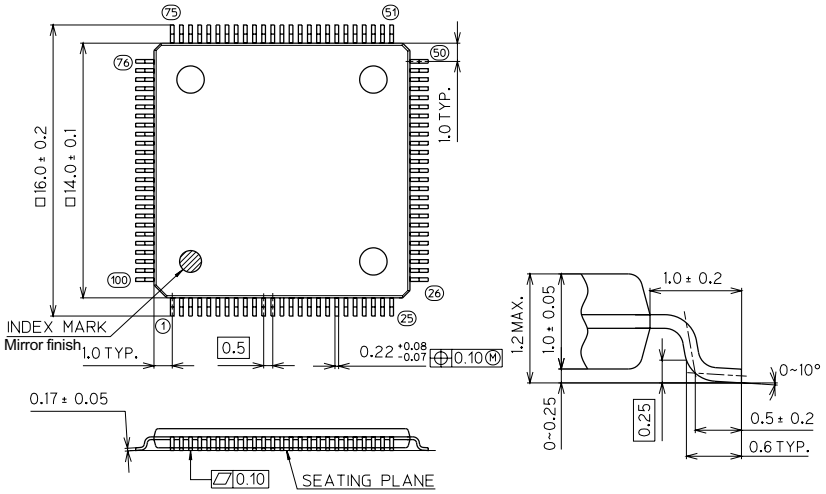
Read Cycle Timing (Output Enable): MODE1 = V_{CC}/V_{SS}, MODE2 =V_{CC}



PACKAGE DIMENSIONS

(Unit: mm)

TQFP100-P-1414-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	0.55 TYP.
Rev. No./Last Revised	4/Oct. 28, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDS8104160A-01	Nov. 21, 2002	–	–	Final edition 1

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2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

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