

# Low-Voltage, High-Precision, Push-Pull Output Comparator

#### PRODUCT DESCRIPTION

The MS8923/8923S is a differential input, high-speed and low power dissipation comparator with complementary TTL outputs. Its propagation delay is about 10ns and its common-mode input range includes the negative rail. The MS8923/8923S output can remain stable output in the linear region. The single power supply is +5.0V and the dual power supply is ±5V.

The MS8923 is available in SOP8 package. The MS8923S is available in SOT23-5 package.





SOT23-5

### **FEATURES**

- Fast Propagation Delay: 10ns
- Single Power Supply +5V or Dual Power Supply ±5V
- Input Voltage Range below the Negative Rail
- Low Power Dissipation: 6mA
- No Requirement for the Minimum Input Signal Changing Rate
- Stable in the Linear Region
- Input Offset Voltage: 0.8mV
- Operating Temperature: -40°C ~ 120°C

### **APPLICATIONS**

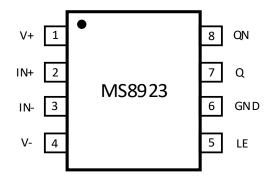
- Handheld and Battery-powered Systems
- Scanner and Set Top Box
- High-speed Differential Line Receiver
- Window Comparator
- Zero-crossing Monitor
- High-peed Sampling Circuit
- V/F Converter

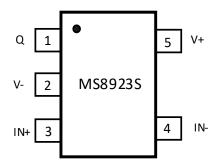
### PRODUCT SPECIFICATION

Part Number	Package	Marking
MS8923	SOP8	MS8923
MS8923S	SOT23-5	8923S



## **PIN CONFIGURATION**





## **PIN DESCRIPTION**

Pin	Name	Туре	Description				
	MS8923						
1	V+	-	Positive Power Supply				
2	IN+	I	Positive Input				
3	IN-	I	Negative Input				
4	V-	-	Negative Power Supply				
5	LE	I	Latch Enable Pin. When LE is in high level or floating, Q and QN outputs are latched; When LE is in low level, the outputs of Q and QN change with input.				
6	GND	-	Logic Ground				
7	Q	0	Positive Output of Comparator				
8	QN	0	Negative Output of Comparator				
			MS8923S				
1	Q	0	Positive Output of Comparator				
2	V-	-	Negative Power Supply				
3	IN+	I	Positive Input				
4	IN-	I	Negative Input				
5	V+	-	Positive Power Supply				



### **ABSOLUTE MAXIMUM RATINGS**

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Positive Power Supply Range	V+	+7	V
Negative Power Supply Range	V-	-7	V
Power Supply Range	(V+)-(V-)	+13	V
Differential Input Voltage Range	VID	+15	V
Input Voltage Range (Referred to V-)		-0.3 ∼ <b>+1</b> 4	V
Maximum Voltage on Latch Pin	V(LE)	Power Supply	V
Maximum Junction Temperature		+150	°C
Storage Temperature	Tstg	-60 ~ 150	°C
Lead Temperature(10s)		260	°C
ESD Voltage(HBM)		2000	V
ESD Voltage(MM)		200	٧



## **ELECTRICAL CHARACTERISTICS**

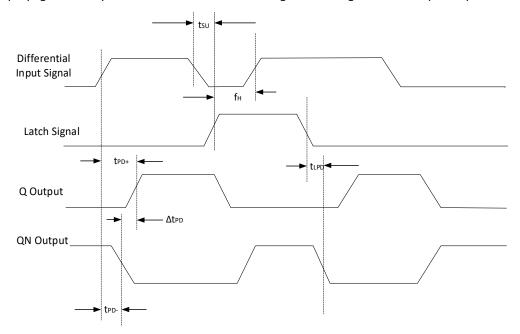
Unless otherwise noted, Ta = Tmin  $\sim$  Tmax, Vq=+1.4V, V+ = +5V, V- = -5V, VLE=0V.

	Parameter	Symbol	Condition	Min	Тур	Max	Unit	
Input Offset Voltage		Vos	Rs≤100Ω, Ta=+25°C		0.1	2	mV	
			Rs≤100Ω, Ta= TMIN ~ TMAX			3		
Input Offse	t Drift	TCVos			2		μV/°C	
			TA=+25°C		2 5			
Input Bias (	Lurrent	Ів	C, E Temperature Ranges			8	μΑ	
			TA=+25°C		0.3	0.5		
Input Offse	t Current	los	TA= TMIN ~ TMAX			1	μΑ	
Common-m	node Rejection Ratio	CMRR	-4.2V < VcM < +3.5V	80	110		dB	
_			C, E Temperature Ranges	-4.2		+3.5		
Input Comr		CMVR	Single Power Supply: +5V,				V	
Voltage Rar	nge		C, E Temperature Ranges	0.8		+3.5		
			Positive Power Supply:		85			
Power Supp	oly	PSRR	4.5V≤V+≤5.5V	60			dB	
Rejection R	atio		Negative Power Supply:		100			
			-4.5V≤V+≤-5.5V	80				
Small Signa	l Voltage Gain	Av	1V≤VQ≤2V, TA = +25°C	1500	3500		V/V	
Output	High-level	Vон	V+≥4.5V, Iouт= 10mA	3.0	3.3			
Voltage	Low-level	Vol	Isink=4mA		0.3	0.5	V	
Positive Po	wer Supply Current	l+	C, E Temperature Ranges		6.7	10	mA	
Negative Po	ower Supply Current	I-			1	2	mA	
High-level	Input on Latch pin	ViH		2.0			V	
Low-level Input on Latch pin		VIL				0.8	V	
Input Current on Latch pin		lıL	VLE=0V		-3	-20	μΑ	
Propagation Delay		tPD+	ΔVIN=100mV, Vod=5mV, 25°C		5.5	8		
		tpd-	ΔVIN=100mV, Vod=20mV, 25°C		5.5	8	ns	
Propagation Delay Skew		Δtpd			1	3	ns	
Latch Setup Time <sup>1</sup>		<b>t</b> su		2	0		ns	
Latch Hold Time <sup>1</sup>		tн		5	2		ns	
Latch Propogation Delay <sup>2</sup>		tlpd			7		ns	



#### Note:

- 1. Latch setup time is the stable time when input signal is prior to latch signal. Latch hold time is the time when input signal remains unchanged after latch time.
- 2. Latch propagation delay time is the time from the change of latch signal to the output response.



#### TYPICAL APPLICATION DIAGRAM

#### **Simple Comparator**

A simple comparator is used to convert the analog input signal to digital output signal. The comparator compares an input voltage(VIN) on the non-inverting pin with the reference voltage(VREF) on the inverting pin. If VIN is less than VREF, the output voltage is low. If VIN is greater than VREF, the output voltage is high.

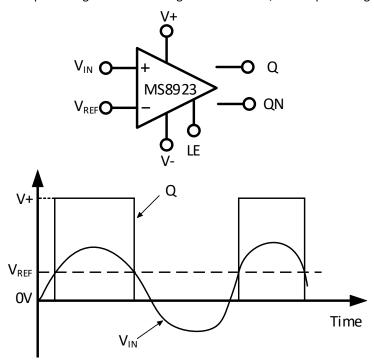


Figure 1. Simple Comparator

### **Hysteresis Effect**

If the differential input of the simple comparator is close to the offset voltage, the comparator will oscillate or produce noisy oscillation. It usually occurs when one input voltage is equal or very close to the other input voltage. Hysteresis can address this problem. Hysteresis can produce two comparison thresholds (one for the rising process and the other for the falling process). Hysteresis value is the difference between two comparison thresholds. When both inputs are very close, hysteresis would cause one input voltage to exceed the other voltage quickly. Thus, the input voltage is moved out of the region in which oscillation may occur.

As shown in Figure 2, hysteresis can be formed by connecting two resistors to the non-inverting pin, which is the positive feedback. When VIN rises up to VIN1, the output would change from low to high. VIN1 can be calculated from the following formula:

$$V_{IN1} = V_{REF} \times \frac{R_1 + R_2}{R_2}$$

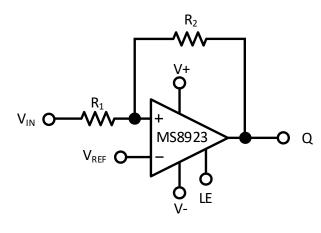
When Vin falls to Vin2, the output would change from high to low. Vin2 can be calculated from the following formula:

$$V_{IN2} = V_{REF} \times \frac{R_1 + R_2}{R_2} - (V+) \times \frac{R_1}{R_2}$$



The hysteresis value is the difference between VIN1 and VIN2:

$$\Delta V_{IN} = V_{IN1} - V_{IN2} = V_{CC} \times \frac{R_1}{R_2}$$



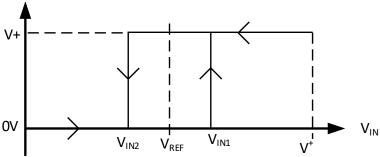


Figure 2. Non-inverting Comparator Circuit

### Input

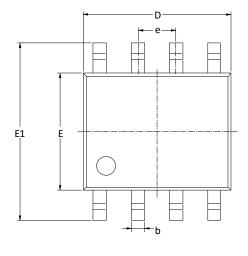
Input bias current of the MS8923/8923S is near zero, which allows the use of high-impedance circuit without considering impedance match. This also allows the use of small-capacitor in R-C type timing circuit and reduces the use of the capacitor and the space of circuit board.

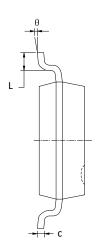
### **Board Layout and Bypassing**

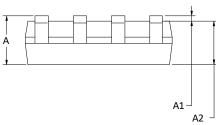
Although the MS8923/8923S is stable and has an anti-interference ability, it is important to use appropriate bypassing capacitors and ground pickups. The  $0.1\mu F$  ceramic capacitor can provide clean power and the shortest signal line can reduce stray capacitance.

# **PACKAGE OUTLINE DIMENSIONS**

# SOP8

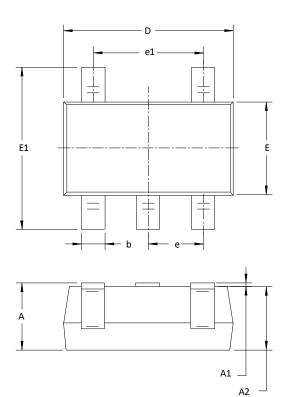


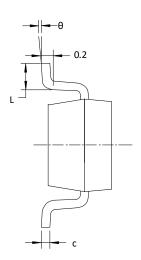




	Dimensions i	n Millimeters	Dimensions in Inches		
Symbol	Min	Max	Min	Max	
А	1.350	1.750	0.053	0.069	
A1	0.100	0.225	0.004	0.010	
A2	1.350	1.550	0.053	0.061	
b	0.330	0.510	0.013	0.020	
С	0.170	0.250	0.006	0.010	
D	4.700	5.100	0.185	0.200	
E	3.800	4.000	0.150	0.157	
E1	5.800	6.200	0.228	0.244	
e	1.27(BSC)		0.050(BSC)		
L	0.400	1.270	0.016	0.050	
θ	0°	8°	0°	8°	

## SOT23-5



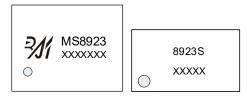


	Dimensions i	n Millimeters	Dimensions in Inches		
Symbol	Min	Max	Min	Max	
А	1.050	1.250	0.041	0.049	
A1	0.000	0.100	0.000	0.004	
A2	1.050	1.150	0.041	0.045	
b	0.300	0.500	0.012	0.020	
С	0.100	0.200	0.004	0.008	
D	2.820	3.020	0.111	0.119	
E	1.500	1.700	0.059	0.067	
E1	2.650	2.950	0.104	0.116	
e	0.950	(BSC)	0.037(BSC)		
e1	1.900	(BSC)	0.075(BSC)		
L	0.300	0.600	0.012	0.024	
θ	0°	8°	0°	8°	



## **MARKING and PACKAGING SPECIFICATIONS**

## 1. Marking Drawing Description



Product Name: MS8923, 8923S Product Code: XXXXX, XXXXXXX

### 2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

## 3. Packaging Specifications

Device	Package	Piece/Reel	Reel/Box	Piece /Box	Box/Carton	Piece/Carton
MS8923	SOP8	2500	1	2500	8	20000
MS8923S	SOT23-5	3000	10	30000	4	120000



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### MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

- 1. The operator shall ground through the anti-static wristband.
- 2. The equipment shell must be grounded.
- 3. The tools used in the assembly process must be grounded.
- 4. Must use conductor packaging or anti-static materials packaging or transportation.



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