+3.3V, 150 MHz, 24-Bit LVDS Flat Panel Display Transmitter

PRODUCT DESCRIPTION

The MS90C385B transmitter converts 28 bits TTL data into four-channel LVDS (Low Voltage Differential Signaling). Clock channel is phase-locked and then is in parallel with data channel. At a transmit clock frequency of 150MHz, 24 bits of RGB data and 3 bits of LCD timing and 1 bit control data are transmitted at a rate of 1050Mbps per LVDS data channel. When input clock frequency is 150MHz, the data transmit rate is 525Mbytes/sec. The MS90C385B can be programmed as valid for rising edge or falling edge via R_FB pin. This chip is an ideal product to solve EMI and cable length problems associated with wide bandwidth, high-speed TTL interfaces.

TSSOP56

FEATURES

- Frequency Range: 20-150MHz Clock Signal
- Less Bus reducing Cable Size and Cost
- IO Power Supply Compatible with 1.8V, 3.3V
- Low Power Dissipation Mode
- Support VGA, SVGA, XGA, SXGA
- Support Extend Frequency Spectrum Clock Generation
- Internal Integrated Input Jitter Filter
- 525Megabytes/sec Bandwidth
- Reduced LVDS Swing to reduce EMI (200mV or 345mV Optional)
- PLL without External Structure
- Observe TIA/EIA-644 LVDS Standard

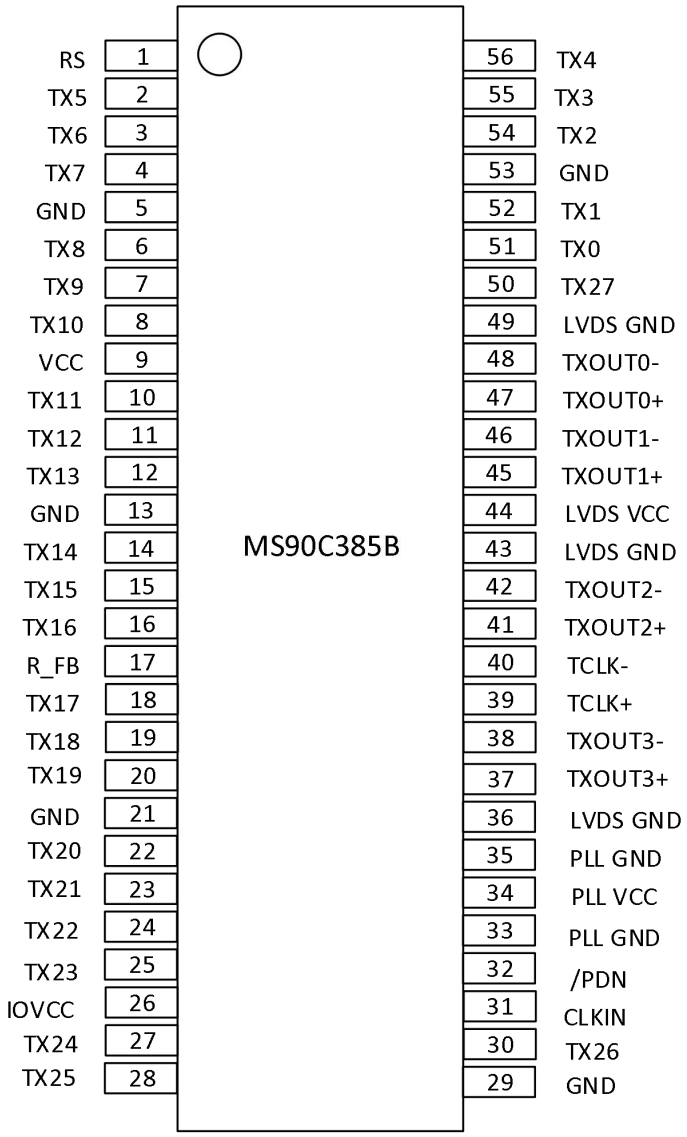
APPLICATIONS

- Monitor Camera
- Desktop/Laptop
- Printer

RODUCT SPECIFICATION

Part Number	Package	Marking
MS90C385B	TSSOP56	MS90C385B

PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
47, 48	TXOUT0+, TXOUT0-	LVDS O	LVDS Differential Data Output
45, 46	TXOUT1+, TXOUT1-	LVDS O	
41, 42	TXOUT2+, TXOUT2-	LVDS O	
37, 38	TXOUT3+, TXOUT3-	LVDS O	
39, 40	TCLK+, TCLK-	LVDS O	LVDS Differential Clock Output
51, 52, 54, 55, 56, 2, 3	TX0~TX6	I	TTL Level Data Input. Include: 8 RED,8 GREEN,8 BLUE, 4 control signals (HSYNC, VXYNC, DE)
4, 6, 7, 8, 10, 11, 12	TX7~TX13	I	
14, 15, 16, 18, 19, 20, 22	TX14~TX20	I	
23, 24, 25, 27, 28, 30, 50	TX21~TX27	I	
31	CLK IN	I	TTL Level Clock Input
32	/PDN	I	TTL Level Input. High: Normal Operation Low: Low Power Dissipation
17	R_FB	I	Select Valid Edge. High: Rising Edge Low: Falling Edge
1	RS	I	LVDS Swing Control (Normal RS=VCC, Small Swing RS=GND)
9	VCC	P	Power Supply for Input Level, 3.3V Typical Value
26	IOVCC	IO P	IO Power Supply, Compatible with 1.8V and 3.3V
5, 13, 21, 29, 53	GND	-	Ground for TTL Level Input
44	LVDS VCC	P	LVDS Power Supply, 3.3V Typical Value
36, 43, 49	LVDS GND	-	Ground for LVDS Ground
34	PLL VCC	P	PLL Power Supply, 3.3V Typical Value
33, 35	PLL GND	-	PLL Ground

ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Condition	Ratings	Unit
Power Supply	VCC		-0.3 ~ 4	V
CMOS/TTL Input Voltage			-0.3 ~ (VCC+0.3)	V
CMOS/TTL Output Voltage			-0.3 ~ (VCC+0.3)	V
LVDS Driver Output Voltage			-0.3 ~ (VCC+0.3)	V
Operating Temperature	T		-40 ~ 100	°C
Maximum Power Dissipation (25°C)			1.4	W
Junction Temperature	T_J		-55 ~ 150	°C
Storage Temperature	T_{stg}		-55 ~ 150	°C
Lead Temperature (no plumbum)	T_{PEAK}		260	°C
Duration Time for Lead Temperature at T_{PEAK} (no plumbum)	T_P		10	s

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all power supplies are 3.3V±10%, V_A=25°C.

Electrical Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input High-level Voltage	V_{IH}		1.5		V_{CC}	V
Input Low-level Voltage	V_{IL}		GND		0.8	V
Input Current	I_{IN}	$0 \le V_{IN} \le V_{CC}$			±10	uA
Low Power Dissipation State Current	I_{PD}	R_FB=V_{CC},V_{IH}=V_{CC}			10	uA

Switch Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Clock Signal Transition Time	T_{TCIT}				5.0	ns
Clock Cycle	T_{TCP}		11.76	T	50	ns
Clock High-level Duration	T_{TCH}		0.35T	0.5T	0.65T	ns
Clock Low-level Duration	T_{TCL}		0.35T	0.5T	0.65T	ns
TTL Data Setup Time	T_{TS}		2.5			ns
TTL Data Hold Time	T_{TH}		0			ns
LVDS Signal Conversion Time	T_{LVT}			0.6		ns
Clock Input to Differential Clock Signal Delay	T_{TCD}			2T/7+2.3		ns
Output Data Bit 0	T_{TDP1}	150MHz	-0.2	0	+0.2	ns
Output Data Bit 1	T_{TDP0}			0.95		ns
Output Data Bit 2	T_{TDP6}			1.90		ns
Output Data Bit 3	T_{TDP5}			2.86		ns
Output Data Bit 4	T_{TDP4}			3.81		ns
Output Data Bit 5	T_{TDP3}			4.76		ns
Output Data Bit 6	T_{TDP2}			5.71		ns
Output Data Bit 0	T_{TDP1}	100MHz	-0.2	0	+0.2	ns
Output Data Bit 1	T_{TDP0}			1.43		ns
Output Data Bit 2	T_{TDP6}			2.86		ns
Output Data Bit 3	T_{TDP5}			4.29		ns
Output Data Bit 4	T_{TDP4}			5.71		ns
Output Data Bit 5	T_{TDP3}			7.14		ns
Output Data Bit 6	T_{TDP2}			8.47		ns

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output Data Bit 0	T_{TDP1}	85MHz	-0.2	0	+0.2	ns
Output Data Bit 1	T_{TDP0}			1.68		ns
Output Data Bit 2	T_{TDP6}			3.36		ns
Output Data Bit 3	T_{TDP5}			5.04		ns
Output Data Bit 4	T_{TDP4}			6.72		ns
Output Data Bit 5	T_{TDP3}			8.40		ns
Output Data Bit 6	T_{TDP2}			10.08		ns
Output Data Bit 0	T_{TDP1}	50MHz	-0.2	0	+0.2	ns
Output Data Bit 1	T_{TDP0}			2.86		ns
Output Data Bit 2	T_{TDP6}			5.71		ns
Output Data Bit 3	T_{TDP5}			8.57		ns
Output Data Bit 4	T_{TDP4}			11.42		ns
Output Data Bit 5	T_{TDP3}			14.28		ns
Output Data Bit 6	T_{TDP2}			17.14		ns
Output Data Bit 0	T_{TDP1}	35MHz	-0.2	0	+0.2	ns
Output Data Bit 1	T_{TDP0}			4.08		ns
Output Data Bit 2	T_{TDP6}			8.16		ns
Output Data Bit 3	T_{TDP5}			12.24		ns
Output Data Bit 4	T_{TDP4}			16.33		ns
Output Data Bit 5	T_{TDP3}			20.41		ns
Output Data Bit 6	T_{TDP2}			24.49		ns
Output Data Bit 0	T_{TDP1}	20MHz	-0.2	0	+0.2	ns
Output Data Bit 1	T_{TDP0}			7.14		ns
Output Data Bit 2	T_{TDP6}			14.28		ns
Output Data Bit 3	T_{TDP5}			21.42		ns
Output Data Bit 4	T_{TDP4}			28.57		ns
Output Data Bit 5	T_{TDP3}			35.71		ns
Output Data Bit 6	T_{TDP2}			42.86		ns
PLL Set Time	T_{TPLLS}		-	-	10	ms

DC Characteristics

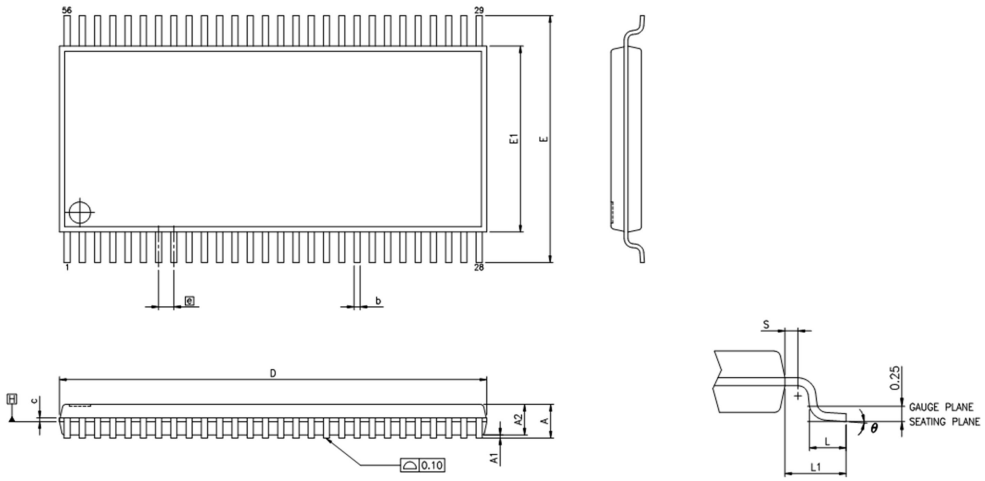
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Differential Output Voltage (RS=VCC)	V_{OD}	RL=100Ω	250	345	450	mV
Differential Output Voltage (RS=GND)			100	200	300	
Change in Differential Output Voltage	ΔV_{OD}				35	mV
Common-mode Output Voltage (RS=VCC)	V_{OC}		1.125	1.25	1.375	V
Common-mode Output Voltage (RS=GND)				1.20		
Change in Common-mode Output Voltage	ΔV_{OC}				35	mV
Tri-state Output Current	I_{OZ}	/PDN=0V, VOUT=0 or VCC			±10	uA

Power Supply Current

Parameter	Symbol	Condition	Typ	Max	Unit
Supply Current 16 Grayscale	I_{CCTG}	f=20MHz	21		mA
		f=35MHz	27		mA
		f=50MHz	29		mA
		f=85MHz	31		mA
		f=100MHz	34		mA
		f=150MHz	37		mA
Shutdown Current	I_{CCTP}	/PDN=0V	21		uA

PACKAGE OUTLINE DIMENSIONS

TSSOP56



Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.17	-	0.27
c	0.09	-	0.20
D	13.90	14.00	14.10
E1	6.00	6.10	6.20
E	8.10BSC		
e	0.50BSC		
L1	1.00REF		
L	0.45	0.60	0.75
S	0.20	-	-
θ	0°	-	8°

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description

Product Name : MS90C385B

Product Code : XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Reel	Reel/Box	Piece /Box	Box/Carton	Piece/Carton
MS90C385B	TSSOP56	3000	1	3000	8	24000

STATEMENT

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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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