

High-speed, Low Power Dissipation DAC

PRODUCT DESCRIPTION

The MS9708/MS9710/MS9714 is a 8-Bit/10-Bit/14-Bit high-speed and low power dissipation DAC. When sample rate reaches 125MSPS, the MS9708/MS9710/MS9714 can also provide perfect AC and DC characteristics.

The normal operating voltage ranges +2.7V to +5.5V. The feature of low power dissipation can make it suitable for portable and low power dissipation products. By decreasing full-scale current output, power dissipation can be reduced to 45mW without affecting performance. In addition, in sleep mode, power dissipation can be reduced to about 20mW.

The MS9708/MS9710/MS9714 combines a segmented current source architecture with specialized switch technique, in order to reduce spurious components and improve dynamic characteristics. Edge-triggered input latch and temperature compensated bandgap reference are integrated together so as to get a complete monolithic DAC solution. Full-scale current output is 20mA and output impedance is more than 100kΩ.

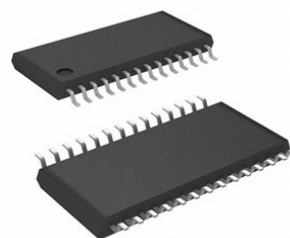
Complementary current output provides single-end or differential applications. Current output terminal can be connected with two output resistors, achieving two complementary, single-ended voltage outputs. The defaulted output voltage is 1.25 V.

The MS9708/MS9710/MS9714 includes a 1.2V internal reference and reference control amplifier, which can set full-scale current by adjusting external resistor. The MS9708/MS9710/MS9714 can also connect with external reference. The output current is from 2mA to 20mA without affecting dynamic characteristics.

The MS9708/MS9710/MS9714 is available in TSSOP28 package.

FEATURES

- 8bit Resolution (MS9708), 10bit Resolution (MS9710), 14bit Resolution (MS9714)
- Update Rate: 125MSPS
- Power Dissipation: 175mW @ 5V to 45mW @ 3V
- Power-down Mode: 20mW @ 5V
- Internal Reference: 1.2V
- Edge-Triggered Latch
- TSSOP28 Package



TSSOP28

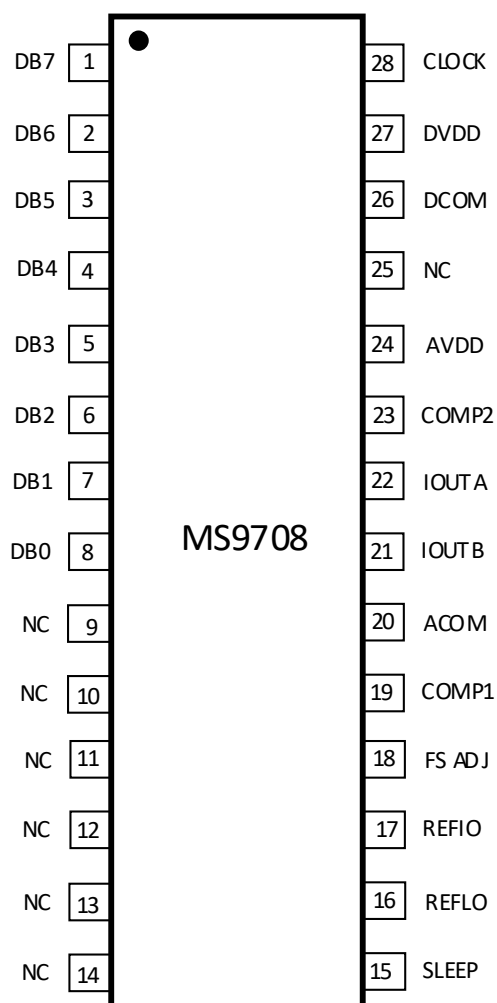
APPLICATIONS

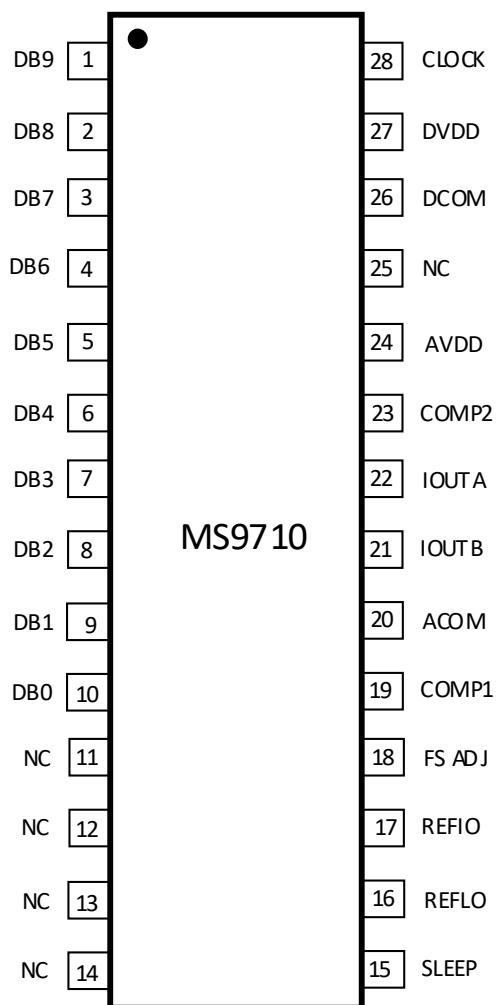
- Communication
- Signal Reconstruction
- Portable Device

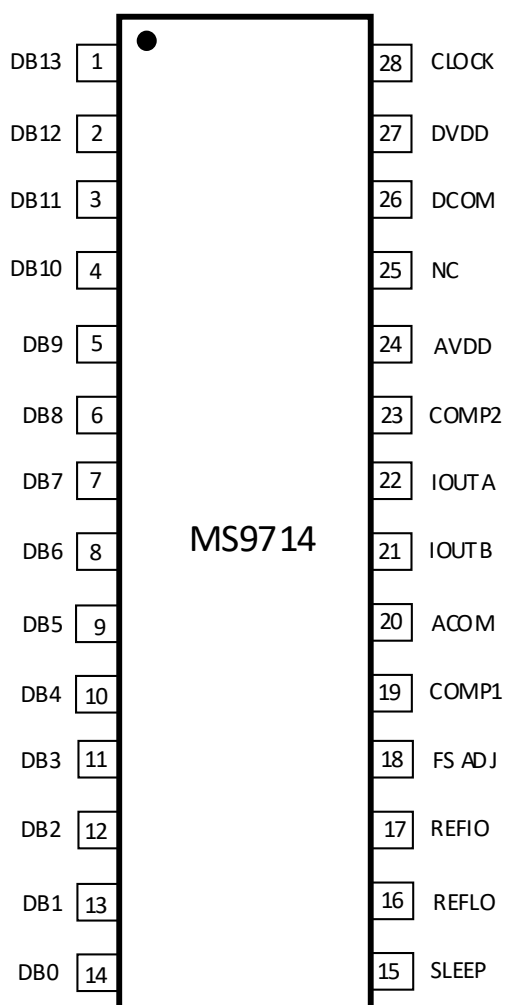
PRODUCT SPECIFICATION

Part Number	Package	Marking
MS9708	TSSOP28	MS9708
MS9710	TSSOP28	MS9710
MS9714	TSSOP28	MS9714

PIN CONFIGURATION



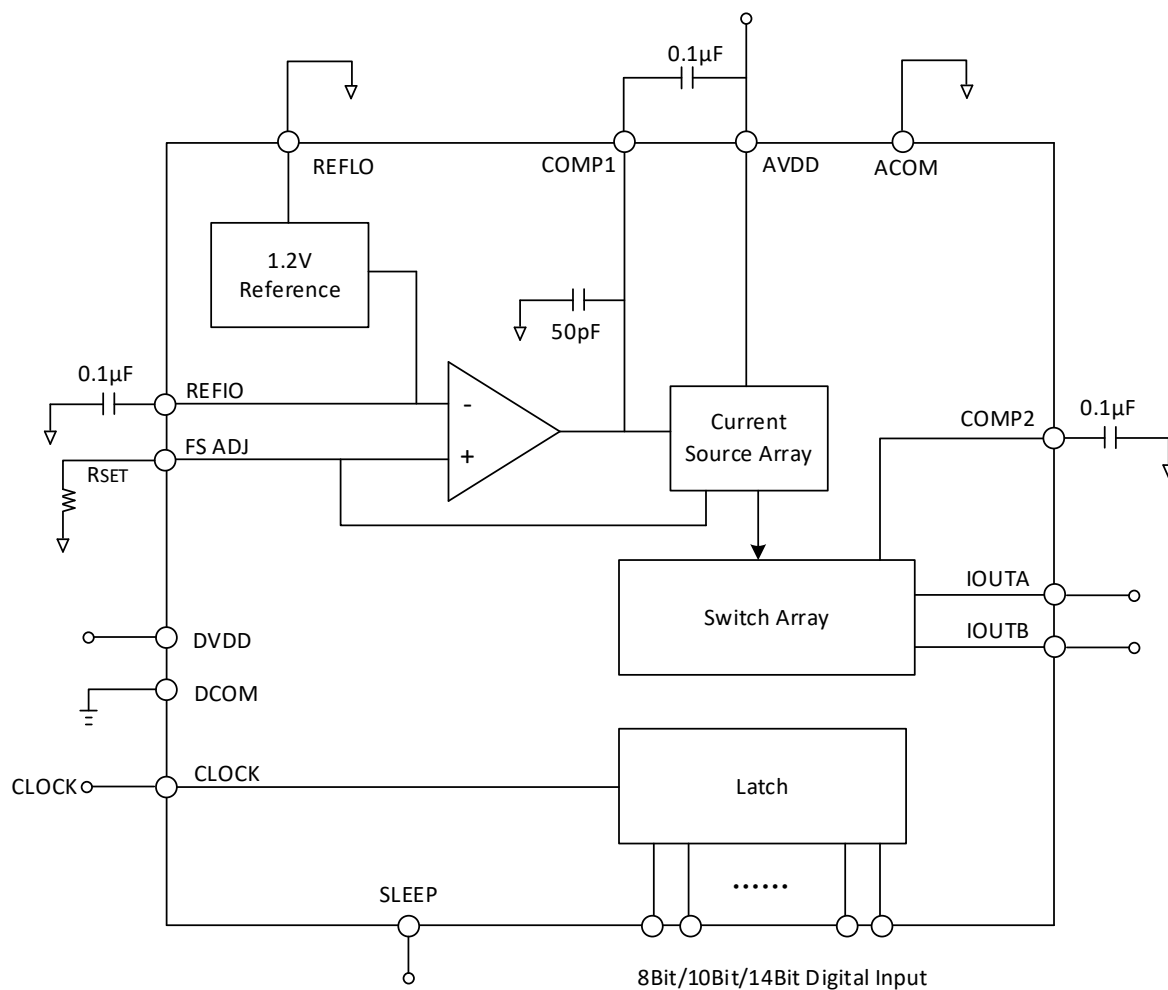




PIN DESCRIPTION

Pin	Name	Description
1-7	DB7-DB0	Digital Data Input (MS9708)
1-10	DB9-DB0	Digital Data Input (MS9710)
1-14	DB13-DB0	Digital Data Input (MS9714)
-	NC	Not Connection
15	SLEEP	Low Power Dissipation Control Input, Activate High. Interior includes valid pull-down circuit, so can float when it is not used.
16	REFLO	When 1.2V internal reference is used, it is connect to reference ground. When it is connected to AVDD, internal reference is disabled.
17	REFIO	Reference Input or Output. It is as reference input when internal reference is inactivate (for example, REFLO is connected to AVDD). It is as 1.2V reference output when internal reference is activate (for example, REFLO is connected to ACOM) and 0.2μF capacitor is externally connected to ACOM at this time.
18	FS ADJ	Full-scale Current Output Adjustment
19	COMP1	Bandwidth/ Noise Reduce Pin. Best effect is get by AVDD connected with 0.1μF capacitor.
20	ACOM	Analog Ground
21	IOUTB	Complementary DAC Current Output. When DB7~DB0/DB9~DB0/DB13~DB0 inputs are all 0, there is the maximum output.
22	IOUTA	DAC Current Output. When DB7~DB0/DB9~DB0/DB13~DB0 inputs are all 1, there is the maximum output.
23	COMP2	Internal Bias Point of Switch Driver Circuit. ACOM is connected with 0.1μF decouple capacitor.
24	AVDD	Analog Power Supply (+2.7V to +5.5V Valid)
26	DCOM	Digital Ground
27	DVDD	Digital Power Supply (+2.7V to +5.5V Valid)
28	CLOCK	Clock Input. Digital latch is valid on the rising edge of CLOCK.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Reference Point	Ratings	Unit
AVDD	ACOM	-0.3 ~ +6.5	V
DVDD	DCOM	-0.3 ~ +6.5	V
ACOM	DCOM	-0.3 ~ +0.3	V
AVDD	DVDD	-6.5 ~ +6.5	V
CLOCK,SLEEP	DCOM	-0.3 ~ DVDD+0.3	V
Digital Input	DCOM	-0.3 ~ DVDD+0.3	V
IOUTA, IOUTB	ACOM	-1.0~ AVDD+0.3	V
COMP1, COMP2	ACOM	-0.3 ~ AVDD+0.3	V
REFIO, FS ADJ	ACOM	-0.3 ~ AVDD+0.3	V
REFLO	ACOM	-0.3 ~ +0.3	
Junction Temperature	T _J	+150	°C
Storage Temperature	T _{stg}	-65 ~ +150	°C
Lead Temperature (10s)		+3000	°C

Thermal Resistor

Parameter	Symbol	参数值	Unit
Junction to Ambient	θ_{JA}	97.9	°C/W
Junction to Package Cover	θ_{JC}	14.0	°C/W

ELECTRICAL CHARACTERISTICS

DC Characteristics

T_{MIN} to T_{MAX}, AVDD=+5V, DVDD=+5V. I_{OUTFS}=20mA, unless other noted.

Parameter	Min	Typ	Max	Unit
Resolution	8/10/14			Bit
DC Precision¹				
INL	-1/2	±1/4	+1/2	LSB
DNL	-1/2	±1/4	+1/2	LSB
Analog Output				
Offset Error	-0.025		+0.025	% of FSR
Gain Error (Without internal reference)	-10	±2	+10	% of FSR
Gain Error (With internal reference)	-10	±1	+10	% of FSR
Full-scale Output Current ²	2.0		20.0	mA
Output Voltage Default Range	-1.0		1.25	V
Output Resistance		100		kΩ
Output Capacitance		5		pF
Reference Output				
Reference Voltage	1.08	1.20	1.32	V
Reference Output Current ³		100		nA
Reference Input				
Input Voltage Range	0.1		1.25	V
Reference Input Resistance		1		MΩ
Small-signal Bandwidth (W/O C _{COMP1}) ⁴		1.4		MHz
Temperature Coefficient				
Offset Value		0		ppm of FSR/°C
Gain Offset (Without internal reference)		±50		ppm of FSR/°C
Gain Offset (With internal reference)		±100		ppm of FSR/°C
Reference Voltage Offset		±50		ppm/°C
Power				
Power Supply				
AVDD ⁵	2.7	5.0	5.5	V
DVDD	2.7	5.0	5.5	V
Analog Input Current (I _{AVDD})		25	30	mA
Digital Input Current (I _{DVDD}) ⁶		3	6	mA
Current in Sleep Mode (I _{AVDD})			8.5	mA
Power Dissipation ⁶ (5V, I _{OUTFS} =20mA)		140	175	mW
Power Dissipation ⁷ (5V, I _{OUTFS} =20mA)		190		mW

Parameter	Min	Typ	Max	Unit
Power Dissipation ⁷ (3V, I _{OUTFS} =2mA)		45		mW
Power Supply Rejection Ratio - AVDD	-0.4		+0.4	% of FSR/V
Power Supply Rejection Ratio - DVDD	-0.025		+0.025	% of FSR/V
Operating Temperature	-40		+85	°C

Note:

1. Measured on IOUTA.
2. Normally, full-scale current is I_{OUTFS}=32×I_{REF}.
3. Use an external buffer amplifier to drive any external load.
4. Reference bandwidth is a function of external capacitance on COMP1 pin.
5. When actual input is less than 3V, output current is recommended to reduce to 12mA or less to maintain optimum performance.
6. Measured when f_{CLOCK}=50 MSPS and f_{OUT}=1.0 MHz.
7. Measured when unbuffered voltage is output into 50Ω R_{LOAD} on IOUTA and IOUTB pins, f_{CLOCK}=100 MSPS and f_{OUT}=40 MHz.

Dynamic Characteristics

T_{MIN} to T_{MAX}, AVDD=+5V, DVDD=+5V, I_{OUTFS}=20mA, Single-ended output, IOUTA, 50Ω doubly terminated, unless other noted.

Parameter	Min	Typ	Max	Unit
Dynamic Characteristic				
Maximum Output Update Frequency (f _{CLOCK})	100	125		MSPS
Output Settling Time (t _{ST}) (to 0.1%) ¹		35		ns
Output Propagation Delay (t _{PD})		1		ns
Glitch Pulse		5		pV-s
Output Rise Time (10% ~ 90%) ¹		2.5		ns
Output Fall Time (10% ~ 90%) ¹		2.5		ns
Output Noise (I _{OUTFS} =20mA)		50		pA/√Hz
Output Noise (I _{OUTFS} =2mA)		30		pA/√Hz
AC Characteristic				
Signal-to-Noise and Distortion Ratio				
f _{CLOCK} =10MSPS; f _{OUT} =1.00MHz		50		dB
f _{CLOCK} =50MSPS; f _{OUT} =1.00MHz		50		dB
f _{CLOCK} =50MSPS; f _{OUT} =12.51MHz		48		dB
f _{CLOCK} =100MSPS; f _{OUT} =5.01MHz		50		dB
f _{CLOCK} =100MSPS; f _{OUT} =25.01MHz		45		dB

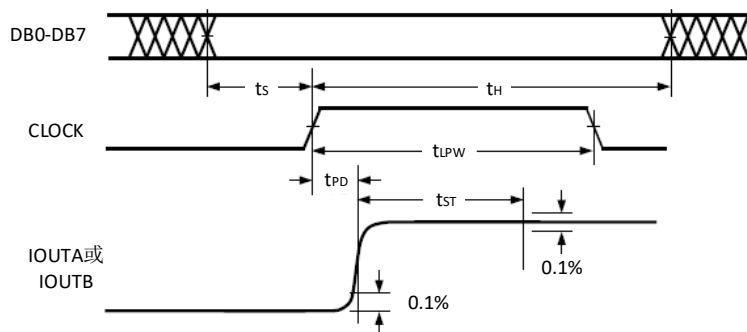
Parameter	Min	Typ	Max	Unit
Total Harmonic Distortion				
$f_{\text{CLOCK}}=10\text{MSPS}; f_{\text{OUT}}=1.00\text{MHz}$		-67		dBc
$f_{\text{CLOCK}}=50\text{MSPS}; f_{\text{OUT}}=1.00\text{MHz}$		-67	-62	dBc
$f_{\text{CLOCK}}=50\text{MSPS}; f_{\text{OUT}}=12.51\text{MHz}$		-59		dBc
$f_{\text{CLOCK}}=100\text{MSPS}; f_{\text{OUT}}=5.01\text{MHz}$		-64		dBc
$f_{\text{CLOCK}}=100\text{MSPS}; f_{\text{OUT}}=25.01\text{MHz}$		-48		dBc
Spurious-Free Dynamic Range				
$f_{\text{CLOCK}}=10\text{MSPS}; f_{\text{OUT}}=1.00\text{MHz}$		68		dBc
$f_{\text{CLOCK}}=50\text{MSPS}; f_{\text{OUT}}=1.00\text{MHz}$	62	68		dBc
$f_{\text{CLOCK}}=50\text{MSPS}; f_{\text{OUT}}=12.51\text{MHz}$		63		dBc
$f_{\text{CLOCK}}=100\text{MSPS}; f_{\text{OUT}}=5.01\text{MHz}$		67		dBc
$f_{\text{CLOCK}}=100\text{MSPS}; f_{\text{OUT}}=25.01\text{MHz}$		50		dBc

Note 1: Measured only when load is 50Ω.

Digital Characteristic

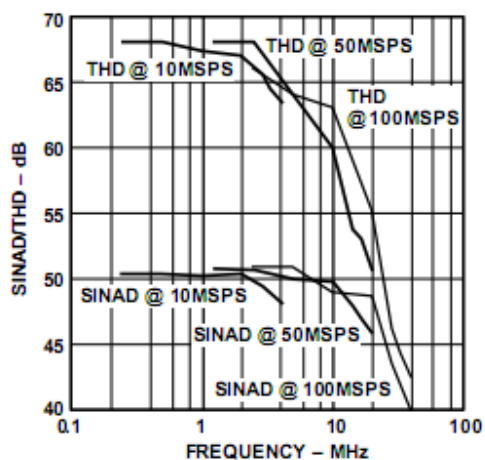
T_{MIN} to T_{MAX} , $\text{AVDD}=+5\text{V}$, $\text{DVDD}=+5\text{V}$, $\text{IOUTFS}=20\text{mA}$, unless other noted.

Parameter	Min	Typ	Max	Unit
Digital Input				
When $\text{DVDD}=+5\text{V}$, Logic "1" Voltage	3.5	5		V
When $\text{DVDD}=+3\text{V}$, Logic "1" Voltage	2.1	3		V
When $\text{DVDD}=+5\text{V}$, Logic "0" Voltage		0	1.3	V
When $\text{DVDD}=+3\text{V}$, Logic "0" Voltage		0	0.9	V
Logic "1" Current	-10		+10	μA
Logic "0" Current	-10		+10	μA
Input Capacitance				
Input Setup Time (t_s)	2.0			ns
Input Hold Time (t_h)	1.5			ns
Latch Pulse Width (t_{LPW})	3.5			ns

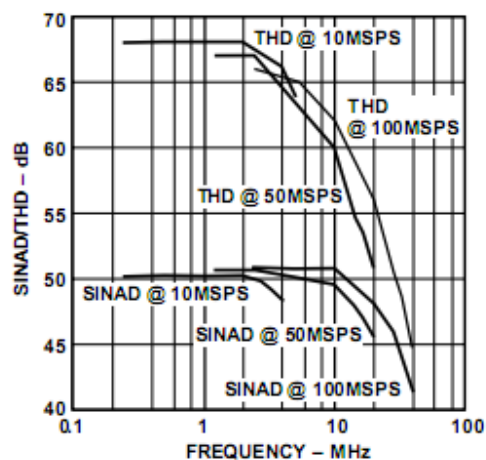


Timing Diagram of the MS9708

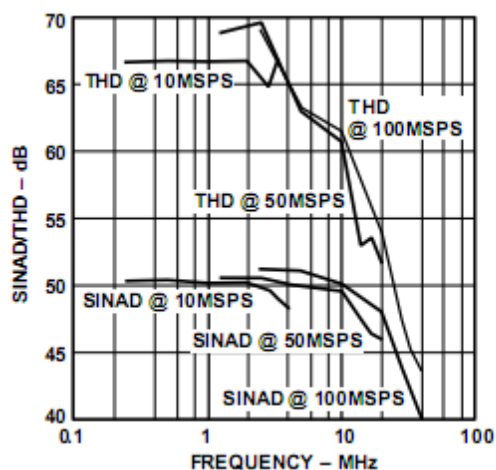
CHARACTERISTIC CURVE



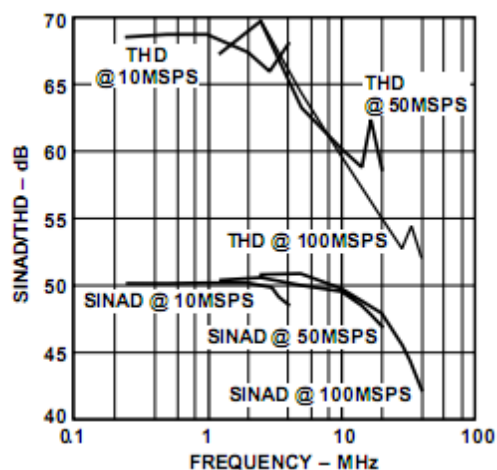
SINAD/THD VS. f_{OUT} (AVDD and DVDD=5.0V)



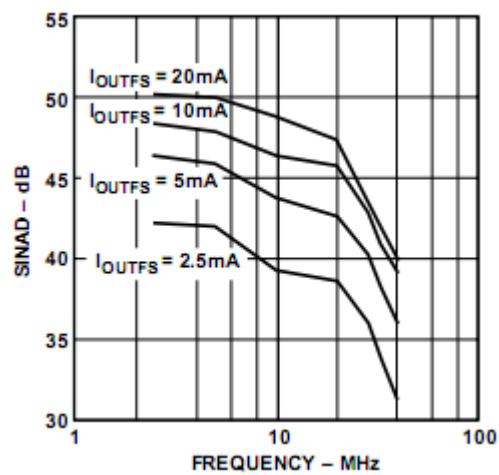
SINAD/THD VS. f_{OUT} (Differential output, AVDD and DVDD=5.0V)



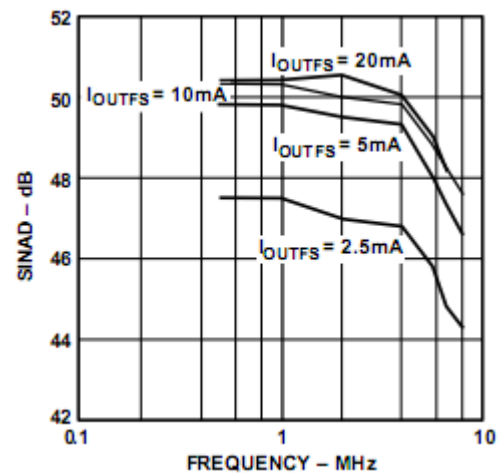
SINAD/THD VS. f_{OUT} (AVDD and DVDD=3.0V)



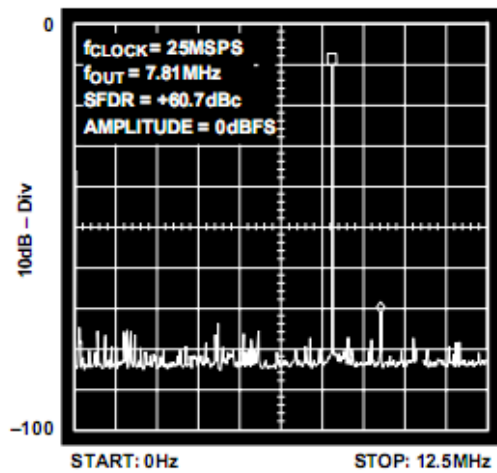
SINAD/THD VS. f_{OUT} (Differential output, AVDD and DVDD=3.0V)



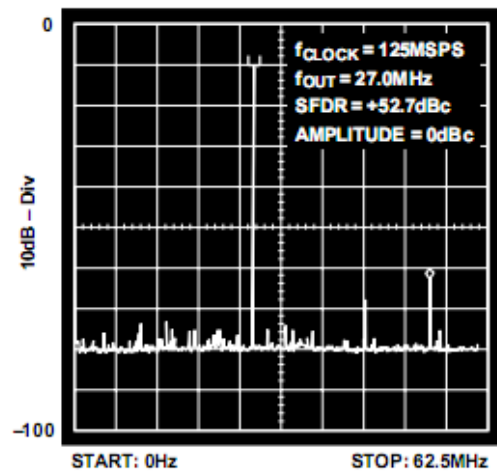
SINAD VS. I_{OUTFS} @ 100MSPS



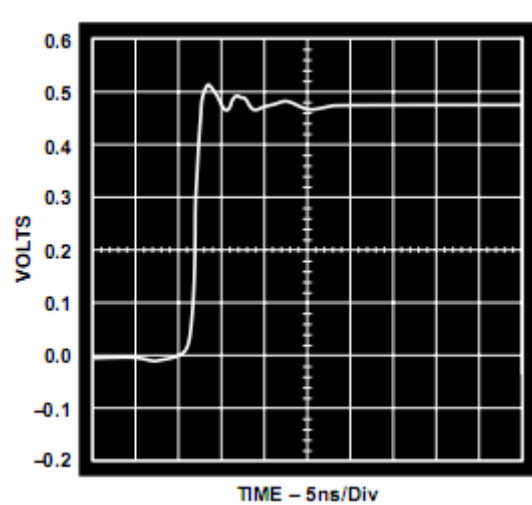
SINAD VS. I_{OUTFS} @ 20MSPS



Single-Tone Spectral Plot @ 25MSPS



Single-Tone Spectral Plot @ 125MSPS



Step Response

FUNCTION DESCRIPTION

The MS9708/MS9710/MS9714 includes a PMOS current source array, which can generate up to 20mA current. The current source array is divided into 31 equal currents that are controlled by the five most significant bits (MSBs). The remaining 3 LSBs control the currents equaling to 7/8th of an MSB current source. Separating the current sources controlled by upper bits and lower bits can remain DAC's high output impedance.

The analog and digital sections of the MS9708/MS9710/MS9714 have differential power supplies (AVDD and DVDD) that can operate from 2.7V to 5.5V. The digital section operates in 125 MSPS clock rate and includes edge-triggered latches and decode unit. The analog section includes the PMOS current source array, the associated differential switches, a 1.2V bandgap voltage reference and a reference control amplifier.

The full-scale current, I_{OUTFS} can be adjusted from 2mA to 20mA by an external resistor, R_{set} . The external resistor is connected with reference control amplifier and voltage reference V_{REFIO} , and generates the reference current I_{REF} . The full-scale current, I_{OUTFS} is thirty-two times the value of I_{REF} .

DAC Transmission Characteristic

The MS9708/MS9710/MS9714 has two complementary outputs, I_{OUTA} and I_{OUTB} . For example, the calculation formula for the MS9708 is as follows:

$$I_{OUTA} = (\text{DAC CODE}/256) \times I_{OUTFS} \quad (1)$$

$$I_{OUTB} = (255 - \text{DAC CODE})/256 \times I_{OUTFS} \quad (2)$$

$$I_{OUTFS} = 32 \times I_{REF} \quad (3)$$

$$I_{REF} = V_{REFIO}/R_{SET} \quad (4)$$

Two current outputs can be directly connected to resistive load. The resistors connected on I_{OUTA} and I_{OUTB} must be matched. The other end of resistor is connected to ground. The resistance is 50Ω or 75Ω.

$$V_{OUTA} = I_{OUTA} \times R_{LOAD} \quad (5)$$

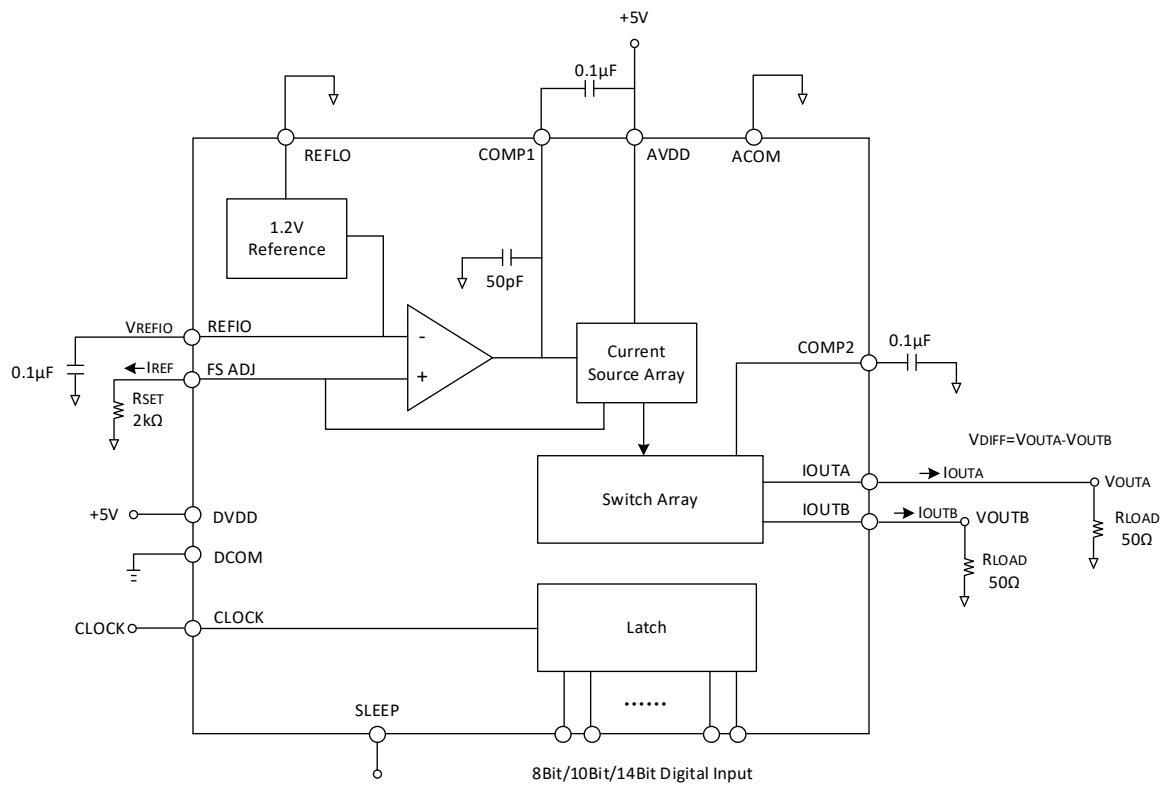
$$V_{OUTB} = I_{OUTB} \times R_{LOAD} \quad (6)$$

The voltage values of V_{OUTA} and V_{OUTB} cannot exceed the allowable maximum, otherwise nonlinearity error would be produced.

The differential value between V_{OUTA} and V_{OUTB} :

$$V_{DIFF} = (I_{OUTA} - I_{OUTB}) \times R_{LOAD} \quad (7)$$

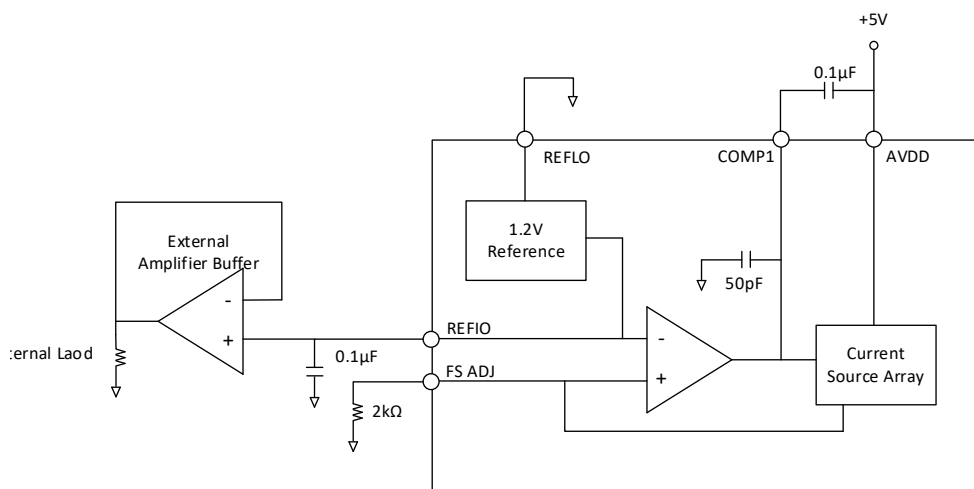
$$V_{DIFF} = \{(2 \text{ DAC CODE} - 255)/256\} \times (32 R_{LOAD}/R_{SET}) \times V_{REFIO} \quad (8)$$



Function Block Diagram

Voltage Reference and Control Amplifier

The MS9708/MS9710/MS9714 includes an internal 1.2V bandgap reference source that can connect with external reference. When REFLO is connected to ground, internal reference is activated and REFIO acts as output pin. When REFLO is connected to power supply, external reference is activated, REFIO acts as input pin and connected to external reference source. When internal reference is used, 0.1μF capacitor needs to be connected on REFIO. REFIO cannot drive any external load. It should be buffered with an external amplifier whose input current should not exceed 100nA if external load is needed.



Internal Reference

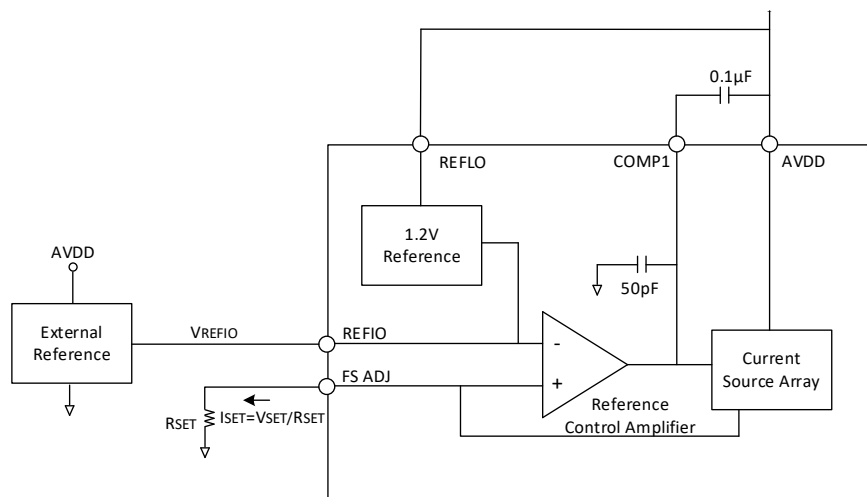
The internal reference can be inactivated by connecting REFLO to AVDD. External reference can be applied to REFIO. The external reference can improve precision. 0.1 μ F capacitor can not be connected when external reference is applied. The input impedance of REFIO is 1M Ω and can minimize the load of external reference.

The MS9708/MS9710/MS9714 includes an internal control amplifier, which can control the DAC's full-scale current, I_{OUTFS} . The amplifier is set as a V-I converter as follows. The current output, I_{REF} is determined by the ratio of V_{REFIO} and an external resistor, R_{SET} .

I_{OUTFS} ranges from 2mA to 20mA and the corresponding I_{REF} range is between 62.5 μ A and 625 μ A. The first benefit is to control power dissipation. Another benefit is to control system gain by 20dB adjustment.

The small-signal input bandwidth is about 1.8MHz for reference control amplifier. It relates to the capacitor connected on COMP1. The capacitor can filter the noise caused by reference amplifier and the recommendation value is 0.1 μ F.

I_{REF} can be changed by changing the value of external reference, whose range is from 0.1V to 1.25V.

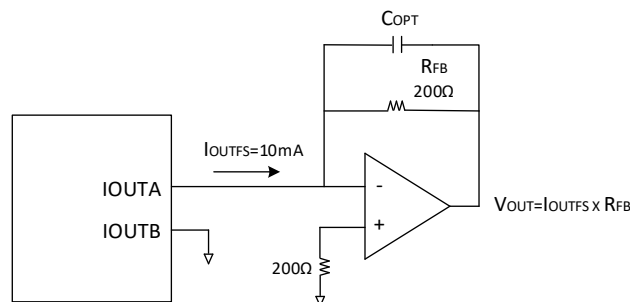


External Reference

Analog Output and Output Setting

The MS9708/MS9710/MS9714 has two complementary current outputs, I_{OUTA} and I_{OUTB} . V_{OUTA} and V_{OUTB} are get by external resistor. Can only use one terminal. The unused terminal can connect with ground or connect with matched resistor.

The output voltage can be converted to negative value by externally connecting operational amplifier, as follows.

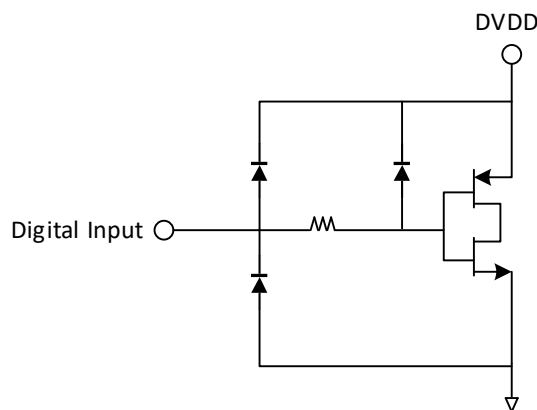


Digital Input

The digital selection of the MS9708/MS9710/MS9714 includes 8bit data input and 1bit clock input. For the MS9708, DB7 is the MSB and DB0 is the LSB. The digital interface is implemented using an edge-triggered latch. The DAC output is latched on the rising edge of the clock. The clock maximum frequency is 125M.

The threshold of digital selection is : $V_{THRESHOLD} = DVDD/2 (\pm 20\%)$.

The input circuit of digital selection is as follows. Include pull-down circuit and chip can operate when input is floating.



The input level of digital selection is from 2.7V to 5.5V. When DVDD level is same as the highest level of digital selection, digital input can be matched with TTL level. 3V to 3.3V DVDD can match with most TTL circuits.

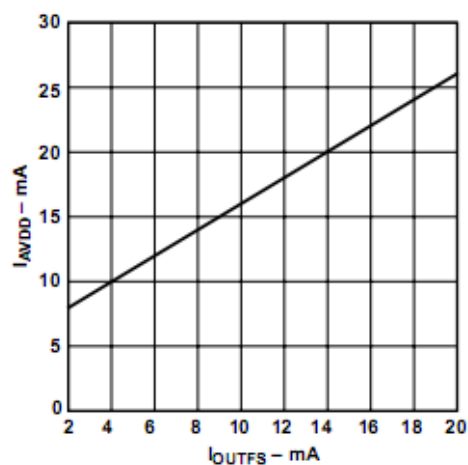
Because the operating frequency is higher, the maximum sample rate is 125MSPS. Must ensure the quality of input digital signal. Settling time and hold time of trigger must be met. Input level also needs to meet requirement.

Sleep Mode

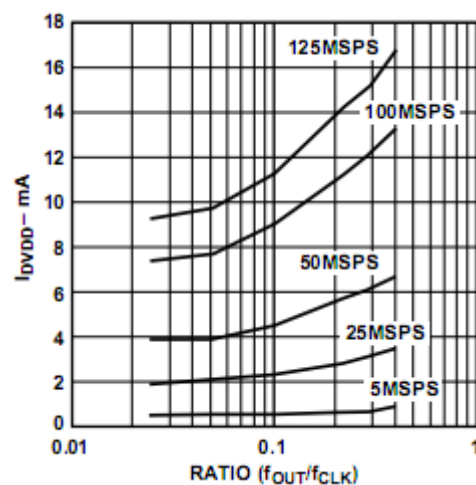
The sleep mode of the MS9708/MS9710/MS9714 can greatly reduce power dissipation. When SLEEP pin is applied to high-level, chip enters into sleep mode and current can drop to less than 8.5mA. SLEEP pin is built in pull-down circuit, which can ensure the normal operation when input is floating. The on and off characteristics of power supply depend on the capacitor on COMP2. The typical value is 0.1μF. The off time is 5μs and restart time is 3.25ms.

Power Dissipation

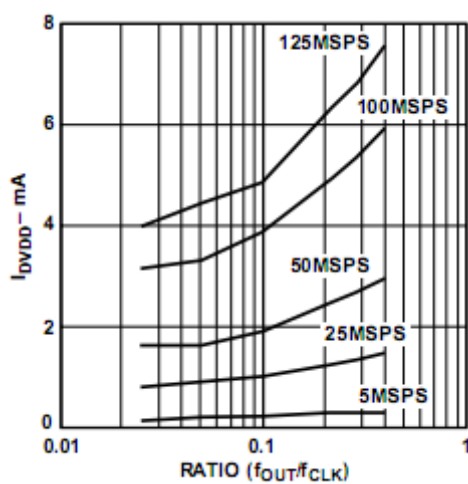
The related factors include: (1) AVDD and DVDD; (2) Full-scale current, I_{OUTFS} ; (3) Clock frequency, f_{CLOCK} ; (4) Input waveform of digital selection. Power dissipation is directly proportional to I_{DVDD} , I_{AVDD} , I_{OUTFS} . In addition, the higher clock frequency, the higher power dissipation.



IAVDD VS. IOUTFS



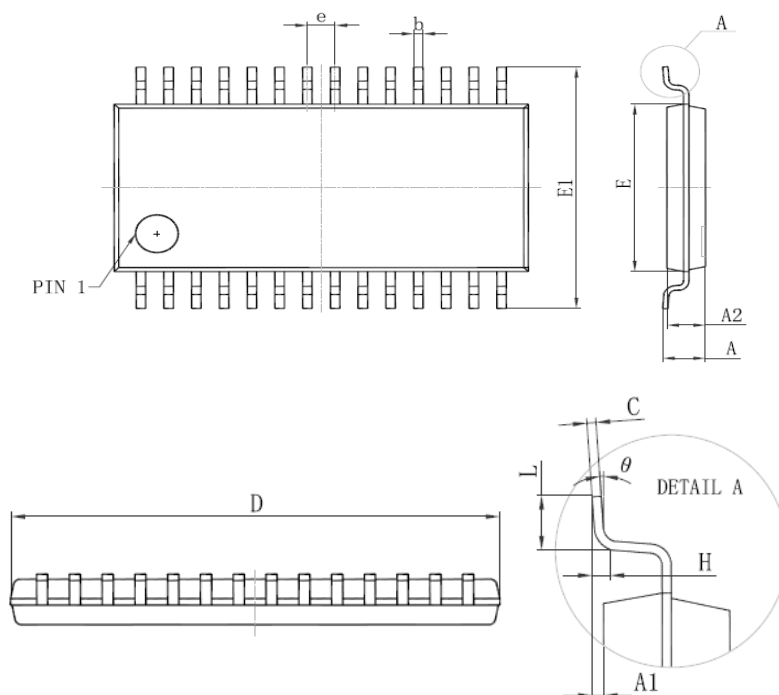
IDVDD VS. Ratio @ DVDD = 5 V



IDVDD VS. Ratio @ DVDD = 3 V

PACKAGE OUTLINE DIMENSIONS

TSSOP28



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
D	9.600	9.800	0.378	0.386
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65BSC		0.026BSC	
L	0.500	0.700	0.020	0.028
H	0.25TYP		0.01TYP	
theta	1°	7°	1°	7°

MARKING and PACKAGE SPECIFICATION

1. Marking Drawing Description



Product Name : MS9708, MS9710, MS9714

Product Code : XXXXXX, XXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece /Box	Box/Carton	Piece/Carton
MS9708	TSSOP28	2000	1	2000	8	16000
MS9710	TSSOP28	2000	1	2000	8	16000
MS9714	TSSOP28	3000	1	3000	8	24000

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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

**MOS CIRCUIT OPERATION PRECAUTIONS**

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.



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