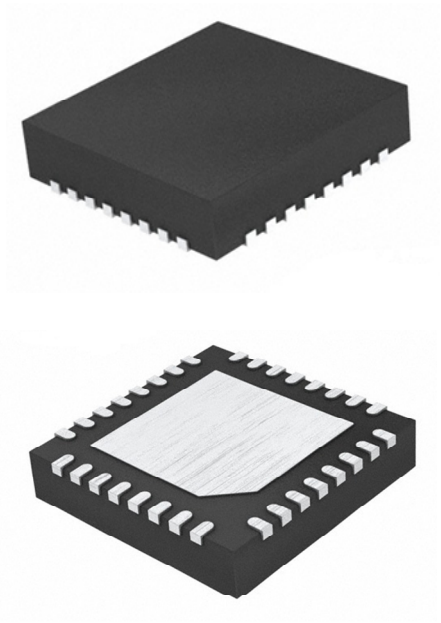
Complete 12-Bit, 40 MHz CCD Signal ADC

GENERAL DESCRIPTION

The MS9945 are complete analog signal processors for CCD applications. They feature a 40 MHz single-channel architecture designed to sample and condition the outputs of interlaced and progressive scan area CCD arrays. The signal chain for the MS9945 consists of a correlated double sampler (CDS), a digitally controlled variable gain amplifier (VGA), and a black level clamp. The MS9945 offers 12-bit ADC resolution.

The internal registers are programmed through a 3-wire serial digital interface. Programmable features include gain adjustment, black level adjustment, input clock polarity, and power-down modes. The MS9945 operate from a single 3 V power supply, typically dissipate 140 mW, and are packaged in space-saving 32-lead QFN packages.



MS9945

FEATURES

- 40 MSPS correlated double sampler (CDS)
- 6 dB to 40 dB 10-bit variable gain amplifier
- Low noise optical black clamp circuit
- Preblanking function
- No missing codes guaranteed
- 3-wire serial digital interface
- 3 V single-supply operation
- QFN32 package

APPLICATIONS

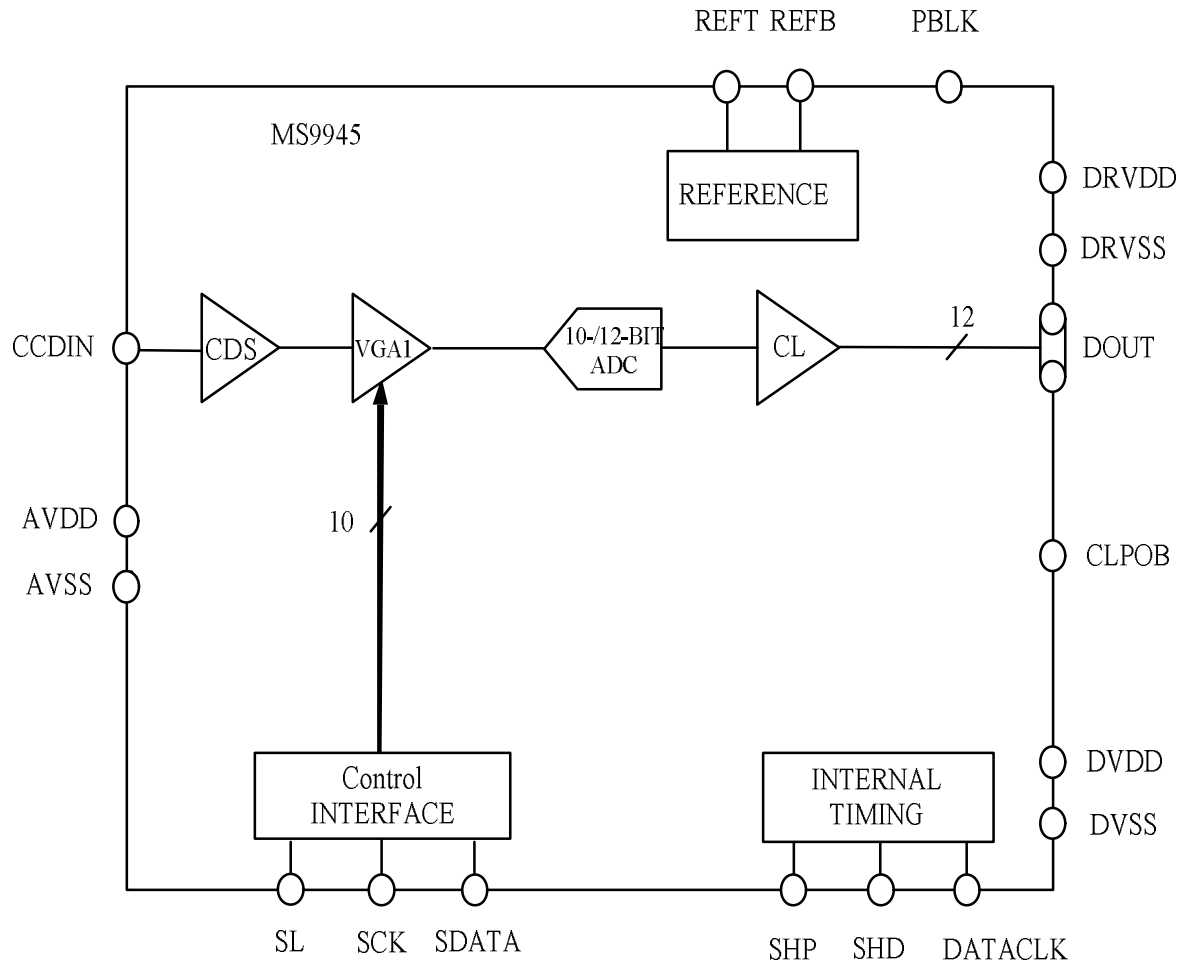
- Digital still cameras
- Digital video camcorders
- PC cameras
- Portable CCD imaging devices
- CCTV cameras

Class

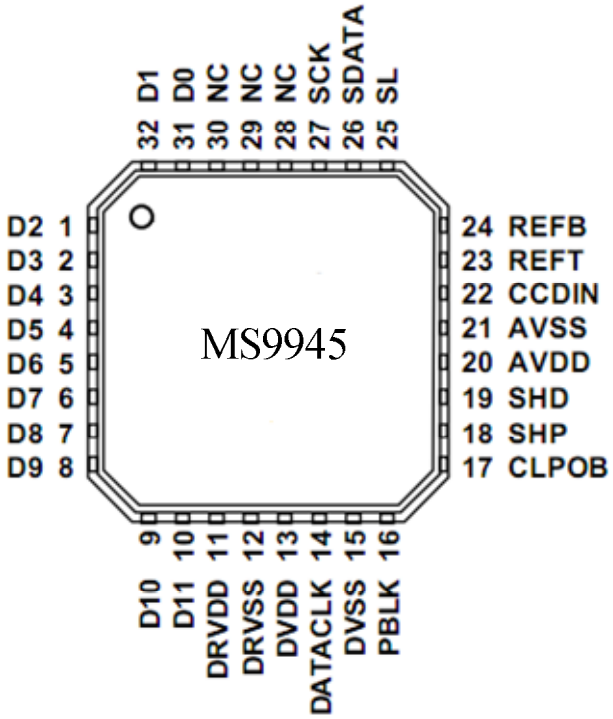
chip	package

MS9945	QFN32

FUNCTIONAL BLOCK DIAGRAM



Pin Configuration



Pin Configuration

Pin Number	Pin Name	I/O	function
MS9945			
1～10	D2～D11	O	Digital Data Outputs.
11	DRVDD	--	Digital Output Driver Supply.
12	DRVSS	--	Digital Output Driver Ground.
13	DVDD	--	Digital Supply.
14	DATACLK	I	Digital Data Output Latch Clock.
15	DVSS	--	Digital Supply Ground.
16	PBLK	I	Preblanking Clock Input.
17	CLPOB	I	Black Level Clamp Clock Input.
18	SHP	I	CDS Sampling Clock for CCD Reference
19	SHD	I	CDS Sampling Clock for CCD Data Level.
20	AVDD	--	Analog Supply.
21	AVSS	--	Analog Ground.
22	CCDIN	I	Analog Input for CCD Signal.
23	REFT	I	A/D Converter Top Reference Voltage

24	REFB	I	A/D Converter Bottom Reference Voltage
25	SL	O	Serial Digital Interface Load Pulse.
26	SDATA	I	Serial Digital Interface Data Input.
27	SCK	I	Serial Digital Interface Clock Input.
28～30	NC	NC	Internally pulled down.
31	D0	O	Digital Data Output.
32	D1	O	Digital Data Output.

ABSOLUTE MAXIMUM RATINGS

Parameter	Range	Unit
AVDD (AVSS)	-0.3～+3.9	V
DVDD (DVSS)	-0.3～+3.9	V
DRVDD (DRVSS)	-0.3～+3.9	V
Digital Outputs (DRVSS)	-0.3～DRVDD+0.3	V
SHP, SHD, DATACLK (DVSS)	-0.3～DVDD+0.3	V
CLPOB, PBLK (DVSS)	-0.3～DVDD+0.3	V
SCK, SL, SDATA DVSS (AVSS)	-0.3～DVDD+0.3	V
REFT, REFB, CCDIN	-0.3～AVDD+0.3	V
Junction Temperature	150	C
Lead Temperature (10 sec)	300	C

SYSTEM SPECIFICATIONS

GENERAL SPECIFICATIONS：TMIN to TMAX, AVDD = DVDD = DRVDD = 3 V, fSAMP = 40 MHz

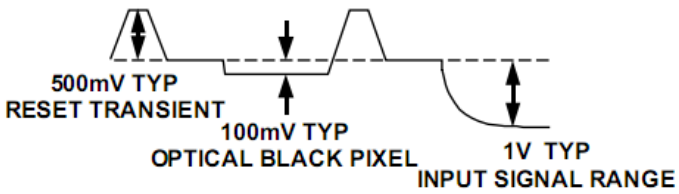
Parameter	Min	Typ	Max	Unit
Operating TEMPERATURE	-20		+85	C
Storage TEMPERATURE	-65		+150	C
Analog, Digital, Digital Driver	2.7		3.6	V
Normal Operation Power		140		mW
Power-Down Mode Power		1.5		mW
MAXIMUM CLOCK RATE	40			MHz

DIGITAL SPECIFICATIONS：DRVDD = DVDD = 2.7 V, CL = 20 pF

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High Level Input Voltage	VIH		2.1			V
Low Level Input Voltage	VIL				0.6	V
High Level Input Current	IIH			10		uA
Low Level Input Current	IIL			10		uA
Input Capacitance	Cin			10		pF
High Level Output Voltage	VIH	IOH = 2 mA	2.2			V
Low Level Output Voltage	VIL	IOL = 2 mA			0.5	V

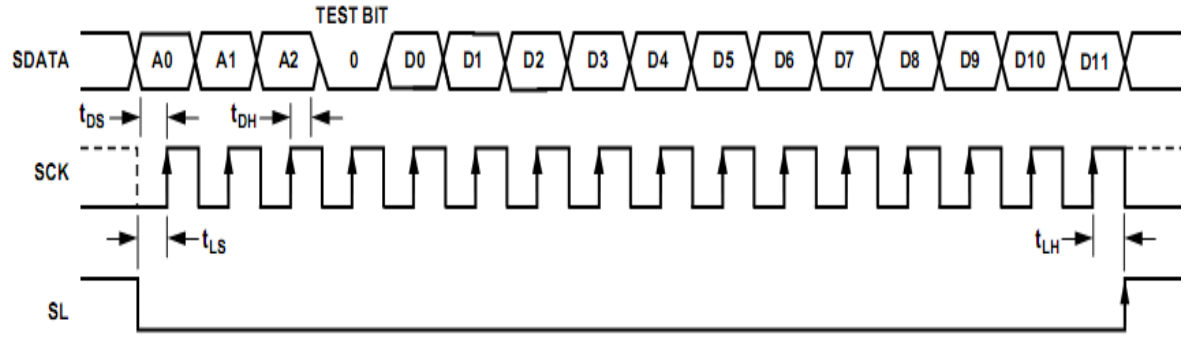
MS9945 Electronic specifications：TMIN to TMAX, AVDD=DVDD=DRVDD=3 V, fSAMP = 40 MHz

Parameter	Conditions	Min	Typ	Max	Unit
（CDS）					
Input Range	See input waveform in footnote		1.0		Vp-p
CCD Reset Transient			500		mV
CCD Black Pixel Amplitude			100		mV
（VGA）					
Gain Control Resolution			1024		Steps
Gain Monotonicity			——		
Gain Range	Minimum Gain		5.3		dB
	Maximum Gain	40	41.5		dB
BLACK LEVEL CLAMP					
Clamp Level Resolution			256		Steps
Clamp Level	Minimum Clamp Level		0		LSB
	Maximum Clamp Level		255		LSB
A/D					
Resolution			12		Bits
Differential Nonlinearity			±0.5		LSB
No Missing Codes			12		Bits
Data Output Coding	Straight binary				
Full-Scale Input Voltage			2.0		V
VOLTAGE REFERENCE					
Reference Top Voltage			2.0		V
Reference Bottom Voltage			1.0		V
SYSTEM PERFORMANCE					
Gain Range	Low Gain (VGA Code = 0)		5.3		dB
	Max Gain (VGA Code = 1023)	40	41.5		dB
Gain Accuracy			±1		dB
Peak Nonlinearity	500 mV Input Signal		0.1		%
Total Output Noise	AC grounded input, 6 dB gain applied.		1.2		LSB rms
Power Supply Rejection	Measured with step change on supply.		40		dB
CCD Input signal characteristics defined as follows:					



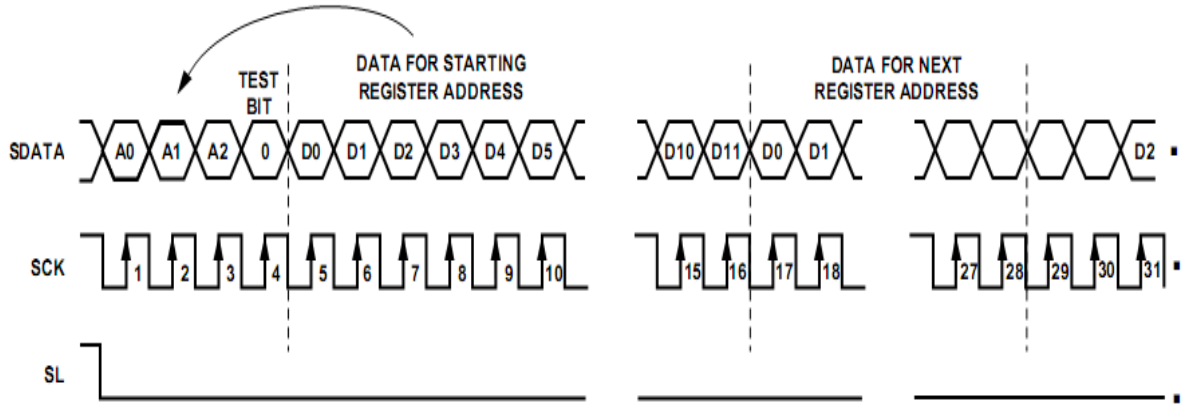
TIMING

1.Serial Write Operation



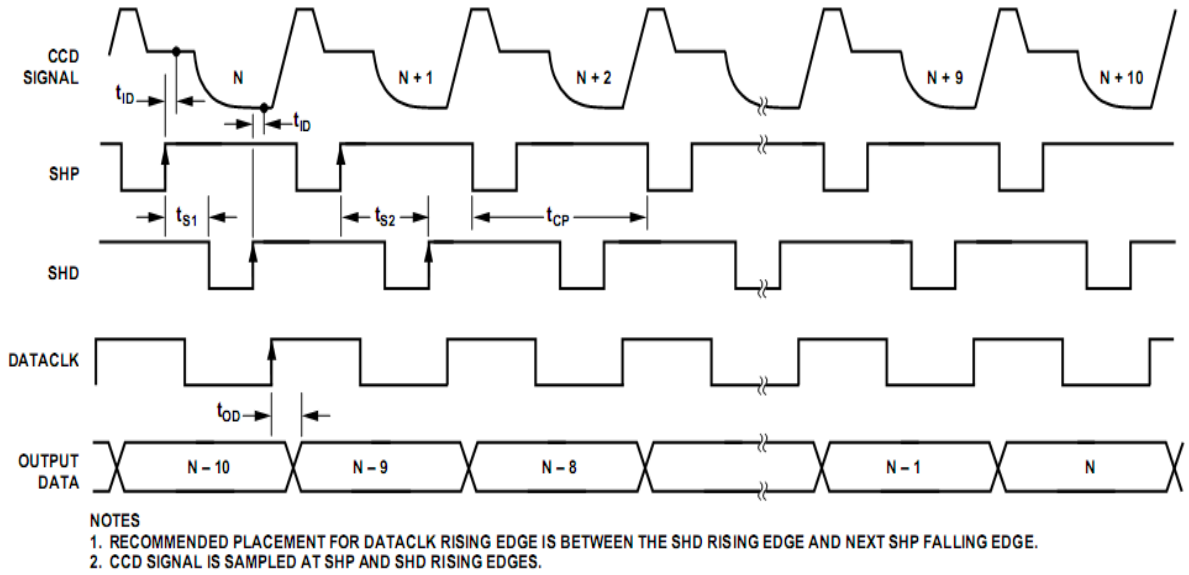
NOTES
1. SDATA BITS ARE INTERNALLY LATCHED ON THE RISING EDGES OF SCK.
2. SYSTEM UPDATE OF LOADED REGISTERS OCCURS ON SL RISING EDGE.
3. ALL 12 DATA BITS D0–D11 MUST BE WRITTEN. IF THE REGISTER CONTAINS FEWER THAN 12 BITS, ZEROS SHOULD BE USED FOR THE UNDEFINED BITS.
4. TEST BIT IS FOR INTERNAL USE ONLY AND MUST BE SET LOW.

2. Continuous Serial Write Operation to All Registers



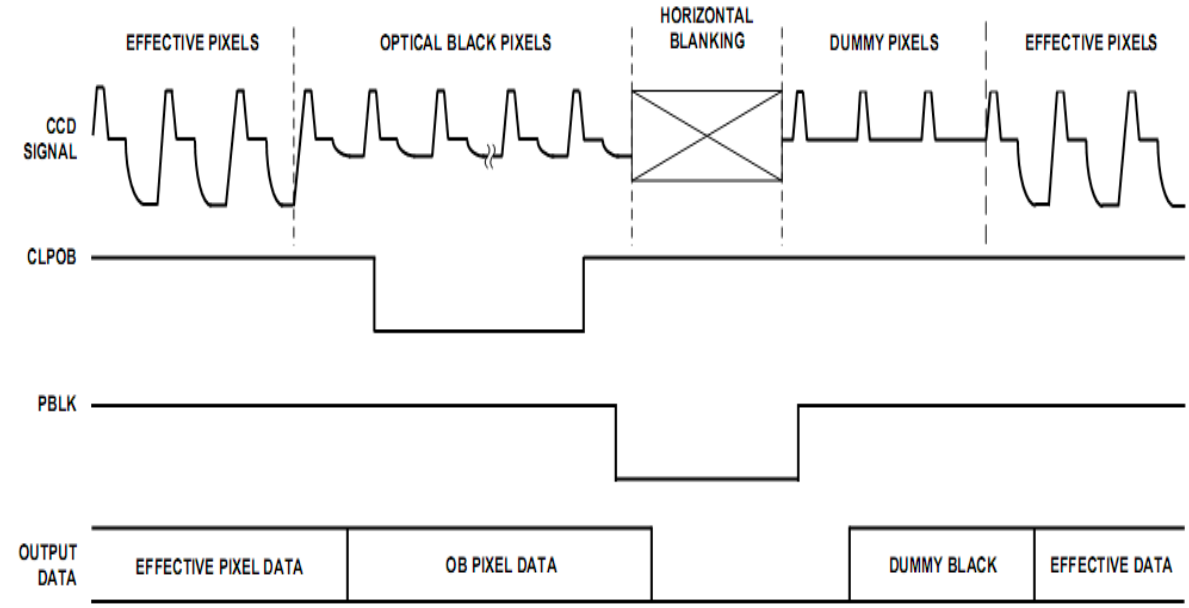
NOTES
1. MULTIPLE SEQUENTIAL REGISTERS MAY BE LOADED CONTINUOUSLY.
2. THE FIRST (LOWEST ADDRESS) REGISTER ADDRESS IS WRITTEN, FOLLOWED BY MULTIPLE 12-BIT DATA-WORDS.
3. THE ADDRESS AUTOMATICALLY INCREMENTS WITH EACH 12-BIT DATA-WORD. (ALL 12 BITS MUST BE WRITTEN.)
4. SL IS HELD LOW UNTIL THE LAST DESIRED REGISTER HAS BEEN LOADED.
5. NEW DATA IS UPDATED AT THE NEXT SL RISING EDGE.

3. CCD Mode Timing



NOTES
1. RECOMMENDED PLACEMENT FOR DATACLK RISING EDGE IS BETWEEN THE SHD RISING EDGE AND NEXT SHP FALLING EDGE.
2. CCD SIGNAL IS SAMPLED AT SHP AND SHD RISING EDGES.

4. Typical CCD Mode Line Clamp Timing

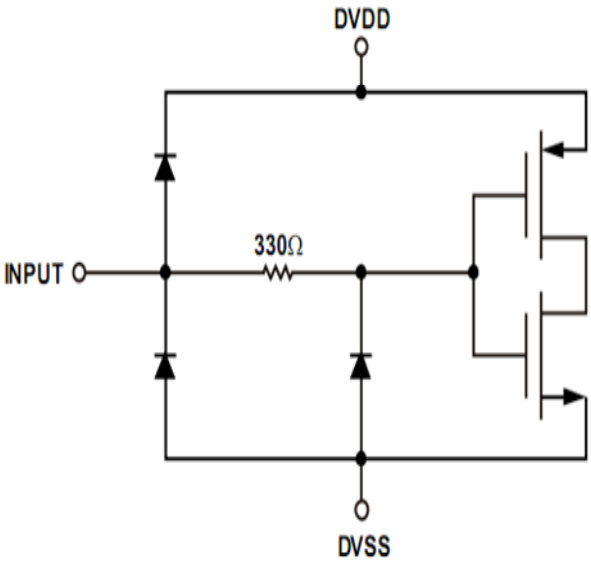


NOTES
1. CLPOB WILL OVERWRITE PBLK. PBLK WILL NOT AFFECT CLAMP OPERATION IF OVERLAPPING WITH CLPOB.
2. PBLK SIGNAL IS OPTIONAL.
3. DIGITAL OUTPUT DATA WILL BE ALL ZEROS DURING PBLK. OUTPUT DATA LATENCY IS NINE DATACLK CYCLES.

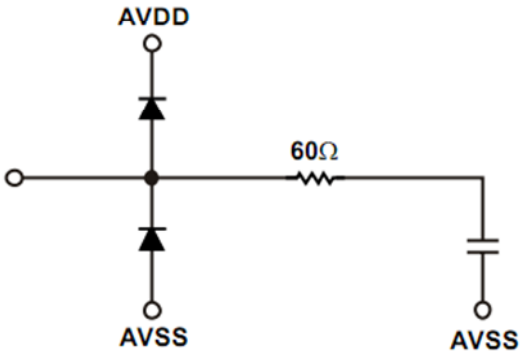
MS9945 timing

Symbol	Parameter	Min	Typ	Max	Unit
SAMPLE CLOCKS					
tCONV	DATACLK, SHP, SHD Clock Period	25			ns
tADC	DATACLK High/Low Pulse Width	10	12.5		ns
tSHP	SHP Pulse Width		6.25		ns
tSHD	SHD Pulse Width		6.25		ns
tCOB	CLPOB Pulse Width1	2	20		Pixels
tS1	SHP Rising Edge to SHD Falling Edge		6.25		ns
tS2	SHP Rising Edge to SHD Rising Edge	11.25	12.5		ns
tID	Internal Clock Delay		3.0		ns
DATA OUTPUTS					
tOD	Output Delay		9.5		ns
	Pipeline Delay		10		Cycles
SERIAL INTERFACE					
fSCLK	Maximum SCK Frequency	10			MHz
tLS	SL to SCK Setup Time	10			ns
tLH	SCK to SL Hold Time	10			ns
tDS	SDATA Valid to SCK Rising Edge Setup	10			ns
tDH	SCK Falling Edge to SDATA Valid Hold	10			ns

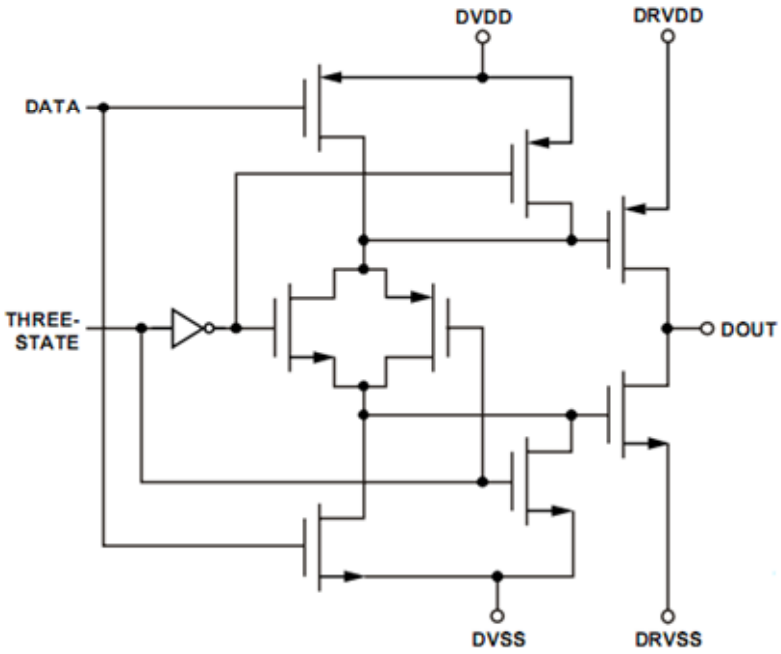
2、EQUIVALENT INPUT CIRCUITS



Digital Inputs

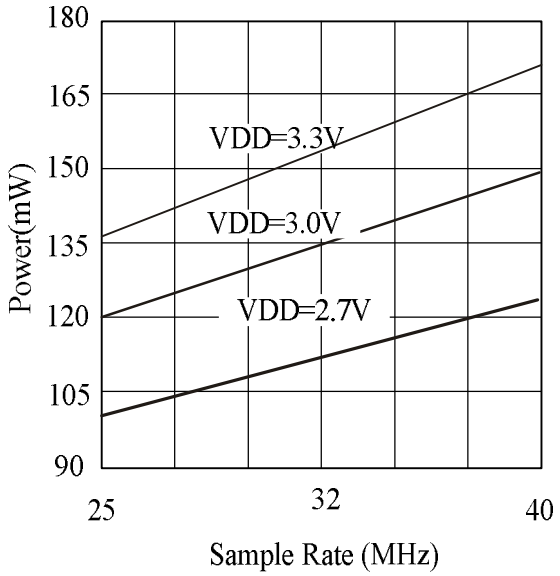


CCDIN (Pin 22)

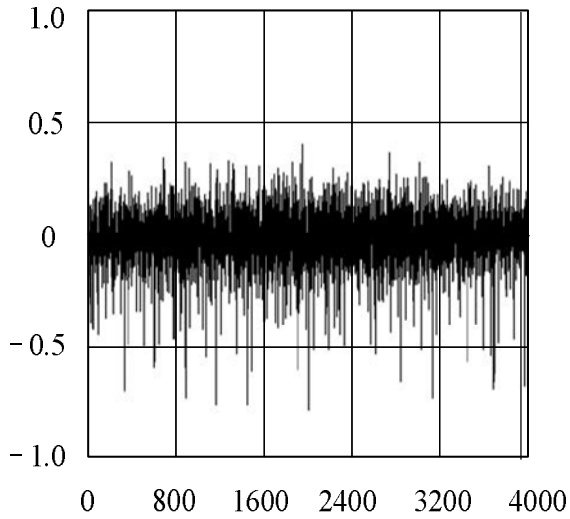


Data Outputs

3、TYPICAL PERFORMANCE CHARACTERISTICS

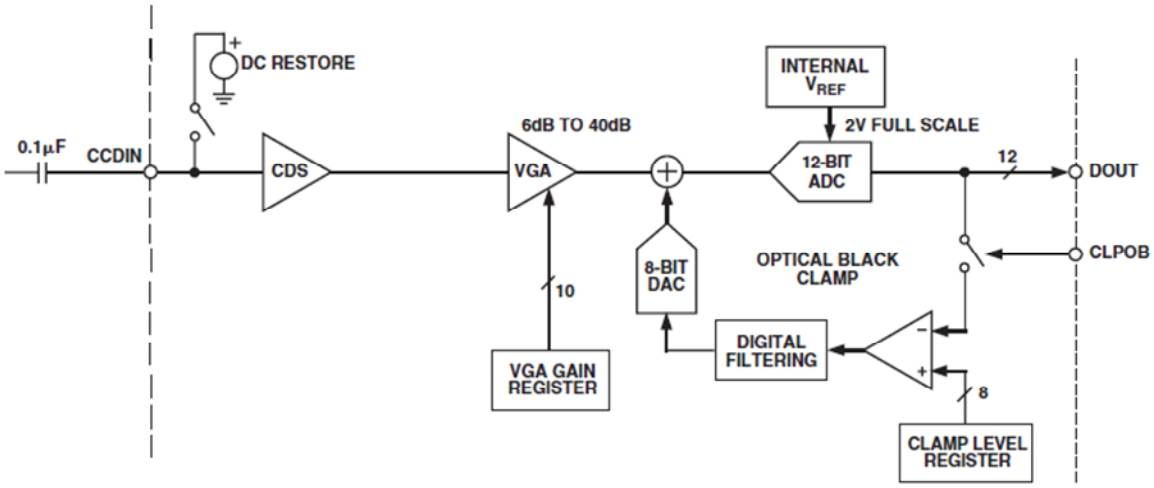


Power vs. Sample Rate



MS9945 Typical DNL Performance

4、CIRCUIT DESCRIPTION AND OPERATION



CCD Mode Block Diagram

4.1 DC RESTORE

To reduce the large dc offset of the CCD output signal, a dc restore circuit is used with an external 0.1 µF series coupling capacitor. This restores the dc level of the CCD signal to approximately 1.5 V, which is compatible with the 3 V single supply of the MS9945.

4.2 CORRELATED DOUBLE SAMPLER

The CDS circuit samples each CCD pixel twice to extract video information and reject low frequency noise. The timing shown in Figure illustrates how the two CDS clocks, SHP and SHD, are used, respectively, to sample the reference level and data level of the CCD signal. The CCD signal is sampled on the rising edges of SHP and SHD. Placement of these two clock signals is critical for achieving the best performance from the CCD. An internal SHP/SHD delay (tID) of 3 ns is caused by internal propagation delays.

4.3 OPTICAL BLACK CLAMP

The optical black clamp loop is used to remove residual offsets in the signal chain and to track low frequency variations in the CCD's black level. During the optical black (shielded) pixel interval on each line, the ADC output is compared with the fixed black level reference selected by the user in the clamp level register. The resulting error signal is filtered to reduce noise, and the correction value is applied to the ADC input through a D/A converter. Normally, the optical black clamp loop is turned on once per horizontal line, but this loop can be updated more slowly to suit a particular application. If external digital clamping is used during the post processing, the optical black clamping for the MS9945 may be disabled using Bit D3 in the operation register. When the loop is disabled, the clamp level register may still be used to provide programmable offset adjustment. Horizontal timing is shown in Figure 15. The CLPOB pulse should be placed during the CCD's optical black pixels. It is recommended that the CLPOB pulse be used during valid CCD dark pixels. The CLPOB pulse should be a minimum of 20 pixels wide to

minimize clamp noise. Shorter pulse widths may be used, but clamp noise may increase and the loop's ability to track low frequency variations in the black level is reduced.

4.4 A/D CONVERTER

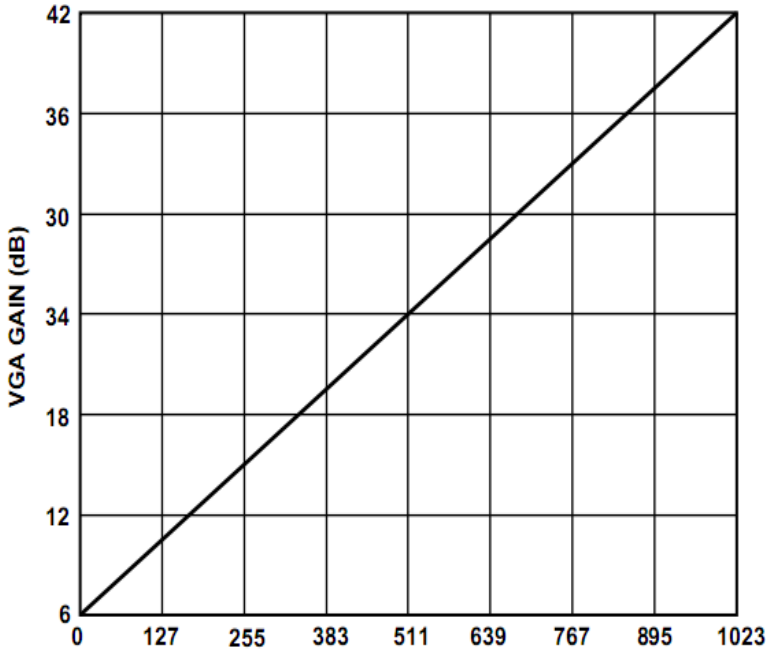
The ADC uses a 2 V input range. Better noise performance results from using a larger ADC full-scale range. The ADC uses a pipelined architecture with a 2 V full-scale input for low noise performance.

4.5 VARIABLE GAIN AMPLIFIER

The VGA stage provides a gain range of 6 dB to 40 dB, programmable with 10-bit resolution through the serial digital interface. The minimum gain of 6 dB is needed to match a 1 V input signal with the ADC full-scale range of 2 V. A plot of the VGA gain curve is shown below.

VGA Gain (dB) = (VGA Code * 0.035 dB) + 5.3 dB

VGA Gain Curve：



VGA Gain Curve

4.6 NTERNAL POWER-ON RESET CIRCUITRY

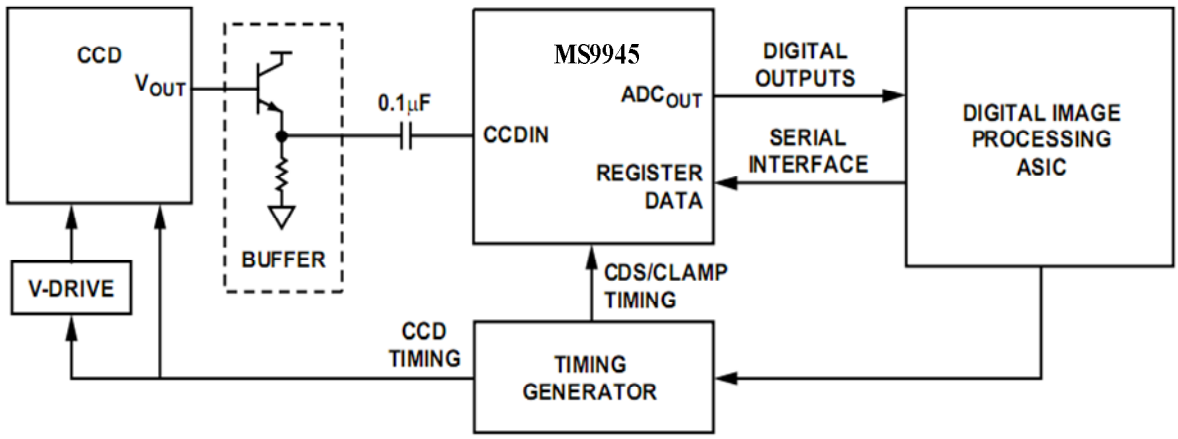
After power-on, the MS9945 automatically reset all internal registers and perform internal calibration procedures. This takes approximately 1 ms to complete. During this time, normal clock signals and serial write operations may occur. However, serial register writes are ignored until the internal reset operation is completed.

5 INTERNAL REGISTER

All register values default to 0x000 at power-up except clamp level, which defaults to 128 decimal (MS9945 = 128 LSB clamp level).

Register Name	Address (A2A1A0)	Data Bits	Function
Operation	000	D0	Software Reset (0 = normal operation, 1 = reset all registers to default).
		D2,D1	Power-Down Modes (00 = normal power, 01 = standby, 10 = total shutdown).
		D3	OB Clamp Disable (0 = clamp on, 1 = clamp off).
		D5,D4	Test Mode. Should always be set to 00.
		D6	PBLK Blanking Level (0 = blank output to zero, 1 = blank to ob clamp level).
		D8,D7	Test Mode 1. Should always be set to 00.
		D11 ～ D9	Test Mode 2. Should always be set to 000.
Control	001	D0	SHP/SHD Input Polarity (0 = active low, 1 = active high).
		D1	DATACLK Input Polarity (0 = active low, 1 = active high).
		D2	CLPOB Input Polarity (0 = active low, 1 = active high).
		D3	PBLK Input Polarity (0 = active low, 1 = active high).
		D4	Three-State Data Outputs (0 = outputs active, 1 = outputs three-stated).
		D5	Data Output Latching (0 = latched by DATACLK, 1 = latch is transparent).
		D6	Data Output Coding (0 = binary output, 1 = gray code output).
		D11 ～ D7	Test Mode. Should always be set to 00000.
Clamp Leve	010	D7～D0	OB Clamp Level (MS9945: 0 = 0 LSB, 255 = 255 LSB).
VGA Gain	011	D9～D0	VGA Gain (0 = 6 dB, 1023 = 40 dB).

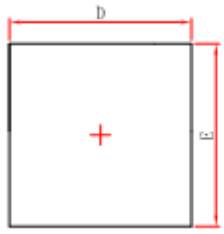
APPLICATIONS INFORMATION



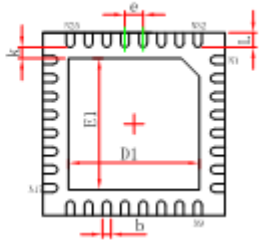
note：

A single ground plane is recommended for the MS9945. This ground plane should be as continuous as possible. This ensures that all analog decoupling capacitors provide the lowest possible impedance path between the power and bypass pins and their respective ground pins. All decoupling capacitors should be located as close as possible to the package pins. A single clean power supply is recommended for the MS9945 and MS9945, but a separate digital driver supply may be used for DRVDD (Pin 11). DRVDD should always be decoupled to DRVSS (Pin 12), which should be connected to the analog ground plane. Advantages of using a separate digital driver supply include using a lower voltage (2.7 V) to match levels with a 2.7 V ASIC, and reducing digital power dissipation and potential noise coupling. If the digital outputs must drive a load larger than 20 pF, buffering is the recommended method to reduce digital code transition noise. Alternatively, placing series resistors close to the digital output pins may also help reduce noise.

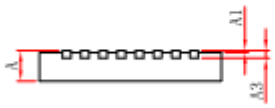
OUTLINE DIMENSIONS



Top View



Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	4.924	5.076	0.194	0.200
E	4.924	5.076	0.194	0.200
D1	3.300	3.500	0.130	0.138
E1	3.300	3.500	0.130	0.138
k	0.200MIN.		0.008MIN.	
b	0.180	0.300	0.007	0.012
e	0.500TYP.		0.020TYP.	
L	0.324	0.476	0.013	0.019