Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0900

Features

- **Broadband, Minimum Ripple Cascadable 50 Ω Gain Block**
- **8.0 ± 0.2 dB Typical Gain Flatness from 0.1 to 4.0 GHz**
- **3 dB Bandwidth:** 0.1 to 6.0 GHz
- **Low VSWR:** ≤ 1.5:1 from 0.1 to 4.0 GHz
- **11.5 dBm Typical P_{1dB} at 1.0 GHz**

Description

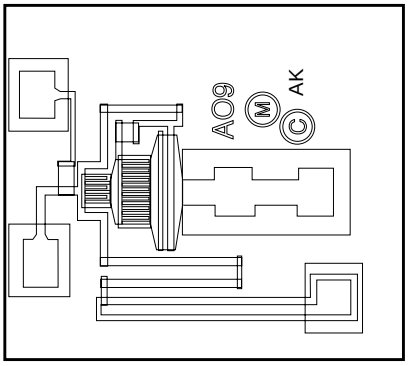
The MSA-0900 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) chip. This MMIC is designed for very wide bandwidth industrial and military applications that require flat gain and low VSWR.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire.

This chip is intended to be used with an external blocking capacitor completing the shunt feedback path (closed loop). Data sheet characterization is given for a 45 pF capacitor. Low frequency performance can be extended by using a larger valued capacitor.[1]

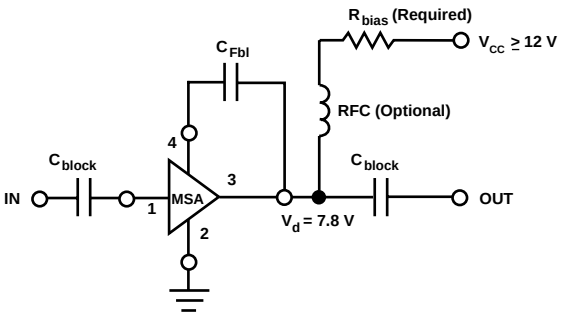
Chip Outline[1]



Note:

1. Refer to the APPLICATIONS section "Silicon MMIC Chip Use" for additional information.

Typical Biasing Configuration



MSA-0900 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	80 mA
Power Dissipation[2,3]	750 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance[2,4]:
$\theta_{jc} = 70°C/W$

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{Mounting\ Surface}$ (T_{MS}) = 25°C.
3. Derate at 14 mW/°C for $T_{Mounting\ Surface} > 148°C$.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods.

Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions[2]: I_d = 35 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.1 GHz	dB		8.0	
ΔG_P	Gain Flatness[3]	f = 0.1 to 4.0 GHz	dB		±0.2	
$f_{3\ dB}$	3 dB Bandwidth[3,4]		GHz		6.0	
VSWR	Input VSWR	f = 1.0 to 4.0 GHz			1.4:1	
	Output VSWR	f = 1.0 to 4.0 GHz			1.5:1	
NF	50 Ω Noise Figure	f = 1.0 GHz f = 4.0 GHz	dB		6.0 6.5	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 1.0 GHz f = 4.0 GHz	dBm		11.5 6.5	
IP_3	Third Order Intercept Point	f = 1.0 GHz	dBm		23.0	
t_D	Group Delay	f = 1.0 GHz	psec		60	
V_d	Device Voltage		V	7.0	7.8	8.6
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–16.0	

Notes:
1. The recommended operating current range for this device is 25 to 45 mA. Typical performance as a function of current is on the following page.
2. RF performance of the chip is determined by packaging and testing 10 devices per wafer.
3. The value is the expected achievable performance for the MSA-0900 used with an external 45 pF capacitor mounted in a 100 mil stripline package.
4. Referenced from 0.1 GHz gain (G_P).

Part Number Ordering Information

Part Number	Devices Per Tray
MSA-0900-GP4	100

MSA-0900 Typical Scattering Parameters[1,2] (Z_O = 50 Ω, T_A = 25°C, I_d = 35 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}		k
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	
0.02	.32	–107	10.8	3.48	151	–13.9	.203	17	.32	–106	0.83
0.05	.22	–143	8.6	2.70	164	–13.6	.209	6	.22	–142	1.09
0.1	.11	–144	8.2	2.57	171	–13.3	.215	3	.11	–142	1.16
0.2	.10	–160	8.1	2.54	172	–13.5	.211	1	.10	–158	1.19
0.4	.10	–171	8.1	2.54	175	–13.4	.215	2	.10	–166	1.18
0.6	.09	–170	8.1	2.55	166	–13.3	.216	1	.10	–166	1.18
0.8	.08	–171	8.2	2.57	162	–13.3	.216	1	.11	–166	1.17
1.0	.08	–170	8.3	2.59	158	–13.1	.220	1	.11	–167	1.15
1.5	.07	–166	8.6	2.68	147	–13.1	.221	1	.14	–172	1.12
2.0	.07	–138	8.9	2.80	136	–12.6	.234	1	.15	–172	1.07
2.5	.08	–131	9.3	2.92	126	–12.6	.236	1	.18	179	1.04
3.0	.12	–119	9.6	3.01	112	–12.0	.250	1	.21	171	0.99
3.5	.17	–125	9.6	3.02	95	–11.8	.256	–1	.22	157	0.97
4.0	.22	–132	9.1	2.86	78	–11.5	.265	–3	.19	144	0.96
4.5	.27	–140	8.4	2.64	63	–11.5	.265	–5	.16	138	0.97
5.0	.32	–149	7.5	2.36	50	–11.4	.268	–6	.12	138	1.00
5.5	.34	–154	6.4	2.09	38	–11.3	.272	–6	.10	162	1.02
6.0	.36	–158	5.3	1.84	29	–11.3	.272	–6	.10	–166	1.07
6.5	.38	–158	4.2	1.62	22	–11.4	.271	–6	.16	–151	1.12
7.0	.39	–157	3.2	1.45	15	–11.5	.267	–6	.23	–147	1.17

Notes:

1. S-parameters are de-embedded from 100 mil BeO package measured data using the package model found in the DEVICE MODELS section.
2. S-parameter data assumes an external 45 pF capacitor. Low fequency performance can be extended using a larger valued capacitor.

Typical Performance, T_A = 25°C

(unless otherwise noted)

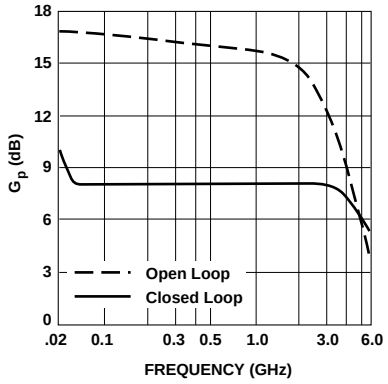


Figure 1. Typical Power Gain vs. Frequency, I_d = 35 mA.

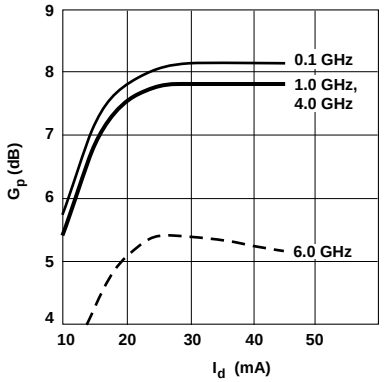


Figure 2. Power Gain vs. Current.

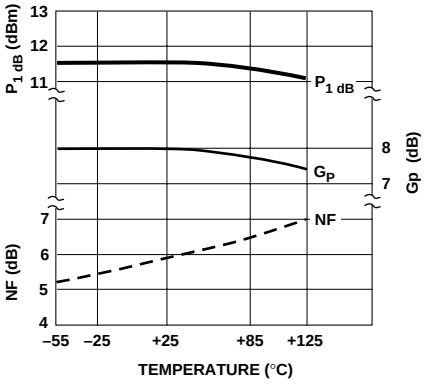


Figure 3. Output Power at 1 dB Gain Compression, Noise Figure and Power Gain vs. Case Temperature, f = 1.0 GHz, I_d = 35 mA.

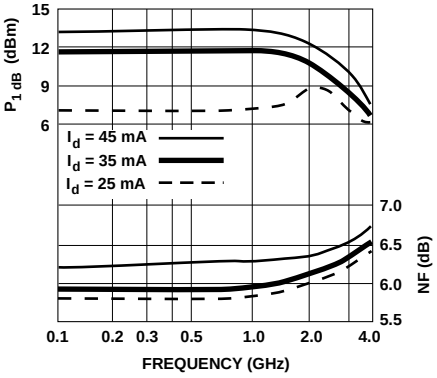
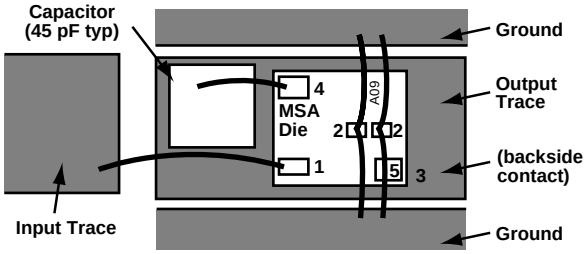


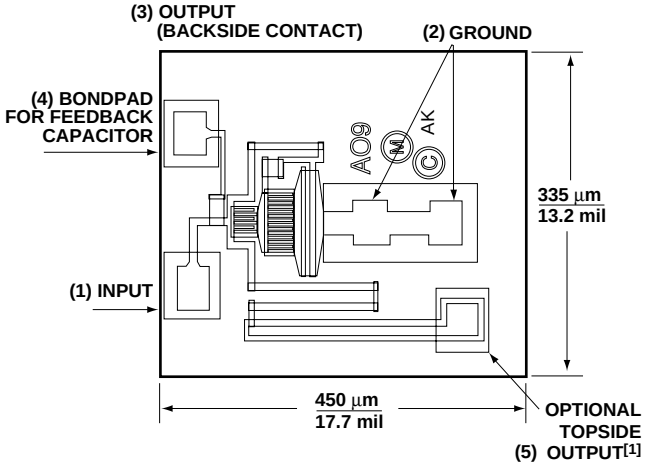
Figure 4. Output Power at 1 dB Gain Compression and Noise Figure vs. Frequency.

MSA-0900 Bonding Diagram



Numbers refer to pin contacts listed on the Chip Outline.

MSA-0900 Chip Dimensions



Unless otherwise specified, tolerances are ±13 μm/±0.5 mils. Chip thickness is 114 μm/4.5 mil. Bond Pads are 41 μm/1.6 mil typical on each side.
Note 1: Output contact is made by die attaching the backside of the die.