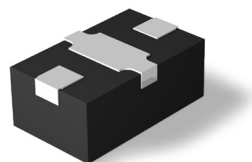


MSAT-P25

PIN Diode Attenuator Shunt Element



(2012)
Plastic Molded DFN

Description

A broadband, High Linearity medium power shunt PIN Attenuator element 1.9 X 1.1 mm DFN package. This device is designed for wireless Telecommunication infrastructure and test instrument applications. It is also suited for other applications in 0.1 ~ 10 GHz range.

Features

- Low Distortion Harmonics at 85 dBc Typical
- Broadband performance, beyond 10 GHz
- Low Insertion loss & high attenuation range, 27 dB

Electrical Specifications, $T_c = +25\text{ }^\circ\text{C}$

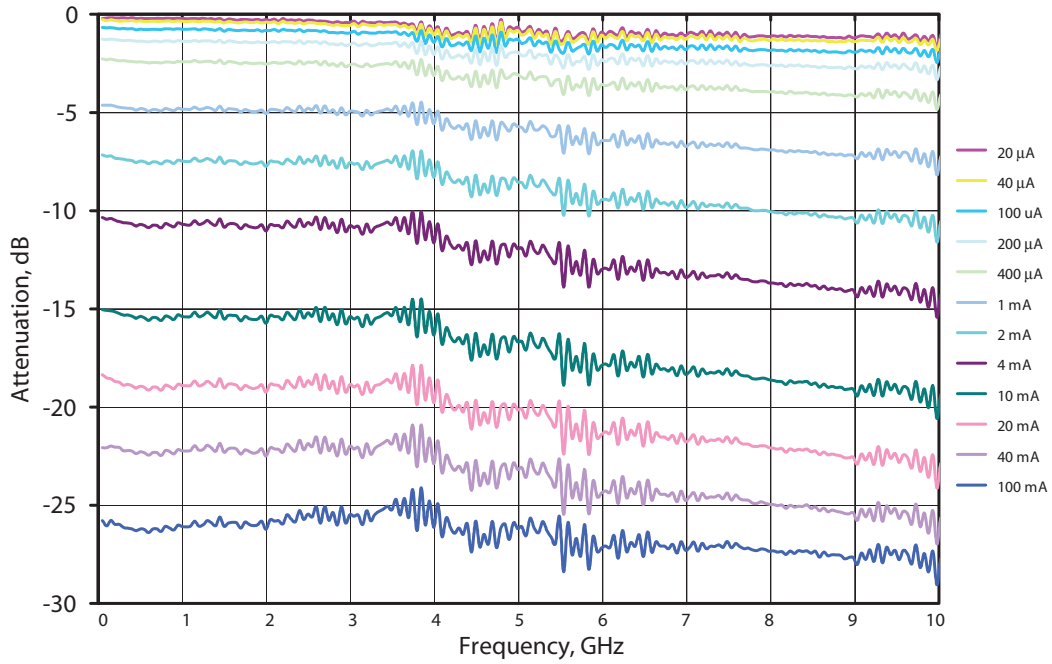
SYMBOL	TEST CONDITIONS			MIN	TYPICAL	MAX	UNITS
V_{BR}	$I_R = 10\text{ }\mu\text{A}$			200	–	–	V
τ	IF = 10 mA	IR = 6 mA	10% / 90%	2000	3000	5000	ns
Rs min	I = 100 mA		F = 500 MHz	–	1.5	2.5	Ω
Rs High	I = 10 μA		F = 500 MHz	1200	2200	3000	Ω
Rs Low	I = 1 mA		F = 500 MHz	20	30	40	Ω
ATTEN	I = 100 mA		F \leq 10.0 GHz	20	30	–	dB

Absolute Maximum Ratings

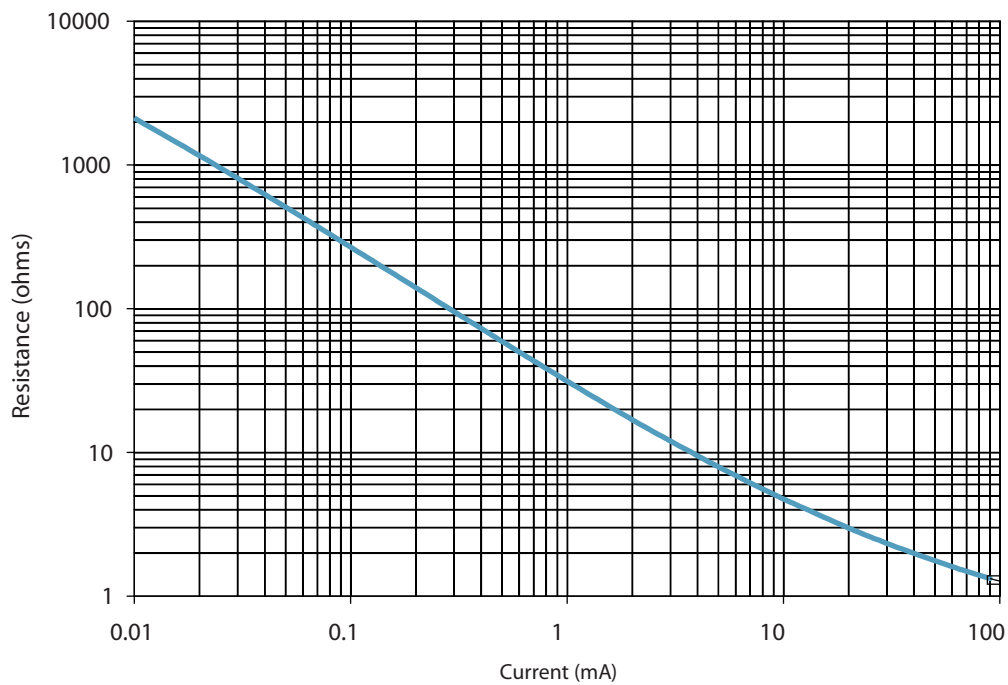
RATING	LIMITS	UNITS
V_R	200	V
I_F	200	mA
θ_{JC}	20	$^\circ\text{C/W}$
T_J	+175	$^\circ\text{C}$
T_{STG}	-65 to +125	$^\circ\text{C}$
T_{SOLDER}	+260 $^\circ\text{C}$ per JEDEC J-STD-20C	



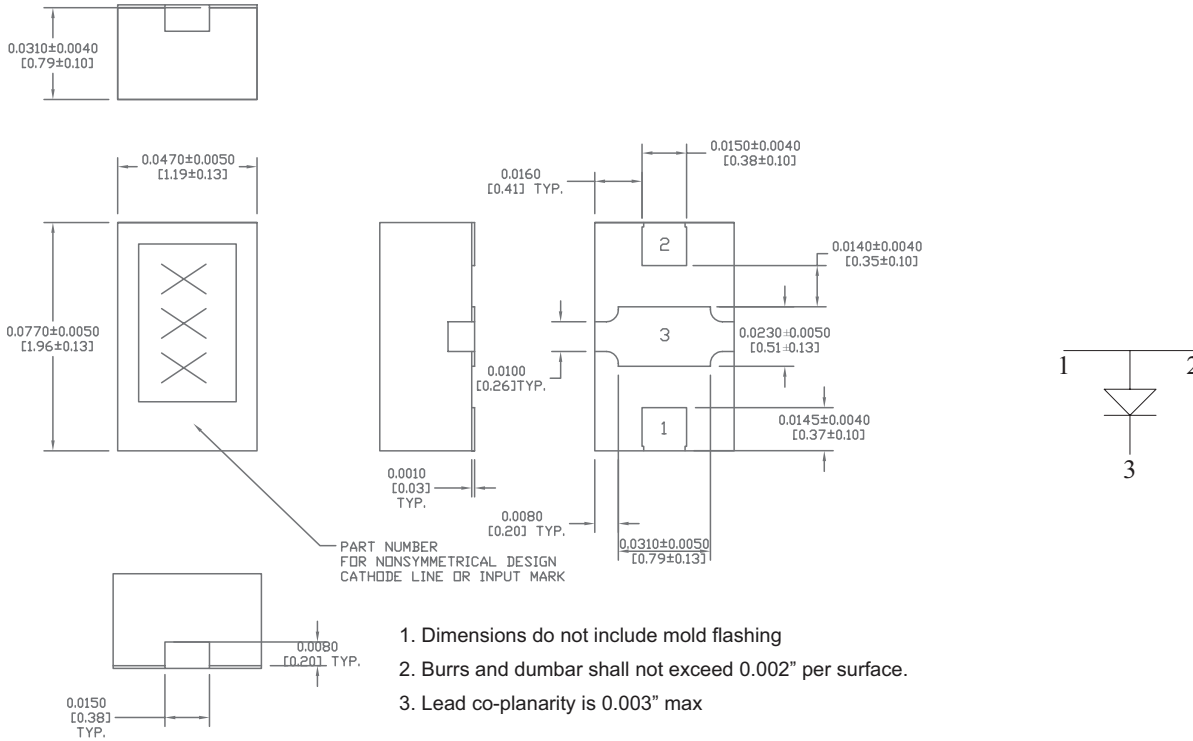
RF Performance Attenuation vs Current



RF Performance Isolation

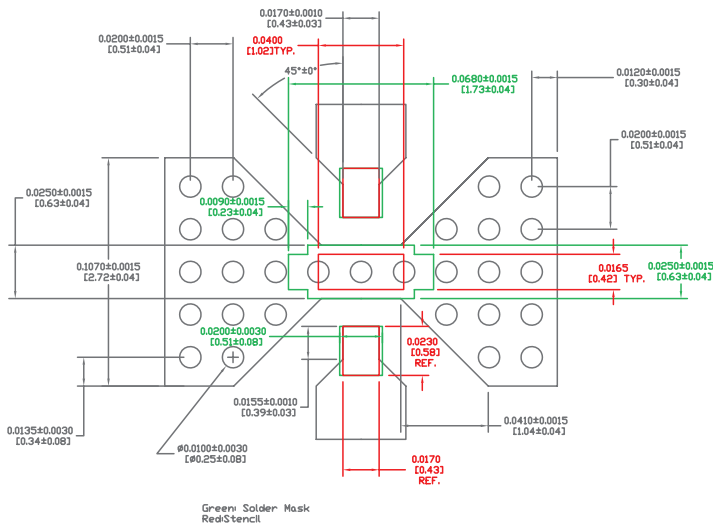


Package Outline (2012) and Electrical Schematic



Dimensions: inches [mm]

PCB Layout



NOTE: If possible, use copper filled vias underneath pin 3 for better thermals; otherwise, use vias that are plated through, filled and plated over.

Solder mask should provide a 60 um clearance between copper pad and soldermask. Rounded pkg pads should have matching rounded solder mask openings.

Use circles or squares for the thermal land stencil such that only get 50% to 80% solder paste coverage.

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