Doc. No.: 2011010027

FEATURES

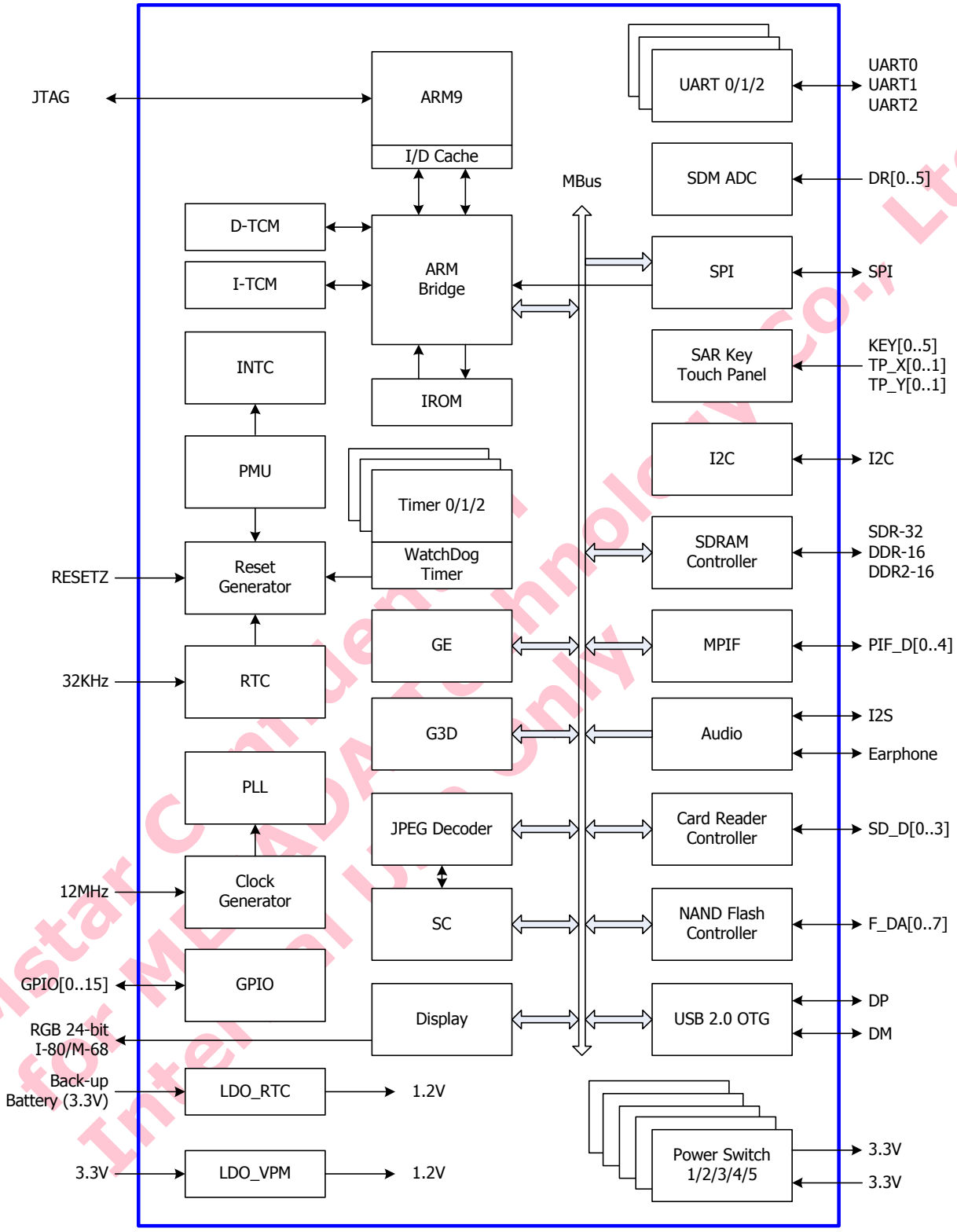
High Performance Portable Navigation Device (PND) Application Processor

- High-Performance 32-bit RISC CPU
  - ARM9
  - Supports frequency up to 500MHz
- High-Integrated Power Management Unit
  - Power control logic for efficient power management and event detection
  - Adjustable output LDOs with internal pass devices for the whole chip and peripheral devices
  - Adjustable output bucks provide power supplies for memory and processor
  - Boost for LCD backlight
  - Battery charger system supports parallel charging for USB charging
  - AUX ADC for battery monitoring and auxiliary input
- High-Efficiency GPS Baseband
  - GPS L1, C/A Code, with all-in-view processing
  - High sensitivity enabling deep indoor application
  - Assisted/autonomous operation involving optimum use of all available assistance data
  - Fast TTFF in all modes
  - DGPS and WAAS capable
- 2D Graphics Engine
  - Line draw and rectangle draw/fill
  - BitBlt
  - Clipping, rotate or mirror
  - Dithering and alpha blending
  - Supports tile mode
- 3D Graphics Engine for Map Navigation
  - Consists of a transfer engine, a setup engine and a rendering engine
  - Supports triangle list and triangle fan primitive types
  - World view, projection view and view-port transform
  - Supports CW and CCW back-face culling
  - Supports scissor box
  - Line anti-aliasing
  - Supports flat shading and smooth shading
  - Supports 1 texture
  - Supports MipMap texturing with the maximum level 9
  - Supports texture formats RGBA5551, RGBA4444, RGB565, LA88, L8 and A8
  - Supports 4-bit, 8-bit palletized texture with formats RGBA5551, RGBA 4444, RGB565
  - Supports alpha blending and alpha test
  - Supports logical pixel operation
- Real Time Clock
  - Works with 32.768 KHz crystal
  - Alarm interrupt or wakeup
  - Tick time interrupt (millisecond)
  - Built-in regulator
- JPEG Decoder
  - Supports resolution up to 16K x 16K pixels
  - Supports multiple color formats and grayscale
  - High speed decoder with downscaling
  - Integrated ROI, rotate and mirror

- Audio Interface
  - I2S/PCM digital audio/voice input and output interface
  - Built-in earphone driver
  - Built-in classD amplifier for speaker
  - Earphone plug-in detection
  - Analog audio stereo line out
- High-Quality Scaling Engine and Video Interface
  - Supports pre-scaling down filter
  - Support 2/4-line vertical scaling for different use cases
  - Share the line buffer in 2/4 line mode
  - Support 1:1 scaling and bypass mode
  - Supports digital panels up to 1024x768
  - Support 422/444 format
  - Supports 8-bit TTL panel output
  - Supports 6-bit TTL panel with DTCON output
  - Supports Intel-80/Motorola-68 format panel
  - Support TTL RGB 565 dither function
  - Support CCIR656 input
- Proprietary MPIF High Speed Interface
  - Compatible with SPI (3-wire or 4-wire)
  - DMA for large amount of data transfer
  - Supports flow control with hardware CRC/checksum mechanism
- Flash Card and NAND Interface
  - Compatible with SDIO spec. 1.10, data bus 1/4 bit mode.
  - Compatible with SD spec. 2.0, data bus 1/4 bit mode.
  - Compatible with MMC spec. 4.3, data bus 1/4/8 bit mode. But no boot mode.
  - Compatible with MS spec. 1.3, data bus 1 bit mode
  - Compatible with MSPro spec. 1.0, data bus 1/4 bit mode
  - Supports i-NAND (support eSD mode, 8bits eMMC mode)
  - Support Movi-NAND
  - Supports SLC/MLC NAND Flash (8-bit interface, and 32-bit ECC)
- USB Interface
  - USB2.0 compliant integrated transceiver
  - Built-in USB device controller
  - Supports EHCI USB2.0 host mode
  - Supports device mode
- DRAM Memory
  - Supports Mobile DDR-16 400 MHz
  - Support DDR2-16 800 MHz
  - Support DDR3-8 1.6 GHz
  - Supports memory size up to 512MB
- Peripherals
  - Up to 20 dedicated GPIOs for system control
  - Up to 6 PWMs shared with GPIO
  - Up to 3 UARTs, 1 UART has flow control
  - Three 16-bit Timers
  - Watchdog Timer
  - SPI (CSx2) master, to support NOR flash ISP
  - One I2C Master
  - Built-in keypad SAR and touch panel ADC
- Operating Voltage Range
  - Core: 1.1 ~ 1.32V
  - I/O: 2.7 ~ 3.6V
  - DRAM: 1.8/1.5V
  - Power Consumption: TBD
- Package
  - 12 x 12 (mm) 293-ball LFBGA

Note: Some features are available as options

BLOCK DIAGRAM

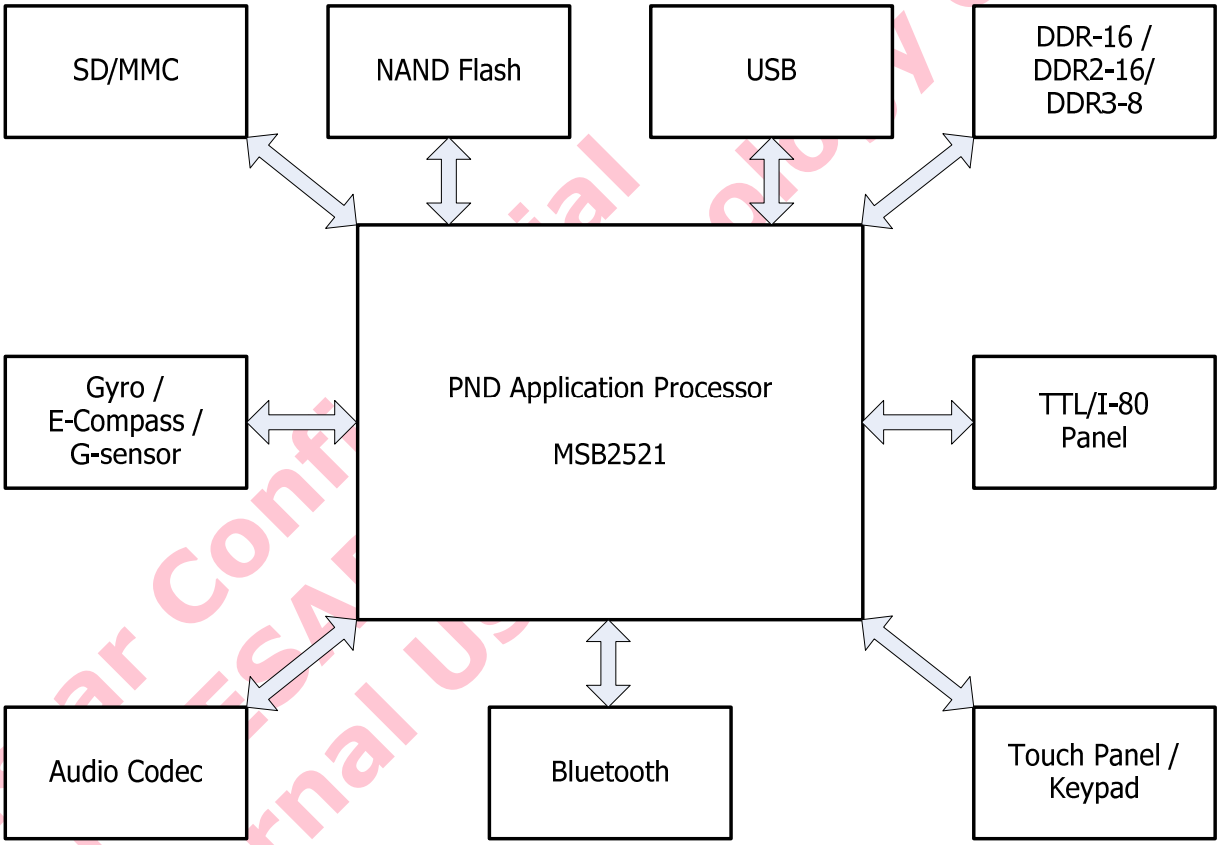


SYSTEM APPLICATION

A typical utilization of the MSB2521 application processor is demonstrated in the following block diagram. The complete system includes a GPS RF receiver, an LCD module (LCM) with touch panel, a NAND flash, an SD/MMC card, a Bluetooth chip and an audio codec. External crystal of 32 kHz frequency is used to drive the Real Time Clock (RTC), which can keep time scale when the main power is off. The MSB2521 storage media interface supports the most popular storage cards on market, including SD/T-Flash and MMC. It also supports NAND-type flash and SPI serial flash interface. Moreover, other peripherals like UARTs and GPIOs are supported to realize applications with maximal flexibility.

There is only one battery power supply line entering the chip in the whole system:

- Battery supplies main power to MSB2521, and then MSB2521 would supply miscellaneous power to other peripherals. It is unnecessary to include other external power manager chips.



GENERAL DESCRIPTION

The MSB2521 PND application processor is a highly integrated SoC which incorporates a high-performance 32-bit RISC processor core, an high-integrated power management unit, an high-efficiency GPS baseband, an enhanced 32-bit coprocessor for GPS, an mobile-DDR/DDR2/DD3 DRAM controller, a 2D and 3D graphic accelerator for map navigation, an hardware JPEG decoder, an high quality scaling engine with display and other peripheral interfaces. The MSB2521 processor is controlled by highly flexible, adaptive signal-processing and navigation firmware, which is optimized for execution on the low-power ARM9 microprocessor and ideal for cost/power sensitive consumer applications.

The MSB2521 supports I-80 for low cost requirement or 6/8-bit TTL for high quality request. To optimize the BOM cost, the MSB2521 integrates as many components as possible into a single chip. It also integrates all the possible storage devices such as card reader, NAND flash and USB. The embedded OSD and graphics engine (GE) support fantastic display effect. The hardware JPEG engine allows the pictures to be displayed smoothly and fast.

PIN DIAGRAM (MSB2521)

	1	2	3	4	5	6	7	8	9	10	11	12
A	R1	R0		DDR2_CKZ	DDR2_CK		DDR2_D7	DDR2_D13		DDR2_UDQSZ	DDR2_UDQS	
B	R2	VSS_CORE	DDR2_A11	DDR2_CKE	DDR2_D5	DDR2_D2	DDR2_D0	DDR2_D10	DDR2_D8	DDR2_D15	DDR2_LDQSZ	DDR2_LDQS
C	R3	R4				DDR2_A8	DDR2_A0				VSS_CORE	
D		R5										
E	R7	R6	UART_RX0			DDR2_A13		DDR2_A2	DDR2_RASZ	VSS_CORE	VDD_DDR	VSS_CORE
F	G0	G1			UART_TX0	VSS_CORE	DDR2_A4	DDR2_A6	DDR2_CASZ		VSS_CORE	
G		G2			UART_RX1	UART_TX1						
H	G4	G3			UART_RX2	UART_TX2		VDD_LCM	VDD_APLL	VDD_MEM_2	VDD_MEM_2	VDD_MEM_1
J	G5	G6			UART_CTS2	UART_RTS2		VDD_CORE				
K		G7			MIIC_SCL	MIIC_SDA		VDD_VPER4		VSS_CORE	VSS_CORE	VSS_CORE
L	B1	B0			CCIR_D1	CCIR_D0		AVDD_VSYS_1		VSS_CORE		VSS_CORE
M	B2	B3			CCIR_D3	CCIR_D2		VDD_VPER1		VSS_CORE	VSS_CORE	
N		B4			CCIR_D5	CCIR_D4		PIF_CS1Z		VSS_CORE		VSS_CORE
P	B6	B5			CCIR_D7	CCIR_D6		PIF_CS0Z		VFSOURCE	VSS_CORE	VSS_CORE
R	B7	LDISP			CCIR_CLK			PIF_D0				
T		LCK			IIS_TRX_BCK	IIS_TRX_WS		VDD_CORE	PIF_D1	PIF_D2	PIF_D3	PIF_CLK
U	LVSYNC	LHSYNC			IIS_TRX_OUT	IIS_TRX_IN						
V	LDE	VSS_CORE			SAR_KEY1		MS_INS	GPIO_G01				NC
W	X1	Y1			SAR_KEY0	SD_CDZ	GPIO_G00	GPIO_G02	GPIO_G03	GPIO_G04	GPIO_G05	GPIO_G06
Y		X2										
AA	VSS_MPLL	Y2										
AB	XOUT	VSS_AUX	VSS_CORE	VSS_CORE	VBUS	USB_CID	VDD_USB	VSS_XTAL	VSS_PM	VADA_DIV	AVDD_VCS	ISENSE
AC	XIN	VSS_CORE	DP	DM			VSS_CORE	RTC_XOUT	RTC_XIN	VSS_CORE	GATEDRV	
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**

13	14	15	16	17	18	19	20	21	22	23	
DDR2_UDM	DDR2_D14		DDR2_D6	DDR2_D1		DDR2_A7	DDR2_A12		GPIO_G11	GPIO_G13	A
DDR2_LDM	DDR2_D9	DDR2_D12	DDR2_D11	DDR2_D3	DDR2_D4	DDR2_A10	DDR2_A3	VSS_CORE	GPIO_G12	GPIO_G14	B
	DDR2_A5			DDR2_WEZ					F_DA6	F_DA7	C
									F_DA5		D
DDR3_A15		DDR2_A14	DDR2_BA0			AFE_MAG			F_DA4	F_DA3	E
DDR2_A1	DDR2_A9	DDR2_BA1	DDR2_BA2	DDR2_ODT	VSS_CORE	AFE_SGN			F_DA1	F_DA2	F
					RFSPI_CLK	AFE_CLK			F_DA0		G
VSS_CORE	AVDD_VSYS_3	VDD_VPER3	VDD_CORE			RFSPI_DO			F_RBZ	F_REZ	H
			VDD_FLASH		RFSPI_CSZ	GPIO_G16			F_CE1Z	F_CEZ	J
VSS_CORE	ARM_TEST		GPIO_G17		GPIO_G15	GPIO_G18			F_CLE		K
	VSS_CORE		32KHz_OUT		GPIO_G19	GPIO_G20			F_ALE	F_WEZ	L
VSS_CORE	VSS_CORE		NC		GPIO_G21	SPI_DI			SD_D1	F_WPZ	M
	VSS_CORE		VDD_VPER2		NC	SPI_DO			SD_D0		N
VSS_CORE	PM_TEST		AVDD_VSYS_2		SPI_CK	NC			SD_CLK	SD_CMD	P
			NC		SPI_CS1Z	SPI_CS0Z			SD_D2	SD_D3	R
PIF_BUSY	ON/OFF	CHRGLED	VDD_CORE		VSS_CORE	VDD_AUDIO			SD_WPZ		T
					LINEIN1_P	LINEIN2_P			SPKOP	SPKON	U
RESETZ	GPIO_G08	NC	VSS_AUDIO	LINEIN1_N		LINEIN2_N			VSS_CLD	AVDD_VBAT_CLD	V
GPIO_G07	VSS_CORE	AUXC0	VDD_VABB	EAR_DET	EAR_OUT_R	EAR_OUT_L			VCLAMP_CLD	AVDD_VBAT_BK2	W
									VDD_VL		Y
										VBK2FB	AA
AVDD_VBATSENSE	SW_CHRG	VSS_BST	VDIM	BSTFB	VSS_CORE	VDD_VPM	VCLAMP_BK1	VSS_CORE	VCLAMP_BK2	VSS_BK2	AB
AVDD_VSYS	AVDD_BST	BST_GATE	AVDD_VBAT	BSTOVP	BST_ISENSE	VBK1FB	VSS_BK1	SW_VBK1	AVDD_VBAT_BK1	SW_VBK2	AC
13	14	15	16	17	18	19	20	21	22	23	

PIN DESCRIPTION

NAND (SDIO) Interface

Pin Name	Pin Type	Function	Pin
F_ALE	Output	NAND Flash Address Latch Enable	L22
F_CEZ	Output	NAND Flash Chip 0 Enable (active low)	J23
F_CE1Z	Output	NAND Flash Chip 1 Enable (active low)	J22
F_CLE	Output	NAND Flash Command Latch Enable	K22
F_DA[7:0]	Input/Output	NAND Flash Data Bus	C23, C22, D22, E22, E23, F23, F22, G22
F_RBZ	Input	NAND Flash Status (high: ready, low: busy)	H22
F_REZ	Output	NAND Flash Read Enable (active low)	H23
F_WEZ	Output	NAND Flash Write Enable (active low)	L23
F_WPZ	Output	NAND Flash Write Protect (active low)	M23

TTL Interface

Pin Name	Pin Type	Function	Pin
R[7:0]	Output	TTL Panel Red Data Bus	E1, E2, D2, C2, C1, B1, A1, A2
G[7:0]	Output	TTL Panel Green Data Bus	K2, J2, J1, H1, H2, G2, F2, F1
B[7:0]	Output	TTL Panel Blue Data Bus	R1, P1, P2, N2, M2, M1, L1, L2
LCK	Output	TTL Panel Clock	T2
LDISP	Input/Output	TTL Panel Display ON/OFF	R2
LHSYNC	Output	TTL Panel Horizontal Synchronization	U2
LVSYNC	Output	TTL Panel Vertical Synchronization	U1
LDE	Output	TTL Panel Data Enable	V1

UART(x3) Interface

Pin Name	Pin Type	Function	Pin
UART_RX0	Input	UART_0 Receiver	E3
UART_TX0	Output	UART_0 Transmitter	F5
UART_RX1	Input	UART_1 Receiver	G5
UART_TX1	Output	UART_1 Transmitter	G6
UART_RX2	Input	UART_2 Receiver	H5
UART_TX2	Output	UART_2 Transmitter	H6
UART_CTS2	Output	UART_2 Clear to Set	J5
UART_RTS2	Output	UART_2 Request to Set	J6

I2C Master Interface

Pin Name	Pin Type	Function	Pin
MIIC_SDA	Input/Output	Master I2C Serial Data	K6
MIIC_SCL	Output	Master I2C Serial Clock	K5

I2S / PCM Interface

Pin Name	Pin Type	Function	Pin
IIS_TRX_BCK	Input/Output	I2S Master Bit Clock	T5
IIS_TRX_WS	Input/Output	I2S Master Word Select	T6
IIS_TRX_IN	Input	I2S Data In	U6
IIS_TRX_OUT	Output	I2S Data Out	U5

SPI / HS-SPI (NOR) Interface

Pin Name	Pin Type	Function	Pin
SPI_CK	Output	SPI Serial Clock	P18
SPI_DI	Output	SPI Serial Data To Device	M19
SPI_DO	Input	SPI Serial Data From Device	N19
SPI_CS0Z	Output	SPI Chip 0 Select (active low)	R19
SPI_CS1Z	Output	SPI Chip 1 Select (active low)	R18

SD/MMC/MS Interface

Pin Name	Pin Type	Function	Pin
MS_INS	Input	MS Card Detect	V7
SD_CDZ	Input	SD Card Detect	W6
SD_CLK	Output	SD Card Clock	P22
SD_CMD	Input/Output	SD Card Command	P23
SD_D[3:0]	Input/Output	SD Card Data Bus	R23, R22, M22, N22
SD_WPZ	Output	SD Card Write Protect	T22

MPIF / SSP Interface

Pin Name	Pin Type	Function	Pin
PIF_BUSY	Input	MPIF Flow Control / SPI Data In	T13
PIF_CLK	Output	MPIF/SPI Bus Clock	T12
PIF_CS0Z	Output	MPIF/SPI Slave 0 Chip Select	P8
PIF_CS1Z	Output	MPIF/SPI Slave 1 Chip Select	N8
PIF_D[3:0]	Input/Output	MPIF Data Bus / SPI Data Out	T11-T9, R8

GPIO Interface

Pin Name	Pin Type	Function	Pin
GPIO_G[8:0]	Input/Output	General Purpose Input/Output (external interrupt)	V14, W13-W8, V8, W7
GPIO_G[21:11]	Input/Output	General Purpose Input/Output	M18, L19, L18, K19, K16, J19, K18, B23, A23, B22, A22

Video Input Interface

Pin Name	Pin Type	Function	Pin
CCIR_CLK	Input	CCIR Clock	R5
CCIR_D[7:0]	Input	CCIR Data Bus	P5, P6, N5, N6, M5, M6, L5, L6

GPS Interface

Pin Name	Pin Type	Function	Pin
AFE_CLK	Input	GPS Clock	G19
AFE_MAG	Input	GPS Magnitude	E19
AFE_SGN	Input	GPS Sign	F19
RFSPI_CLK	Output	RF SPI Clock	G18
RFSPI_CSZ	Output	RF SPI Chip Select (active low)	J18
RFSPI_DO	Output	RF SPI Data	H19

Keypad (ADC) Interface

Pin Name	Pin Type	Function	Pin
SAR_KEY0	Input	Keypad 0 ADC (wakeup key)	W5
SAR_KEY1	Input	Keypad 1 ADC	V5

Touch Panel Interface

Pin Name	Pin Type	Function	Pin
X1	Input	Touch Panel X1	W1
Y1	Input	Touch Panel Y1	W2
X2	Input	Touch Panel X2	Y2
Y2	Input	Touch Panel Y2	AA2

USB 2.0 Host/Device Interface

Pin Name	Pin Type	Function	Pin
VBUS	Input	USB VBUS Power	AB5
DM	Input/Output	USB Inverting Data	AC4
DP	Input/Output	USB Non-inverting Data	AC3
USB_CID	Input	USB OTG ID (high slave mode, low host mode)	AB6

Audio Interface

Pin Name	Pin Type	Function	Pin
EAR_OUT_L	Output	Earphone Left Channel	W19
EAR_OUT_R	Output	Earphone Right Channel	W18
EAR_DET	Input	Earphone Detect (active high)	W17
SPKOP	Output	Speaker Positive Output	U22
SPKON	Output	Speaker Negative Output	U23
LINEIN1_N	Input	Audio Line 1 Negative Input	V17
LINEIN1_P	Input	Audio Line 1 Positive Input	U18
LINEIN2_N	Input	Audio Line 2 Negative Input	V19
LINEIN2_P	Input	Audio Line 3 Positive Input	U19

DDR Interface

Pin Name	Pin Type	Function	Pin
DDR2_A [14:0]	Output	DRAM Memory Address	E15, E6, A20, B3, B19, F14, C6, A19, F8, C14, F7, B20, E8, F13, C7
DDR2_D [15:0]	Input/Output	DRAM Memory Data Bus	B10, A14, A8, B15, B16, B8, B14, B9, A7, A16, B5, B18, B17, B6, A17, B7
DDR2_BA [2:0]	Output	DRAM Memory Bank Address	F16, F15, E16
DDR2_CASZ	Output	DRAM Memory Column Address Strobe (active low)	F9
DDR2_CK	Output	DRAM Memory Positive Differential Clock	A5
DDR2_CKE	Output	DRAM Memory Clock Enable	B4
DDR2_CKZ	Output	DRAM Memory Negative Differential Clock	A4
DDR2_LDM	Output	DRAM Memory Left Data Mask for Low Byte (active high)	B13
DDR2_LDQS	Output	DRAM Memory Left Data Strobe	B12
DDR2_LDQSZ	Output	DRAM Memory Left Data Strobe Inverse	B11
DDR2_ODT	Output	DRAM Memory On-Die Termination	F17
DDR2_RASZ	Output	DRAM Memory Row Address Strobe (active low)	E9
DDR2_UDM	Output	DRAM Memory Upper Data Mask for Low Byte (active high)	A13
DDR2_UDQS	Output	DRAM Memory Upper Data Strobe	A11
DDR2_UDQSZ	Output	DRAM Memory Upper Data Strobe Inverse	A10
DDR2_WEZ	Output	DRAM Memory Write Enable (active low)	C17
DDR3_A15	Output	DRAM Memory Address (only for ddr3)	E13

System Interface

Pin Name	Pin Type	Function	Pin
ARM_TEST	Input	Chip Test Pin	K14
ON/OFF	Input	Chip ON/OFF (active low)	T14
PM_TEST	Input	Chip Test Enable (active high)	P14
RESETZ	Input	Chip Reset (active low)	V13
VFSOURCE	Input	Efuse Programming Voltage	P10
XIN	Input	24MHz Crystal Input	AC1
XOUT	Input/Output	24MHz Crystal Output 16.369MHz TCXO Input	AB1
RTC_XIN	Input	32KHz Crystal Input	AC9
RTC_XOUT	Output	32KHz Crystal Output	AC8
32KHz_OUT	Output	32KHz Clock output	L16

Power Management Interface

Pin Name	Pin Type	Function	Pin
AUXC0	Input	Auxiliary ADC Input	W15
BST_GATE	Output	Boost NMOS Gate Control	AC15
BSTFB	Input	Boost Voltage Feedback	AB17
BST_ISENSE	Input	Boost Current Sense	AC18
BSTOVP	Input	Boost Voltage Sense for Over Voltage Detection	AC17
CHRGLED	Output	Charging LED Driver	T15
GATEDRV	Output	Charging Current/Voltage Control	AC11
ISENSE	Input	Charging Current Sense	AB12
SW_CHRG	Output	Charging PMOS Gate Control (from VSYS to VBAT)	AB14
SW_VBK1	Output	BUCK1 Switching Output	AC21
SW_VBK2	Output	BUCK2 Switching Output	AC23
VADA_DIV	Input	Charger Voltage Divider for Over Voltage Detection	AB10
VBK1FB	Input	BUCK1 Voltage Feedback	AC19
VDIM	Input	Boost Voltage Dimming Control	AB16

Power Pins

Pin Name	Pin Type	Function	Pin
AVDD_VBATSENSE	4.2V Power (V_{VBAT})	Power Supply	AB13
AVDD_VBAT	4.2V Power (V_{VSYS})	Power Supply	AC16
AVDD_VBAT_BK1	4.2V Power (V_{VSYS})	Power Supply	AC22
AVDD_VBAT_BK2	4.2V Power (V_{VSYS})	Power Supply	W23
AVDD_VBAT_CLD	4.2V Power (V_{VSYS})	Power Supply	V23
AVDD_VSYS	4.2V Power (V_{VSYS})	Power Supply	AC13
AVDD_VSYS_1	4.2V Power (V_{VSYS})	Power Supply	L8
AVDD_VSYS_2	4.2V Power (V_{VSYS})	Power Supply	P16
AVDD_VSYS_3	4.2V Power (V_{VSYS})	Power Supply	H14
AVDD_VCS	3.2V Power	Analog Power	AB11
AVDD_BST	3.2V Power	Analog Power	AC14
VBK2FB	Input/Output	BUCK2 Voltage Feedback & VMEM LDO Output	AA23
VCLAMP_BK1	3.2V Power	BUCK1 Clamp Voltage	AB20
VCLAMP_BK2	3.2V Power	BUCK2 Clamp Voltage	AB22
VCLAMP_CLD	3.2V Power	CLASSD Clamp Voltage	W22
VDD_AUDIO	3.2V Power	Audio Analog Power	T19
VDD_FLASH	3.2V Power	Flash Pad Power	J16
VDD_LCM	3.2V Power	LCM Pad Power	H8
VDD_USB	3.2V Power	MPLL/LPLL/USB Analog Power	AB7
VDD_VABB	3.2V Power	Analog Power	W16
VDD_VPER4	3.2V Power	Wi-Fi PA Power	K8
VDD_VPER3	2.9V Power	GPS RF Pad Power	H15
VDD_VPER2	2.9V Power	SD Card Pad Power	N16
VDD_VPER1	2.9V Power	UART/I^2C/I^2S/CCIR/MPIF Pad Power	M8
VDD_MEM_1	1.8V Power	DDR Analog Power	H12
VDD_MEM_2	1.8v Power	DDR Analog Power	H10, H11
VDD_VPM	1.2V Power	PM Digital Power	AB19
VDD_CORE	1.2V Power	Digital Power	H16, J8, T8, T16
VDD_DDR	1.2V Power	Digital Power	E11
VDD_VL	Power	Analog Power, VDD_VL=VSYS-VABB	Y22

Pin Name	Pin Type	Function	Pin
VSS_CORE	Ground	Ground	B2, B21, C11, E10, E12, F6, F11, F18, H13, K10-K13, L10, L12, L14, M10.M11, M13, M14, N10, N12, N14, P11-13, T18, V2, W14, AB3, AB4, AB18, AB21, AC2, AC7, AC10
VSS_AUDIO	Ground	Ground	V16
VSS_MPLL	Ground	Ground	AA1
VSS_PM	Ground	Ground	AB9
VSS_AUX	Ground	Ground	AB2
VSS_BK1	Ground	Ground	AC20
VSS_BK2	Ground	Ground	AB23
VSS_BST	Ground	Ground	AB15
VSS_XTAL	Ground	Ground	AB8
VSS_CLD	Ground	Ground	V22

No Connects

Pin Name	Pin Type	Function	Pin
NC		No connect	M16, N18, P19, R16, V12, V15

ELECTRICAL SPECIFICATIONS

Interface Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
DIGITAL INPUTS					
Input Voltage, High	V_{IH}	2.5			V
Input Voltage, Low	V_{IL}			0.8	V
Input Current, High	I_{IH}			-1.0	uA
Input Current, Low	I_{IL}			1.0	uA
Input Capacitance			5		pF
DIGITAL OUTPUTS					
Output Voltage, High	V_{OH}	VDDP-0.1[Note]			V
Output Voltage, Low	V_{OL}			0.1	V
AUX ADC Input		0		V_{VDD_32}	V
Keypad ADC Input		0		V_{VDD_32}	V
AUDIO OUTPUTS					
Line-Out			2.0		Vp-p
Earphone Pre-Amp			2.0		Vp-p
Speaker				7.5	Vp-p

Note: VDDP can be V_{VDD_32}, V_{VDD_29}, V_{VDD_18}, V_{VDD_15}

Recommended Operating Power Conditions

Parameter	Symbol	Min	Typ.	Max.	Unit
System Supply Voltage	V_{VSYS}		3.6		V
Battery Supply Voltage	V_{VBAT}		3.6		V
3.2V Supply Voltage	V_{VDD_32}		3.2		V
2.9V Supply Voltage (Peripheral)	V_{VDD_29}		2.9		V
1.8V Supply Voltage (DDR I/II)	V_{VDD_18}		1.8		V
1.5V Supply Voltage (DDR III)	V_{VDD_15}		1.5		V
1.2V Supply Voltage (Core)	V_{VDD_12}		1.2		V

Absolute Maximum Ratings

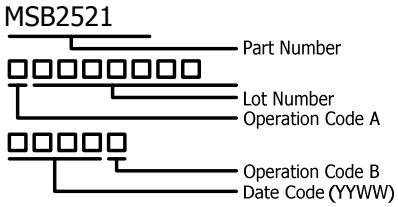
Parameter	Symbol	Min	Typ.	Max.	Unit
System Supply Voltage	V_{VSYS}			4.2	V
Battery Supply Voltage	V_{VBAT}			4.2	V
Ambient Operation Temperature	T_A	-40		85	°C
Storage Temperature	T_{STG}	-40		150	°C
Junction Temperature	T_J			150	°C

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and does not imply functional operation of device. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ORDERING GUIDE

Part Number	Temperature Range	Package Description	Package Option
MSB2521	-40°C to +85°C	LFBGA	293-ball

MARKING INFORMATION



DISCLAIMER

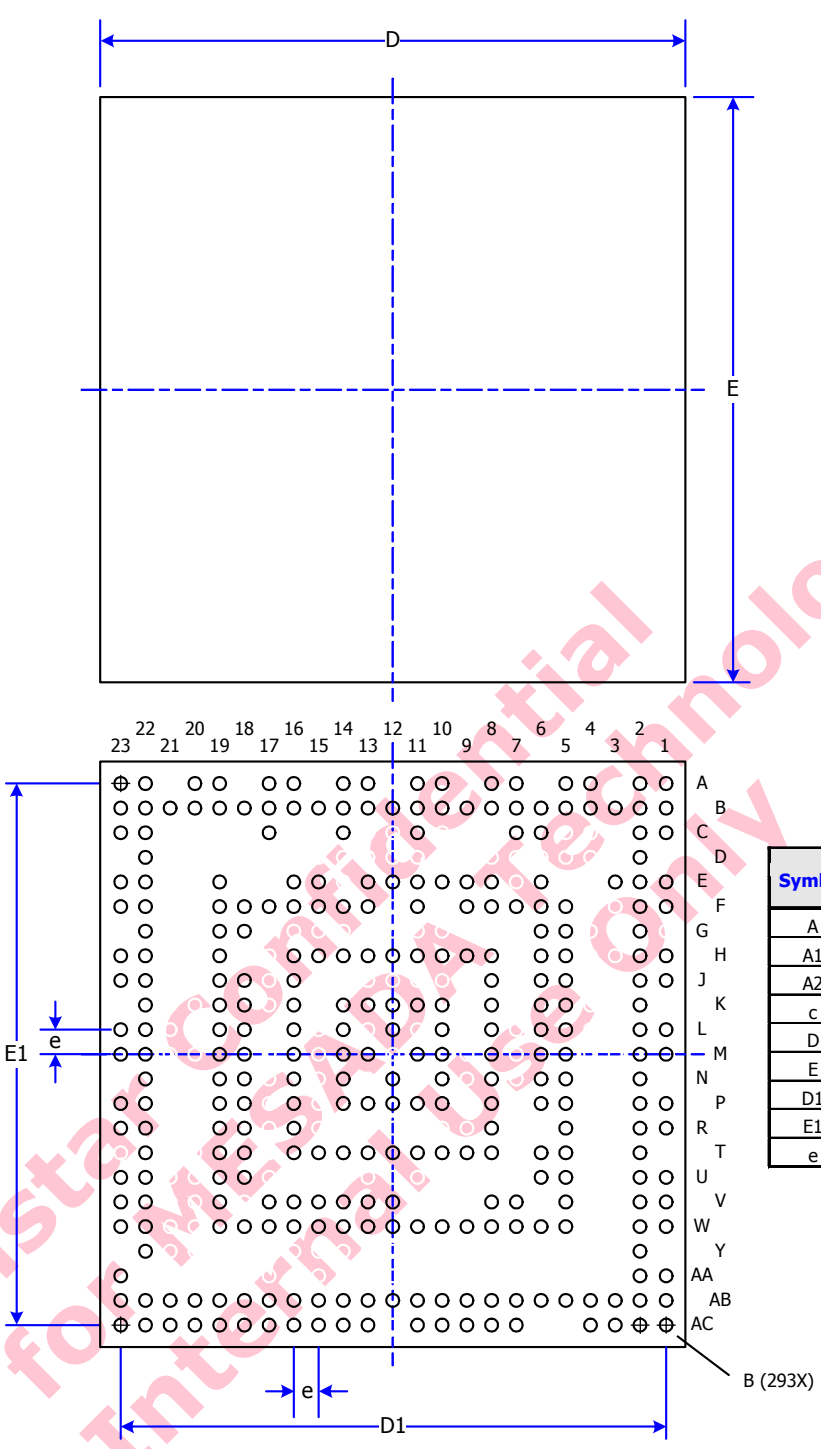
MSTAR SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. NO RESPONSIBILITY IS ASSUMED BY MSTAR SEMICONDUCTOR ARISING OUT OF THE APPLICATION OR USER OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

Electrostatic charges accumulate on both test equipment and human body and can discharge without detection. MSB2521 comes with ESD protection circuitry, however, the device may be permanently damaged when subjected to high energy discharges. The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.

REVISION HISTORY

Document	Description	Date
MSB2521_ds_v01	• Initial release	Jan 2011

MECHANICAL DIMENSIONS



Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.25	-	-	0.049
A1	0.17	0.22	0.27	0.007	0.009	0.011
A2	0.84	0.91	0.98	0.033	0.036	0.039
c	0.22	0.26	0.30	0.009	0.010	0.012
D	11.90	12.00	12.10	0.469	0.472	0.476
E	11.90	12.00	12.10	0.469	0.472	0.476
D1	-	11.00	-	-	0.433	-
E1	-	11.00	-	-	0.433	-
e	-	0.50	-	-	0.020	-

REGISTER DESCRIPTIONS

MPIF Register (Bank = 06)

MPIF Register (Bank = 06)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (0C00h)	**REG0C00**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MPIF_LC1A_IDX[2:0]	6:4	MPIF Logical Channel 1a index.	
	MPIF_LC1A_SID[1:0]	3:2	MPIF Logical Channel 1a Slave ID.	
	MPIF_LC1A_RW	1	MPIF Logical Channel 1a read/write.	
	MPIF_LC1A_VLD	0	MPIF Logical Channel 1a valid.	
00h (0C01h)	**REG0C01**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC1A_DATA[7:0]	7:0	MPIF Logical Channel 1a data.	
	MPIF_LC1A_DATA[7:0]	7:0	MPIF Logical Channel 1a data.	
01h (0C04h)	**REG0C04**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC2A_RETRX_LIMIT[1:0]	7:6	MPIF re-transmit/receive count limit. 0: 0 time. 1: 1 time. 2: 2 times. 3: 3 times.	
	-	5	Reserved.	
	MPIF_LC2A_CHK	4	MPIF Logical Channel 2a check enable.	
	MPIF_LC2A_SID[1:0]	3:2	MPIF Logical Channel 2a Slave ID.	
	MPIF_LC2A_RW	1	MPIF Logical Channel 2a read/write.	
	MPIF_LC2A_VLD	0	MPIF Logical Channel 2a valid.	
02h (0C08h)	**REG0C08**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC2A_ADR[7:0]	7:0	MPIF Logical Channel 2a address.	
02h (0C09h)	**REG0C09**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC2A_ADR[15:8]	7:0	See description of '0C08h'.	
03h (0C0Ch)	**REG0C0C**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	MPIF_LC2A_DATA[7:0]	7:0	MPIF Logical Channel 2a data.	
	STS_MPIF_LC2A_DATA[7:0]	7:0	MPIF Logical Channel 2a data.	
03h (0C0Dh)	**REG0C0D**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	MPIF_LC2A_DATA[15:8]	7:0	See description of '0C0Ch'.	
	STS_MPIF_LC2A_DATA[15:8]	7:0	See description of '0C0Ch'.	
04h	**REG0C10**	**7:0**	**Default : 0x00**	**Access : R/W**

MPIF Register (Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description	
(0C10h)	MPIF_LC2B_RETRX_LIMIT[1:0]	7:6	MPIF re-transmit/receive count limit. 0: 0 time. 1: 1 time. 2: 2 times. 3: 3 times.	
	-	5	Reserved.	
	MPIF_LC2B_CHK	4	MPIF Logical Channel 2b check enable.	
	MPIF_LC2B_SID[1:0]	3:2	MPIF Logical Channel 2b Slave ID.	
	MPIF_LC2B_RW	1	MPIF Logical Channel 2b read/write.	
	MPIF_LC2B_VLD	0	MPIF Logical Channel 2b valid.	
05h (0C14h)	**REG0C14**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC2B_ADR[7:0]	7:0	MPIF Logical Channel 2b address.	
05h (0C15h)	**REG0C15**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC2B_ADR[15:8]	7:0	See description of '0C14h'.	
06h (0C18h)	**REG0C18**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC2B_DATA[7:0]	7:0	MPIF Logical Channel 2b data.	
	MPIF_LC2B_DATA[7:0]	7:0	MPIF Logical Channel 2b data.	
06h (0C19h)	**REG0C19**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC2B_DATA[15:8]	7:0	See description of '0C18h'.	
	MPIF_LC2B_DATA[15:8]	7:0	See description of '0C18h'.	
07h (0C1Ch)	**REG0C1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC3A_RETRX_LIMIT[1:0]	7:6	MPIF re-transmit/receive count limit. 0: 0 time. 1: 1 time. 2: 2 times. 3: 3 times.	
	MPIF_LC3A_RETRX	5	MPIF Logical Channel 3a re-transmit/receive packet indicator.	
	MPIF_LC3A_CHK	4	MPIF Logical Channel 3a check enable.	
	MPIF_LC3A_SID[1:0]	3:2	MPIF Logical Channel 3a Slave ID.	
	MPIF_LC3A_RW	1	MPIF Logical Channel 3a read/write.	
	MPIF_LC3A_VLD	0	MPIF Logical Channel 3a valid.	
07h (0C1Dh)	**REG0C1D**	**7:0**	**Default : 0x40**	**Access : R/W**
	MPIF_LC3A_WCNT[3:0]	7:4	MPIF Logical Channel 3a max wait number.	

MPIF Register (Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description	
	MPIF_LC3A_RX_NWMIU	3	MPIF Logical Channel 3a not wait miu done.	
	MPIF_LC3A_FMODE	2	MPIF Logical Channel 3a fast read/write mode.	
	MPIF_LC3A_MIUSEL	1	MPIF Logical Channel 3a MIU path selection. 0: MIU (SRAM). 1: EMI (SDRAM).	
	MPIF_LC3A_SRC	0	MPIF Logical Channel 3a source/destination selection. 0: To/from RIU. 1: To/from MIU.	
08h (0C20h)	**REG0C20**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC3A_PKTLEN[7:0]	7:0	MPIF Logical Channel 3a packet total length.	
08h (0C21h)	**REG0C21**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC3A_PKTLEN[15:8]	7:0	See description of '0C20h'.	
09h (0C24h)	**REG0C24**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3A_DATA[7:0]	7:0	MPIF Logical Channel 3a data.	
	MPIF_LC3A_DATA[7:0]	7:0	MPIF Logical Channel 3a data.	
09h (0C25h)	**REG0C25**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3A_DATA[15:8]	7:0	See description of '0C24h'.	
	MPIF_LC3A_DATA[15:8]	7:0	See description of '0C24h'.	
0Ah (0C28h)	**REG0C28**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3A_DATA[23:16]	7:0	See description of '0C24h'.	
	MPIF_LC3A_DATA[23:16]	7:0	See description of '0C24h'.	
0Ah (0C29h)	**REG0C29**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3A_DATA[31:24]	7:0	See description of '0C24h'.	
	MPIF_LC3A_DATA[31:24]	7:0	See description of '0C24h'.	
0Bh (0C2Ch)	**REG0C2C**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3A_DATA[39:32]	7:0	See description of '0C24h'.	
	MPIF_LC3A_DATA[39:32]	7:0	See description of '0C24h'.	
0Bh (0C2Dh)	**REG0C2D**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3A_DATA[47:40]	7:0	See description of '0C24h'.	
	MPIF_LC3A_DATA[47:40]	7:0	See description of '0C24h'.	
0Ch (0C30h)	**REG0C30**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3A_DATA[55:48]	7:0	See description of '0C24h'.	
	MPIF_LC3A_DATA[55:48]	7:0	See description of '0C24h'.	

MPIF Register (Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description	
0Ch (0C31h)	**REG0C31**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3A_DATA[63:56]	7:0	See description of '0C24h'.	
	MPIF_LC3A_DATA[63:56]	7:0	See description of '0C24h'.	
0Dh (0C34h)	**REG0C34**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3A_DATA[71:64]	7:0	See description of '0C24h'.	
	MPIF_LC3A_DATA[71:64]	7:0	See description of '0C24h'.	
0Dh (0C35h)	**REG0C35**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3A_DATA[79:72]	7:0	See description of '0C24h'.	
	MPIF_LC3A_DATA[79:72]	7:0	See description of '0C24h'.	
0Eh (0C38h)	**REG0C38**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3A_DATA[87:80]	7:0	See description of '0C24h'.	
	MPIF_LC3A_DATA[87:80]	7:0	See description of '0C24h'.	
0Eh (0C39h)	**REG0C39**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3A_DATA[95:88]	7:0	See description of '0C24h'.	
	MPIF_LC3A_DATA[95:88]	7:0	See description of '0C24h'.	
0Fh (0C3Ch)	**REG0C3C**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3A_DATA[103:96]	7:0	See description of '0C24h'.	
	MPIF_LC3A_DATA[103:96]	7:0	See description of '0C24h'.	
0Fh (0C3Dh)	**REG0C3D**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3A_DATA[111:104]	7:0	See description of '0C24h'.	
	MPIF_LC3A_DATA[111:104]	7:0	See description of '0C24h'.	
10h (0C40h)	**REG0C40**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3A_DATA[119:112]	7:0	See description of '0C24h'.	
	MPIF_LC3A_DATA[119:112]	7:0	See description of '0C24h'.	
10h (0C41h)	**REG0C41**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3A_DATA [127:120]	7:0	See description of '0C24h'.	
	MPIF_LC3A_DATA[127:120]	7:0	See description of '0C24h'.	
11h (0C44h)	**REG0C44**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC3A_MADR[7:0]	7:0	MPIF Logical Channel 3a data to/from MIU base address.	
11h (0C45h)	**REG0C45**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC3A_MADR[15:8]	7:0	See description of '0C44h'.	

MPIF Register (Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description	
12h (0C48h)	**REG0C48**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC3A_MADR[23:16]	7:0	See description of '0C44h'.	
12h (0C49h)	**REG0C49**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC3A_MADR[31:24]	7:0	See description of '0C44h'.	
13h (0C4Ch)	**REG0C4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC3B_RETRX_LIMIT[1:0]	7:6	MPIF re-transmit/receive count limit. 0: 0 time. 1: 1 time. 2: 2 times. 3: 3 times.	
	MPIF_LC3B_RETRX	5	MPIF Logical Channel 3b re-transmit/receive packet indicator.	
	MPIF_LC3B_CHK	4	MPIF Logical Channel 3b check enable.	
	MPIF_LC3B_SID[1:0]	3:2	MPIF Logical Channel 3b Slave ID.	
	MPIF_LC3B_RW	1	MPIF Logical Channel 3b read/write.	
	MPIF_LC3B_VLD	0	MPIF Logical Channel 3b valid.	
13h (0C4Dh)	**REG0C4D**	**7:0**	**Default : 0x40**	**Access : R/W**
	MPIF_LC3B_WCNT[3:0]	7:4	MPIF Logical Channel 3b max wait number.	
	MPIF_LC3B_RX_NWMIU	3	MPIF Logical Channel 3b not wait miu done.	
	MPIF_LC3B_FMODE	2	MPIF Logical Channel 3b fast read/write mode.	
	MPIF_LC3B_MIUSEL	1	MPIF Logical Channel 3b MIU path selection. 0: MIU (SRAM). 1: EMI (SDRAM).	
	MPIF_LC3B_SRC	0	MPIF Logical Channel 3b source/destination selection. 0: To/from RIU. 1: To/from MIU.	
14h (0C50h)	**REG0C50**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC3B_PKTLEN[7:0]	7:0	MPIF Logical Channel 3b packet total length.	
14h (0C51h)	**REG0C51**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC3B_PKTLEN[15:8]	7:0	See description of '0C50h'.	
15h (0C54h)	**REG0C54**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[7:0]	7:0	MPIF Logical Channel 3b data/. SPI data for RIU path.	
	MPIF_LC3B_DATA[7:0]	7:0	MPIF Logical Channel 3b data/. SPI data for RIU path.	

MPIF Register (Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description	
15h (0C55h)	**REG0C55**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[15:8]	7:0	See description of '0C54h'.	
	MPIF_LC3B_DATA[15:8]	7:0	See description of '0C54h'.	
16h (0C58h)	**REG0C58**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[23:16]	7:0	See description of '0C54h'.	
	MPIF_LC3B_DATA[23:16]	7:0	See description of '0C54h'.	
16h (0C59h)	**REG0C59**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[31:24]	7:0	See description of '0C54h'.	
	MPIF_LC3B_DATA[31:24]	7:0	See description of '0C54h'.	
17h (0C5Ch)	**REG0C5C**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[39:32]	7:0	See description of '0C54h'.	
	MPIF_LC3B_DATA[39:32]	7:0	See description of '0C54h'.	
17h (0C5Dh)	**REG0C5D**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[47:40]	7:0	See description of '0C54h'.	
	MPIF_LC3B_DATA[47:40]	7:0	See description of '0C54h'.	
18h (0C60h)	**REG0C60**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[55:48]	7:0	See description of '0C54h'.	
	MPIF_LC3B_DATA[55:48]	7:0	See description of '0C54h'.	
18h (0C61h)	**REG0C61**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[63:56]	7:0	See description of '0C54h'.	
	MPIF_LC3B_DATA[63:56]	7:0	See description of '0C54h'.	
19h (0C64h)	**REG0C64**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[71:64]	7:0	See description of '0C54h'.	
	MPIF_LC3B_DATA[71:64]	7:0	See description of '0C54h'.	
19h (0C65h)	**REG0C65**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[79:72]	7:0	See description of '0C54h'.	
	MPIF_LC3B_DATA[79:72]	7:0	See description of '0C54h'.	
1Ah (0C68h)	**REG0C68**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[87:80]	7:0	See description of '0C54h'.	
	MPIF_LC3B_DATA[87:80]	7:0	See description of '0C54h'.	
1Ah (0C69h)	**REG0C69**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[95:88]	7:0	See description of '0C54h'.	
	MPIF_LC3B_DATA[95:88]	7:0	See description of '0C54h'.	

MPIF Register (Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description	
1Bh (0C6Ch)	**REG0C6C**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[103:96]	7:0	See description of '0C54h'.	
	MPIF_LC3B_DATA[103:96]	7:0	See description of '0C54h'.	
1Bh (0C6Dh)	**REG0C6D**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[111:104]	7:0	See description of '0C54h'.	
	MPIF_LC3B_DATA[111:104]	7:0	See description of '0C54h'.	
1Ch (0C70h)	**REG0C70**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[119:112]	7:0	See description of '0C54h'.	
	MPIF_LC3B_DATA[119:112]	7:0	See description of '0C54h'.	
1Ch (0C71h)	**REG0C71**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	STS_MPIF_LC3B_DATA[127:120]	7:0	See description of '0C54h'.	
	MPIF_LC3B_DATA[127:120]	7:0	See description of '0C54h'.	
1Dh (0C74h)	**REG0C74**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC3B_MADR[7:0]	7:0	MPIF Logical Channel 3b data to/from MIU base address.	
1Dh (0C75h)	**REG0C75**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC3B_MADR[15:8]	7:0	See description of '0C74h'.	
1Eh (0C78h)	**REG0C78**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC3B_MADR[23:16]	7:0	See description of '0C74h'.	
1Eh (0C79h)	**REG0C79**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC3B_MADR[31:24]	7:0	See description of '0C74h'.	
1Fh (0C7Ch)	**REG0C7C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC4A_RETRX_LIMIT [1:0]	7:6	MPIF re-transmit/receive count limit. 0: 0 time. 1: 1 time. 2: 2 times. 3: 3 times.	
	-	5:4	Reserved.	
	MPIF_LC4A_SID[1:0]	3:2	MPIF Logical Channel 4a Slave ID.	
	MPIF_LC4A_RW	1	MPIF Logical Channel 4a read/write.	
	MPIF_LC4A_VLD	0	MPIF Logical Channel 4a valid.	
1Fh (0C7Dh)	**REG0C7D**	**7:0**	**Default : 0x80**	**Access : R/W**
	MPIF_LC4A_WCNT[3:0]	7:4	MPIF Logical Channel 4a max wait number.	

MPIF Register (Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description	
	MPIF_LC4A_GRANULAR[1:0]	3:2	MPIF Logical Channel 4a breakpoint. 00: 1x256 bytes. 01: 2x256 bytes. 10: 3x256 bytes. 11: 4x256 bytes.	
	MPIF_LC4A_MIUSEL	1	MPIF Logical Channel 4a MIU path selection. 0: MIU (SRAM). 1: EMI (SDRAM).	
	MPIF_LC4A_RX_NWMIU	0	MPIF Logical Channel 4a not wait miu done.	
20h (0C80h)	**REG0C80**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC4A_STMLEN[7:0]	7:0	MPIF Logical Channel 4a stream total length (byte unit).	
20h (0C81h)	**REG0C81**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC4A_STMLEN[15:8]	7:0	See description of '0C80h'.	
21h (0C84h)	**REG0C84**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC4A_MADR[7:0]	7:0	MPIF Logical Channel 4a data to/from MIU base address.	
21h (0C85h)	**REG0C85**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC4A_MADR[15:8]	7:0	See description of '0C84h'.	
22h (0C88h)	**REG0C88**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC4A_MADR[23:16]	7:0	See description of '0C84h'.	
22h (0C89h)	**REG0C89**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC4A_MADR[31:24]	7:0	See description of '0C84h'.	
23h (0C8Ch)	**REG0C8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MPIF_4WSPI_DUPLEX	2	MPIF 4-wire SPI duplex enable. Note: Only valid for read command.	
	MPIF_4WSPI_RW	1	MPIF 4-wire SPI read/write.	
	MPIF_4WSPI_VLD	0	MPIF 4-wire SPI valid.	
24h (0C90h)	**REG0C90**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	MPIF_3WSPI_RW	1	MPIF 3-wire SPI read/write.	
	MPIF_3WSPI_VLD	0	MPIF 3-wire SPI valid.	
25h (0C94h)	**REG0C94**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_SPI_TT[1:0]	7:6	MPIF SPI trailing cycle.	

MPIF Register (Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description	
	MPIF_SPI_TL[1:0]	5:4	MPIF SPI leading cycle.	
	MPIF_SPI_CPOL	3	MPIF SPI clock polarity.	
	MPIF_SPI_CPHA	2	MPIF SPI clock phase.	
	MPIF_SPI_SID[1:0]	1:0	MPIF SPI Slave ID.	
25h (0C95h)	**REG0C95**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7	Reserved.	
	MPIF_SPI_RX_NWMIU	6	MPIF SPI not wait miu done.	
	MPIF_SPI_SEP_IO	5	MPIF SPI separate IO mode.	
	MPIF_SPI_MIUSEL	4	MPIF SPI MIU path selection. 0: MIU (SRAM). 1: EMI (SDRAM).	
	MPIF_SPI_SRC	3	MPIF SPI source/destination selection. 0: To/from RIU. 1: To/from MIU.	
	MPIF_SPI_CMD_LEN[2:0]	2:0	MPIF SPI command length. "000" - 0 byte. "001" - 1 byte. "010" - 2 bytes. "011" - 3 bytes. "100" - 4 bytes. "101" - 5 bytes. "110" - 6 bytes. "111" - 7 bytes.	
26h (0C98h)	**REG0C98**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_SPI_CMD[7:0]	7:0	MPIF SPI command value.	
26h (0C99h)	**REG0C99**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_SPI_CMD[15:8]	7:0	See description of '0C98h'.	
27h (0C9Ch)	**REG0C9C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_SPI_CMD[23:16]	7:0	See description of '0C98h'.	
27h (0C9Dh)	**REG0C9D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_SPI_CMD[31:24]	7:0	See description of '0C98h'.	
28h (0CA0h)	**REG0CA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_SPI_DAT_LEN[7:0]	7:0	MPIF SPI data total length (byte unit).	
28h (0CA1h)	**REG0CA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_SPI_DAT_LEN[15:8]	7:0	See description of '0CA0h'.	

MPIF Register (Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description	
29h (0CA4h)	**REG0CA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_SPI_MADR[7:0]	7:0	MPIF SPI MIU base address.	
29h (0CA5h)	**REG0CA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_SPI_MADR[15:8]	7:0	See description of '0CA4h'.	
2Ah (0CA8h)	**REG0CA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_SPI_MADR[23:16]	7:0	See description of '0CA4h'.	
2Ah (0CA9h)	**REG0CA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_SPI_MADR[31:24]	7:0	See description of '0CA4h'.	
2Bh (0CACh)	**REG0CAC**	**7:0**	**Default : 0x00**	**Access : RO**
	MPIF_LC4A_BUSY	7	MPIF Logical Channel 4a busy flag.	
	MPIF_LC3B_BUSY	6	MPIF Logical Channel 3b busy flag.	
	MPIF_LC3A_BUSY	5	MPIF Logical Channel 3a busy flag.	
	MPIF_LC2B_BUSY	4	MPIF Logical Channel 2b busy flag.	
	MPIF_LC2A_BUSY	3	MPIF Logical Channel 2a busy flag.	
	MPIF_LC1A_BUSY	2	MPIF Logical Channel 1a busy flag.	
	MPIF_3WSPI_BUSY	1	MPIF 3-wire SPI busy flag.	
	MPIF_4WSPI_BUSY	0	MPIF 4-wire SPI busy flag.	
2Ch (0CB0h)	**REG0CB0**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_INT_ENABLE[7:0]	7:0	MPIF Interrupt event enable. [0]: 4-wire SPI trx done. [1]: 3-wire SPI trx done. [2]: Logical Channel 1a trx done. [3]: Logical Channel 2a trx done. [4]: Logical Channel 2b trx done. [5]: Logical Channel 3a trx done. [6]: Logical Channel 3b trx done. [7]: Logical Channel 4a trx done. [8]: Logical Channel 2a trx error. [9]: Logical Channel 2b trx error. [10]: Logical Channel 3a trx error. [11]: Logical Channel 3b trx error. [12]: Logical Channel 4a trx error. [13]: Busy time out. [14]: Slave request.	
2Ch (0CB1h)	**REG0CB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

MPIF Register (Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description	
	MPIF_INT_ENABLE[14:8]	6:0	See description of '0CB0h'.	
2Dh (0CB4h)	**REG0CB4**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_LC4A_DONE	7	Logical Channel 4a trx done.	
	MPIF_LC3B_DONE	6	Logical Channel 3b trx done.	
	MPIF_LC3A_DONE	5	Logical Channel 3a trx done.	
	MPIF_LC2B_DONE	4	Logical Channel 2b trx done.	
	MPIF_LC2A_DONE	3	Logical Channel 2a trx done.	
	MPIF_LC1A_DONE	2	Logical Channel 1a trx done.	
	MPIF_3WSPI_DONE	1	3-wire SPI trx done.	
	MPIF_4WSPI_DONE	0	4-wire SPI trx done.	
2Dh (0CB5h)	**REG0CB5**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	MPIF_SLAVE_REQ	6	Slave request.	
	MPIF_BUSY_TIMEOUT	5	MPIF busy time out.	
	MPIF_LC4A_ERR	4	Logical Channel 4a trx error.	
	MPIF_LC3B_ERR	3	Logical Channel 3b trx error.	
	MPIF_LC3A_ERR	2	Logical Channel 3a trx error.	
	MPIF_LC2B_ERR	1	Logical Channel 2b trx error.	
	MPIF_LC2A_ERR	0	Logical Channel 2a trx error.	
2Eh (0CB8h)	**REG0CB8**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_TIMEOUT[7:0]	7:0	MPIF wait time limit for busy de-assert.	
2Eh (0CB9h)	**REG0CB9**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_TIMEOUT[15:8]	7:0	See description of '0CB8h'.	
2Fh	**REG0CBC**	**7:0**	**Default : 0x00**	**Access : RO**

MPIF Register (Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description	
(0CBCh)	STS_BUSY_TO[7:0]	7:0	Busy time out status. [4:0]: command id. "00000" - MPIF_1A_R. "00001" - MPIF_1A_W. "00010" - MPIF_2A_R. "00011" - MPIF_2A_W. "00100" - MPIF_2A_RC. "00101" - MPIF_2A_WC. "00110" - MPIF_2B_R. "00111" - MPIF_2B_W. "01000" - MPIF_2B_RC. "01001" - MPIF_2B_WC. "01010" - MPIF_3A_R. "01011" - MPIF_3A_W. "01100" - MPIF_3A_RC. "01101" - MPIF_3A_WC. "01110" - MPIF_3B_R. "01111" - MPIF_3B_W. "10000" - MPIF_3B_RC. "10001" - MPIF_3B_WC. "10010" - MPIF_4A_R. "10011" - MPIF_4A_W. [9:8]: slave id.	
2Fh (0CBDh)	**REG0CBD**	**7:0**	**Default : 0x00**	**Access : RO**
	STS_BUSY_TO[15:8]	7:0	See description of '0CBCh'.	
30h (0CC0h)	**REG0CC0**	**7:0**	**Default : 0x01**	**Access : R/W**
	MPIF_SLV0_DW[1:0]	7:6	Slave 0 data width. 0: 1. 1: 2. 2: 4. 3: 8.	
	MPIF_WAIT_CYCLE[1:0]	5:4	MPIF wait ACK/NAK cycle. 0: 0T. 1: 1T. 2: 2T. 3: 3T.	

MPIF Register (Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description
	MPIF_TR_CYCLE[1:0]	3:2	MPIF read/write turn around cycle (MSB=h31. [3]). 0: 0T. 1: 1T. 2: 2T. 3: 3T. 4: 4T. 5: 5T. 6: 6T. 7: 7T.
	MPIF_DYNAMIC_GATE_EN	1	MPIF dynamic clock gating enable.
	MPIF_SWRSTN	0	MPIF software reset, active low.
30h (0CC1h)	**REG0CC1**	**7:0**	**Default : 0x00** **Access : R/W**
	MPIF_CMD_DW[1:0]	7:6	Slave 3 data width. 0: 1. 1: 2. 2: 4. 3: 8.
	MPIF_SLV3_DW[1:0]	5:4	Slave 3 data width. 0: 1. 1: 2. 2: 4. 3: 8.
	MPIF_SLV2_DW[1:0]	3:2	Slave 2 data width. 0: 1. 1: 2. 2: 4. 3: 8.
	MPIF_SLV1_DW[1:0]	1:0	Slave 1 data width. 0: 1. 1: 2. 2: 4. 3: 8.
31h (0CC4h)	**REG0CC4**	**7:0**	**Default : 0x10** **Access : R/W**
	CLR_LC4X_ERRCNT	7	Clear Logical Channel 4A error counter.
	CLR_LC3X_ERRCNT	6	Clear Logical Channel 3A/3B error counter.
	CLR_LC2X_ERRCNT	5	Clear Logical Channel 2A/2B error counter.
	MPIF_SRAM_CG_EN	4	SRAM dynamic clock gating enable.

MPIF Register (Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description
	MPIF_TR_CYCLE_B2	3	MPIF read/write turn around cycle MSB bit.
	MPIF_WWTR_CYCLE[2:0]	2:0	MPIF write/write turn around cycle for LC3A/LC3B/LC4A. 0: 0T. 1: 1T. 2: 2T. 3: 3T. 4: 4T. 5: 5T. 6: 6T. 7: 7T.
31h (0CC5h)	**REG0CC5**	**7:0**	**Default : 0x00** **Access : R/W**
	LC3X_NOCHK_TOG_EN	7	Enable LC3X_NOCHK toggle bit enable.
	MPIF_EXTRDCMD_CYCLE[2:0]	6:4	MPIF RX command state extend cycle.
	-	3	Reserved.
	MPIF_MIU_W4WLAST_DONE	2	MPIF_MIU_W4WLAST_DONE.
	MPIF_MIU_PRI1	1	MPIF MIU interface 1 priority.
	MPIF_MIU_PRI0	0	MPIF MIU interface 0 priority.
32h (0CC8h)	**REG0CC8**	**7:0**	**Default : 0x40** **Access : R/W**
	CLK_DLY[3:0]	7:4	PIF_CLK delay selection.
	MPIF_BYPASS_DLY	3	MPIF Bypass delay chain.
	MPIF_BSY_SYNC_EN	2	MPIF Busy Sync Enable.
	SYNC_8B	1	MPIF RX via Feedback path sync boundary. 0: 4 byte boundary. 1: 8 byte boundary.
	RX_FB_ON	0	MPIF RX via Feedback path.
32h (0CC9h)	**REG0CC9**	**7:0**	**Default : 0x44** **Access : R/W**
	DI0_DLY[3:0]	7:4	PIF_DI0 delay selection.
	CSN_DLY[3:0]	3:0	PIF_CSN delay selection.
33h (0CCCh)	**REG0CCC**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:3	Reserved.
	MPIF_SYNC_LEN[2:0]	2:0	MPIF Sync pattern length. 0: 1 bit. … 7: 8 bits.

MPIF Register (Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description	
33h (0CCDh)	**REG0CCD**	**7:0**	**Default : 0x55**	**Access : R/W**
	MPIF_SYNC_PAT[7:0]	7:0	MPIF Sync pattern, LSB first.	
34h (0CD0h)	**REG0CD0**	**7:0**	**Default : 0x00**	**Access : RO**
	STS_SPI_UCPLT_TRX_LEN[7:0]	7:0	MPIF SPI transmit/receive un-complete data length.	
34h (0CD1h)	**REG0CD1**	**7:0**	**Default : 0x00**	**Access : RO**
	STS_SPI_UCPLT_TRX_LEN[15:8]	7:0	See description of '0CD0h'.	
35h (0CD4h)	**REG0CD4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MPIF_DUMMY_WR_LEN	3	MPIF MIU dummy write length. 0: 2. 1: 4.	
	MPIF_DUMMY_WRITE_EN	2	MPIF MIU dummy write enable.	
	MPIF_MIUWR_CLR_OB	1	Clear MIU write out of range status.	
	MPIF_MIU_MASK_WR	0	MPIF MIU write request mask.	
35h (0CD5h)	**REG0CD5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	STS_MIUWR_OB	0	MPIF MIU write address out of range.	
36h (0CD8h)	**REG0CD8**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_MIU_ADR_LB[7:0]	7:0	MPIF MIU write address lower bound.	
36h (0CD9h)	**REG0CD9**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_MIU_ADR_LB[15:8]	7:0	See description of '0CD8h'.	
37h (0CDCh)	**REG0CDC**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_MIU_ADR_LB[23:16]	7:0	See description of '0CD8h'.	
37h (0CDDh)	**REG0CDD**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_MIU_ADR_LB[31:24]	7:0	See description of '0CD8h'.	
38h (0CE0h)	**REG0CE0**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MPIF_MIU_ADR_UB[7:0]	7:0	MPIF MIU write address upper bound.	
38h (0CE1h)	**REG0CE1**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MPIF_MIU_ADR_UB[15:8]	7:0	See description of '0CE0h'.	
39h (0CE4h)	**REG0CE4**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MPIF_MIU_ADR_UB[23:16]	7:0	See description of '0CE0h'.	
39h (0CE5h)	**REG0CE5**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MPIF_MIU_ADR_UB[31:24]	7:0	See description of '0CE0h'.	

MPIF Register (Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description	
3Ah (0CE8h)	**REG0CE8**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_D_GPO[3:0]	7:4	MPIF data pins used as GPO value.	
	MPIF_D_GPO_EN[3:0]	3:0	MPIF data pins used as GPO enable.	
3Ah (0CE9h)	**REG0CE9**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_CS_GPO[3:0]	7:4	MPIF cs pins used as GPO value.	
	MPIF_CS_GPO_EN[3:0]	3:0	MPIF cs pins used as GPO enable.	
3Bh (0CECh)	**REG0CEC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MPIF_THROTTLE_SIZE[1:0]	5:4	MPIF clock throttle boundary in data phase. 0: 4 bytes boundary. 1: 8 bytes boundary. 2: 16 bytes boundary. 3: 32 bytes boundary.	
	-	3:2	Reserved.	
	MPIF_THROTTLE_RATE[1:0]	1:0	MPIF clock throttle rate. 0: 0 cycle. 1: 1 cycle. 2: 2 cycles. 3: 3 cycles.	
3Eh (0CF8h)	**REG0CF8**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_SPARE[7:0]	7:0	MPIF spare registers.	
3Eh (0CF9h)	**REG0CF9**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPIF_SPARE[15:8]	7:0	See description of '0CF8h'.	
3Fh (0CFCh)	**REG0CFC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MPIF_SPARE[23:16]	7:0	See description of '0CF8h'.	
3Fh (0CFDh)	**REG0CFD**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MPIF_SPARE[31:24]	7:0	See description of '0CF8h'.	
40h ~ 4Dh (0D00h~0D34h)		**7:0**	**Default : 0x00**	**Access : RO**
			Reserved.	

GDMA Register (Bank = 07)

GDMA Register (Bank = 07)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (0E00h)	**REG0E00**	**7:0**	**Default : 0x00**	**Access : R/W**
	GDMA_C[7:0]	7:0	GDMA configuration register. BIT [7:6]: Source addressing mode. 00: Fixed. 01: Incremented by one. 10: Reserved. 11: Reserved. BIT [5:4]: Destination addressing mode. 00: Fixed. 01: Incremented by one. 10: Reserved. 11: Reserved. BIT [2]: Interrupt enable. 0: Disable. 1: Enable. BIT [1]: Reset. 0: Reset. 1: Not Reset. BIT [0]: Enable GDMA. 0: Disable. 1: Enable.	
00h (0E01h)	**REG0E01**	**7:0**	**Default : 0x00**	**Access : R/W**
	GDMA_PIU_DS[2:0]	7:5	PIU destination module selection. 011: R2 IQMEM. Other: Reserved.	
	GDMA_PIU_SS[2:0]	4:2	PIU source module selection. 000: SPI. Other: Reserved.	
	GDMA_PATH_SEL[1:0]	1:0	GDMA transfer path selection. 00: MIU----> MIU. 01: PIU ----> MIU. 10: MIU----> PIU. 11: PIU ----> PIU.	
01h (0E04h)	**REG0E04**	**7:0**	**Default : 0x00**	**Access : R/W**
	GDMA_SA[7:0]	7:0	GDMA source address register.	
01h (0E05h)	**REG0E05**	**7:0**	**Default : 0x00**	**Access : R/W**
	GDMA_SA[15:8]	7:0	See description of '0E04h'.	

GDMA Register (Bank = 07)

Index (Absolute)	Mnemonic	Bit	Description	
02h (0E08h)	**REG0E08**	**7:0**	**Default : 0x00**	**Access : R/W**
	GDMA_SA[23:16]	7:0	See description of '0E04h'.	
02h (0E09h)	**REG0E09**	**7:0**	**Default : 0x00**	**Access : R/W**
	GDMA_SA[31:24]	7:0	See description of '0E04h'.	
03h (0E0Ch)	**REG0E0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GDMA_DA[7:0]	7:0	GDMA destination address register.	
03h (0E0Dh)	**REG0E0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	GDMA_DA[15:8]	7:0	See description of '0E0Ch'.	
04h (0E10h)	**REG0E10**	**7:0**	**Default : 0x00**	**Access : R/W**
	GDMA_DA[23:16]	7:0	See description of '0E0Ch'.	
04h (0E11h)	**REG0E11**	**7:0**	**Default : 0x00**	**Access : R/W**
	GDMA_DA[31:24]	7:0	See description of '0E0Ch'.	
05h (0E14h)	**REG0E14**	**7:0**	**Default : 0x00**	**Access : R/W**
	GDMA_TC[7:0]	7:0	GDMA transfer count register.	
05h (0E15h)	**REG0E15**	**7:0**	**Default : 0x00**	**Access : R/W**
	GDMA_TC[15:8]	7:0	See description of '0E14h'.	
06h (0E18h)	**REG0E18**	**7:0**	**Default : 0x00**	**Access : R/W**
	GDMA_TC[23:16]	7:0	See description of '0E14h'.	
07h (0E1Ch)	**REG0E1C**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	GDMA_TRIGGER	0	GDMA transfer start.	
08h (0E20h)	**REG0E20**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	GDMA_TRANSFER_DONE_FLAG	0	Busy status. HW sets to one when transfer is completed. 1: Transfer Done or interrupt pending. 0: Transfer Busy or interrupt not pending.	
09h (0E24h)	**REG0E24**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	GDMA_CLEAR_TRANSFER_DONE	0	SW needs to set this bit to clear transfer_done flag or interrupt in order to receive the subsequent DMA transfer_done flag or interrupt.	

ISP Register (Bank = 08)

ISP Register (Bank = 08)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (1000h)	**REG1000**	**7:0**	**Default : 0x55**	**Access : R/W**
	ISP_PASSWORD[7:0]	7:0	ISP Password 0xAAAA. If password correct, enable ISP. If password incorrect, disable ISP.	
00h (1001h)	**REG1001**	**7:0**	**Default : 0x55**	**Access : R/W**
	ISP_PASSWORD[15:8]	7:0	See description of '1000h'.	
01h (1004h)	**REG1004**	**7:0**	**Default : 0x00**	**Access : WO**
	SPI_COMMAND[7:0]	7:0	SPI command. If write data to this port, ISP will start operation.	
02h (1008h)	**REG1008**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADDRESS1[7:0]	7:0	SPI address 1, A [7:0].	
02h (1009h)	**REG1009**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADDERSS2[7:0]	7:0	SPI address 2, A [15:8].	
03h (100Ch)	**REG100C**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADDRESS3[7:0]	7:0	SPI address 3, A [23:16].	
04h (1010h)	**REG1010**	**7:0**	**Default : 0x00**	**Access : WO**
	WDATA[7:0]	7:0	SPI write data register.	
05h (1014h)	**REG1014**	**7:0**	**Default : 0x00**	**Access : RO**
	RDATA[7:0]	7:0	SPI read data register.	
06h (1018h)	**REG1018**	**7:0**	**Default : 0x04**	**Access : R/W**
	SPI_CLK_DIV16	7	SPI_CLOCK = MCU_CLOCK/16.	
	SPI_CLK_DIV8	6	SPI_CLOCK = MCU_CLOCK/8.	
	SPI_CLK_DIV7	5	Reserved.	
	SPI_CLK_DIV6	4	Reserved.	
	SPI_CLK_DIV5	3	Reserved.	
	SPI_CLK_DIV4	2	SPI_CLOCK = MCU_CLOCK/4.	
	SPI_CLK_DIV3	1	Reserved.	
	SPI_CLK_DIV2	0	SPI_CLOCK = MCU_CLOCK/2.	
06h (1019h)	**REG1019**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SPI_CLK_DIV128	2	SPI_CLOCK = MCU_CLOCK/128.	
	SPI_CLK_DIV64	1	SPI_CLOCK = MCU_CLOCK/64.	

ISP Register (Bank = 08)

Index (Absolute)	Mnemonic	Bit	Description	
	SPI_CLK_DIV32	0	SPI_CLOCK = MCU_CLOCK/32.	
07h (101Ch)	**REG101C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DEVICE_SELECT[2:0]	2:0	Select Device. 000: PMC.MXIC. 001: NextFlash. 010: ST. 011: SST. 100: ATMEL.	
08h (1020h)	**REG1020**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	SPI_CE_CLR	0	SPI chip enable clear. Software can force SPI chip disable at burst SPI read/write, this bit is write-then-clear register. 1: For clear. 0: For not clear.	
09h (1024h)	**REG1024**	**7:0**	**Default : 0x01**	**Access : R/W**
	TCES_TIME[7:0]	7:0	SPI Chip enable setup/hold time. 0x0000: Delay 1 SPI clock. 0x0001: Delay 2 SPI clocks. 0x000f: Delay 16 SPI clocks. 0xffff: Delay 64k SPI clock. Default: Delay 2 SPI clocks.	
09h (1025h)	**REG1025**	**7:0**	**Default : 0x00**	**Access : R/W**
	TCES_TIME[15:8]	7:0	See description of '1024h'.	
0Ah (1028h)	**REG1028**	**7:0**	**Default : 0xF3**	**Access : R/W**
	TBP_TIME[7:0]	7:0	Byte-Program time for device SST. 0x0000: Delay 1 SPI clock. 0x0001: Delay 2 SPI clocks. 0x000f: Delay 16 SPI clocks. 0xffff: Delay 64k SPI clock. Default: Delay 500 SPI clocks. Assume SPI clock 40ns, Delay 500*40 = 20 us.	
0Ah (1029h)	**REG1029**	**7:0**	**Default : 0x01**	**Access : R/W**
	TBP_TIME[15:8]	7:0	See description of '1028h'.	
0Bh	**REG102C**	**7:0**	**Default : 0x04**	**Access : R/W**

ISP Register (Bank = 08)

Index (Absolute)	Mnemonic	Bit	Description	
(102Ch)	TCEH_TIME[7:0]	7:0	SPI Chip enable pulse high time. 0x0000: Delay 1 SPI clock. 0x0001: Delay 2 SPI clocks. 0x000f: Delay 16 SPI clocks. 0xffff: Delay 64k SPI clock. Default: Delay 5 SPI clock.	
0Bh (102Dh)	**REG102D**	**7:0**	**Default : 0x00**	**Access : R/W**
	TCEH_TIME[15:8]	7:0	See description of '102Ch'.	
0Ch (1030h)	**REG1030**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	SPI_RD_REQ	0	SPI READ Data Request. For CPU read SPI data via RIU. If CPU read SPI data via XIU, request is not needed.	
0Dh (1034h)	**REG1034**	**7:0**	**Default : 0x14**	**Access : R/W**
	ISP_RP_ADR1[7:0]	7:0	Programmable ISP Read port address [15:0].	
0Dh (1035h)	**REG1035**	**7:0**	**Default : 0xC2**	**Access : R/W**
	ISP_RP_ADR1[15:8]	7:0	See description of '1034h'.	
0Eh (1038h)	**REG1038**	**7:0**	**Default : 0x81**	**Access : R/W**
	ISP_RP_ADR2[7:0]	7:0	Programmable ISP Read port address [31:0].	
0Eh (1039h)	**REG1039**	**7:0**	**Default : 0x1F**	**Access : R/W**
	ISP_RP_ADR2[15:8]	7:0	See description of '1038h'.	
0Fh (103Ch)	**REG103C**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	ENDIAN_SEL_SPI	0	0: Big_endian. 1: Little_endian.	
10h (1040h)	**REG1040**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	ISP_ACTIVE	0	ISP ACTIVE FLAG.	
11h (1044h)	**REG1044**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	CPU_ACTIVE	1	CPU_ACTIVE FLAG.	
	-	0	Reserved.	
12h (1048h)	**REG1048**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	DMA_ACTIVE	2	DMA_ACTIVE FLAG.	

ISP Register (Bank = 08)

Index (Absolute)	Mnemonic	Bit	Description	
	-	1:0	Reserved.	
13h (104Ch)	**REG104C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	ISP_FSM[5:0]	5:0	ISP_FSM.	
14h (1050h)	**REG1050**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	SPI_MASTER_FSM[2:0]	2:0	SPI_MASTER_FSM.	
15h (1054h)	**REG1054**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	SPI_RD_DATA_RDY	0	SPI Read Data Ready flag. 1: Read data ready. 0: Read data not ready.	
16h (1058h)	**REG1058**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	SPI_WR_DATA_RDY	0	SPI Write Ready flag. 1: Write data ready. 0: Write data not ready.	
17h (105Ch)	**REG105C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	SPI_WR_CM_RDY	0	SPI Write Command Ready flag. 1: Write command ready. 0: Write command not ready.	
18h (1060h)	**REG1060**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	CPU_RST_FM_ISP	0	ISP generates reset to CUP. When ISP programming done, software maybe can issue a reset to CPU.	
19h (1064h)	**REG1064**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	ISP_OLD_EN	0	Read flag, for ISP_OLD_EN.	
20h (1080h)	**REG1080**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	FORCE_ISP_IDLE	0	FORCE_ISP_IDLE.	
21h	**REG1084**	**7:0**	**Default : 0x00**	**Access : R/W**

ISP Register (Bank = 08)

Index (Absolute)	Mnemonic	Bit	Description	
(1084h)	AAI_NUM[7:0]	7:0	For SST SPI FLASH USE. At AAI mode, set how many data will be written. 0x0000: For 1 byte programming. 0x0001: For 2 bytes programming. 0xFFFF: For 64k bytes programming.	
21h (1085h)	**REG1085**	**7:0**	**Default : 0x00**	**Access : R/W**
	AAI_NUM[15:8]	7:0	See description of '1084h'.	
22h (1088h)	**REG1088**	**7:0**	**Default : 0x00**	**Access : R/W**
	PAGE_PRO_REG	7	FORCE SPI COMMAND. Force PAGE PROGRAMMING.	
	FAST_READ_REG	6	FORCE SPI COMMAND. Force FAST READ.	
	READ_REG	5	FORCE SPI COMMAND. Force READ.	
	WRCR_REG	4	FORCE SPI COMMAND. Force WRCR.	
	RDCR_REG	3	FORCE SPI COMMAND. Force RDCR.	
	WRSR_REG	2	FORCE SPI COMMAND. Force WRSR.	
	RDSR_REG	1	FORCE SPI COMMAND. Force RDSR.	
	AAI_REG	0	FORCE SPI COMMAND. Force AAI mode.	
22h (1089h)	**REG1089**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	MAN_ID_REG	1	FORCE SPI COMMAND. Force READ MANUFACTURER ID.	
	B_ERASE_REG	0	FORCE SPI COMMAND. Force BLOCK ERASE.	
25h	**REG1094**	**7:0**	**Default : 0x00**	**Access : R/W**

ISP Register (Bank = 08)

Index (Absolute)	Mnemonic	Bit	Description	
(1094h)	TEST_MODE[7:0]	7:0	TEST_MODE. User define SPI waveform. 0x7777: User define. Others: Not User define. Before entry to TEST_MODE, please make sure ISP/DMA disable.	
25h (1095h)	**REG1095**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_MODE[15:8]	7:0	See description of '1094h'.	
26h (1098h)	**REG1098**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	TEST_SPI_CEB	0	User generates SPI chip enable waveform.	
27h (109Ch)	**REG109C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	TEST_SPI_SCK	0	User generates SPI clock waveform.	
28h (10A0h)	**REG10A0**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	TEST_SPI_SI	0	User generates SPI data waveform.	
29h (10A4h)	**REG10A4**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	TEST_SPI_SO	0	SPI Data output. For RIU read. Please delay 1us for every setting (TEST MODE). EX1. W(0x21,0x0) --> delay 1us --> W(0x23,0x1) -->. Delay 1us --> W(0x22,0x1) --> delay 1us -->. W(0x22,0x0) --> delay 1us .....--> W(ox21,0x1). EX2. W(0x21,0x0) --> delay 1us --> W(0x22,0x1) -->. Delay 1us --> W(0x22,0x0) --> delay 1us -->. R(0x24) --> delay 1us .....> W(0x21,01).	
2Ah (10A8h)	**REG10A8**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRIGGER_MODE[7:0]	7:0	TRIGGER_MODE. 0x3333: Trigger mode. Others: Not Trigger mode. Before entry to Trigger mode, Please make sure ISP/DMA disable.	

ISP Register (Bank = 08)

Index (Absolute)	Mnemonic	Bit	Description	
2Ah (10A9h)	**REG10A9**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRIGGER_MODE[15:8]	7:0	See description of '10A8h'.	
2Fh (10BCh)	**REG10BC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SPI_ABORT_EN	1	Reserved.	
	SPI_PRE_FETCH_EN	0	Reserved.	
37h (10DCh)	**REG10DC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CPHA	1	Configures the data sampling point. When 0: Data is sampled when "SCLK" goes to active state (see reg_cpol). When 1: Data is sampled when "SCLK" goes to idle state (see reg_cpol).	
	CPOL	0	Clock Polarity. Configures the idle state of "SCLK" serial clock when SPI is enabled (when disabled, "SCLK" is at high level). When 1: the "SCLK" output is set as 1; otherwise it is cleared (SCLK = 0).	
3Ch (10F0h)	**REG10F0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_BYPASS_PWD[7:0]	7:0	Force SPI_PAD as input mode. (PWD = 0xaaaa).	
3Ch (10F1h)	**REG10F1**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_BYPASS_PWD[15:8]	7:0	See description of '10F0h'.	
3Fh (10FCh)	**REG10FC**	**7:0**	**Default : 0x07**	**Access : R/W**
	-	7:3	Reserved.	
	SPI_BURST_RESET_Z	2	Software reset spi_burst. 0: Reset. 1: Not reset.	
	SPI_ARBITER_RESET_Z	1	Software reset spi arbiter. 0: Reset. 1 not reset.	
	ISP_TOP_RESET_Z	0	Software reset isp_top. 0: Reset. 1: Not reset.	

FSP Register (Bank = 08)

FSP Register (Bank = 08)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
60h (1180h)	**REG1180**	**7:0**	**Default : 0x00**	**Access : R/W**
	FSP_WD0[7:0]	7:0	Write data buffer0.	
60h (1181h)	**REG1181**	**7:0**	**Default : 0x00**	**Access : R/W**
	FSP_WD1[7:0]	7:0	Write data buffer1.	
61h (1184h)	**REG1184**	**7:0**	**Default : 0x00**	**Access : R/W**
	FSP_WD2[7:0]	7:0	Write data buffer2.	
61h (1185h)	**REG1185**	**7:0**	**Default : 0x00**	**Access : R/W**
	FSP_WD3[7:0]	7:0	Write data buffer3.	
62h (1188h)	**REG1188**	**7:0**	**Default : 0x00**	**Access : R/W**
	FSP_WD4[7:0]	7:0	Write data buffer4.	
62h (1189h)	**REG1189**	**7:0**	**Default : 0x00**	**Access : R/W**
	FSP_WD5[7:0]	7:0	Write data buffer5.	
63h (118Ch)	**REG118C**	**7:0**	**Default : 0x00**	**Access : R/W**
	FSP_WD6[7:0]	7:0	Write data buffer6.	
63h (118Dh)	**REG118D**	**7:0**	**Default : 0x00**	**Access : R/W**
	FSP_WD7[7:0]	7:0	Write data buffer7.	
64h (1190h)	**REG1190**	**7:0**	**Default : 0x00**	**Access : R/W**
	FSP_WD8[7:0]	7:0	Write data buffer8.	
64h (1191h)	**REG1191**	**7:0**	**Default : 0x00**	**Access : R/W**
	FSP_WD9[7:0]	7:0	Write data buffer9.	
65h (1194h)	**REG1194**	**7:0**	**Default : 0x00**	**Access : RO**
	FSP_RD0[7:0]	7:0	Read data buffer0.	
65h (1195h)	**REG1195**	**7:0**	**Default : 0x00**	**Access : RO**
	FSP_RD1[7:0]	7:0	Read data buffer1.	
66h (1198h)	**REG1198**	**7:0**	**Default : 0x00**	**Access : RO**
	FSP_RD2[7:0]	7:0	Read data buffer2.	
66h (1199h)	**REG1199**	**7:0**	**Default : 0x00**	**Access : RO**
	FSP_RD3[7:0]	7:0	Read data buffer3.	
67h (119Ch)	**REG119C**	**7:0**	**Default : 0x00**	**Access : RO**
	FSP_RD4[7:0]	7:0	Read data buffer4.	
67h	**REG119D**	**7:0**	**Default : 0x00**	**Access : RO**

FSP Register (Bank = 08)

Index (Absolute)	Mnemonic	Bit	Description	
(119Dh)	FSP_RD5[7:0]	7:0	Read data buffer5.	
68h (11A0h)	**REG11A0**	**7:0**	**Default : 0x00**	**Access : RO**
	FSP_RD6[7:0]	7:0	Read data buffer6.	
68h (11A1h)	**REG11A1**	**7:0**	**Default : 0x00**	**Access : RO**
	FSP_RD7[7:0]	7:0	Read data buffer7.	
69h (11A4h)	**REG11A4**	**7:0**	**Default : 0x00**	**Access : RO**
	FSP_RD8[7:0]	7:0	Read data buffer8.	
69h (11A5h)	**REG11A5**	**7:0**	**Default : 0x00**	**Access : RO**
	FSP_RD9[7:0]	7:0	Read data buffer9.	
6Ah (11A8h)	**REG11A8**	**7:0**	**Default : 0x00**	**Access : R/W**
	FSP_WBF_SIZE1[3:0]	7:4	Set how many bytes will be transmitted in the second command. Max size is 9Bytes. Min size is 1Byte.	
	FSP_WBF_SIZE0[3:0]	3:0	Set how many bytes will be transmitted in the first command. Max size is 10Bytes. Min size is 1Byte.	
6Ah (11A9h)	**REG11A9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	FSP_WBF_SIZE2[3:0]	3:0	Set how many bytes will be transmitted in the third command. Max size is 8Bytes. Min size is 1Byte.	
6Bh (11ACh)	**REG11AC**	**7:0**	**Default : 0x00**	**Access : R/W**
	FSP_RBF_SIZE1[3:0]	7:4	Set how many bytes will be received in the second command. Max size is 10Bytes. Min size is 0Byte.	
	FSP_RBF_SIZE0[3:0]	3:0	Set how many bytes will be received in the first command. Max size is 10Bytes. Min size is 0Byte.	
6Bh (11ADh)	**REG11AD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

FSP Register (Bank = 08)

Index (Absolute)	Mnemonic	Bit	Description	
	FSP_RBF_SIZE2[3:0]	3:0	Set how many bytes will be received in the third command. Max size is 10 bytes. Min size is 0 byte.	
6Ch (11B0h)	**REG11B0**	**7:0**	**Default : 0x00**	**Access : R/W**
	FSP_CTRL0[7:0]	7:0	Control Register0. Bit [7:4]: Reserved. Bit [3]: Enable auto check error flag. Bit [2]: Enable fsp interrupt. 0: Disable. 1: Enable. Bit [1]: Reset. 0: Reset. 1: Not Reset. Bit [0]: Enable fsp. 0: Disable. 1: Enable.	
6Ch (11B1h)	**REG11B1**	**7:0**	**Default : 0x00**	**Access : R/W**
	FSP_CTRL1[7:0]	7:0	Control Register1. Bit [7]: Enable Second command. 0: Disable. 1: Enable. Bit [6]: Enable third command. 0: Disable. 1: Enable. Bit [5]: Enable auto check flash status. 0: Disable. 1: Enable. Bit [4:3]: Indicate which command is RDSR. 00: First command. 01: Second command. 10: Third command. 11: Reserved. Bit [2:0]: Indicate which bit is flash ready bit (For auto check flash status). Bit [2:0] = 0x0 ~ 0x7, HW will auto check reg_fsp_rd10 [7:0].	
6Dh (11B4h)	**REG11B4**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	FSP_TRIGGER	0	Start flash self-programming.	

FSP Register (Bank = 08)

Index (Absolute)	Mnemonic	Bit	Description	
6Eh (11B8h)	**REG11B8**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	FSP_AUTO_CHK_ERROR	1	Reserved.	
	FSP_DONE_FLAG	0	Busy status, HW sets to 1 when self-programming is completed. 1: Self-programming done or interrupt pending. 0: Self-programming busy or interrupt not pending.	
6Fh (11BCh)	**REG11BC**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	FSP_CLEAR_DONE_FLAG	0	SW needs to set this bit to clear done flag or interrupt.	

QSPI Register (Bank = 08)

QSPI Register (Bank = 08)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
70h (11C0h)	**REG11C0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CKG_SPI[6:0]	6:0	CKG_SPI [5:0]: for spi clock selection. Bit [0]: for gating clock. Bit [1]: for clock invert. Bit [5]: 0, select XTAL. 1, It is decided by Bit [4:2]. Bit [4:2]. 000: XTAL. 001: 27M. 010: 36M. 011: 43M. 100: 54M. 101: 72M. Others: Reserved.	
71h (11C4h)	**REG11C4**	**7:0**	**Default : 0x1A**	**Access : R/W**
	CSZ_SETUP[3:0]	7:4	CSZ setup time.(Relative to SCK). 4'h0: 1 SPI clock cycle. 4'h1: 2 SPI clock cycles. 4'hf: 16 SPI clock cycles.	
	CSZ_HIGH[3:0]	3:0	CSZ deselect time (SCZ = high). 4'h0: 1 SPI clock cycle. 4'h1: 2 SPI clock cycles. 4'hf: 16 SPI clock cycles.	
71h (11C5h)	**REG11C5**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CSZ_HOLD[3:0]	3:0	CSZ hold time. (Relative to SCK). 4'h0: 1 SPI clock cycle. 4'h1: 2 SPI clock cycles. 4'hf: 16 SPI clock cycles.	
72h (11C8h)	**REG11C8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

QSPI Register (Bank = 08)

Index (Absolute)	Mnemonic	Bit	Description	
	MODE_SEL[3:0]	3:0	SPI model select. 0x0: Normal mode, (SPI command is 0x03). 0x1: Enable fast read mode, (SPI command is 0x0B). 0x2: Enable address single & data dual mode, (SPI command is 0x3B). 0x3: Enable address dual & data dual mode, (SPI command is 0xBB). 0xa: Enable address single & data quad mode, (SPI command is 0x6B) (Reserved). 0xb: Enable address quad & data quad mode, (SPI command is 0xEB).(Reserved).	
7Ah (11E8h)	**REG11E8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CHIP_SELECT[1:0]	1:0	00: Select external #1 SPI Flash. 01: Select external #2 SPI Flash. 10: Select external #3 SPI Flash. 11: Reserved.	
7Fh (11FCh)	**REG11FC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	ENDIA	0	For 32bit CPU read data.	

R2_CORE Register (Bank = 09)

R2_CORE Register (Bank = 09)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (1200h)	**REG1200**	**7:0**	**Default : 0x00**	**Access : R/W**
	REV0_0	7	R2 core top control. Bit [0]: r2_enable. Bit [1]: r2_sw_rstz. Bit [2]: miu_sw_rstz. Bit [3]: riu_sw_rstz. Bit [4]: spi_boot. Bit [5]: sdram_boot. Bit [6]:r2_into. Bit [7]: REV0_0.	
	R2_INTO	6	R2 core top control. Bit [0]: r2_enable. Bit [1]: r2_sw_rstz. Bit [2]: miu_sw_rstz. Bit [3]: riu_sw_rstz. Bit [4]: spi_boot. Bit [5]: sdram_boot. Bit [6]: R2_INTO. Bit [7]: rev0_0.	
	SDRAM_BOOT	5	R2 core top control. Bit [0]: r2_enable. Bit [1]: r2_sw_rstz. Bit [2]: miu_sw_rstz. Bit [3]: riu_sw_rstz. Bit [4]: spi_boot. Bit [5]: SDRAM_BOOT. Bit [6]: r2_into. Bit [7]: rev0_0.	
	SPI_BOOT	4	R2 core top control. Bit [0]: r2_enable. Bit [1]: r2_sw_rstz. Bit [2]: miu_sw_rstz. Bit [3]: riu_sw_rstz. Bit [4]: SPI_BOOT. Bit [5]: sdram_boot. Bit [6]: r2_into. Bit [7]: rev0_0.	

R2_CORE Register (Bank = 09)

Index (Absolute)	Mnemonic	Bit	Description	
	RIU_SW_RSTZ	3	R2 core top control. Bit [0]: r2_enable. Bit [1]: r2_sw_rstz. Bit [2]: miu_sw_rstz. Bit [3]: RIU_SW_RSTZ. Bit [4]: spi_boot. Bit [5]: sdram_boot. Bit [6]: r2_into. Bit [7]: rev0_0.	
	MIU_SW_RSTZ	2	R2 core top control. Bit [0]: r2_enable. Bit [1]: r2_sw_rstz. Bit [2]: MIU_SW_RSTZ. Bit [3]: riu_sw_rstz. Bit [4]: spi_boot. Bit [5]: sdram_boot. Bit [6]: r2_into. Bit [7]: rev0_0.	
	R2_SW_RSTZ	1	R2 core top control. Bit [0]: r2_enable. Bit [1]: R2_SW_RSTZ. Bit [2]: miu_sw_rstz. Bit [3]: riu_sw_rstz. Bit [4]: spi_boot. Bit [5]: sdram_boot. Bit [6]: r2_into. Bit [7]: rev0_0.	
	R2_ENABLE	0	R2 core top control. Bit [0]: R2_ENABLE. Bit [1]: r2_sw_rstz. Bit [2]: miu_sw_rstz. Bit [3]: riu_sw_rstz. Bit [4]: spi_boot. Bit [5]: sdram_boot. Bit [6]: r2_into. Bit [7]: rev0_0.	
00h	**REG1201**	**7:0**	**Default : 0x00**	**Access : R/W, WO**

R2_CORE Register (Bank = 09)

Index (Absolute)	Mnemonic	Bit	Description
(1201h)	DBG_SEL_4[3:0]	7:4	R2 core top control. Bit [8]: dbg_on_dcu. Bit [9]: dbg_on_icu. Bit [10]: dbg_clk_sel. Bit [11]: dbg_clk_toggle. Bit [12]: DBG_SEL_4, cpu: 4'd0; icu: 4d1; dcu: 4d2. Bit [13]:DBG_SEL_4. Bit [14]:DBG_SEL_4. Bit [15]: DBG_SEL_4.
	DBG_CLK_TOGGLE	3	R2 core top control. Bit [8]: dbg_on_dcu. Bit [9]: dbg_on_icu. Bit [10]: dbg_clk_sel. Bit [11]: DBG_CLK_TOGGLE. Bit [12]: dbg_sel_4. Bit [13]: dbg_sel_4. Bit [14]: dbg_sel_4. Bit [15]: dbg_sel_4.
	DBG_CLK_SEL	2	R2 core top control. Bit [8]: dbg_on_dcu. Bit [9]: dbg_on_icu. Bit [10]: DBG_CLK_SEL. Bit [11]: dbg_clk_toggle. Bit [12]: dbg_sel_4. Bit [13]: dbg_sel_4. Bit [14]: dbg_sel_4. Bit [15]: dbg_sel_4.
	DBG_ON_ICU	1	R2 core top control. Bit [8]: dbg_on_dcu. Bit [9]: DBG_ON_ICU. Bit [10]: dbg_clk_sel. Bit [11]: dbg_clk_toggle. Bit [12]: dbg_sel_4. Bit [13]: dbg_sel_4. Bit [14]: dbg_sel_4. Bit [15]: dbg_sel_4.

R2_CORE Register (Bank = 09)

Index (Absolute)	Mnemonic	Bit	Description	
	DBG_ON_DCU	0	R2 core top control. Bit [8]: DBG_ON_DCU. Bit [9]: dbg_on_icu. Bit [10]: dbg_clk_sel. Bit [11]: dbg_clk_toggle. Bit [12]: dbg_sel_4. Bit [13]: dbg_sel_4. Bit [14]: dbg_sel_4. Bit [15]: dbg_sel_4.	
01h (1204h)	**REG1204**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_BASE_LOW_INSN[7:0]	7:0	Icu sdr_base_low.	
01h (1205h)	**REG1205**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_BASE_LOW_INSN[15:8]	7:0	See description of '1204h'.	
02h (1208h)	**REG1208**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_BASE_HIGH_INSN[7:0]	7:0	Icu sdr_base_high.	
02h (1209h)	**REG1209**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_BASE_HIGH_INSN[15:8]	7:0	See description of '1208h'.	
03h (120Ch)	**REG120C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_BASE_LOW_DATA[7:0]	7:0	Dcu sdr_base_low.	
03h (120Dh)	**REG120D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_BASE_LOW_DATA[15:8]	7:0	See description of '120Ch'.	
04h (1210h)	**REG1210**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_BASE_HIGH_DATA[7:0]	7:0	Dcu sdr_base_high.	
04h (1211h)	**REG1211**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_BASE_HIGH_DATA[15:8]	7:0	See description of '1210h'.	
05h (1214h)	**REG1214**	**7:0**	**Default : 0x00**	**Access : R/W**
	REG32_BASE[7:0]	7:0	Reg io base => IO [0]: RIU.	
05h (1215h)	**REG1215**	**7:0**	**Default : 0xA0**	**Access : R/W**
	REG32_BASE[15:8]	7:0	See description of '1214h'.	
06h (1218h)	**REG1218**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_MAP_MASK_LOW[7:0]	7:0	SDR_MAP_MASK_LOW.	
06h (1219h)	**REG1219**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_MAP_MASK_LOW[15:8]	7:0	See description of '1218h'.	
07h	**REG121C**	**7:0**	**Default : 0xFF**	**Access : R/W**

R2_CORE Register (Bank = 09)

Index (Absolute)	Mnemonic	Bit	Description	
(121Ch)	SDR_MAP_MASK_HIGH[7:0]	7:0	SDR_MAP_MASK_HIGH.	
07h (121Dh)	**REG121D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SDR_MAP_MASK_HIGH[15:8]	7:0	See description of '121Ch'.	
08h (1220h)	**REG1220**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_BASE[7:0]	7:0	Spi base.	
08h (1221h)	**REG1221**	**7:0**	**Default : 0xD0**	**Access : R/W**
	SPI_BASE[15:8]	7:0	See description of '1220h'.	
09h (1224h)	**REG1224**	**7:0**	**Default : 0x00**	**Access : R/W**
	QMEM_BASE_LOW_INSN[7:0]	7:0	Qmem_base_low.	
09h (1225h)	**REG1225**	**7:0**	**Default : 0x00**	**Access : R/W**
	QMEM_BASE_LOW_INSN[15:8]	7:0	See description of '1224h'.	
0Ah (1228h)	**REG1228**	**7:0**	**Default : 0xFF**	**Access : R/W**
	QMEM_BASE_HIGH_INSN[7:0]	7:0	Qmem_base_high.	
0Ah (1229h)	**REG1229**	**7:0**	**Default : 0xFF**	**Access : R/W**
	QMEM_BASE_HIGH_INSN[15:8]	7:0	See description of '1228h'.	
0Bh (122Ch)	**REG122C**	**7:0**	**Default : 0x00**	**Access : R/W**
	QMEM_MASK_LOW_INSN[7:0]	7:0	Qmem_base_low.	
0Bh (122Dh)	**REG122D**	**7:0**	**Default : 0x80**	**Access : R/W**
	QMEM_MASK_LOW_INSN[15:8]	7:0	See description of '122Ch'.	
0Ch (1230h)	**REG1230**	**7:0**	**Default : 0x00**	**Access : R/W**
	QMEM_MASK_HIGH_INSN[7:0]	7:0	Qmem_base_high.	
0Ch (1231h)	**REG1231**	**7:0**	**Default : 0x00**	**Access : R/W**
	QMEM_MASK_HIGH_INSN[15:8]	7:0	See description of '1230h'.	
0Dh (1234h)	**REG1234**	**7:0**	**Default : 0x00**	**Access : R/W**
	QMEM_BASE_LOW_DATA[7:0]	7:0	Qmem_base_low.	
0Dh (1235h)	**REG1235**	**7:0**	**Default : 0x00**	**Access : R/W**
	QMEM_BASE_LOW_DATA[15:8]	7:0	See description of '1234h'.	
0Eh (1238h)	**REG1238**	**7:0**	**Default : 0x00**	**Access : R/W**
	QMEM_BASE_HIGH_DATA[7:0]	7:0	Qmem_base_high.	
0Eh (1239h)	**REG1239**	**7:0**	**Default : 0x00**	**Access : R/W**
	QMEM_BASE_HIGH_DATA[15:8]	7:0	See description of '1238h'.	
0Fh (123Ch)	**REG123C**	**7:0**	**Default : 0x00**	**Access : R/W**
	QMEM_MASK_LOW_DATA[7:0]	7:0	Qmem_base_low.	

R2_CORE Register (Bank = 09)

Index (Absolute)	Mnemonic	Bit	Description	
0Fh (123Dh)	**REG123D**	**7:0**	**Default : 0x00**	**Access : R/W**
	QMEM_MASK_LOW_DATA[15:8]	7:0	See description of '123Ch'.	
10h (1240h)	**REG1240**	**7:0**	**Default : 0x00**	**Access : R/W**
	QMEM_MASK_HIGH_DATA[7:0]	7:0	Qmem_base_high.	
10h (1241h)	**REG1241**	**7:0**	**Default : 0x00**	**Access : R/W**
	QMEM_MASK_HIGH_DATA[15:8]	7:0	See description of '1240h'.	
11h (1244h)	**REG1244**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR1_BASE[7:0]	7:0	SDR1_BASE.	
11h (1245h)	**REG1245**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR1_BASE[15:8]	7:0	See description of '1244h'.	
12h (1248h)	**REG1248**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR1_MASK[7:0]	7:0	SDR1_MASK.	
12h (1249h)	**REG1249**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR1_MASK[15:8]	7:0	See description of '1248h'.	
13h (124Ch)	**REG124C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR2_BASE[7:0]	7:0	SDR2_BASE.	
13h (124Dh)	**REG124D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR2_BASE[15:8]	7:0	See description of '124Ch'.	
14h (1250h)	**REG1250**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR2_MASK[7:0]	7:0	SDR2_MASK.	
14h (1251h)	**REG1251**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR2_MASK[15:8]	7:0	See description of '1250h'.	
15h (1254h)	**REG1254**	**7:0**	**Default : 0x00**	**Access : R/W**
	IO1_BASE[7:0]	7:0	IO1_BASE => IO[1] : UART.	
15h (1255h)	**REG1255**	**7:0**	**Default : 0x90**	**Access : R/W**
	IO1_BASE[15:8]	7:0	See description of '1254h'.	
16h (1258h)	**REG1258**	**7:0**	**Default : 0x00**	**Access : R/W**
	IO2_BASE[7:0]	7:0	IO2_BASE => IO[2] : SPI data read.	
16h (1259h)	**REG1259**	**7:0**	**Default : 0x00**	**Access : R/W**
	IO2_BASE[15:8]	7:0	See description of '1258h'.	
17h (125Ch)	**REG125C**	**7:0**	**Default : 0x00**	**Access : R/W**
	IO3_BASE[7:0]	7:0	IO3_BASE => IO[3] : IP use.	
17h	**REG125D**	**7:0**	**Default : 0x00**	**Access : R/W**

R2_CORE Register (Bank = 09)

Index (Absolute)	Mnemonic	Bit	Description	
(125Dh)	IO3_BASE[15:8]	7:0	See description of '125Ch'.	
18h (1260h)	**REG1260**	**7:0**	**Default : 0x03**	**Access : R/W**
	WMB_AUTO_OFF	7	WMB_AUTO_OFF.	
	WMB_FORCE_OFF	6	WMB_FORCE_OFF.	
	MMU_IO_EN	5	DMMU_IO_EN.	
	QMEM_SPACE_EN	4	QMEM_SPACE_EN.	
	IO_SPACE_EN[3:0]	3:0	IO_SPACE_EN , default IO[1:0]=[UART, RIU] enable.	
18h (1261h)	**REG1261**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	MMU_ADDRESS_MODE	4	MMU_ADDRESS_MODE.	
	DQM_BANK_SEL[3:0]	3:0	DQM_BANK_SEL.	
19h (1264h)	**REG1264**	**7:0**	**Default : 0x00**	**Access : WO**
	CPU_TOGGLE_REV[7:1]	7:1	CPU_TOGGLE_REV.	
	CPU_WAKE_UP	0	CPU_WAKE_UP.	
19h (1265h)	**REG1265**	**7:0**	**Default : 0x00**	**Access : R/W**
	CPU_REV00[15:8]	7:0	CPU_REV00.	
1Ah (1268h)	**REG1268**	**7:0**	**Default : 0x00**	**Access : R/W**
	CPU_RESET_BASE[7:0]	7:0	CPU_RESET_BASE.	
1Ah (1269h)	**REG1269**	**7:0**	**Default : 0x00**	**Access : R/W**
	CPU_RESET_BASE[15:8]	7:0	See description of '1268h'.	
1Bh (126Ch)	**REG126C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CPU_REV01[7:0]	7:0	CPU_REV01.	
1Bh (126Dh)	**REG126D**	**7:0**	**Default : 0x00**	**Access : R/W**
	CPU_REV01[15:8]	7:0	See description of '126Ch'.	
1Ch (1270h)	**REG1270**	**7:0**	**Default : 0x00**	**Access : R/W**
	CPU_REV02[7:0]	7:0	CPU_REV02.	
1Ch (1271h)	**REG1271**	**7:0**	**Default : 0x00**	**Access : R/W**
	CPU_REV02[15:8]	7:0	See description of '1270h'.	
1Dh (1274h)	**REG1274**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:2	Reserved.	
	R2_JTAG_SEL	1	Jtag_sel.	
	R2_JTAG_BONDOV	0	Jtag_bondov.	
1Eh	**REG1278**	**7:0**	**Default : 0xFF**	**Access : R/W**

R2_CORE Register (Bank = 09)

Index (Absolute)	Mnemonic	Bit	Description	
(1278h)	AHB_MASK_LOW[7:0]	7:0	AHB_MASK_LOW.	
1Eh (1279h)	**REG1279**	**7:0**	**Default : 0xFF**	**Access : R/W**
	AHB_MASK_LOW[15:8]	7:0	See description of '1278h'.	
1Fh (127Ch)	**REG127C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	AHB_MASK_HIGH[7:0]	7:0	AHB_MASK_HIGH.	
1Fh (127Dh)	**REG127D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	AHB_MASK_HIGH[15:8]	7:0	See description of '127Ch'.	
20h (1280h)	**REG1280**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_BITMAP_15_0[7:0]	7:0	BIST_BITMAP_15_0.	
20h (1281h)	**REG1281**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_BITMAP_15_0[15:8]	7:0	See description of '1280h'.	
21h (1284h)	**REG1284**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_BITMAP_31_16[7:0]	7:0	BIST_BITMAP_31_16.	
21h (1285h)	**REG1285**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_BITMAP_31_16[15:8]	7:0	See description of '1284h'.	
22h (1288h)	**REG1288**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_BITMAP_47_32[7:0]	7:0	BIST_BITMAP_47_32.	
22h (1289h)	**REG1289**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_BITMAP_47_32[15:8]	7:0	See description of '1288h'.	
23h (128Ch)	**REG128C**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_BITMAP_63_48[7:0]	7:0	BIST_BITMAP_63_48.	
23h (128Dh)	**REG128D**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_BITMAP_63_48[15:8]	7:0	See description of '128Ch'.	
24h (1290h)	**REG1290**	**7:0**	**Default : 0xC0**	**Access : R/W**
	PRE_FETCH_EN	7	1: Ins pre_fetch enable, 0: disable.	
	PRE_FETCH_BUFFER	6	1: PRE_FETCH_BUFFER size 32 byte, 0: 0 byte.	
	IMEM_BOOT	5	Imem_boot: 1 boot from IMEM.	
	IMEM_SEL	4	Iqmem_select: 1 DMA, 0 CPU.	
	IQMEM_DMA_SRC_SEL[3:0]	3:0	Iqmem_dma_source select.	
24h (1291h)	**REG1291**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	ICU_LOW_POWER	1	1: Power saving for I cache 0: Disable.	

R2_CORE Register (Bank = 09)

Index (Absolute)	Mnemonic	Bit	Description	
	IMEM_LOW_POWER	0	1: Power saving for imem, 0: Disable.	
25h (1294h)	**REG1294**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	INT_USER_MODE_EN	0	INT_USER_MODE_EN.	
26h (1298h)	**REG1298**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	ROM_BIST_DONE[7:1]	7:1	ROM_BIST_DONE.	
	ROM_BIST_START	0	ROM_BIST_START.	
26h (1299h)	**REG1299**	**7:0**	**Default : 0x00**	**Access : RO**
	ROM_BIST_DONE[15:8]	7:0	See description of '1298h'.	
27h (129Ch)	**REG129C**	**7:0**	**Default : 0x00**	**Access : R/W**
	ROM_BIST_GOLD_IROM0[7:0]	7:0	ROM_BIST_GOLD_IROM0.	
27h (129Dh)	**REG129D**	**7:0**	**Default : 0x00**	**Access : RO**
	ROM_BIST_PAT_IROM0[15:8]	7:0	ROM_BIST_PAT_IROM0.	
28h (12A0h)	**REG12A0**	**7:0**	**Default : 0x00**	**Access : R/W**
	ROM_BIST_GOLD_IROM1[7:0]	7:0	ROM_BIST_GOLD_IROM1.	
28h (12A1h)	**REG12A1**	**7:0**	**Default : 0x00**	**Access : RO**
	ROM_BIST_PAT_IROM1[15:8]	7:0	ROM_BIST_PAT_IROM1.	
29h (12A4h)	**REG12A4**	**7:0**	**Default : 0x00**	**Access : R/W**
	ROM_BIST_GOLD_IROM2[7:0]	7:0	ROM_BIST_GOLD_IROM2.	
29h (12A5h)	**REG12A5**	**7:0**	**Default : 0x00**	**Access : RO**
	ROM_BIST_PAT_IROM2[15:8]	7:0	ROM_BIST_PAT_IROM2.	
2Ah (12A8h)	**REG12A8**	**7:0**	**Default : 0x00**	**Access : R/W**
	ROM_BIST_GOLD_IROM3[7:0]	7:0	ROM_BIST_GOLD_IROM3.	
2Ah (12A9h)	**REG12A9**	**7:0**	**Default : 0x00**	**Access : RO**
	ROM_BIST_PAT_IROM3[15:8]	7:0	ROM_BIST_PAT_IROM3.	
2Bh (12ACh)	**REG12AC**	**7:0**	**Default : 0x00**	**Access : R/W**
	ROM_BIST_GOLD_IROM4[7:0]	7:0	ROM_BIST_GOLD_IROM4.	
2Bh (12ADh)	**REG12AD**	**7:0**	**Default : 0x00**	**Access : RO**
	ROM_BIST_PAT_IROM4[15:8]	7:0	ROM_BIST_PAT_IROM4.	
2Ch (12B0h)	**REG12B0**	**7:0**	**Default : 0x00**	**Access : R/W**
	ROM_BIST_GOLD_IROM5[7:0]	7:0	ROM_BIST_GOLD_IROM5.	
2Ch	**REG12B1**	**7:0**	**Default : 0x00**	**Access : RO**

R2_CORE Register (Bank = 09)

Index (Absolute)	Mnemonic	Bit	Description	
(12B1h)	ROM_BIST_PAT_IROM5[15:8]	7:0	ROM_BIST_PAT_IROM5.	
2Dh (12B4h)	**REG12B4**	**7:0**	**Default : 0x00**	**Access : R/W**
	ROM_BIST_GOLD_IROM6[7:0]	7:0	ROM_BIST_GOLD_IROM6.	
2Dh (12B5h)	**REG12B5**	**7:0**	**Default : 0x00**	**Access : RO**
	ROM_BIST_PAT_IROM6[15:8]	7:0	ROM_BIST_PAT_IROM6.	
2Eh (12B8h)	**REG12B8**	**7:0**	**Default : 0x00**	**Access : R/W**
	ROM_BIST_GOLD_IROM7[7:0]	7:0	ROM_BIST_GOLD_IROM7.	
2Eh (12B9h)	**REG12B9**	**7:0**	**Default : 0x00**	**Access : RO**
	ROM_BIST_PAT_IROM7[15:8]	7:0	ROM_BIST_PAT_IROM7.	
2Fh (12BCh)	**REG12BC**	**7:0**	**Default : 0x00**	**Access : R/W**
	ROM_BIST_GOLD_DROM0[7:0]	7:0	ROM_BIST_GOLD_DROM0.	
2Fh (12BDh)	**REG12BD**	**7:0**	**Default : 0x00**	**Access : RO**
	ROM_BIST_PAT_DROM0[15:8]	7:0	ROM_BIST_PAT_DROM0.	
30h (12C0h)	**REG12C0**	**7:0**	**Default : 0x00**	**Access : R/W**
	ROM_BIST_GOLD_DROM1[7:0]	7:0	ROM_BIST_GOLD_DROM1.	
30h (12C1h)	**REG12C1**	**7:0**	**Default : 0x00**	**Access : RO**
	ROM_BIST_PAT_DROM1[15:8]	7:0	ROM_BIST_PAT_DROM1.	
31h (12C4h)	**REG12C4**	**7:0**	**Default : 0x00**	**Access : R/W**
	ROM_BIST_GOLD_DROM2[7:0]	7:0	ROM_BIST_GOLD_DROM2.	
31h (12C5h)	**REG12C5**	**7:0**	**Default : 0x00**	**Access : RO**
	ROM_BIST_PAT_DROM2[15:8]	7:0	ROM_BIST_PAT_DROM2.	
32h (12C8h)	**REG12C8**	**7:0**	**Default : 0x00**	**Access : R/W**
	ROM_BIST_GOLD_DROM3[7:0]	7:0	ROM_BIST_GOLD_DROM3.	
32h (12C9h)	**REG12C9**	**7:0**	**Default : 0x00**	**Access : RO**
	ROM_BIST_PAT_DROM3[15:8]	7:0	ROM_BIST_PAT_DROM3.	

GPS0 Register (Bank = 0A)

GPS0 Register (Bank = 0A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (1400h)	**REG1400**	**7:0**	**Default : 0x00**	**Access : R/W**
	CODE_PHASE[7:0]	7:0		
00h (1401h)	**REG1401**	**7:0**	**Default : 0x00**	**Access : R/W**
	CODE_PHASE[15:8]	7:0	See description of '1400h'.	
01h (1404h)	**REG1404**	**7:0**	**Default : 0x00**	**Access : R/W**
	CODE_PHASE[23:16]	7:0	See description of '1400h'.	
01h (1405h)	**REG1405**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CODE_PHASE[29:24]	5:0	See description of '1400h'.	
02h (1408h)	**REG1408**	**7:0**	**Default : 0x00**	**Access : R/W**
	CODE_FREQ[7:0]	7:0		
02h (1409h)	**REG1409**	**7:0**	**Default : 0x00**	**Access : R/W**
	CODE_FREQ[15:8]	7:0	See description of '1408h'.	
03h (140Ch)	**REG140C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CODE_FREQ[23:16]	7:0	See description of '1408h'.	
03h (140Dh)	**REG140D**	**7:0**	**Default : 0x00**	**Access : R/W**
	CODE_FREQ[31:24]	7:0	See description of '1408h'.	
04h (1410h)	**REG1410**	**7:0**	**Default : 0x00**	**Access : R/W**
	CARR_PHASE[7:0]	7:0		
04h (1411h)	**REG1411**	**7:0**	**Default : 0x00**	**Access : R/W**
	CARR_PHASE[15:8]	7:0	See description of '1410h'.	
05h (1414h)	**REG1414**	**7:0**	**Default : 0x00**	**Access : R/W**
	CARR_PHASE[23:16]	7:0	See description of '1410h'.	
05h (1415h)	**REG1415**	**7:0**	**Default : 0x00**	**Access : R/W**
	CARR_PHASE[31:24]	7:0	See description of '1410h'.	
06h (1418h)	**REG1418**	**7:0**	**Default : 0x00**	**Access : R/W**
	CARR_PHASE[39:32]	7:0	See description of '1410h'.	
08h (1420h)	**REG1420**	**7:0**	**Default : 0x00**	**Access : R/W**
	CARR_FREQ[7:0]	7:0		
08h (1421h)	**REG1421**	**7:0**	**Default : 0x00**	**Access : R/W**
	CARR_FREQ[15:8]	7:0	See description of '1420h'.	

GPS0 Register (Bank = 0A)

Index (Absolute)	Mnemonic	Bit	Description	
09h (1424h)	**REG1424**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CARR_FREQ[19:16]	3:0	See description of '1420h'.	
0Ah (1428h)	**REG1428**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRN_CTRL[7:0]	7:0		
0Ah (1429h)	**REG1429**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRN_CTRL[15:8]	7:0	See description of '1428h'.	
0Bh (142Ch)	**REG142C**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRN_CTRL[23:16]	7:0	See description of '1428h'.	
0Bh (142Dh)	**REG142D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	PRN_CTRL[28:24]	4:0	See description of '1428h'.	
0Ch (1430h)	**REG1430**	**7:0**	**Default : 0x00**	**Access : R/W**
	CHTIME[7:0]	7:0		
0Ch (1431h)	**REG1431**	**7:0**	**Default : 0x00**	**Access : R/W**
	CHTIME[15:8]	7:0	See description of '1430h'.	
0Dh (1434h)	**REG1434**	**7:0**	**Default : 0x00**	**Access : R/W**
	CHTIME[23:16]	7:0	See description of '1430h'.	
0Dh (1435h)	**REG1435**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CHTIME[27:24]	3:0	See description of '1430h'.	
0Eh (1438h)	**REG1438**	**7:0**	**Default : 0x00**	**Access : R/W**
	ACC_CTRL[7:0]	7:0		
0Eh (1439h)	**REG1439**	**7:0**	**Default : 0x00**	**Access : R/W**
	ACC_CTRL[15:8]	7:0	See description of '1438h'.	
0Fh (143Ch)	**REG143C**	**7:0**	**Default : 0x00**	**Access : R/W**
	ACC_CTRL[23:16]	7:0	See description of '1438h'.	
0Fh (143Dh)	**REG143D**	**7:0**	**Default : 0x00**	**Access : R/W**
	ACC_CTRL[31:24]	7:0	See description of '1438h'.	
10h (1440h)	**REG1440**	**7:0**	**Default : 0x00**	**Access : R/W**
	RUN_CTRL[7:0]	7:0		
10h (1441h)	**REG1441**	**7:0**	**Default : 0x00**	**Access : R/W**
	RUN_CTRL[15:8]	7:0	See description of '1440h'.	

GPS0 Register (Bank = 0A)

Index (Absolute)	Mnemonic	Bit	Description	
11h (1444h)	**REG1444**	**7:0**	**Default : 0x00**	**Access : R/W**
	RUN_CTRL[23:16]	7:0	See description of '1440h'.	
11h (1445h)	**REG1445**	**7:0**	**Default : 0x00**	**Access : R/W**
	RUN_CTRL[31:24]	7:0	See description of '1440h'.	
12h (1448h)	**REG1448**	**7:0**	**Default : 0x00**	**Access : RO**
	CODE_PHASE_OBS[7:0]	7:0		
12h (1449h)	**REG1449**	**7:0**	**Default : 0x00**	**Access : RO**
	CODE_PHASE_OBS[15:8]	7:0	See description of '1448h'.	
13h (144Ch)	**REG144C**	**7:0**	**Default : 0x00**	**Access : RO**
	CODE_PHASE_OBS[23:16]	7:0	See description of '1448h'.	
13h (144Dh)	**REG144D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	CODE_PHASE_OBS[29:24]	5:0	See description of '1448h'.	
14h (1450h)	**REG1450**	**7:0**	**Default : 0x00**	**Access : RO**
	CARR_PHASE_OBS[7:0]	7:0		
14h (1451h)	**REG1451**	**7:0**	**Default : 0x00**	**Access : RO**
	CARR_PHASE_OBS[15:8]	7:0	See description of '1450h'.	
15h (1454h)	**REG1454**	**7:0**	**Default : 0x00**	**Access : RO**
	CARR_PHASE_OBS[23:16]	7:0	See description of '1450h'.	
15h (1455h)	**REG1455**	**7:0**	**Default : 0x00**	**Access : RO**
	CARR_PHASE_OBS[31:24]	7:0	See description of '1450h'.	
16h (1458h)	**REG1458**	**7:0**	**Default : 0x00**	**Access : RO**
	CARR_PHASE_OBS[39:32]	7:0	See description of '1450h'.	
18h (1460h)	**REG1460**	**7:0**	**Default : 0x00**	**Access : RO**
	BLANKING_CNTR[7:0]	7:0		
18h (1461h)	**REG1461**	**7:0**	**Default : 0x00**	**Access : RO**
	BLANKING_CNTR[15:8]	7:0	See description of '1460h'.	
19h (1464h)	**REG1464**	**7:0**	**Default : 0x00**	**Access : RO**
	BLANKING_CNTR[23:16]	7:0	See description of '1460h'.	
19h (1465h)	**REG1465**	**7:0**	**Default : 0x00**	**Access : RO**
	BLANKING_CNTR[31:24]	7:0	See description of '1460h'.	
1Ah (1468h)	**REG1468**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS[7:0]	7:0		

GPS0 Register (Bank = 0A)

Index (Absolute)	Mnemonic	Bit	Description	
1Ah (1469h)	**REG1469**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS[15:8]	7:0	See description of '1468h'.	
1Bh (146Ch)	**REG146C**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS[23:16]	7:0	See description of '1468h'.	
1Ch (1470h)	**REG1470**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	PATH_SEL	0	Access Path Select. [0]: RIU. [1]: AEON.	
20h (1480h)	**REG1480**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLK_EN[7:0]	7:0	Sigp submodule clock enable. [0]: CLK_EN_ddc_gps; [1]: CLK_EN_ddc_glns; [2]: CLK_EN_cwr_gps; [3]: CLK_EN_isim; [4]: CLK_EN_dma; [5]: CLK_EN_corr; [6]: CLK_EN_cvc; [7]: CLK_EN_tmg; [8]: CLK_EN_sb; [9]: CLK_EN_ddc_gps_lpf; [10]: CLK_EN_ddc_glns_lpf.	
20h (1481h)	**REG1481**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	CLK_EN[10:8]	2:0	See description of '1480h'.	
21h	**REG1484**	**7:0**	**Default : 0x00**	**Access : R/W**

GPS0 Register (Bank = 0A)

Index (Absolute)	Mnemonic	Bit	Description
(1484h)	RST_Z_VECTOR[7:0]	7:0	Sigp submodule rst_z vector, actove low. [0]: Reg_rst_z_ddc_gps; [1]: Reg_rst_z_ddc_glns; [2]: Reg_rst_z_cwr_gps; [3]: Reg_rst_z_isim; [4]: Reg_rst_z_dma; [5]: Reg_rst_z_corr; [6]: Reg_rst_z_cvc; [7]: Reg_rst_z_tmg; [8]: Reg_rst_z_sb; [9]: Reg_rstz_ddc_gps_lpf; [10]: Reg_rstz_ddc_glns_lpf.
21h (1485h)	**REG1485**	**7:0**	**Default : 0x00** **Access : R/W**
	RST_Z_ALL	7	Sigp global rst_z , actove low.
	-	6:3	Reserved.
	RST_Z_VECTOR[10:8]	2:0	See description of '1484h'.
22h (1488h)	**REG1488**	**7:0**	**Default : 0x00** **Access : RO**
	BIST_STS[7:0]	7:0	BIST status: (0/1 = pass/fail). BIST_FAIL_ROM1, //35. BIST_FAIL_ROM0, //34. BIST_FAIL_CVC_IP1, // 33. BIST_FAIL_CVC_IP0, // 32. BIST_FAIL_CVC_INT3,// 31. BIST_FAIL_CVC_INT2,// 30. BIST_FAIL_CVC_INT1,// 29. BIST_FAIL_CVC_INT0,// 28. BIST_FAIL_FFTRAM, // 27. BIST_FAIL_HISTRAM, // 26. BIST_FAIL_NABRAM1, // 25. BIST_FAIL_NABRAM0, // 24. BIST_FAIL_SRBRAM, // 23. BIST_FAIL_SBRAM5, // 22. BIST_FAIL_SBRAM4, // 21. BIST_FAIL_SBRAM3, // 20. BIST_FAIL_SBRAM2, // 19. BIST_FAIL_SBRAM1, // 18. BIST_FAIL_SBRAM0, // 17. BIST_FAIL_CH0RAM1, // 16. BIST_FAIL_CH0RAM0, // 15.

GPS0 Register (Bank = 0A)

Index (Absolute)	Mnemonic	Bit	Description	
			BIST_FAIL_CH1RAM1, // 14. BIST_FAIL_CH1RAM0, // 13. BIST_FAIL_CH2RAM1, // 12. BIST_FAIL_CH2RAM0, // 11. BIST_FAIL_CH3RAM1, // 10. BIST_FAIL_CH3RAM0, // 9. BIST_FAIL_CH4RAM1, // 8. BIST_FAIL_CH4RAM0, // 7. BIST_FAIL_CH5RAM1, // 6. BIST_FAIL_CH5RAM0, // 5. BIST_FAIL_CH6RAM1, // 4. BIST_FAIL_CH6RAM0, // 3. BIST_FAIL_CH7RAM1, // 2. BIST_FAIL_CH7RAM0, // 1. BIST_FAIL_DMARAM // 0.	
22h (1489h)	**REG1489**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_STS[15:8]	7:0	See description of '1488h'.	
23h (148Ch)	**REG148C**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_STS[23:16]	7:0	See description of '1488h'.	
23h (148Dh)	**REG148D**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_STS[31:24]	7:0	See description of '1488h'.	
24h (1490h)	**REG1490**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_STS[39:32]	7:0	See description of '1488h'.	
2Bh (14ACh)	**REG14AC**	**7:0**	**Default : 0x00**	**Access : RO**
	VERSION_ID[3:0]	7:4	Version ID.	
	REVISION_ID[3:0]	3:0	Revision ID.	
2Ch (14B0h)	**REG14B0**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBG_IP_SEL[7:0]	7:0	IP select for debug port.	
2Ch (14B1h)	**REG14B1**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBG_IP_SEL[15:8]	7:0	See description of '14B0h'.	
2Dh (14B4h)	**REG14B4**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBG_SEL[7:0]	7:0	Debug selection for each module output debug port.	
2Dh (14B5h)	**REG14B5**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBG_SEL[15:8]	7:0	See description of '14B4h'.	
2Eh	**REG14B8**	**7:0**	**Default : 0x00**	**Access : RO**

GPS0 Register (Bank = 0A)

Index (Absolute)	Mnemonic	Bit	Description	
(14B8h)	DBG[7:0]	7:0	Debug data.	
2Eh (14B9h)	**REG14B9**	**7:0**	**Default : 0x00**	**Access : RO**
	DBG[15:8]	7:0	See description of '14B8h'.	
2Fh (14BCh)	**REG14BC**	**7:0**	**Default : 0x00**	**Access : RO**
	DBG[23:16]	7:0	See description of '14B8h'.	
2Fh (14BDh)	**REG14BD**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY[7:0]	7:0	DUMMY register.	
30h (14C0h)	**REG14C0**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	GPS_FILLSTOP	6	Show gps fillstop status (0 - write was stopped).	
	-	5	Reserved.	
	FILL_GPS	4	Enable write to gps part sbram.	
	FILLSTOP_EN	3	1 - fill the requested amount of data and stop.	
	FILL_CYCLE[2:0]	2:0	Buffer Cycles Number: 0 corresponds to 1 cycle.	
30h (14C1h)	**REG14C1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	BLANKING_EN	1	Enable blanking in sbram.	
	INPUT_SEL	0	Enable debug mode in SB.	
32h (14C8h)	**REG14C8**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPS_WPV[7:0]	7:0	Value of gps Write Pointer Virtual.	
32h (14C9h)	**REG14C9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	GPS_WPV[12:8]	4:0	See description of '14C8h'.	
33h (14CCh)	**REG14CC**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPS_WPP[7:0]	7:0	Value of glns Write Pointer Physical.	
33h (14CDh)	**REG14CD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GPS_WPP[11:8]	3:0	See description of '14CCh'.	
36h (14D8h)	**REG14D8**	**7:0**	**Default : 0x00**	**Access : RO**
	RPV[7:0]	7:0	Value of Read Pointer Virtual.	
36h (14D9h)	**REG14D9**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	RPV[13:8]	5:0	See description of '14D8h'.	

GPS0 Register (Bank = 0A)

Index (Absolute)	Mnemonic	Bit	Description	
37h (14DCh)	**REG14DC**	**7:0**	**Default : 0x00**	**Access : R/W**
	RPP[7:0]	7:0	Value of Read Pointer Physical.	
37h (14DDh)	**REG14DD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	RPP[11:8]	3:0	See description of '14DCh'.	
38h (14E0h)	**REG14E0**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPS_MODE_CNT[7:0]	7:0	GPS packets number of current s rate mode.	
38h (14E1h)	**REG14E1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GPS_MODE_CNT[11:8]	3:0	See description of '14E0h'.	
39h (14E4h)	**REG14E4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	GPS_WPV_MOD3[1:0]	5:4	Value of current GPS low rate counter.	
	-	3:1	Reserved.	
	GPS_MODE	0	Value of current GPS s rate mode.	
3Ah (14E8h)	**REG14E8**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[7:0]	7:0	Debug packet in the sbram.	
3Ah (14E9h)	**REG14E9**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[15:8]	7:0	See description of '14E8h'.	
3Bh (14ECh)	**REG14EC**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[23:16]	7:0	See description of '14E8h'.	
3Bh (14EDh)	**REG14ED**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[31:24]	7:0	See description of '14E8h'.	
3Ch (14F0h)	**REG14F0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[39:32]	7:0	See description of '14E8h'.	
3Ch (14F1h)	**REG14F1**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[47:40]	7:0	See description of '14E8h'.	
3Dh (14F4h)	**REG14F4**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[55:48]	7:0	See description of '14E8h'.	
3Dh (14F5h)	**REG14F5**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[63:56]	7:0	See description of '14E8h'.	
3Eh (14F8h)	**REG14F8**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[71:64]	7:0	See description of '14E8h'.	

GPS0 Register (Bank = 0A)

Index (Absolute)	Mnemonic	Bit	Description	
3Eh (14F9h)	**REG14F9**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[79:72]	7:0	See description of '14E8h'.	
3Fh (14FCh)	**REG14FC**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[87:80]	7:0	See description of '14E8h'.	
3Fh (14FDh)	**REG14FD**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[95:88]	7:0	See description of '14E8h'.	
40h (1500h)	**REG1500**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[103:96]	7:0	See description of '14E8h'.	
40h (1501h)	**REG1501**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[111:104]	7:0	See description of '14E8h'.	
41h (1504h)	**REG1504**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[119:112]	7:0	See description of '14E8h'.	
41h (1505h)	**REG1505**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[127:120]	7:0	See description of '14E8h'.	
42h (1508h)	**REG1508**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[135:128]	7:0	See description of '14E8h'.	
42h (1509h)	**REG1509**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[143:136]	7:0	See description of '14E8h'.	
43h (150Ch)	**REG150C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[151:144]	7:0	See description of '14E8h'.	
43h (150Dh)	**REG150D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[159:152]	7:0	See description of '14E8h'.	
44h (1510h)	**REG1510**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[167:160]	7:0	See description of '14E8h'.	
44h (1511h)	**REG1511**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[175:168]	7:0	See description of '14E8h'.	
45h (1514h)	**REG1514**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[183:176]	7:0	See description of '14E8h'.	
45h (1515h)	**REG1515**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[191:184]	7:0	See description of '14E8h'.	
46h (1518h)	**REG1518**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[199:192]	7:0	See description of '14E8h'.	
46h	**REG1519**	**7:0**	**Default : 0x00**	**Access : R/W**

GPS0 Register (Bank = 0A)

Index (Absolute)	Mnemonic	Bit	Description	
(1519h)	SBRAM_PACKET[207:200]	7:0	See description of '14E8h'.	
47h (151Ch)	**REG151C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[215:208]	7:0	See description of '14E8h'.	
47h (151Dh)	**REG151D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[223:216]	7:0	See description of '14E8h'.	
48h (1520h)	**REG1520**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[231:224]	7:0	See description of '14E8h'.	
48h (1521h)	**REG1521**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[239:232]	7:0	See description of '14E8h'.	
49h (1524h)	**REG1524**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[247:240]	7:0	See description of '14E8h'.	
49h (1525h)	**REG1525**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[255:248]	7:0	See description of '14E8h'.	
4Ah (1528h)	**REG1528**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[263:256]	7:0	See description of '14E8h'.	
4Ah (1529h)	**REG1529**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[271:264]	7:0	See description of '14E8h'.	
4Bh (152Ch)	**REG152C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[279:272]	7:0	See description of '14E8h'.	
4Bh (152Dh)	**REG152D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[287:280]	7:0	See description of '14E8h'.	
4Ch (1530h)	**REG1530**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[295:288]	7:0	See description of '14E8h'.	
4Ch (1531h)	**REG1531**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[303:296]	7:0	See description of '14E8h'.	
4Dh (1534h)	**REG1534**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[311:304]	7:0	See description of '14E8h'.	
4Dh (1535h)	**REG1535**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[319:312]	7:0	See description of '14E8h'.	
4Eh (1538h)	**REG1538**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[327:320]	7:0	See description of '14E8h'.	
4Eh (1539h)	**REG1539**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[335:328]	7:0	See description of '14E8h'.	

GPS0 Register (Bank = 0A)

Index (Absolute)	Mnemonic	Bit	Description	
4Fh (153Ch)	**REG153C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[343:336]	7:0	See description of '14E8h'.	
4Fh (153Dh)	**REG153D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[351:344]	7:0	See description of '14E8h'.	
50h (1540h)	**REG1540**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[359:352]	7:0	See description of '14E8h'.	
50h (1541h)	**REG1541**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[367:360]	7:0	See description of '14E8h'.	
51h (1544h)	**REG1544**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[375:368]	7:0	See description of '14E8h'.	
51h (1545h)	**REG1545**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBRAM_PACKET[383:376]	7:0	See description of '14E8h'.	
52h (1548h)	**REG1548**	**7:0**	**Default : 0x00**	**Access : RO**
	GPS_ME_MARKER[7:0]	7:0	Value of gps me marker.	
52h (1549h)	**REG1549**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	GPS_ME_MARKER[12:8]	4:0	See description of '1548h'.	
54h (1550h)	**REG1550**	**7:0**	**Default : 0x00**	**Access : RO**
	WATCHER_STATUS[7:0]	7:0	Value of watcher interrupts.	
54h (1551h)	**REG1551**	**7:0**	**Default : 0x00**	**Access : RO**
	WATCHER_STATUS[15:8]	7:0	See description of '1550h'.	
55h (1554h)	**REG1554**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	WATCHER_STATUS[19:16]	3:0	See description of '1550h'.	
56h (1558h)	**REG1558**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	WATCHER_NUM[4:0]	4:0	Debug number of watcher channel.	
57h (155Ch)	**REG155C**	**7:0**	**Default : 0x00**	**Access : R/W**
	WATCHER_MARK[7:0]	7:0	Debug mark of current debug watcher channel.	
57h (155Dh)	**REG155D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	WATCHER_MARK[14:8]	6:0	See description of '155Ch'.	
59h	**REG1564**	**7:0**	**Default : 0x00**	**Access : R/W**

GPS0 Register (Bank = 0A)

Index (Absolute)	Mnemonic	Bit	Description	
(1564h)	LONG_IRQ_LENGTH[7:0]	7:0	Duration of long irq (in packets).	
59h (1565h)	**REG1565**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	LONG_IRQ_LENGTH[13:8]	5:0	See description of '1564h'.	
5Ah (1568h)	**REG1568**	**7:0**	**Default : 0x00**	**Access : R/W**
	SHORT_IRQ_LENGTH[7:0]	7:0	Duration of short irq (in packets).	
5Bh (156Ch)	**REG156C**	**7:0**	**Default : 0x00**	**Access : R/W**
	WRME_LENGTH[7:0]	7:0	Duration of WRME signal (in packets).	
5Bh (156Dh)	**REG156D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	WRME_LENGTH[13:8]	5:0	See description of '156Ch'.	
5Ch (1570h)	**REG1570**	**7:0**	**Default : 0x00**	**Access : R/W**
	MINT_LENGTH[7:0]	7:0	Delay of MINT signal after WRME (in packets).	
5Ch (1571h)	**REG1571**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MINT_LENGTH[13:8]	5:0	See description of '1570h'.	
5Eh (1578h)	**REG1578**	**7:0**	**Default : 0x00**	**Access : RO**
	GPS_BLANKING[7:0]	7:0	Value of gps blanking counter in SigBuffer.	
5Eh (1579h)	**REG1579**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	GPS_BLANKING[14:8]	6:0	See description of '1578h'.	
60h (1580h)	**REG1580**	**7:0**	**Default : 0x00**	**Access : R/W**
	INIT_G2[7:0]	7:0	Satellite Vehicle Gold Code Initial Phase. If written with zero the code is disabled.	
60h (1581h)	**REG1581**	**7:0**	**Default : 0x00**	**Access : R/W**
	SN_MIX_MODE[1:0]	7:6	S_N_Mixer_MODE (2'd1), 0/1/2/3 = Noise/Sig+Noise/Sig/Zero.	
	SIG_POWER[3:0]	5:2	Signal_power (4'd12).	
	INIT_G2[9:8]	1:0	See description of '1580h'.	
61h (1584h)	**REG1584**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	ISIM_BLANKING_EN	3	ISIM blanking function enable ('1' - ISIM mode, '0' - normal mode).	

GPS0 Register (Bank = 0A)

Index (Absolute)	Mnemonic	Bit	Description	
	SAT_DATA_EN	2	GPS Satellite Data Enabled.	
	-	1	Reserved.	
	WORK_EN	0	Internal Simulation Enabled.	
62h (1588h)	**REG1588**	**7:0**	**Default : 0x00**	**Access : R/W**
	CODE_PHASE_INC[7:0]	7:0	Code Increment.	
62h (1589h)	**REG1589**	**7:0**	**Default : 0x00**	**Access : R/W**
	CODE_PHASE_INC[15:8]	7:0	See description of '1588h'.	
63h (158Ch)	**REG158C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CODE_PHASE_INC[23:16]	7:0	See description of '1588h'.	
63h (158Dh)	**REG158D**	**7:0**	**Default : 0x00**	**Access : R/W**
	CODE_PHASE_INC[31:24]	7:0	See description of '1588h'.	
64h (1590h)	**REG1590**	**7:0**	**Default : 0x00**	**Access : R/W**
	CARR_PHASE_INC[7:0]	7:0	Doppler + IF Increment.	
64h (1591h)	**REG1591**	**7:0**	**Default : 0x00**	**Access : R/W**
	CARR_PHASE_INC[15:8]	7:0	See description of '1590h'.	
65h (1594h)	**REG1594**	**7:0**	**Default : 0x00**	**Access : R/W**
	CARR_PHASE_INC[23:16]	7:0	See description of '1590h'.	
65h (1595h)	**REG1595**	**7:0**	**Default : 0x00**	**Access : R/W**
	CARR_PHASE_INC[31:24]	7:0	See description of '1590h'.	
66h (1598h)	**REG1598**	**7:0**	**Default : 0x00**	**Access : R/W**
	NOISE_SEED[7:0]	7:0	Noise Seed.	
66h (1599h)	**REG1599**	**7:0**	**Default : 0x00**	**Access : R/W**
	NOISE_SEED[15:8]	7:0	See description of '1598h'.	
67h (159Ch)	**REG159C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAT_DATA[7:0]	7:0	Satellite Data.	
67h (159Dh)	**REG159D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAT_DATA[15:8]	7:0	See description of '159Ch'.	
68h (15A0h)	**REG15A0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAT_DATA[23:16]	7:0	See description of '159Ch'.	
68h (15A1h)	**REG15A1**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAT_DATA[31:24]	7:0	See description of '159Ch'.	
69h (15A4h)	**REG15A4**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAT_DATA[39:32]	7:0	See description of '159Ch'.	

GPS0 Register (Bank = 0A)

Index (Absolute)	Mnemonic	Bit	Description	
69h (15A5h)	**REG15A5**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAT_DATA[47:40]	7:0	See description of '159Ch'.	
6Ah (15A8h)	**REG15A8**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAT_DATA[55:48]	7:0	See description of '159Ch'.	
6Ah (15A9h)	**REG15A9**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAT_DATA[63:56]	7:0	See description of '159Ch'.	
6Bh (15ACh)	**REG15AC**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAT_DATA[71:64]	7:0	See description of '159Ch'.	
6Bh (15ADh)	**REG15AD**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAT_DATA[79:72]	7:0	See description of '159Ch'.	
6Ch (15B0h)	**REG15B0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAT_DATA[87:80]	7:0	See description of '159Ch'.	
6Ch (15B1h)	**REG15B1**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAT_DATA[95:88]	7:0	See description of '159Ch'.	
6Dh (15B4h)	**REG15B4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SAT_DATA[99:96]	3:0	See description of '159Ch'.	
76h (15D8h)	**REG15D8**	**7:0**	**Default : 0x00**	**Access : R/W**
	BLANKING_1_LENGTH[7:0]	7:0	Blanking active length (in master clocks).	
76h (15D9h)	**REG15D9**	**7:0**	**Default : 0x00**	**Access : R/W**
	BLANKING_1_LENGTH[15:8]	7:0	See description of '15D8h'.	
77h (15DCh)	**REG15DC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	BLANKING_1_LENGTH[18:16]	2:0	See description of '15D8h'.	

GPS1 Register (Bank = 0B)

GPS1 Register (Bank = 0B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (1604h)	**REG1604**	**7:0**	**Default : 0x30**	**Access : R/W**
	-	7:6	Reserved.	
	DDC_SW_RST	5	Software reset for ddc circuit, 1 for reset.	
	CWR_SW_RST	4	Software reset for cwr circuit, 1 for reset.	
	FLOW_CONTROL[3:0]	3:0	CWR unit control mode setting. bit3: 0 for auto mode, 1 for manual mode. bit2: (manual mode) 1 for active CWR detection. bit1: (manual mode) 1 for active CWR selection. bit0: (manual mode) 1 for active notch coefficient calculator.	
02h (1608h)	**REG1608**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CLK_2X_MODE	4	(RTL use) 1: clock 2x filter, 0: clock_1x filter (for FPGA).	
	ISIM_IN_SEL	3	ISIM test pattern input selection. 1: ISIM pattern. 0: RF input.	
	DDC_DEBUG_SEL[2:0]	2:0	Debug output. 000: Disable. 001: Afe input. 010: Ddc_mixer input. 011: Ddc_lpf input. 100: Ddc_intp input. 101: Ddc_adap_qua input. 110: ISIM output.	
03h (160Ch)	**REG160C**	**7:0**	**Default : 0x10**	**Access : R/W**
	FREQ_MIXER0[7:0]	7:0	First frequency of CWR mixer (= freq_mixer/2^14 * fs).	
03h (160Dh)	**REG160D**	**7:0**	**Default : 0x45**	**Access : R/W**
	SWEEP_MODE[1:0]	7:6	Sweep mode: 0=> fixed, 1=>mode1 (4 histogram) 2=>mode2 (8 histogram).	
	FREQ_MIXER0[13:8]	5:0	See description of '160Ch'.	
04h (1610h)	**REG1610**	**7:0**	**Default : 0x09**	**Access : R/W**
	INIT_PN[7:0]	7:0	Initial noise power as floating format.	
04h (1611h)	**REG1611**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:2	Reserved.	

GPS1 Register (Bank = 0B)

Index (Absolute)	Mnemonic	Bit	Description	
	INIT_PN[9:8]	1:0	See description of '1610h'.	
05h (1614h)	**REG1614**	**7:0**	**Default : 0x90**	**Access : R/W**
	LEAKAGE_MODE	7	0/1: turn off/on leakage.	
	PN_RATIO[6:0]	6:0	Ratio to exclude non-noise signals, <4,3>. Ratio = PN_RATIO*2^-3.	
05h (1615h)	**REG1615**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:6	Reserved.	
	LTH3[5:0]	5:0	Leakage threshold of floating exponent for alpha=1-2^-3 <5,0>.	
06h (1618h)	**REG1618**	**7:0**	**Default : 0x4E**	**Access : R/W**
	LTH5[1:0]	7:6	Leakage threshold of floating exponent for alpha=1-2^-5 <5,0>.	
	LTH4[5:0]	5:0	Leakage threshold of floating exponent for alpha=1-2^-4 <5,0>.	
06h (1619h)	**REG1619**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:4	Reserved.	
	LTH5[5:2]	3:0	See description of '1618h'.	
07h (161Ch)	**REG161C**	**7:0**	**Default : 0x04**	**Access : R/W**
	SCALE_THRES_IN[7:0]	7:0	Dynamic scale threshold of FFT.	
07h (161Dh)	**REG161D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SCALE_THRES_IN[9:8]	1:0	See description of '161Ch'.	
08h (1620h)	**REG1620**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	FFT_LATENCY[1:0]	4:3	(RTL use) 0: 2048 samples at 16MHzl, 1: 4096, 2: 8192.	
	UPDATE_NOTCH_HIST[2:0]	2:0	Update notch filter for each 2^n histogram, 3-b, (n=0~7).	
09h (1624h)	**REG1624**	**7:0**	**Default : 0x40**	**Access : R/W**
	MAX_NP[7:0]	7:0	Max. number exceeding threshold during a cluster.	
09h (1625h)	**REG1625**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:3	Reserved.	
	MAX_NH[2:0]	2:0	Number of hysterics for CW selection.	
0Ah	**REG1628**	**7:0**	**Default : 0xE0**	**Access : R/W**

GPS1 Register (Bank = 0B)

Index (Absolute)	Mnemonic	Bit	Description	
(1628h)	FC0[7:0]	7:0	Frequency of histogram index 0, <-1, 14>. (1296-4*140=736=0x2E0).	
0Ah (1629h)	**REG1629**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:5	Reserved.	
	FC0[12:8]	4:0	See description of '1628h'.	
0Bh (162Ch)	**REG162C**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7	Reserved.	
	TH_RATIO[6:0]	6:0	Threshold ratio for CW tones <4,3>. Ratio=TH_RATIO*2^-3. Threshold=ratio * estimated_noise_power.	
0Bh (162Dh)	**REG162D**	**7:0**	**Default : 0x0C**	**Access : R/W**
	-	7	Reserved.	
	INTP_R1[6:0]	6:0	Ratio 1 of linear interpolator <4,3>. R1=INTP_R1*2^-3.	
0Ch (1630h)	**REG1630**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7	Reserved.	
	INTP_R2[6:0]	6:0	Ratio 2 of linear interpolator <4,3>. R2=INTP_R2*2^-3.	
0Dh (1634h)	**REG1634**	**7:0**	**Default : 0x1E**	**Access : R/W**
	TH_PN1[7:0]	7:0	CW power threshold ratio 1, <8,0>. TH1=255x.	
0Dh (1635h)	**REG1635**	**7:0**	**Default : 0x3A**	**Access : R/W**
	TH_PN2[7:0]	7:0	CW power threshold ratio 2, <7,1>. TH2=225*2^-1=112.5x.	
0Eh (1638h)	**REG1638**	**7:0**	**Default : 0x50**	**Access : R/W**
	TH_PN3[7:0]	7:0	CW power threshold ratio 3, <6,2>. TH3=160*2^-2=40x.	
0Eh (1639h)	**REG1639**	**7:0**	**Default : 0x23**	**Access : R/W**
	TH_PN4[7:0]	7:0	CW power threshold ratio 4, <5,3>. TH4=35*2^-3=4.375x.	
0Fh (163Ch)	**REG163C**	**7:0**	**Default : 0x0C**	**Access : R/W**
	-	7:5	Reserved.	
	A2FIX_M1[4:0]	4:0	A2fix setting=12, main lobe, >80dBHz, cascade 2 notch filters.	
0Fh	**REG163D**	**7:0**	**Default : 0x1F**	**Access : R/W**

GPS1 Register (Bank = 0B)

Index (Absolute)	Mnemonic	Bit	Description	
(163Dh)	-	7:5	Reserved.	
	A2FIX_M10[4:0]	4:0	A2fix setting=31, main lobe, >80dBHz, 1 notch filters.	
10h (1640h)	**REG1640**	**7:0**	**Default : 0x0C**	**Access : R/W**
	-	7:5	Reserved.	
	A2FIX_S1[4:0]	4:0	A2fix setting=12, side lobe, >80dBHz, cascade 2 notch filters.	
10h (1641h)	**REG1641**	**7:0**	**Default : 0x1F**	**Access : R/W**
	-	7:5	Reserved.	
	A2FIX_S10[4:0]	4:0	A2fix setting=31, side lobe, >80dBHz, 1 notch filters.	
11h (1644h)	**REG1644**	**7:0**	**Default : 0x07**	**Access : R/W**
	-	7:5	Reserved.	
	A2FIX_M2[4:0]	4:0	A2fix setting=7, main lobe, >70dBHz, cascade 2 notch filters.	
11h (1645h)	**REG1645**	**7:0**	**Default : 0x1F**	**Access : R/W**
	-	7:5	Reserved.	
	A2FIX_M20[4:0]	4:0	A2fix setting=31, main lobe, >70dBHz, 1 notch filters.	
12h (1648h)	**REG1648**	**7:0**	**Default : 0x07**	**Access : R/W**
	-	7:5	Reserved.	
	A2FIX_S2[4:0]	4:0	A2fix setting=7, side lobe, >70dBHz,. Cascade 2 notch filters.	
12h (1649h)	**REG1649**	**7:0**	**Default : 0x1F**	**Access : R/W**
	-	7:5	Reserved.	
	A2FIX_S20[4:0]	4:0	A2fix setting=31, side lobe, >70dBHz, 1 notch filters.	
13h (164Ch)	**REG164C**	**7:0**	**Default : 0x05**	**Access : R/W**
	-	7:5	Reserved.	
	A2FIX_M3[4:0]	4:0	A2fix setting=5, main lobe, >60dBHz, cascade 2 notch filters.	
13h (164Dh)	**REG164D**	**7:0**	**Default : 0x0E**	**Access : R/W**
	-	7:5	Reserved.	
	A2FIX_M30[4:0]	4:0	A2fix setting=14, main lobe, >60dBHz, 1 notch filters.	
14h (1650h)	**REG1650**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	A2FIX_S30[4:0]	4:0	A2fix setting=20, side lobe, >60dBHz, 1 notch filters.	

GPS1 Register (Bank = 0B)

Index (Absolute)	Mnemonic	Bit	Description	
14h (1651h)	**REG1651**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:5	Reserved.	
	A2FIX_M4[4:0]	4:0	A2fix setting=4, main lobe, >50dBHz, cascade 2 notch filters.	
15h (1654h)	**REG1654**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:5	Reserved.	
	A2FIX_M40[4:0]	4:0	A2fix setting=8, main lobe, >50dBHz, 1 notch filters.	
15h (1655h)	**REG1655**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:5	Reserved.	
	A2FIX_S40[4:0]	4:0	A2fix setting=8, side lobe, >50dBHz, 1 notch filters.	
16h (1658h)	**REG1658**	**7:0**	**Default : 0x05**	**Access : R/W**
	-	7:5	Reserved.	
	A2FIX_M50[4:0]	4:0	A2fix setting=5, main lobe, <50dBHz, 1 notch filters.	
16h (1659h)	**REG1659**	**7:0**	**Default : 0x05**	**Access : R/W**
	-	7:5	Reserved.	
	A2FIX_S50[4:0]	4:0	A2fix setting=5, side lobe, <50dBHz, 1 notch filters.	
17h (165Ch)	**REG165C**	**7:0**	**Default : 0xE8**	**Access : R/W**
	FC_TH_HI[7:0]	7:0	Main lobe boundary: high threshold.	
17h (165Dh)	**REG165D**	**7:0**	**Default : 0x13**	**Access : R/W**
	-	7:5	Reserved.	
	FC_TH_HI[12:8]	4:0	See description of '165Ch'.	
18h (1660h)	**REG1660**	**7:0**	**Default : 0x18**	**Access : R/W**
	FC_TH_LO[7:0]	7:0	Main lobe boundary: low threshold.	
18h (1661h)	**REG1661**	**7:0**	**Default : 0x0C**	**Access : R/W**
	-	7:5	Reserved.	
	FC_TH_LO[12:8]	4:0	See description of '1660h'.	
19h (1664h)	**REG1664**	**7:0**	**Default : 0x00**	**Access : R/W**
	DELTA_PH[7:0]	7:0	DDC_mixer center frequency. Fc/fs*2^24 (4.092/16.368*2^24).	
19h (1665h)	**REG1665**	**7:0**	**Default : 0x00**	**Access : R/W**
	DELTA_PH[15:8]	7:0	See description of '1664h'.	
1Ah (1668h)	**REG1668**	**7:0**	**Default : 0x40**	**Access : R/W**
	DELTA_PH[23:16]	7:0	See description of '1664h'.	

GPS1 Register (Bank = 0B)

Index (Absolute)	Mnemonic	Bit	Description	
1Bh (166Ch)	**REG166C**	**7:0**	**Default : 0x2B**	**Access : R/W**
	INV_R[7:0]	7:0	Reciprocal of r=fout/fs, format: <4,4>. =>INV_R=fs/fout*2^4 (16.368/6.144*2^4).	
1Ch (1670h)	**REG1670**	**7:0**	**Default : 0x06**	**Access : R/W**
	NCO_INC[7:0]	7:0	NCO_INC of interpolator, format: <0,64>. Ft/fs (ft: target freq.) (6.144/16.368*2^64).	
1Ch (1671h)	**REG1671**	**7:0**	**Default : 0x18**	**Access : R/W**
	NCO_INC[15:8]	7:0	See description of '1670h'.	
1Dh (1674h)	**REG1674**	**7:0**	**Default : 0x60**	**Access : R/W**
	NCO_INC[23:16]	7:0	See description of '1670h'.	
1Dh (1675h)	**REG1675**	**7:0**	**Default : 0x80**	**Access : R/W**
	NCO_INC[31:24]	7:0	See description of '1670h'.	
1Eh (1678h)	**REG1678**	**7:0**	**Default : 0x01**	**Access : R/W**
	NCO_INC[39:32]	7:0	See description of '1670h'.	
1Eh (1679h)	**REG1679**	**7:0**	**Default : 0x06**	**Access : R/W**
	NCO_INC[47:40]	7:0	See description of '1670h'.	
1Fh (167Ch)	**REG167C**	**7:0**	**Default : 0x18**	**Access : R/W**
	NCO_INC[55:48]	7:0	See description of '1670h'.	
1Fh (167Dh)	**REG167D**	**7:0**	**Default : 0x60**	**Access : R/W**
	NCO_INC[63:56]	7:0	See description of '1670h'.	
20h (1680h)	**REG1680**	**7:0**	**Default : 0x00**	**Access : R/W**
	TH_LOAD[7:0]	7:0	Initial threshold value of adaptive quantizer.	
20h (1681h)	**REG1681**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	
	TH_LOAD[13:8]	5:0	See description of '1680h'.	
21h (1684h)	**REG1684**	**7:0**	**Default : 0x07**	**Access : R/W**
	-	7:4	Reserved.	
	FRAC_TH[3:0]	3:0	Number bits of threshold fractional parts (as convergent rate). Limited to 0-10.	
23h (168Ch)	**REG168C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	WCNT_SW[7:0]	7:0	Bit12=0, Start to switch when word count=WCNT_SW[11:0]. Bit12=1 (WCNT_SW='1FFF') start to switch at any wcnt.	

GPS1 Register (Bank = 0B)

Index (Absolute)	Mnemonic	Bit	Description	
23h (168Dh)	**REG168D**	**7:0**	**Default : 0x1F**	**Access : R/W**
	-	7:6	Reserved.	
	MODE2M6M	5	0: Switch to 2M, 1: switch to 6M.	
	WCNT_SW[12:8]	4:0	See description of '168Ch'.	
24h (1690h)	**REG1690**	**7:0**	**Default : 0x00**	**Access : R/W**
	COEF_A2FIX_1[2:0]	7:5	Notch filter coefficient software control.	
	COEF_A2FIX_0[4:0]	4:0	Notch filter coefficient software control.	
24h (1691h)	**REG1691**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	COEF_A2FIX_2[4:0]	6:2	Notch filter coefficient software control.	
	COEF_A2FIX_1[4:3]	1:0	See description of '1690h'.	
25h (1694h)	**REG1694**	**7:0**	**Default : 0x00**	**Access : R/W**
	COEF_A2FIX_4[2:0]	7:5	Notch filter coefficient software control.	
	COEF_A2FIX_3[4:0]	4:0	Notch filter coefficient software control.	
25h (1695h)	**REG1695**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	COEF_A2FIX_5[4:0]	6:2	Notch filter coefficient software control.	
	COEF_A2FIX_4[4:3]	1:0	See description of '1694h'.	
26h (1698h)	**REG1698**	**7:0**	**Default : 0x00**	**Access : R/W**
	COEF_A2FIX_7[2:0]	7:5	Notch filter coefficient software control.	
	COEF_A2FIX_6[4:0]	4:0	Notch filter coefficient software control.	
26h (1699h)	**REG1699**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	COEF_A2FIX_8[4:0]	6:2	Notch filter coefficient software control.	
	COEF_A2FIX_7[4:3]	1:0	See description of '1698h'.	
27h (169Ch)	**REG169C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	COEF_A2FIX_9[4:0]	4:0	Notch filter coefficient software control.	
28h (16A0h)	**REG16A0**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IIR_BYPASS_CONTROL[7:0]	7:0	Notch filter bypass control, 10bits for 10 filters, bit=1/0: bypass/enable, LSB bits is for notch#0.	
28h (16A1h)	**REG16A1**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	

GPS1 Register (Bank = 0B)

Index (Absolute)	Mnemonic	Bit	Description	
	IIR_BYPASS_CONTROL[9:8]	1:0	See description of '16A0h'.	
29h (16A4h)	**REG16A4**	**7:0**	**Default : 0x00**	**Access : R/W**
	COEF_A1_0[7:0]	7:0	Notch filter coefficient software control.	
29h (16A5h)	**REG16A5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	COEF_A1_0[14:8]	6:0	See description of '16A4h'.	
2Ah (16A8h)	**REG16A8**	**7:0**	**Default : 0x00**	**Access : R/W**
	COEF_A1_1[7:0]	7:0	Notch filter coefficient software control.	
2Ah (16A9h)	**REG16A9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	COEF_A1_1[14:8]	6:0	See description of '16A8h'.	
2Bh (16ACh)	**REG16AC**	**7:0**	**Default : 0x00**	**Access : R/W**
	COEF_A1_2[7:0]	7:0	Notch filter coefficient software control.	
2Bh (16ADh)	**REG16AD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	COEF_A1_2[14:8]	6:0	See description of '16ACh'.	
2Ch (16B0h)	**REG16B0**	**7:0**	**Default : 0x00**	**Access : R/W**
	COEF_A1_3[7:0]	7:0	Notch filter coefficient software control.	
2Ch (16B1h)	**REG16B1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	COEF_A1_3[14:8]	6:0	See description of '16B0h'.	
2Dh (16B4h)	**REG16B4**	**7:0**	**Default : 0x00**	**Access : R/W**
	COEF_A1_4[7:0]	7:0	Notch filter coefficient software control.	
2Dh (16B5h)	**REG16B5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	COEF_A1_4[14:8]	6:0	See description of '16B4h'.	
2Eh (16B8h)	**REG16B8**	**7:0**	**Default : 0x00**	**Access : R/W**
	COEF_A1_5[7:0]	7:0	Notch filter coefficient software control.	
2Eh (16B9h)	**REG16B9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	COEF_A1_5[14:8]	6:0	See description of '16B8h'.	
2Fh (16BCh)	**REG16BC**	**7:0**	**Default : 0x00**	**Access : R/W**
	COEF_A1_6[7:0]	7:0	Notch filter coefficient software control.	

GPS1 Register (Bank = 0B)

Index (Absolute)	Mnemonic	Bit	Description	
2Fh (16BDh)	**REG16BD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	COEF_A1_6[14:8]	6:0	See description of '16BCh'.	
30h (16C0h)	**REG16C0**	**7:0**	**Default : 0x00**	**Access : R/W**
	COEF_A1_7[7:0]	7:0	Notch filter coefficient software control.	
30h (16C1h)	**REG16C1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	COEF_A1_7[14:8]	6:0	See description of '16C0h'.	
31h (16C4h)	**REG16C4**	**7:0**	**Default : 0x00**	**Access : R/W**
	COEF_A1_8[7:0]	7:0	Notch filter coefficient software control.	
31h (16C5h)	**REG16C5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	COEF_A1_8[14:8]	6:0	See description of '16C4h'.	
32h (16C8h)	**REG16C8**	**7:0**	**Default : 0x00**	**Access : R/W**
	COEF_A1_9[7:0]	7:0	Notch filter coefficient software control.	
32h (16C9h)	**REG16C9**	**7:0**	**Default : 0x00**	**Access : R/W**
	COEF_CPU_SET_PULSE	7	Notch filter coefficient active. SW: Setting as 0->1->0 (need two steps).	
	COEF_A1_9[14:8]	6:0	See description of '16C8h'.	
33h (16CCh)	**REG16CC**	**7:0**	**Default : 0x00**	**Access : R/W**
	READ_HIST_ADDR[7:0]	7:0	Hist ram read address.	
33h (16CDh)	**REG16CD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CPU_READ_PULSE	4	Hist ram read active. SW: Setting as 0->1->0 (need two steps).	
	-	3	Reserved.	
	READ_HIST_ADDR[10:8]	2:0	See description of '16CCh'.	
35h (16D4h)	**REG16D4**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	STATE_CWR[4:0]	4:0	State machine for cwr.	
35h (16D5h)	**REG16D5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	STATE_NOTCH_CALC[2:0]	6:4	State machine for notch calc.	

GPS1 Register (Bank = 0B)

Index (Absolute)	Mnemonic	Bit	Description	
	STATE_SELECT[3:0]	3:0	State machine for select.	
36h (16D8h)	**REG16D8**	**7:0**	**Default : 0x00**	**Access : RO**
	READ_HIST_DATA[7:0]	7:0	Hist ram data out.	
36h (16D9h)	**REG16D9**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	NC[3:0]	5:2	Select output.	
	READ_HIST_DATA[9:8]	1:0	See description of '16D8h'.	
37h (16DCh)	**REG16DC**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_FC_0[7:0]	7:0	Select output.	
37h (16DDh)	**REG16DD**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	CLUSTER_FC_0[12:8]	4:0	See description of '16DCh'.	
38h (16E0h)	**REG16E0**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_FC_1[7:0]	7:0	Select output.	
38h (16E1h)	**REG16E1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	CLUSTER_FC_1[12:8]	4:0	See description of '16E0h'.	
39h (16E4h)	**REG16E4**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_FC_2[7:0]	7:0	Select output.	
39h (16E5h)	**REG16E5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	CLUSTER_FC_2[12:8]	4:0	See description of '16E4h'.	
3Ah (16E8h)	**REG16E8**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_FC_3[7:0]	7:0	Select output.	
3Ah (16E9h)	**REG16E9**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	CLUSTER_FC_3[12:8]	4:0	See description of '16E8h'.	
3Bh (16ECh)	**REG16EC**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_FC_4[7:0]	7:0	Select output.	
3Bh (16EDh)	**REG16ED**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	CLUSTER_FC_4[12:8]	4:0	See description of '16ECh'.	
3Ch	**REG16F0**	**7:0**	**Default : 0x00**	**Access : RO**

GPS1 Register (Bank = 0B)

Index (Absolute)	Mnemonic	Bit	Description	
(16F0h)	CLUSTER_FC_5[7:0]	7:0	Select output.	
3Ch (16F1h)	**REG16F1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	CLUSTER_FC_5[12:8]	4:0	See description of '16F0h'.	
3Dh (16F4h)	**REG16F4**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_FC_6[7:0]	7:0	Select output.	
3Dh (16F5h)	**REG16F5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	CLUSTER_FC_6[12:8]	4:0	See description of '16F4h'.	
3Eh (16F8h)	**REG16F8**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_FC_7[7:0]	7:0	Select output.	
3Eh (16F9h)	**REG16F9**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	CLUSTER_FC_7[12:8]	4:0	See description of '16F8h'.	
3Fh (16FCh)	**REG16FC**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_FC_8[7:0]	7:0	Select output.	
3Fh (16FDh)	**REG16FD**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	CLUSTER_FC_8[12:8]	4:0	See description of '16FCh'.	
40h (1700h)	**REG1700**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_FC_9[7:0]	7:0	Select output.	
40h (1701h)	**REG1701**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	CLUSTER_FC_9[12:8]	4:0	See description of '1700h'.	
41h (1704h)	**REG1704**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_IDX_0[7:0]	7:0	Select output.	
41h (1705h)	**REG1705**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	CLUSTER_IDX_0[10:8]	2:0	See description of '1704h'.	
42h (1708h)	**REG1708**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_IDX_1[7:0]	7:0	Select output.	
42h (1709h)	**REG1709**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	

GPS1 Register (Bank = 0B)

Index (Absolute)	Mnemonic	Bit	Description	
	CLUSTER_IDX_1[10:8]	2:0	See description of '1708h'.	
43h (170Ch)	**REG170C**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_IDX_2[7:0]	7:0	Select output.	
43h (170Dh)	**REG170D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	CLUSTER_IDX_2[10:8]	2:0	See description of '170Ch'.	
44h (1710h)	**REG1710**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_IDX_3[7:0]	7:0	Select output.	
44h (1711h)	**REG1711**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	CLUSTER_IDX_3[10:8]	2:0	See description of '1710h'.	
45h (1714h)	**REG1714**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_IDX_4[7:0]	7:0	Select output.	
45h (1715h)	**REG1715**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	CLUSTER_IDX_4[10:8]	2:0	See description of '1714h'.	
46h (1718h)	**REG1718**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_IDX_5[7:0]	7:0	Select output.	
46h (1719h)	**REG1719**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	CLUSTER_IDX_5[10:8]	2:0	See description of '1718h'.	
47h (171Ch)	**REG171C**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_IDX_6[7:0]	7:0	Select output.	
47h (171Dh)	**REG171D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	CLUSTER_IDX_6[10:8]	2:0	See description of '171Ch'.	
48h (1720h)	**REG1720**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_IDX_7[7:0]	7:0	Select output.	
48h (1721h)	**REG1721**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	CLUSTER_IDX_7[10:8]	2:0	See description of '1720h'.	
49h (1724h)	**REG1724**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_IDX_8[7:0]	7:0	Select output.	

GPS1 Register (Bank = 0B)

Index (Absolute)	Mnemonic	Bit	Description	
49h (1725h)	**REG1725**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	CLUSTER_IDX_8[10:8]	2:0	See description of '1724h'.	
4Ah (1728h)	**REG1728**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_IDX_9[7:0]	7:0	Select output.	
4Ah (1729h)	**REG1729**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	CLUSTER_IDX_9[10:8]	2:0	See description of '1728h'.	
4Bh (172Ch)	**REG172C**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_NUM_POW_0[7:0]	7:0	Select output.	
4Bh (172Dh)	**REG172D**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_NUM_POW_1[7:0]	7:0	Select output.	
4Ch (1730h)	**REG1730**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_NUM_POW_2[7:0]	7:0	Select output.	
4Ch (1731h)	**REG1731**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_NUM_POW_3[7:0]	7:0	Select output.	
4Fh (173Ch)	**REG173C**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_NUM_POW_4[7:0]	7:0	Select output.	
4Fh (173Dh)	**REG173D**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_NUM_POW_5[7:0]	7:0	Select output.	
50h (1740h)	**REG1740**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_NUM_POW_6[7:0]	7:0	Select output.	
50h (1741h)	**REG1741**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_NUM_POW_7[7:0]	7:0	Select output.	
51h (1744h)	**REG1744**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_NUM_POW_8[7:0]	7:0	Select output.	
51h (1745h)	**REG1745**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_NUM_POW_9[7:0]	7:0	Select output.	
52h (1748h)	**REG1748**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_POW_0[7:0]	7:0	Select output.	
52h (1749h)	**REG1749**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	CLUSTER_POW_0[9:8]	1:0	See description of '1748h'.	

GPS1 Register (Bank = 0B)

Index (Absolute)	Mnemonic	Bit	Description	
53h (174Ch)	**REG174C**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_POW_1[7:0]	7:0	Select output.	
53h (174Dh)	**REG174D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	CLUSTER_POW_1[9:8]	1:0	See description of '174Ch'.	
54h (1750h)	**REG1750**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_POW_2[7:0]	7:0	Select output.	
54h (1751h)	**REG1751**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	CLUSTER_POW_2[9:8]	1:0	See description of '1750h'.	
55h (1754h)	**REG1754**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_POW_3[7:0]	7:0	Select output.	
55h (1755h)	**REG1755**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	CLUSTER_POW_3[9:8]	1:0	See description of '1754h'.	
56h (1758h)	**REG1758**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_POW_4[7:0]	7:0	Select output.	
56h (1759h)	**REG1759**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	CLUSTER_POW_4[9:8]	1:0	See description of '1758h'.	
57h (175Ch)	**REG175C**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_POW_5[7:0]	7:0	Select output.	
57h (175Dh)	**REG175D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	CLUSTER_POW_5[9:8]	1:0	See description of '175Ch'.	
58h (1760h)	**REG1760**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_POW_6[7:0]	7:0	Select output.	
58h (1761h)	**REG1761**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	CLUSTER_POW_6[9:8]	1:0	See description of '1760h'.	
59h (1764h)	**REG1764**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_POW_7[7:0]	7:0	Select output.	
59h	**REG1765**	**7:0**	**Default : 0x00**	**Access : RO**

GPS1 Register (Bank = 0B)

Index (Absolute)	Mnemonic	Bit	Description	
(1765h)	-	7:2	Reserved.	
	CLUSTER_POW_7[9:8]	1:0	See description of '1764h'.	
5Ah (1768h)	**REG1768**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_POW_8[7:0]	7:0	Select output.	
5Ah (1769h)	**REG1769**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	CLUSTER_POW_8[9:8]	1:0	See description of '1768h'.	
5Bh (176Ch)	**REG176C**	**7:0**	**Default : 0x00**	**Access : RO**
	CLUSTER_POW_9[7:0]	7:0	Select output.	
5Bh (176Dh)	**REG176D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	CLUSTER_POW_9[9:8]	1:0	See description of '176Ch'.	
5Ch (1770h)	**REG1770**	**7:0**	**Default : 0x00**	**Access : RO**
	SORT_ARRAY_1[3:0]	7:4	Select output.	
	SORT_ARRAY_0[3:0]	3:0	Select output.	
5Ch (1771h)	**REG1771**	**7:0**	**Default : 0x00**	**Access : RO**
	SORT_ARRAY_3[3:0]	7:4	Select output.	
	SORT_ARRAY_2[3:0]	3:0	Select output.	
5Dh (1774h)	**REG1774**	**7:0**	**Default : 0x00**	**Access : RO**
	SORT_ARRAY_5[3:0]	7:4	Select output.	
	SORT_ARRAY_4[3:0]	3:0	Select output.	
5Dh (1775h)	**REG1775**	**7:0**	**Default : 0x00**	**Access : RO**
	SORT_ARRAY_7[3:0]	7:4	Select output.	
	SORT_ARRAY_6[3:0]	3:0	Select output.	
5Eh (1778h)	**REG1778**	**7:0**	**Default : 0x00**	**Access : RO**
	SORT_ARRAY_9[3:0]	7:4	Select output.	
	SORT_ARRAY_8[3:0]	3:0	Select output.	
5Fh (177Ch)	**REG177C**	**7:0**	**Default : 0x00**	**Access : RO**
	READ_COEF_A2FIX_1[2:0]	7:5	Coefficient output.	
	READ_COEF_A2FIX_0[4:0]	4:0	Coefficient output.	
5Fh (177Dh)	**REG177D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	READ_COEF_A2FIX_2[4:0]	6:2	Coefficient output.	

GPS1 Register (Bank = 0B)

Index (Absolute)	Mnemonic	Bit	Description	
	READ_COEF_A2FIX_1[4:3]	1:0	See description of '177Ch'.	
60h (1780h)	**REG1780**	**7:0**	**Default : 0x00**	**Access : RO**
	READ_COEF_A2FIX_4[2:0]	7:5	Coefficient output.	
	READ_COEF_A2FIX_3[4:0]	4:0	Coefficient output.	
60h (1781h)	**REG1781**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	READ_COEF_A2FIX_5[4:0]	6:2	Coefficient output.	
	READ_COEF_A2FIX_4[4:3]	1:0	See description of '1780h'.	
61h (1784h)	**REG1784**	**7:0**	**Default : 0x00**	**Access : RO**
	READ_COEF_A2FIX_7[2:0]	7:5	Coefficient output.	
	READ_COEF_A2FIX_6[4:0]	4:0	Coefficient output.	
61h (1785h)	**REG1785**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	READ_COEF_A2FIX_8[4:0]	6:2	Coefficient output.	
	READ_COEF_A2FIX_7[4:3]	1:0	See description of '1784h'.	
62h (1788h)	**REG1788**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	READ_COEF_A2FIX_9[4:0]	4:0	Coefficient output.	
63h (178Ch)	**REG178C**	**7:0**	**Default : 0x00**	**Access : RO**
	READ_COEF_A1_0[7:0]	7:0	Coefficient output.	
63h (178Dh)	**REG178D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	READ_COEF_A1_0[14:8]	6:0	See description of '178Ch'.	
64h (1790h)	**REG1790**	**7:0**	**Default : 0x00**	**Access : RO**
	READ_COEF_A1_1[7:0]	7:0	Coefficient output.	
64h (1791h)	**REG1791**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	READ_COEF_A1_1[14:8]	6:0	See description of '1790h'.	
65h (1794h)	**REG1794**	**7:0**	**Default : 0x00**	**Access : RO**
	READ_COEF_A1_2[7:0]	7:0	Coefficient output.	
65h (1795h)	**REG1795**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	READ_COEF_A1_2[14:8]	6:0	See description of '1794h'.	

GPS1 Register (Bank = 0B)

Index (Absolute)	Mnemonic	Bit	Description	
66h (1798h)	**REG1798**	**7:0**	**Default : 0x00**	**Access : RO**
	READ_COEF_A1_3[7:0]	7:0	Coefficient output.	
66h (1799h)	**REG1799**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	READ_COEF_A1_3[14:8]	6:0	See description of '1798h'.	
67h (179Ch)	**REG179C**	**7:0**	**Default : 0x00**	**Access : RO**
	READ_COEF_A1_4[7:0]	7:0	Coefficient output.	
67h (179Dh)	**REG179D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	READ_COEF_A1_4[14:8]	6:0	See description of '179Ch'.	
68h (17A0h)	**REG17A0**	**7:0**	**Default : 0x00**	**Access : RO**
	READ_COEF_A1_5[7:0]	7:0	Coefficient output.	
68h (17A1h)	**REG17A1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	READ_COEF_A1_5[14:8]	6:0	See description of '17A0h'.	
69h (17A4h)	**REG17A4**	**7:0**	**Default : 0x00**	**Access : RO**
	READ_COEF_A1_6[7:0]	7:0	Coefficient output.	
69h (17A5h)	**REG17A5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	READ_COEF_A1_6[14:8]	6:0	See description of '17A4h'.	
6Ah (17A8h)	**REG17A8**	**7:0**	**Default : 0x00**	**Access : RO**
	READ_COEF_A1_7[7:0]	7:0	Coefficient output.	
6Ah (17A9h)	**REG17A9**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	READ_COEF_A1_7[14:8]	6:0	See description of '17A8h'.	
6Bh (17ACh)	**REG17AC**	**7:0**	**Default : 0x00**	**Access : RO**
	READ_COEF_A1_8[7:0]	7:0	Coefficient output.	
6Bh (17ADh)	**REG17AD**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	READ_COEF_A1_8[14:8]	6:0	See description of '17ACh'.	
6Ch (17B0h)	**REG17B0**	**7:0**	**Default : 0x00**	**Access : RO**
	READ_COEF_A1_9[7:0]	7:0	Coefficient output.	
6Ch	**REG17B1**	**7:0**	**Default : 0x00**	**Access : RO**

GPS1 Register (Bank = 0B)

Index (Absolute)	Mnemonic	Bit	Description	
(17B1h)	-	7	Reserved.	
	READ_COEF_A1_9[14:8]	6:0	See description of '17B0h'.	
6Dh (17B4h)	**REG17B4**	**7:0**	**Default : 0x00**	**Access : RO**
	FS_CHANGE_WP[7:0]	7:0	Fs change write point.	
6Dh (17B5h)	**REG17B5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	MODE2M6M_BOUNDARY	5	2m6m boundary indicator for sigbuf.	
	FS_CHANGE_WP[12:8]	4:0	See description of '17B4h'.	
70h (17C0h)	**REG17C0**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_STATUS[7:0]	7:0	Interrupt Status.	
70h (17C1h)	**REG17C1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	IRQ_STATUS[12:8]	4:0	See description of '17C0h'.	
71h (17C4h)	**REG17C4**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_EN[7:0]	7:0	Interrupt Enable (0=disable, 1=enable).	
71h (17C5h)	**REG17C5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	IRQ_EN[12:8]	4:0	See description of '17C4h'.	
72h (17C8h)	**REG17C8**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_CLR[7:0]	7:0	Interrupt status clear (0=nothing, 1=clear bit).	
72h (17C9h)	**REG17C9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	IRQ_CLR[12:8]	4:0	See description of '17C8h'.	
73h (17CCh)	**REG17CC**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER[7:0]	7:0	Debug TIMER.	
73h (17CDh)	**REG17CD**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER[15:8]	7:0	See description of '17CCh'.	
74h (17D0h)	**REG17D0**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER[23:16]	7:0	See description of '17CCh'.	
74h (17D1h)	**REG17D1**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER[31:24]	7:0	See description of '17CCh'.	
75h (17D4h)	**REG17D4**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM_CTRL[7:0]	7:0	PWM control Register.	

GPS1 Register (Bank = 0B)

Index (Absolute)	Mnemonic	Bit	Description	
75h (17D5h)	**REG17D5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	PWM_CTRL[10:8]	2:0	See description of '17D4h'.	
76h (17D8h)	**REG17D8**	**7:0**	**Default : 0x00**	**Access : RO**
	FIX_CNTR[7:0]	7:0	PWM fix counter.	
77h (17DCh)	**REG17DC**	**7:0**	**Default : 0x00**	**Access : RO**
	PWM_DATA[7:0]	7:0	PWM data reg.	
77h (17DDh)	**REG17DD**	**7:0**	**Default : 0x00**	**Access : RO**
	PWM_DATA[15:8]	7:0	See description of '17DCh'.	
78h (17E0h)	**REG17E0**	**7:0**	**Default : 0x00**	**Access : RO**
	PWM_DATA[23:16]	7:0	See description of '17DCh'.	
78h (17E1h)	**REG17E1**	**7:0**	**Default : 0x00**	**Access : RO**
	PWM_DATA[31:24]	7:0	See description of '17DCh'.	
79h (17E4h)	**REG17E4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	READ_LATCH	0	Latch for regs more then 16bits.	
7Ah (17E8h)	**REG17E8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	F_BLANKING[1:0]	1:0	Force blanking reg: 0bit - gps, 1bit - glns.	

GPS2 Register (Bank = 0C)

GPS2 Register (Bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (1800h)	**REG1800**	**7:0**	**Default : 0x00**	**Access : RO**
	EVENT0[7:0]	7:0	TMG EVENT0 data.	
00h (1801h)	**REG1801**	**7:0**	**Default : 0x00**	**Access : RO**
	EVENT0[15:8]	7:0	See description of '1800h'.	
01h (1804h)	**REG1804**	**7:0**	**Default : 0x00**	**Access : RO**
	EVENT0[23:16]	7:0	See description of '1800h'.	
01h (1805h)	**REG1805**	**7:0**	**Default : 0x00**	**Access : RO**
	EVENT0[31:24]	7:0	See description of '1800h'.	
02h (1808h)	**REG1808**	**7:0**	**Default : 0x00**	**Access : RO**
	EVENT1[7:0]	7:0	TMG EVENT1 data.	
02h (1809h)	**REG1809**	**7:0**	**Default : 0x00**	**Access : RO**
	EVENT1[15:8]	7:0	See description of '1808h'.	
03h (180Ch)	**REG180C**	**7:0**	**Default : 0x00**	**Access : RO**
	EVENT1[23:16]	7:0	See description of '1808h'.	
03h (180Dh)	**REG180D**	**7:0**	**Default : 0x00**	**Access : RO**
	EVENT1[31:24]	7:0	See description of '1808h'.	
04h (1810h)	**REG1810**	**7:0**	**Default : 0x00**	**Access : RO**
	EVENT2[7:0]	7:0	TMG EVENT2 data.	
04h (1811h)	**REG1811**	**7:0**	**Default : 0x00**	**Access : RO**
	EVENT2[15:8]	7:0	See description of '1810h'.	
05h (1814h)	**REG1814**	**7:0**	**Default : 0x00**	**Access : RO**
	EVENT2[23:16]	7:0	See description of '1810h'.	
05h (1815h)	**REG1815**	**7:0**	**Default : 0x00**	**Access : RO**
	EVENT2[31:24]	7:0	See description of '1810h'.	
06h (1818h)	**REG1818**	**7:0**	**Default : 0x00**	**Access : RO**
	EVENT3[7:0]	7:0	TMG EVENT3 data.	
06h (1819h)	**REG1819**	**7:0**	**Default : 0x00**	**Access : RO**
	EVENT3[15:8]	7:0	See description of '1818h'.	
07h (181Ch)	**REG181C**	**7:0**	**Default : 0x00**	**Access : RO**
	EVENT3[23:16]	7:0	See description of '1818h'.	
07h	**REG181D**	**7:0**	**Default : 0x00**	**Access : RO**

GPS2 Register (Bank = 0C)

Index (Absolute)	Mnemonic	Bit	Description	
(181Dh)	EVENT3[31:24]	7:0	See description of '1818h'.	
08h (1820h)	**REG1820**	**7:0**	**Default : 0x00**	**Access : RO**
	EVENT4[7:0]	7:0	TMG EVENT4 data.	
08h (1821h)	**REG1821**	**7:0**	**Default : 0x00**	**Access : RO**
	EVENT4[15:8]	7:0	See description of '1820h'.	
09h (1824h)	**REG1824**	**7:0**	**Default : 0x00**	**Access : RO**
	EVENT4[23:16]	7:0	See description of '1820h'.	
09h (1825h)	**REG1825**	**7:0**	**Default : 0x00**	**Access : RO**
	EVENT4[31:24]	7:0	See description of '1820h'.	
0Ah (1828h)	**REG1828**	**7:0**	**Default : 0x00**	**Access : RO**
	EVENT5[7:0]	7:0	TMG EVENT5 data.	
0Ah (1829h)	**REG1829**	**7:0**	**Default : 0x00**	**Access : RO**
	EVENT5[15:8]	7:0	See description of '1828h'.	
0Bh (182Ch)	**REG182C**	**7:0**	**Default : 0x00**	**Access : RO**
	EVENT5[23:16]	7:0	See description of '1828h'.	
0Bh (182Dh)	**REG182D**	**7:0**	**Default : 0x00**	**Access : RO**
	EVENT5[31:24]	7:0	See description of '1828h'.	
0Ch (1830h)	**REG1830**	**7:0**	**Default : 0x00**	**Access : RO**
	EVENT6[7:0]	7:0	TMG EVENT6 data.	
0Ch (1831h)	**REG1831**	**7:0**	**Default : 0x00**	**Access : RO**
	EVENT6[15:8]	7:0	See description of '1830h'.	
0Dh (1834h)	**REG1834**	**7:0**	**Default : 0x00**	**Access : RO**
	EVENT6[23:16]	7:0	See description of '1830h'.	
0Dh (1835h)	**REG1835**	**7:0**	**Default : 0x00**	**Access : RO**
	EVENT6[31:24]	7:0	See description of '1830h'.	
0Eh (1838h)	**REG1838**	**7:0**	**Default : 0x00**	**Access : RO**
	EVENT7[7:0]	7:0	TMG EVENT7 data.	
0Eh (1839h)	**REG1839**	**7:0**	**Default : 0x00**	**Access : RO**
	EVENT7[15:8]	7:0	See description of '1838h'.	
0Fh (183Ch)	**REG183C**	**7:0**	**Default : 0x00**	**Access : RO**
	EVENT7[23:16]	7:0	See description of '1838h'.	
0Fh (183Dh)	**REG183D**	**7:0**	**Default : 0x00**	**Access : RO**
	EVENT7[31:24]	7:0	See description of '1838h'.	

GPS2 Register (Bank = 0C)

Index (Absolute)	Mnemonic	Bit	Description	
10h (1840h)	**REG1840**	**7:0**	**Default : 0x00**	**Access : RO**
	WRME_EVENT[7:0]	7:0	TMG wrme event data.	
10h (1841h)	**REG1841**	**7:0**	**Default : 0x00**	**Access : RO**
	WRME_EVENT[15:8]	7:0	See description of '1840h'.	
11h (1844h)	**REG1844**	**7:0**	**Default : 0x00**	**Access : RO**
	WRME_EVENT[23:16]	7:0	See description of '1840h'.	
11h (1845h)	**REG1845**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	WRME_EVENT[30:24]	6:0	See description of '1840h'.	
12h (1848h)	**REG1848**	**7:0**	**Default : 0x00**	**Access : RO**
	PPS_EVENT[7:0]	7:0	TMG pps event data.	
12h (1849h)	**REG1849**	**7:0**	**Default : 0x00**	**Access : RO**
	PPS_EVENT[15:8]	7:0	See description of '1848h'.	
13h (184Ch)	**REG184C**	**7:0**	**Default : 0x00**	**Access : RO**
	PPS_EVENT[23:16]	7:0	See description of '1848h'.	
13h (184Dh)	**REG184D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	PPS_EVENT[30:24]	6:0	See description of '1848h'.	
14h (1850h)	**REG1850**	**7:0**	**Default : 0x00**	**Access : RO**
	CAL_TIMER[7:0]	7:0	Latched tmg timer value.	
14h (1851h)	**REG1851**	**7:0**	**Default : 0x00**	**Access : RO**
	CAL_TIMER[15:8]	7:0	See description of '1850h'.	
15h (1854h)	**REG1854**	**7:0**	**Default : 0x00**	**Access : RO**
	CAL_TIMER[23:16]	7:0	See description of '1850h'.	
15h (1855h)	**REG1855**	**7:0**	**Default : 0x00**	**Access : RO**
	CAL_TIMER[31:24]	7:0	See description of '1850h'.	
16h (1858h)	**REG1858**	**7:0**	**Default : 0x00**	**Access : RO**
	CAL_TIMER[39:32]	7:0	See description of '1850h'.	
16h (1859h)	**REG1859**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	CAL_TIMER[45:40]	5:0	See description of '1850h'.	
17h (185Ch)	**REG185C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	

GPS2 Register (Bank = 0C)

Index (Absolute)	Mnemonic	Bit	Description	
	WR_EVENT_PTR[2:0]	2:0	TMG write event pointer.	
18h (1860h)	**REG1860**	**7:0**	**Default : 0x00**	**Access : R/W**
	PERCTRL[7:0]	7:0	TMG Control Register.	
18h (1861h)	**REG1861**	**7:0**	**Default : 0x00**	**Access : R/W**
	PERCTRL[15:8]	7:0	See description of '1860h'.	
19h (1864h)	**REG1864**	**7:0**	**Default : 0x00**	**Access : R/W**
	PERCTRL[23:16]	7:0	See description of '1860h'.	
19h (1865h)	**REG1865**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	PERCTRL[26:24]	2:0	See description of '1860h'.	
1Ah (1868h)	**REG1868**	**7:0**	**Default : 0x00**	**Access : R/W**
	PERFRAC[7:0]	7:0	TM Period Fraction Register.	
1Bh (186Ch)	**REG186C**	**7:0**	**Default : 0x00**	**Access : R/W**
	TMPHS[7:0]	7:0	TM Phase Register.	
1Bh (186Dh)	**REG186D**	**7:0**	**Default : 0x00**	**Access : R/W**
	TMPHS[15:8]	7:0	See description of '186Ch'.	
1Ch (1870h)	**REG1870**	**7:0**	**Default : 0x00**	**Access : R/W**
	TMPHS[23:16]	7:0	See description of '186Ch'.	
1Ch (1871h)	**REG1871**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	TMPHS[25:24]	1:0	See description of '186Ch'.	
1Dh (1874h)	**REG1874**	**7:0**	**Default : 0x00**	**Access : R/W**
	TMWIDTH[7:0]	7:0	TMG Width Register.	
1Dh (1875h)	**REG1875**	**7:0**	**Default : 0x00**	**Access : R/W**
	TMWIDTH[15:8]	7:0	See description of '1874h'.	
1Eh (1878h)	**REG1878**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	TMWIDTH[16]	0	See description of '1874h'.	
1Fh (187Ch)	**REG187C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DECICTRL[7:0]	7:0	Decimation Control Register.	
1Fh (187Dh)	**REG187D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DECICTRL[15:8]	7:0	See description of '187Ch'.	
20h	**REG1880**	**7:0**	**Default : 0x00**	**Access : R/W**

GPS2 Register (Bank = 0C)

Index (Absolute)	Mnemonic	Bit	Description	
(1880h)	DECICTRL[23:16]	7:0	See description of '187Ch'.	
20h (1881h)	**REG1881**	**7:0**	**Default : 0x00**	**Access : R/W**
	DECICTRL[31:24]	7:0	See description of '187Ch'.	
21h (1884h)	**REG1884**	**7:0**	**Default : 0x00**	**Access : R/W**
	MISC[7:0]	7:0	Miscellaneous TMG Register.	
22h (1888h)	**REG1888**	**7:0**	**Default : 0x00**	**Access : RO**
	GLNS_SWITCH_TIME[7:0]	7:0	Latched TMG timer value at GLNS start/stop.	
22h (1889h)	**REG1889**	**7:0**	**Default : 0x00**	**Access : RO**
	GLNS_SWITCH_TIME[15:8]	7:0	See description of '1888h'.	
23h (188Ch)	**REG188C**	**7:0**	**Default : 0x00**	**Access : RO**
	GLNS_SWITCH_TIME[23:16]	7:0	See description of '1888h'.	
23h (188Dh)	**REG188D**	**7:0**	**Default : 0x00**	**Access : RO**
	GLNS_SWITCH_TIME[31:24]	7:0	See description of '1888h'.	
24h (1890h)	**REG1890**	**7:0**	**Default : 0x00**	**Access : RO**
	GLNS_SWITCH_TIME[39:32]	7:0	See description of '1888h'.	
24h (1891h)	**REG1891**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	GLNS_SWITCH_TIME[45:40]	5:0	See description of '1888h'.	
25h (1894h)	**REG1894**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	EVENT_SEL	0	Event select: 0: Event from PAD. 1: Event from RTC 16Hz clk.	
26h (1898h)	**REG1898**	**7:0**	**Default : 0x00**	**Access : RO**
	SLEEP_CNT[7:0]	7:0	Sleep timer value.	
26h (1899h)	**REG1899**	**7:0**	**Default : 0x00**	**Access : RO**
	SLEEP_CNT[15:8]	7:0	See description of '1898h'.	
27h (189Ch)	**REG189C**	**7:0**	**Default : 0x00**	**Access : RO**
	SLEEP_CNT[23:16]	7:0	See description of '1898h'.	
27h (189Dh)	**REG189D**	**7:0**	**Default : 0x00**	**Access : WO**
	CLR_SLEEP_CNT	7	Clear sleep cnt after write operation.	
	EN_SLEEP_CNT	6	Enable for sleep cnt '1' - enabled.	
	-	5:0	Reserved.	

GPS2 Register (Bank = 0C)

Index (Absolute)	Mnemonic	Bit	Description	
28h (18A0h)	**REG18A0**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:2	Reserved.	
	PPS_UPDATED_CLR	1	Pps event updated clear (0=nothing, 1=clear bit).	
	WRME_UPDATED_CLR	0	Wrme event updated clear (0=nothing, 1=clear bit).	
30h (18C0h)	**REG18C0**	**7:0**	**Default : 0x00**	**Access : R/W, WO**
	DUMMY[0]	7	Reserved for ECO.	
	MEM_CE	6	Probe memory chip select.	
	MEM_SEL[1:0]	5:4	Probe memory select. [0]: NAB. [1]: SRB. [2]: CHB.	
	MEM_RW[1:0]	3:2	Probe memory read/write select. 0: Read. 3: Write 64-bit.	
	MEM_PROBE	1	0/1: Probe memory disabled/enable.	
	SWRST	0	Software Reset, active high.	
30h (18C1h)	**REG18C1**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY[8:1]	7:0	See description of '18C0h'.	
31h (18C4h)	**REG18C4**	**7:0**	**Default : 0x00**	**Access : R/W**
	NAB_BASE[7:0]	7:0	NAB memory base.	
31h (18C5h)	**REG18C5**	**7:0**	**Default : 0x00**	**Access : R/W**
	NAB_BASE[15:8]	7:0	See description of '18C4h'.	
32h (18C8h)	**REG18C8**	**7:0**	**Default : 0x00**	**Access : R/W**
	NAB_BASE_MASK[7:0]	7:0	NAB memory base mask.	
32h (18C9h)	**REG18C9**	**7:0**	**Default : 0x00**	**Access : R/W**
	NAB_BASE_MASK[15:8]	7:0	See description of '18C8h'.	
33h (18CCh)	**REG18CC**	**7:0**	**Default : 0x00**	**Access : R/W**
	SRB_BASE[7:0]	7:0	SRB memory base.	
33h (18CDh)	**REG18CD**	**7:0**	**Default : 0x00**	**Access : R/W**
	SRB_BASE[15:8]	7:0	See description of '18CCh'.	
34h (18D0h)	**REG18D0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SRB_BASE_MASK[7:0]	7:0	SRB memory base mask.	
34h (18D1h)	**REG18D1**	**7:0**	**Default : 0x00**	**Access : R/W**
	SRB_BASE_MASK[15:8]	7:0	See description of '18D0h'.	

GPS2 Register (Bank = 0C)

Index (Absolute)	Mnemonic	Bit	Description	
35h (18D4h)	**REG18D4**	**7:0**	**Default : 0x00**	**Access : R/W**
	CHB_BASE[7:0]	7:0	CHB memory base.	
35h (18D5h)	**REG18D5**	**7:0**	**Default : 0x00**	**Access : R/W**
	CHB_BASE[15:8]	7:0	See description of '18D4h'.	
36h (18D8h)	**REG18D8**	**7:0**	**Default : 0x00**	**Access : R/W**
	CHB_BASE_MASK[7:0]	7:0	CHB memory base mask.	
36h (18D9h)	**REG18D9**	**7:0**	**Default : 0x00**	**Access : R/W**
	CHB_BASE_MASK[15:8]	7:0	See description of '18D8h'.	
37h (18DCh)	**REG18DC**	**7:0**	**Default : 0x00**	**Access : R/W**
	MEM_ADDR[7:0]	7:0	Probe memory address.	
37h (18DDh)	**REG18DD**	**7:0**	**Default : 0x00**	**Access : R/W**
	MEM_ADDR[15:8]	7:0	See description of '18DCh'.	
38h (18E0h)	**REG18E0**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	MEM_WD[7:0]	7:0	Probe memory write data.	
	MEM_RD[7:0]	7:0	Probe memory read data.	
38h (18E1h)	**REG18E1**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	MEM_WD[15:8]	7:0	See description of '18E0h'.	
	MEM_RD[15:8]	7:0	See description of '18E0h'.	
39h (18E4h)	**REG18E4**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	MEM_WD[23:16]	7:0	See description of '18E0h'.	
	MEM_RD[23:16]	7:0	See description of '18E0h'.	
39h (18E5h)	**REG18E5**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	MEM_WD[31:24]	7:0	See description of '18E0h'.	
	MEM_RD[31:24]	7:0	See description of '18E0h'.	
3Ah (18E8h)	**REG18E8**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	MEM_WD[39:32]	7:0	See description of '18E0h'.	
	MEM_RD[39:32]	7:0	See description of '18E0h'.	
3Ah (18E9h)	**REG18E9**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	MEM_WD[47:40]	7:0	See description of '18E0h'.	
	MEM_RD[47:40]	7:0	See description of '18E0h'.	
3Bh (18ECh)	**REG18EC**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	MEM_WD[55:48]	7:0	See description of '18E0h'.	
	MEM_RD[55:48]	7:0	See description of '18E0h'.	

GPS2 Register (Bank = 0C)

Index (Absolute)	Mnemonic	Bit	Description	
3Bh (18EDh)	**REG18ED**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	MEM_WD[63:56]	7:0	See description of '18E0h'.	
	MEM_RD[63:56]	7:0	See description of '18E0h'.	
3Ch (18F0h)	**REG18F0**	**7:0**	**Default : 0x00**	**Access : RO**
	ARB_STS[7:0]	7:0	ARB Status. [0]: 1=NAB grant CVC. [1]: 1=SRB grant CVC. [2]: 1=CHB grant CORR.	
3Ch (18F1h)	**REG18F1**	**7:0**	**Default : 0x00**	**Access : RO**
	ARB_STS[15:8]	7:0	See description of '18F0h'.	
3Dh (18F4h)	**REG18F4**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED[7:0]	7:0	RESERVED for ECO.	
3Dh (18F5h)	**REG18F5**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED[15:8]	7:0	See description of '18F4h'.	
40h (1900h)	**REG1900**	**7:0**	**Default : 0x04**	**Access : R/W, WO**
	-	7:5	Reserved.	
	MI_DISCON	4	0/1: Disconnect MI interface.	
	DMAW_PROTECT_EN	3	0/1: DMA write protect enabled/disabled.	
	INT_MASK	2	0/1: interrupt enabled/disabled.	
	INT_CLR	1	Clear DMA interrupt in, one-shot.	
	-	0	Reserved.	
41h (1904h)	**REG1904**	**7:0**	**Default : 0x00**	**Access : R/W**
	CMD[7:0]	7:0	DMA command. [7:0]: Block length minus one, 64-bit words. [13:8]: (SigP Core data gap length minus one), 32-bit words. [17:14]: Data blocks number minus one. [30:18]: Reserved. [31]: Direction (0: core->sram, 1: sram->core).	
41h (1905h)	**REG1905**	**7:0**	**Default : 0x00**	**Access : R/W**
	CMD[15:8]	7:0	See description of '1904h'.	
42h (1908h)	**REG1908**	**7:0**	**Default : 0x00**	**Access : R/W**
	CMD[23:16]	7:0	See description of '1904h'.	
42h	**REG1909**	**7:0**	**Default : 0x00**	**Access : R/W**

GPS2 Register (Bank = 0C)

Index (Absolute)	Mnemonic	Bit	Description	
(1909h)	CMD[31:24]	7:0	See description of '1904h'.	
43h (190Ch)	**REG190C**	**7:0**	**Default : 0x00**	**Access : R/W**
	A_CORE[7:0]	7:0	Core domain address.	
43h (190Dh)	**REG190D**	**7:0**	**Default : 0x00**	**Access : R/W**
	A_CORE[15:8]	7:0	See description of '190Ch'.	
44h (1910h)	**REG1910**	**7:0**	**Default : 0x00**	**Access : R/W**
	A_SRAM[7:0]	7:0	SRAM domain address.	
44h (1911h)	**REG1911**	**7:0**	**Default : 0x00**	**Access : R/W**
	A_SRAM[15:8]	7:0	See description of '1910h'.	
45h (1914h)	**REG1914**	**7:0**	**Default : 0x00**	**Access : RO**
	TASKS_N[7:0]	7:0	Number tasks for process. 8'b00000001: 1 job. 8'b00000011: 2 jobs. 8'b00000111: 3 jobs. 8'b00001111: 4 jobs. ... 8'b11111111: 8 jobs.	
46h (1918h)	**REG1918**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMAW_LBND[7:0]	7:0	DMA write lower bound.	
46h (1919h)	**REG1919**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMAW_LBND[15:8]	7:0	See description of '1918h'.	
47h (191Ch)	**REG191C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMAW_UBND[7:0]	7:0	DMA write upper bound.	
47h (191Dh)	**REG191D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMAW_UBND[15:8]	7:0	See description of '191Ch'.	
48h (1920h)	**REG1920**	**7:0**	**Default : 0x10**	**Access : R/W**
	BURST_CNT[2:0]	7:5	DMA burst counter (Unit: 16T).	
	BRSTCTRL_EN	4	DMA burst counter enable.	
	PRI_CNT[2:0]	3:1	DMA priority counter (Unit: 32T).	
	PRICTRL_EN	0	DMA priority counter enable.	
48h	**REG1921**	**7:0**	**Default : 0x00**	**Access : R/W**

GPS2 Register (Bank = 0C)

Index (Absolute)	Mnemonic	Bit	Description	
(1921h)	REQ_PRI_RW[1:0]	7:6	Arbitration mode. [0]: Round robin. [1]: Write > read. [2]: Read > write.	
	FIXED_PRI_W	5	0/1: Fixed priority enabled/disabled for write.	
	FIXED_PRI_R	4	0/1: Fixed priority enabled/disabled for read.	
	REQ_HIPRI_W[1:0]	3:2	Write high priority enable. [0]: DMA engine write. [1]: SB FIFO write.	
	REQ_HIPRI_R[1:0]	1:0	Read high priority enable. [0]: DMA engine read. [1]: CORR FIFO read.	
4Bh (192Ch)	**REG192C**	**7:0**	**Default : 0x44**	**Access : R/W**
	ISYN_CNT[3:0]	7:4	Sync cnt base address init (Unit: 4T).	
	SYNC_CNT[3:0]	3:0	Sync cnt for clock switch (Unit: 4T).	
4Ch (1930h)	**REG1930**	**7:0**	**Default : 0x00**	**Access : RO**
	DMA_STS[7:0]	7:0	DMA status. [0]: 1=Busy for read SigP-RAM. [1]: 1=Busy for write SigP-RAM. [2]: 1=Busy for read Core-RAM. [3]: 1=Busy for write Core-RAM.	
4Ch (1931h)	**REG1931**	**7:0**	**Default : 0x00**	**Access : RO**
	DMA_STS[15:8]	7:0	See description of '1930h'.	
4Dh (1934h)	**REG1934**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_THR[3:0]	7:4	Interrupt threshold.	
	-	3:0	Reserved.	
4Dh (1935h)	**REG1935**	**7:0**	**Default : 0x00**	**Access : R/W**
	MI_ADDR_23_16[7:0]	7:0	MI address bit 23:16.	
4Eh (1938h)	**REG1938**	**7:0**	**Default : 0x55**	**Access : R/W**
	RESERVED[7:0]	7:0	Reserved for ECO.	
4Eh (1939h)	**REG1939**	**7:0**	**Default : 0x55**	**Access : R/W**
	ECO_RESERVED[15:8]	7:0	See description of '1938h'.	

GPS3 Register (Bank = 0D)

GPS3 Register (Bank = 0D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
70h (1BC0h)	**REG1BC0**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	DCDSB_ST[0]	7		
	VALID_INTERVAL	6		
	VALID_DISABLE	5		
	HEADER_GEN_ENABLE	4		
	BYPASS_DCDSB	3		
	DCDSB_TO_CLR	2		
	DCD_ENABLE	1		
	SWRST	0		
70h (1BC1h)	**REG1BC1**	**7:0**	**Default : 0x08**	**Access : RO, R/W**
	VCNT_BND[2:0]	7:5	Valid cnt bound.	
	VALID_SEL[1:0]	4:3	Valid select. [0]: 0/1 = tie 1/from ECD. [1]: 0/1 = from ECD/DCD.	
	VCNT_CLR	2	Clear ecd/valid cnt.	
	VCNT_EN	1	Enable ecd/valid cnt.	
	DCDSB_ST[1]	0	See description of '1BC0h'.	
71h (1BC4h)	**REG1BC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	DCD_PARA[7:0]	7:0		
71h (1BC5h)	**REG1BC5**	**7:0**	**Default : 0x00**	**Access : R/W**
	DCD_PARA[15:8]	7:0	See description of '1BC4h'.	
72h (1BC8h)	**REG1BC8**	**7:0**	**Default : 0x00**	**Access : RO, R/W, WO**
	-	7:6	Reserved.	
	DCD_ERR_FLAG	5	Dcd error flag.	
	DCD_CHK_CNT_SEL	4	0: Dcd_check counter. 1: Current latch data.	
	DCD_PARA_W	3	Reg_dcd_para write enable (one shot).	

GPS3 Register (Bank = 0D)

Index (Absolute)	Mnemonic	Bit	Description	
	DCD_PARA_SEL[2:0]	2:0	0: Dcd_header[15:0]. 1: Dcd_header[31:16]. 2: Dcd_header[47:32]. 3: Dcd_header[63:48]. 4: Dcd_timeout[15:0]. 5: Dcd_timeout[31:16]. 6: Dcd_cnt_init_val[15:0].	
73h (1BCCh)	**REG1BCC**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0[7:0]	7:0	Dummy register 0.	
73h (1BCDh)	**REG1BCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0[15:8]	7:0	See description of '1BCCh'.	
74h (1BD0h)	**REG1BD0**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY1[7:0]	7:0	Dummy register 1.	
74h (1BD1h)	**REG1BD1**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY1[15:8]	7:0	See description of '1BD0h'.	
75h (1BD4h)	**REG1BD4**	**7:0**	**Default : 0x00**	**Access : RO**
	DCD_CHK_CNT[7:0]	7:0	Dcd check counter.	
75h (1BD5h)	**REG1BD5**	**7:0**	**Default : 0x00**	**Access : RO**
	DCD_CHK_CNT[15:8]	7:0	See description of '1BD4h'.	
77h (1BDCh)	**REG1BDC**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	OUT_TEST_ERROR_FLG	7		
	IN_TEST_ERROR_FLG	6		
	OUT_TEST_COMP_START	5		
	IN_TEST_COMP_START	4		
	OUT_TEST_MODE	3		
	OUT_TEST_RST	2		
	IN_TEST_MODE	1		
	IN_TEST_RST	0		
77h (1BDDh)	**REG1BDD**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	AFE_I_SEL	7	AFE_I Select. 0: From PAD. 1: From local 2-bit counter.	
	ECNT_BND[2:0]	6:4	Ecd cnt bound.	
	OUT_GOLDEN_DATA[1:0]	3:2		
	IN_GOLDEN_DATA[1:0]	1:0		

GPS4 Register (Bank = 0E)

GPS4 Register (Bank = 0E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (1C00h)	**REG1C00**	**7:0**	**Default : 0x00**	**Access : R/W, WO**
	-	7:4	Reserved.	
	RFSPI_RF_TYPE	3	0/1: MSR2102/MSR2112.	
	RFSPI_GLS_MODE	2	0/1: control gps/glonas RF.	
	RFSPI_RESET	1	Rfspi software reset, active high.	
	RFSPI_GO	0	Fire SPI command, one-shot.	
01h (1C04h)	**REG1C04**	**7:0**	**Default : 0x00**	**Access : R/W**
	RFSPI_COMMAND[7:0]	7:0	MSR2102: [7:0] -> wdata. [11:8] -> addr. [12] -> 0/1: r/w. [14:13]: not used. MSR2112: [7:0] -> wdata. [13:8] -> addr. [14] -> 0/1: r/w.	
01h (1C05h)	**REG1C05**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	RFSPI_COMMAND[14:8]	6:0	See description of '1C04h'.	
02h (1C08h)	**REG1C08**	**7:0**	**Default : 0x00**	**Access : RO**
	RFSPI_RDATA[7:0]	7:0	Read data from GPS/GLS RF.	
03h (1C0Ch)	**REG1C0C**	**7:0**	**Default : 0x00**	**Access : RO**
	RFSPI_DEBUG[7:0]	7:0	Rfspi debug bus.	
03h (1C0Dh)	**REG1C0D**	**7:0**	**Default : 0x00**	**Access : RO**
	RFSPI_DEBUG[15:8]	7:0	See description of '1C0Ch'.	
04h (1C10h)	**REG1C10**	**7:0**	**Default : 0x00**	**Access : RO**
	RFSPI_DEBUG[23:16]	7:0	See description of '1C0Ch'.	
05h (1C14h)	**REG1C14**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY[7:0]	7:0	DUMMY register.	
05h (1C15h)	**REG1C15**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY[15:8]	7:0	See description of '1C14h'.	
10h (1C40h)	**REG1C40**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	

GPS4 Register (Bank = 0E)

Index (Absolute)	Mnemonic	Bit	Description	
	GPS_DB_SEL[1:0]	1:0	GPS_TOP debug port selection. 2'h0: sigp_debug. 2'h1: sigp_ram_debug. 2'h2: rfspi_top_debug.	
20h (1C80h)	**REG1C80**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SWRST	0		
20h (1C81h)	**REG1C81**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	CAL_STEPS[2:0]	2:0	[8]DAC accumulation. [9]XO estimation. [10] 0: clk_sigp estimation, 1: clk_afe_gps estimation.	
21h (1C84h)	**REG1C84**	**7:0**	**Default : 0x00**	**Access : R/W**
	ACC_NUM[7:0]	7:0	DAC accumulation number.	
21h (1C85h)	**REG1C85**	**7:0**	**Default : 0x00**	**Access : R/W**
	ACC_NUM[15:8]	7:0	See description of '1C84h'.	
22h (1C88h)	**REG1C88**	**7:0**	**Default : 0x00**	**Access : RO**
	ACC_RESULT[7:0]	7:0	DAC acc result.	
22h (1C89h)	**REG1C89**	**7:0**	**Default : 0x00**	**Access : RO**
	ACC_RESULT[15:8]	7:0	See description of '1C88h'.	
23h (1C8Ch)	**REG1C8C**	**7:0**	**Default : 0x00**	**Access : RO**
	ACC_RESULT[23:16]	7:0	See description of '1C88h'.	
23h (1C8Dh)	**REG1C8D**	**7:0**	**Default : 0x00**	**Access : RO**
	ACC_RESULT[31:24]	7:0	See description of '1C88h'.	
24h (1C90h)	**REG1C90**	**7:0**	**Default : 0x00**	**Access : RO**
	CLK_COUNTER[7:0]	7:0	Clock drift.	
24h (1C91h)	**REG1C91**	**7:0**	**Default : 0x00**	**Access : RO**
	CLK_COUNTER[15:8]	7:0	See description of '1C90h'.	
25h (1C94h)	**REG1C94**	**7:0**	**Default : 0x00**	**Access : RO**
	CLK_COUNTER[23:16]	7:0	See description of '1C90h'.	
25h (1C95h)	**REG1C95**	**7:0**	**Default : 0x00**	**Access : RO**
	CLK_COUNTER[31:24]	7:0	See description of '1C90h'.	
26h (1C98h)	**REG1C98**	**7:0**	**Default : 0x00**	**Access : R/W**
	EST_DURATION[7:0]	7:0	Clock estimation duration.	

GPS4 Register (Bank = 0E)

Index (Absolute)	Mnemonic	Bit	Description	
26h (1C99h)	**REG1C99**	**7:0**	**Default : 0x00**	**Access : R/W**
	EST_DURATION[15:8]	7:0	See description of '1C98h'.	
27h (1C9Ch)	**REG1C9C**	**7:0**	**Default : 0x00**	**Access : R/W**
	EST_DURATION[23:16]	7:0	See description of '1C98h'.	
27h (1C9Dh)	**REG1C9D**	**7:0**	**Default : 0x00**	**Access : R/W**
	EST_DURATION[31:24]	7:0	See description of '1C98h'.	
28h (1CA0h)	**REG1CA0**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:4	Reserved.	
	STATUS_CLR[1:0]	3:2	[2] To clear ADC acc ready flag. [3] To clear XO estimation ready flag.	
	STATUS[1:0]	1:0	[0] ADC acc ready. [1] XO estimation ready.	
40h (1D00h)	**REG1D00**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	FIXED_PRI	4	Fixed priority enable.	
	-	3:1	Reserved.	
	SWRST	0	Software Reset, active high.	
41h (1D04h)	**REG1D04**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	REQ_HIPRI[3:0]	3:0	High priority enable. [0]: AEON. [1]: SigP DMA. [2]: Test Channel. [3]: ARM.	
43h (1D0Ch)	**REG1D0C**	**7:0**	**Default : 0x07**	**Access : R/W**
	-	7:4	Reserved.	
	REQ_MASK[3:0]	3:0	Request Mask.	
44h (1D10h)	**REG1D10**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	W_PROTECT_EN	5	Write protect enable.	
	BRSTCTRL_EN	4	Burst cnt enable.	
	BURST_CNT[3:0]	3:0	Burst cnt.	
44h	**REG1D11**	**7:0**	**Default : 0x00**	**Access : RO**

GPS4 Register (Bank = 0E)

Index (Absolute)	Mnemonic	Bit	Description	
(1D11h)	BIST_STS[7:0]	7:0	[0]: Ram0, [1]: ram1, etc. 0/1 = pass/fail.	
45h (1D14h)	**REG1D14**	**7:0**	**Default : 0x00**	**Access : R/W**
	READ_CMP_RESULT	7	Read compare result.	
	TEST_BYTE[1:0]	6:5	Test byte.	
	TEST_LOOP	4	Test loop.	
	INV_DATA	3	Invert data.	
	TEST_MODE[1:0]	2:1	Test mode.	
	TEST_EN	0	Test mode enable.	
45h (1D15h)	**REG1D15**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:6	Reserved.	
	TEST_FLAG	5	Test flag.	
	TEST_FAIL	4	Test fail.	
	TEST_FINISH	3	Test finish.	
	ANA_BIST_EN	2	Bist en.	
	WRITE_ONLY	1	Write only.	
	READ_ONLY	0	Read only.	
46h (1D18h)	**REG1D18**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_BASE[7:0]	7:0	Test base.	
46h (1D19h)	**REG1D19**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_BASE[15:8]	7:0	See description of '1D18h'.	
47h (1D1Ch)	**REG1D1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_LENGTH[7:0]	7:0	Test length.	
47h (1D1Dh)	**REG1D1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_LENGTH[15:8]	7:0	See description of '1D1Ch'.	
48h (1D20h)	**REG1D20**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_LENGTH[23:16]	7:0	See description of '1D1Ch'.	
49h (1D24h)	**REG1D24**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_MASK[7:0]	7:0	Test mask.	
4Ah (1D28h)	**REG1D28**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_DATA[7:0]	7:0	Test data.	
4Ah (1D29h)	**REG1D29**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_DATA[15:8]	7:0	See description of '1D28h'.	

GPS4 Register (Bank = 0E)

Index (Absolute)	Mnemonic	Bit	Description	
4Bh (1D2Ch)	**REG1D2C**	**7:0**	**Default : 0x00**	**Access : RO**
	TEST_STATUS[7:0]	7:0	Test status.	
4Bh (1D2Dh)	**REG1D2D**	**7:0**	**Default : 0x00**	**Access : RO**
	TEST_STATUS[15:8]	7:0	See description of '1D2Ch'.	
4Ch (1D30h)	**REG1D30**	**7:0**	**Default : 0x00**	**Access : RO**
	TEST_BYTE_FAIL[7:0]	7:0	Test byte fail.	
4Ch (1D31h)	**REG1D31**	**7:0**	**Default : 0x00**	**Access : RO**
	TEST_BYTE_FAIL[15:8]	7:0	See description of '1D30h'.	
4Dh (1D34h)	**REG1D34**	**7:0**	**Default : 0x00**	**Access : R/W**
	W_LBND[7:0]	7:0	Low bound.	
4Dh (1D35h)	**REG1D35**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	W_LBND[12:8]	4:0	See description of '1D34h'.	
4Eh (1D38h)	**REG1D38**	**7:0**	**Default : 0x00**	**Access : R/W**
	W_UBND[7:0]	7:0	High bound.	
4Eh (1D39h)	**REG1D39**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	W_UBND[12:8]	4:0	See description of '1D38h'.	
4Fh (1D3Ch)	**REG1D3C**	**7:0**	**Default : 0x00**	**Access : RO**
	W_OUT_ADR[7:0]	7:0	Out of bound address.	
4Fh (1D3Dh)	**REG1D3D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	W_OUT_ADR[12:8]	4:0	See description of '1D3Ch'.	
50h (1D40h)	**REG1D40**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLK_GATED	7	0: Enable sram clock. 1: Disable sram clock.	
	DEBUG_SEL[6:0]	6:0	Debug select.	
51h (1D44h)	**REG1D44**	**7:0**	**Default : 0x00**	**Access : RO**
	DEBUG[7:0]	7:0	DEBUG port.	
51h (1D45h)	**REG1D45**	**7:0**	**Default : 0x00**	**Access : RO**
	DEBUG[15:8]	7:0	See description of '1D44h'.	
52h (1D48h)	**REG1D48**	**7:0**	**Default : 0x00**	**Access : RO**
	DEBUG[23:16]	7:0	See description of '1D44h'.	

GPS4 Register (Bank = 0E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
53h (1D4Ch)	**REG1D4C**	**7:0**	**Default : 0xAA**	**Access : R/W**
	DUMMY0[7:0]	7:0	Reserved.	
53h (1D4Dh)	**REG1D4D**	**7:0**	**Default : 0xAA**	**Access : R/W**
	DUMMY0[15:8]	7:0	See description of '1D4Ch'.	

ARM Register (Bank = 0F)

ARM Register (Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (1E00h)	**REG1E00**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	ARM_BOOTSEL	0	Boot address map. [0]: BootROM @ 0xFFFF0000. [1]: Map 0xFFFF0000 to NOR flash.	
01h (1E04h)	**REG1E04**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:2	Reserved.	
	ARM_VINITHI	1	Exception vector location at reset 0(0x00000000); 1(0xFFFF0000).	
	ARM_INITRAM	0	Enable instruction TCM at system reset.	
02h (1E08h)	**REG1E08**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	ARM_TCM_TIMING[1:0]	1:0	[0]: Pipeline_disable. [1]: Multicycle.	
02h (1E09h)	**REG1E09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	ARM_ROM_ZERO_WAIT	0	Enable zero wait state timing for ROM.	
03h (1E0Ch)	**REG1E0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	AHB_CLK_DIV[2:0]	2:0	AHB clock divider.	
04h (1E10h)	**REG1E10**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GPS_CLK_DIV[2:0]	2:0	GPS HCLK divider.	
05h (1E14h)	**REG1E14**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	ARM_WFI_DISABLE[2:0]	2:0	Disable wait for interrupt clock gating. [0]: Cpu. [1]: Ahb. [2]: Gps.	
10h (1E40h)	**REG1E40**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:4	Reserved.	
	AB_RXIU_RST	3	Reset arm bridge riu xiu I/F.	
	AB_SXIU_RST	2	Reset arm bridge spi xiu I/F.	

ARM Register (Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description	
	AB_MIU_RST	1	Reset arm bridge miu I/F.	
	ARM_RST	0	Reset arm cpu.	
20h (1E80h)	**REG1E80**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	JTAG_SYNC_BYPASS	1	Bypass jtag synchronize circuit.	
	ARM_CLKGEN_BYPASS	0	Bypass arm gated clk circuit.	
30h (1EC0h)	**REG1EC0**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:2	Reserved.	
	ROMBIST_DONE	1	Bist done.	
	ROMBIST_START	0	0 -> 1 Start the bist.	
31h (1EC4h)	**REG1EC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	ROMBIST_SEL[1:0]	5:4	Select bist target.	
	ROMBIST_WIDTH[3:0]	3:0	Target bist width: (width+1)x8 bit.	
32h (1EC8h)	**REG1EC8**	**7:0**	**Default : 0x00**	**Access : R/W**
	ROMBIST_WORD[7:0]	7:0	Target bist words.	
32h (1EC9h)	**REG1EC9**	**7:0**	**Default : 0x00**	**Access : R/W**
	ROMBIST_WORD[15:8]	7:0	See description of '1EC8h'.	
33h (1ECCh)	**REG1ECC**	**7:0**	**Default : 0x00**	**Access : RO**
	ROMBIST_CUR[7:0]	7:0	Current testing words.	
33h (1ECDh)	**REG1ECD**	**7:0**	**Default : 0x00**	**Access : RO**
	ROMBIST_CUR[15:8]	7:0	See description of '1ECCh'.	
34h (1ED0h)	**REG1ED0**	**7:0**	**Default : 0x00**	**Access : RO**
	ROMBIST_CRC[7:0]	7:0	Final crc result.	
34h (1ED1h)	**REG1ED1**	**7:0**	**Default : 0x00**	**Access : RO**
	ROMBIST_CRC[15:8]	7:0	See description of '1ED0h'.	
35h (1ED4h)	**REG1ED4**	**7:0**	**Default : 0x00**	**Access : RO**
	ROMBIST_CRC[23:16]	7:0	See description of '1ED0h'.	
35h (1ED5h)	**REG1ED5**	**7:0**	**Default : 0x00**	**Access : RO**
	ROMBIST_CRC[31:24]	7:0	See description of '1ED0h'.	
38h (1EE0h)	**REG1EE0**	**7:0**	**Default : 0x00**	**Access : RO**
	TCM_BIST_FAIL[7:0]	7:0	TCM Bist fail.	
40h	**REG1F00**	**7:0**	**Default : 0x00**	**Access : R/W**

ARM Register (Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description	
(1F00h)	-	7:6	Reserved.	
	IAHB_INCR_WORDS[1:0]	5:4	IAHB INCR words.	
	IAHB_HPROT_PR[3:0]	3:0	IAHB HPROT Mask.	
40h (1F01h)	**REG1F01**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	DAHB_INCR_WORDS[1:0]	5:4	DAHB INCR words.	
	DAHB_HPROT_PR[3:0]	3:0	DAHB HPROT Mask.	
41h (1F04h)	**REG1F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	IAHB_MIU_MASK[1:0]	1:0	[0]: IAHB MIU Mask. [1]: IAHB MIU last from AHB mask.	
41h (1F05h)	**REG1F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	DAHB_MIU_MASK[1:0]	1:0	[0]: DAHB MIU Mask. [1]: DAHB MIU last from AHB mask.	

ARMPFET Register (Bank = 10)

ARMPFET Register (Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2000h)	**REG2000**	**7:0**	**Default : 0x10**	**Access : R/W**
	REQ_LAST_CTRL_OFF_ICH	7	Disable request to MIU last flag.	
	-	6	Reserved.	
	REQ_CNT_RPT_MODE_ICH	5	For test.	
	REQ_CNT_CLEAR_ICH	4	For test.	
	DATA_BUF_SIZE_ICH	3	Instruction buffer size 0: 32-bytes, 1: 64-bytes.	
	DATA_BUF_EN_ICH	2	Instruction buffer enable.	
	MIU_ACCESS_MODE_ICH	1	Instruction request to MIU path select.	
	MFET_ENABLE_ICH	0	Instruction prefetch enable.	
00h (2001h)	**REG2001**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	BIST_FAIL_PFET_ICH	6	For test.	
	PFET_ROUT_SEL_ICH[1:0]	5:4	For test.	
	MREQ_RESET_ICH	3	Reset request signal.	
	TAG_VALID_CLEAR_ICH	2	Clear prefetch buffer valid bits flag.	
	FLUSH_PIPE_EN_ICH	1	Flush pipe enable.	
	-	0	Reserved.	
03h (200Ch)	**REG200C**	**7:0**	**Default : 0x00**	**Access : RO**
	PFET_ROUT_STATUS0_ICH[7:0]	7:0	For debug.	
03h (200Dh)	**REG200D**	**7:0**	**Default : 0x00**	**Access : RO**
	PFET_ROUT_STATUS0_ICH[15:8]	7:0	See description of '200Ch'.	
04h (2010h)	**REG2010**	**7:0**	**Default : 0x00**	**Access : RO**
	PFET_ROUT_STATUS1_ICH[7:0]	7:0	For debug.	
04h (2011h)	**REG2011**	**7:0**	**Default : 0x00**	**Access : RO**
	PFET_ROUT_STATUS1_ICH[15:8]	7:0	See description of '2010h'.	
05h (2014h)	**REG2014**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY05_15_0[7:0]	7:0	Reserved.	
05h (2015h)	**REG2015**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY05_15_0[15:8]	7:0	See description of '2014h'.	
06h (2018h)	**REG2018**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY06_15_0[7:0]	7:0	Reserved.	

ARMPFET Register (Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
06h (2019h)	**REG2019**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY06_15_0[15:8]	7:0	See description of '2018h'.	
08h (2020h)	**REG2020**	**7:0**	**Default : 0x10**	**Access : R/W**
	REQ_LAST_CTRL_OFF_DCH	7	Disable request to MIU last flag.	
	-	6	Reserved.	
	REQ_CNT_RPT_MODE_DCH	5	For test.	
	REQ_CNT_CLEAR_DCH	4	For test.	
	DATA_BUF_SIZE_DCH	3	Data buffer size 0: 32-bytes, 1: 64-bytes.	
	DATA_BUF_EN_DCH	2	Data buffer enable.	
	MIU_ACCESS_MODE_ICH	1	Instruction request to MIU path select.	
	MFET_ENABLE_ICH	0	Instruction prefetch enable.	
08h (2021h)	**REG2021**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	BIST_FAIL_PFET_DCH	6	For test.	
	PFET_ROUT_SEL_DCH[1:0]	5:4	For test.	
	MREQ_RESET_DCH	3	Reset request signal.	
	TAG_VALID_CLEAR_DCH	2	Clear prefetch buffer valid bits flag.	
	FLUSH_PIPE_EN_DCH	1	Flush pipe enable.	
	-	0	Reserved.	
09h (2024h)	**REG2024**	**7:0**	**Default : 0x0F**	**Access : R/W**
	REQ_TIMEOUT_FLUSH_DCH[7:0]	7:0	Start to flush write request when waiting timeout.	
09h (2025h)	**REG2025**	**7:0**	**Default : 0x0F**	**Access : R/W**
	W_PACK_TIMEOUT_DCH[7:0]	7:0	Start to flush write pack data when waiting timeout.	
0Ah (2028h)	**REG2028**	**7:0**	**Default : 0xC8**	**Access : R/W**
	MCU_REQ_PRIOR_DCH[3:0]	7:4	Set high priority flag to 1 when request number meets the threshold.	
	MCU_REQ_THRD_DCH[3:0]	3:0	Start to request when request number meets the threshold.	
0Ah (2029h)	**REG2029**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7	Reserved.	
	MCU_REQ_MAX_DCH[6:0]	6:0	Stop the request when request number meets the threshold.	
0Bh	**REG202C**	**7:0**	**Default : 0x00**	**Access : RO**

ARMPFET Register (Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
(202Ch)	PFET_ROUT_STATUS0_DCH[7:0]	7:0	For debug.	
0Bh (202Dh)	**REG202D**	**7:0**	**Default : 0x00**	**Access : RO**
	PFET_ROUT_STATUS0_DCH[15:8]	7:0	See description of '202Ch'.	
0Ch (2030h)	**REG2030**	**7:0**	**Default : 0x00**	**Access : RO**
	PFET_ROUT_STATUS1_DCH[7:0]	7:0	For debug.	
0Ch (2031h)	**REG2031**	**7:0**	**Default : 0x00**	**Access : RO**
	PFET_ROUT_STATUS1_DCH[15:8]	7:0	See description of '2030h'.	
0Dh (2034h)	**REG2034**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0D_15_0[7:0]	7:0	Reserved.	
0Dh (2035h)	**REG2035**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0D_15_0[15:8]	7:0	See description of '2034h'.	
0Eh (2038h)	**REG2038**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0E_15_0[7:0]	7:0	Reserved.	
0Eh (2039h)	**REG2039**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0E_15_0[15:8]	7:0	See description of '2038h'.	

MIU_ATOP Register (Bank = 11)

MIU_ATOP Register (Bank = 11)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2200h)	**REG2200**	**7:0**	**Default : 0x38**	**Access : R/W**
	-	7	Reserved.	
	DDRPLL_CLKIN_DIV2_EN	6		
	MCLK_PD	5		
	GPIO_MODE	4		
	GPIO_OENZ	3		
	-	2:1	Reserved.	
	PKG_SEL	0	1: BGA, 0: QFP.	
00h (2201h)	**REG2201**	**7:0**	**Default : 0x80**	**Access : R/W**
	ATOP_PD	7		
	RESERVED_00[2:0]	6:4		
	BYPASS_IOM	3		
	ODT_EN[1:0]	2:1		
	SEL_INTERNAL_DQS	0		
01h (2204h)	**REG2204**	**7:0**	**Default : 0xAA**	**Access : R/W**
	CKO_STATE[7:0]	7:0	Set the clock waveform: 8x mode: 10101010. 4x mode: 11001100.	
01h (2205h)	**REG2205**	**7:0**	**Default : 0xAA**	**Access : R/W**
	DQS_STATE[7:0]	7:0	Set the DQS waveform: 8x mode: 10101010. 4x mode: 11001100.	
02h (2208h)	**REG2208**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_02[7:0]	7:0		
02h (2209h)	**REG2209**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_02[15:8]	7:0	See description of '2208h'.	
03h (220Ch)	**REG220C**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_03[7:0]	7:0		
03h (220Dh)	**REG220D**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_03[15:8]	7:0	See description of '220Ch'.	
04h (2210h)	**REG2210**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	

MIU_ATOP Register (Bank = 11)

Index (Absolute)	Mnemonic	Bit	Description	
	RX_EN[5:0]	5:0		
05h (2214h)	**REG2214**	**7:0**	**Default : 0x00**	**Access : R/W**
	DQSM0_RD_PHASE[3:0]	7:4		
	DQSM0_RD_TIMING[3:0]	3:0		
05h (2215h)	**REG2215**	**7:0**	**Default : 0x00**	**Access : R/W**
	DQSM1_RD_PHASE[3:0]	7:4		
	DQSM1_RD_TIMING[3:0]	3:0		
06h (2218h)	**REG2218**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_06[1:0]	7:6		
	LOOPBACK_DIG_EN[2:0]	5:3		
	LOOPBACK_EN[2:0]	2:0		
06h (2219h)	**REG2219**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_SEL[3:0]	7:4		
	SYN_DEB_BUS_SEL[1:0]	3:2		
	TEST_EN	1		
	TEST_CLK_EN	0		
07h (221Ch)	**REG221C**	**7:0**	**Default : 0x21**	**Access : R/W**
	DQSM_STA_RST	7		
	DQSM_RST_SEL	6		
	DQSM_SW_RST	5		
	REF_WPTR_EN	4		
	DQSM_DLY[2:0]	3:1		
	EN_MASK	0		
07h (221Dh)	**REG221D**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	R_DQSM_STATUS_RISE[1:0]	7:6	Dqs mask rising edge status.	
	R_DQSM_STATUS_FALL[1:0]	5:4	Dqs mask falling edge status.	
	RESERVED_1F	3		
	DQSM1_SKEW[2:0]	2:0		
08h (2220h)	**REG2220**	**7:0**	**Default : 0x00**	**Access : R/W**
	DLL1_LOW_SPD_EN	7		
	DLL0_LOW_SPD_EN	6		
	DLL_BYPASS_EN[5:0]	5:0		
08h	**REG2221**	**7:0**	**Default : 0x00**	**Access : R/W**

MIU_ATOP Register (Bank = 11)

Index (Absolute)	Mnemonic	Bit	Description	
(2221h)	DRV_DATA	7		
	DRV_CMD	6		
	RXCLK_CPL_EN[5:0]	5:0		
09h (2224h)	**REG2224**	**7:0**	**Default : 0x00**	**Access : R/W**
	TDLINE_SEL[3:0]	7:4		
	-	3:2	Reserved.	
	DQS_DLY_SEL[1:0]	1:0		
09h (2225h)	**REG2225**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_09[2:0]	7:5		
	DQS_TEST_EN_A	4		
	RESERVED_09_0[1:0]	3:2		
	DQS1_DLY_SEL[1:0]	1:0		
0Ah (2228h)	**REG2228**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	ODTM_DLY[2:0]	7:5	Odt mask delay.	
	EN_ODT_MASK	4	Chip side odt mask.	
	R_DQS025X_CNT[3:0]	3:0	Dqs025x cnt status.	
0Ah (2229h)	**REG2229**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_0A[6:0]	7:1		
	DDRPLL_CLKPH_MAP_EN	0	DDRPLL_CLKPH_MAP_EN.	
0Bh (222Ch)	**REG222C**	**7:0**	**Default : 0x00**	**Access : R/W**
	IO_TEST_DATA[7:0]	7:0		
0Bh (222Dh)	**REG222D**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_0B[7:0]	7:0		
0Ch (2230h)	**REG2230**	**7:0**	**Default : 0x00**	**Access : R/W**
	CMD_LFSR_EN	7	For internal test only.	
	RDCRC_DATA_SEL[2:0]	6:4	For internal test only.	
	RDPTG_EN	3	For internal test only.	
	WDCRC_STOP	2	For internal test only.	
	WDCRC_START	1	For internal test only.	
	WDCRC_RST	0	For internal test only.	
0Ch (2231h)	**REG2231**	**7:0**	**Default : 0x0E**	**Access : R/W**
	RESERVED_0C	7		
	DDR2_8BIT	6	For sel ddr2 8bits.	

MIU_ATOP Register (Bank = 11)

Index (Absolute)	Mnemonic	Bit	Description	
	SEL_DQS_SINGLE_LATCH	5	For sel dqs single latch.	
	SEL_DQS_DIF	4	For sel dqs dif.	
	IO_TEST_RST[2:0]	3:1	For internal test only.	
	IO_TEST_EN	0	For internal test only.	
0Dh (2234h)	**REG2234**	**7:0**	**Default : 0x00**	**Access : R/W**
	PTN_MODE[7:0]	7:0	For internal test only.	
0Dh (2235h)	**REG2235**	**7:0**	**Default : 0x00**	**Access : R/W**
	PTN_MODE[15:8]	7:0	See description of '2234h'.	
0Eh (2238h)	**REG2238**	**7:0**	**Default : 0x00**	**Access : R/W**
	PTN_DATA[7:0]	7:0	For internal test only.	
0Eh (2239h)	**REG2239**	**7:0**	**Default : 0x00**	**Access : R/W**
	PTN_DATA[15:8]	7:0	See description of '2238h'.	
0Fh (223Ch)	**REG223C**	**7:0**	**Default : 0x00**	**Access : RO**
	R_READ_CRC[7:0]	7:0	For internal test only.	
0Fh (223Dh)	**REG223D**	**7:0**	**Default : 0x00**	**Access : RO**
	R_READ_CRC[15:8]	7:0	See description of '223Ch'.	
10h (2240h)	**REG2240**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7	Reserved.	
	DDRIP[2:0]	6:4	Clock generator loop filter resistor.	
	-	3:1	Reserved.	
	ENFRUNZ	0	Vco free run disable.	
10h (2241h)	**REG2241**	**7:0**	**Default : 0x00**	**Access : RO**
	R_DDRPLL_LOCK	7	For internal test only.	
	R_DDRPLL_SSC_OFF	6	For internal test only.	
	R_HIGH_FLAG	5	For internal test only.	
	-	4:0	Reserved.	
11h (2244h)	**REG2244**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDRAT[7:0]	7:0		
11h (2245h)	**REG2245**	**7:0**	**Default : 0x3C**	**Access : R/W**
	DDRAT[15:8]	7:0	See description of '2244h'.	
12h (2248h)	**REG2248**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDRAT[23:16]	7:0	See description of '2244h'.	
12h	**REG2249**	**7:0**	**Default : 0x00**	**Access : R/W**

MIU_ATOP Register (Bank = 11)

Index (Absolute)	Mnemonic	Bit	Description	
(2249h)	DDRAT[31:24]	7:0	See description of '2244h'.	
13h (224Ch)	**REG224C**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_13[7:0]	7:0		
13h (224Dh)	**REG224D**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_13[15:8]	7:0	See description of '224Ch'.	
14h (2250h)	**REG2250**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDFSTEP[7:0]	7:0	Clock spread spectrum step.	
14h (2251h)	**REG2251**	**7:0**	**Default : 0x80**	**Access : R/W**
	DDR_SSC_EN	7	Clock spread spectrum enable.	
	DDR_SSC_MODE	6	Clock spread spectrum mode.	
	DDFT[1:0]	5:4	Clock generator test mode.	
	-	3:2	Reserved.	
	DDFSTEP[9:8]	1:0	See description of '2250h'.	
15h (2254h)	**REG2254**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDFSPAN[7:0]	7:0	Clock spread spectrum period.	
15h (2255h)	**REG2255**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	DDFSPAN[13:8]	5:0	See description of '2254h'.	
16h (2258h)	**REG2258**	**7:0**	**Default : 0x04**	**Access : RO, R/W**
	R_DUTY_FLAG	7		
	RESERVED_16_6_	6		
	DUTY_DIV[1:0]	5:4		
	DUTY_VT[1:0]	3:2		
	DUTY_EXPECT	1		
	DUTY_ENDUTY	0		
16h (2259h)	**REG2259**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_16[7:0]	7:0		
17h (225Ch)	**REG225C**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_17[7:0]	7:0		
17h (225Dh)	**REG225D**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_17[15:8]	7:0	See description of '225Ch'.	
18h (2260h)	**REG2260**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDFSET[7:0]	7:0	Clock generator frequency set.	

MIU_ATOP Register (Bank = 11)

Index (Absolute)	Mnemonic	Bit	Description	
18h (2261h)	**REG2261**	**7:0**	**Default : 0x02**	**Access : R/W**
	DDFSET[15:8]	7:0	See description of '2260h'.	
19h (2264h)	**REG2264**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDFSET[23:16]	7:0	See description of '2260h'.	
19h (2265h)	**REG2265**	**7:0**	**Default : 0x80**	**Access : R/W**
	DDRPLL_PD	7	Pll power down mode.	
	DDRPLL_PORST	6	Pll power on reset.	
	DDRPLL_RESET	5	Pll reset.	
	-	4:0	Reserved.	
1Ah (2268h)	**REG2268**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDRPLL_INPUT_DIV_SECOND[7:0]	7:0	Set the clock frequency for dram.	
1Ah (2269h)	**REG2269**	**7:0**	**Default : 0x03**	**Access : R/W**
	DDRPLL_LOOP_DIV_SECOND[7:0]	7:0	Set the clock frequency for dram.	
1Bh (226Ch)	**REG226C**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	CLKPH_CKO[3:0]	3:0	MCLK2X_SKEW_MCLK phase select.	
1Bh (226Dh)	**REG226D**	**7:0**	**Default : 0x40**	**Access : R/W**
	DDRPLL_LOOP_DIV_FIRST[1:0]	7:6	Set the clock frequency for dram.	
	DDRPLL_INPUT_DIV_FIRST[1:0]	5:4	Set the clock frequency for dram.	
	-	3:0	Reserved.	
1Ch (2270h)	**REG2270**	**7:0**	**Default : 0x66**	**Access : R/W**
	CLKPH_DQ1[3:0]	7:4	MCLK2X_SKEW_DQ1 phase select.	
	CLKPH_DQ0[3:0]	3:0	MCLK2X_SKEW_DQ0 phase select.	
1Ch (2271h)	**REG2271**	**7:0**	**Default : 0x22**	**Access : R/W**
	CLKPH_DQS1[3:0]	7:4	MCLK2X_SKEW_DQS1 phase select.	
	CLKPH_DQS0[3:0]	3:0	MCLK2X_SKEW_DQS0 phase select.	
1Dh (2274h)	**REG2274**	**7:0**	**Default : 0x22**	**Access : R/W**
	CLKPH_DQSM[3:0]	7:4	MCLK2X_SKEW_DQSMASK phase select.	
	CLKPH_CMD[3:0]	3:0	MCLK2X_SKEW_CMD phase select.	
1Dh (2275h)	**REG2275**	**7:0**	**Default : 0x22**	**Access : R/W**
	CLKPH_SP1[3:0]	7:4	MCLK2X_SKEW_spare1 phase select.	
	CLKPH_SP0[3:0]	3:0	MCLK2X_SKEW_spare0 phase select.	
1Eh	**REG2278**	**7:0**	**Default : 0x30**	**Access : R/W**

MIU_ATOP Register (Bank = 11)

Index (Absolute)	Mnemonic	Bit	Description	
(2278h)	DQS_PRE_STATE[7:0]	7:0	Set the DQS preamble waveform.	
1Eh (2279h)	**REG2279**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	DQS_SKEW[2:0]	6:4		
	-	3	Reserved.	
	DQSM_SKEW[2:0]	2:0		
1Fh (227Ch)	**REG227C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	DQ_SKEW[2:0]	6:4		
	-	3	Reserved.	
	OEN_SKEW[2:0]	2:0		
1Fh (227Dh)	**REG227D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CKO_SKEW[2:0]	6:4		
	-	3	Reserved.	
	CMD_SKEW[2:0]	2:0		
28h (22A0h)	**REG22A0**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_28[7:0]	7:0		
28h (22A1h)	**REG22A1**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_28[15:8]	7:0	See description of '22A0h'.	
29h (22A4h)	**REG22A4**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_29[7:0]	7:0		
29h (22A5h)	**REG22A5**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_29[15:8]	7:0	See description of '22A4h'.	
2Ah (22A8h)	**REG22A8**	**7:0**	**Default : 0x33**	**Access : R/W**
	RESERVED_2A[0]	7		
	DRVP_CLK[2:0]	6:4		
	-	3	Reserved.	
	DRVN_CLK[2:0]	2:0		
2Ah (22A9h)	**REG22A9**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_2A[8:1]	7:0	See description of '22A8h'.	
2Eh (22B8h)	**REG22B8**	**7:0**	**Default : 0x33**	**Access : R/W**
	-	7	Reserved.	

MIU_ATOP Register (Bank = 11)

Index (Absolute)	Mnemonic	Bit	Description	
	DRVN_UDQS[2:0]	6:4	DRVN.	
	-	3	Reserved.	
	DRVN_LDQS[2:0]	2:0	DRVN.	
2Eh (22B9h)	**REG22B9**	**7:0**	**Default : 0x33**	**Access : R/W**
	-	7	Reserved.	
	DRVN_CMD[2:0]	6:4	DRVN.	
	-	3	Reserved.	
	DRVN_DQ[2:0]	2:0	DRVN.	
2Fh (22BCh)	**REG22BC**	**7:0**	**Default : 0x33**	**Access : R/W**
	-	7	Reserved.	
	DRVP_UDQS[2:0]	6:4	DRVP.	
	-	3	Reserved.	
	DRVP_LDQS[2:0]	2:0	DRVP.	
2Fh (22BDh)	**REG22BD**	**7:0**	**Default : 0x33**	**Access : R/W**
	-	7	Reserved.	
	DRVP_CMD[2:0]	6:4	DRVP.	
	-	3	Reserved.	
	DRVP_DQ[2:0]	2:0	DRVP.	
30h (22C0h)	**REG22C0**	**7:0**	**Default : 0x0A**	**Access : R/W**
	DLL_TEST_CLK_EN	7	Test CLK enable.	
	DLL_LOW_SPD_EN	6	Reduce the speed of the dll, it is for ddr2.	
	AVG_MODE[1:0]	5:4	Average mode setting: 0: Single; 1: by2; 2: by4; 3: by8.	
	DLL_CHG_N	3	Sample clock set by SW.	
	DLL_RST	2	DLL Calibration Reset.	
	DLL_PD	1	DLL Calibration HW power down.	
	DLL_CAL_SW	0	DLL Calibration SW mode.	
30h (22C1h)	**REG22C1**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	R_DLL_REDU_CODE	7	Calibration output.	
	DLL_RD_OUT_SEL[2:0]	6:4	Reg33 read out selection: 0: Reg_r_sar_cnt; 1:reg_r_dll_code; 2: reg_r_avg; 3:reg_r_dll0_code; 4:reg_r_dll1_code.	
	SAR_OFF	3	Test CLK enable.	

MIU_ATOP Register (Bank = 11)

Index (Absolute)	Mnemonic	Bit	Description	
	AVG_EN	2	Reduce the speed of the dll, it is for ddr2.	
	HW_UPCODE_EN	1	Enable HW auto update DLL code setting in refresh period.	
	DYN_UPCODE_EN	0	Enable update DLL code setting in refresh period.	
31h (22C4h)	**REG22C4**	**7:0**	**Default : 0x20**	**Access : R/W**
	DLL_PS_CYCLE[7:0]	7:0	Change the pulse time of DLL.	
31h (22C5h)	**REG22C5**	**7:0**	**Default : 0x00**	**Access : R/W**
	DLL_TEST[7:0]	7:0	For dll test.	
32h (22C8h)	**REG22C8**	**7:0**	**Default : 0x01**	**Access : R/W**
	DLL_CODE[7:0]	7:0	Change the delay time of the DLL (0: max delay,. 1: Min delay).	
32h (22C9h)	**REG22C9**	**7:0**	**Default : 0xF0**	**Access : R/W**
	DLL_PH[3:0]	7:4	Select the phase of DLL.	
	-	3:2	Reserved.	
	DLL_CODE[9:8]	1:0	See description of '22C8h'.	
33h (22CCh)	**REG22CC**	**7:0**	**Default : 0x00**	**Access : RO**
	R_DLL_RD_OUT[7:0]	7:0	For internal test only.	
33h (22CDh)	**REG22CD**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	ALWAYS_IN	7		
	RESERVED_33[4:0]	6:2		
	R_DLL_RD_OUT[9:8]	1:0	See description of '22CCh'.	
34h (22D0h)	**REG22D0**	**7:0**	**Default : 0x00**	**Access : R/W**
	DLL0_CODE[7:0]	7:0	For dqs0 dll.	
34h (22D1h)	**REG22D1**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:2	Reserved.	
	DLL0_CODE[9:8]	1:0	See description of '22D0h'.	
35h (22D4h)	**REG22D4**	**7:0**	**Default : 0x00**	**Access : R/W**
	DLL1_CODE[7:0]	7:0	For dqs1 dll.	
35h (22D5h)	**REG22D5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	DLL1_CODE[9:8]	1:0	See description of '22D4h'.	
36h (22D8h)	**REG22D8**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_36[7:0]	7:0		

MIU_ATOP Register (Bank = 11)

Index (Absolute)	Mnemonic	Bit	Description	
36h (22D9h)	**REG22D9**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_36[15:8]	7:0	See description of '22D8h'.	
37h (22DCh)	**REG22DC**	**7:0**	**Default : 0xDD**	**Access : R/W**
	DLL1_PH[3:0]	7:4	For 1 dqs delay phase select.	
	DLL0_PH[3:0]	3:0	For 0 dqs delay phase select.	
38h (22E0h)	**REG22E0**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_38[4:0]	7:3		
	REC_CAL_HLVL_CHG	2	Inverter the output.	
	REC_CAL_EN	1	Receiver Calibration HW enable.	
	REC_CAL_SW	0	Receiver Calibration SW mode.	
38h (22E1h)	**REG22E1**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	R_REC_CAL_HIGH	7	Calibration output.	
	REC_CAL_REFSEL[2:0]	6:4	Select the trig level reference of the receiver calibration.	
	-	3:2	Reserved.	
	HW_UPTRLVL_EN	1	Enable HW auto update Trigger level setting in refresh period.	
	DYN_UPTRLVL_EN	0	Enable update Trigger level setting in refresh period.	
39h (22E4h)	**REG22E4**	**7:0**	**Default : 0x01**	**Access : R/W**
	RESERVED_39	7		
	REC_CAL_TRIG_CNT[2:0]	6:4	Auto calibration iteration number.	
	REC_CAL_TRIG_LVL[3:0]	3:0	Trigger level setting by SW.	
39h (22E5h)	**REG22E5**	**7:0**	**Default : 0x00**	**Access : RO**
	R_REC_CAL_TRIG_LVL[3:0]	7:4	Auto update value.	
	R_REC_CAL_CNT[3:0]	3:0	Calibration HW counter output.	
3Ah (22E8h)	**REG22E8**	**7:0**	**Default : 0x00**	**Access : R/W**
	REC_TRIG_LVL1[3:0]	7:4	IO pad receiver trigger level control bits.	
	REC_TRIG_LVL0[3:0]	3:0	IO pad receiver trigger level control bits.	
3Ah (22E9h)	**REG22E9**	**7:0**	**Default : 0x00**	**Access : R/W**
	REC_TRIG_LVL3[3:0]	7:4	IO pad receiver trigger level control bits.	
	REC_TRIG_LVL2[3:0]	3:0	IO pad receiver trigger level control bits.	
3Bh (22ECh)	**REG22EC**	**7:0**	**Default : 0x00**	**Access : R/W**
	REC_TRIG_LVL5[3:0]	7:4	IO pad receiver trigger level control bits.	
	REC_TRIG_LVL4[3:0]	3:0	IO pad receiver trigger level control bits.	

MIU_ATOP Register (Bank = 11)

Index (Absolute)	Mnemonic	Bit	Description	
3Bh (22EDh)	**REG22ED**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_3B[1:0]	7:6		
	DRV_CAL_RST_DATA	5		
	DRV_CAL_RST	4		
	REC_TRIG_LVL6[3:0]	3:0	IO pad receiver trigger level control bits.	
3Ch (22F0h)	**REG22F0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEL_DRV_CAL_PMOS	7	Select calibration PMOS.	
	SEL_DRV_CAL_HSCMP	6	Select high speed comparator for calibration.	
	SEL_DDR2	5	Select DDR2 mode.	
	DRV_CAL_RES_MEASURE_EN	4	Enable to measure the internal resistor.	
	DRV_CAL_SAMP	3	Sample clock of offset cancellation comparator.	
	DRV_CAL_HLVL_CHG	2	Inverter the output.	
	DRV_CAL_EN	1	Driving Calibration HW enable.	
	DRV_CAL_SW	0	Driving Calibration SW mode.	
3Ch (22F1h)	**REG22F1**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	R_DRV_CAL_HIGH	7	Calibration output.	
	DRV_CAL_S[2:0]	6:4	Driver strength programmable resister.	
	-	3:2	Reserved.	
	HW_UPDRV_EN	1	Enable HW auto update Trim Resistor setting in refresh period.	
	DYN_UPDRV_EN	0	Enable update Trim Resistor setting in refresh period.	
3Dh (22F4h)	**REG22F4**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRV_CAL_DRV_CNT[2:0]	7:5	Auto calibration iteration number.	
	DRV_CAL_TRMRES_SW	4	Trim resistor setting by SW.	
	DRV_CAL_TRMRES[3:0]	3:0	Trim resistor setting by SW.	
3Dh (22F5h)	**REG22F5**	**7:0**	**Default : 0x00**	**Access : RO**
	R_DRV_CAL_DRV[3:0]	7:4	Auto update value.	
	R_DRV_CAL_CNT[3:0]	3:0	Calibration HW counter output.	
3Eh (22F8h)	**REG22F8**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_3E[7:0]	7:0		
3Eh (22F9h)	**REG22F9**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_3E[15:8]	7:0	See description of '22F8h'.	
3Fh	**REG22FC**	**7:0**	**Default : 0x00**	**Access : R/W**

MIU_ATOP Register (Bank = 11)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(22FCh)	RESERVED_3F[7:0]	7:0		
3Fh (22FDh)	**REG22FD**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_3F[15:8]	7:0	See description of '22FCh'.	

MIU_DIG Register (Bank = 12)

MIU_DIG Register (Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2400h)	**REG2400**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	AUTO_REF_OFF	5	Turn off auto refresh.	
	ODT	4	Turn on ODT (only for ddr2/ddr3).	
	RSTZ	3	Dram reset.	
	CS	2	Dram chip select.	
	CKE	1	Enable CKE.	
	INIT_MIU	0	Auto initial dram cycle.	
00h (2401h)	**REG2401**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	R_INIT_DONE	7	Auto initial dram cycle done flag.	
	R_SINGLE_CMD_DONE	6	Single cmd done flag.	
	SELF_REFRESH	5	Enter self refresh mode.	
	DPD	4	Enter deep power down mode (mobile dram only).	
	SINGLE_CMD[2:0]	3:1	Single cmd= {rasz,casz,wez}.	
	SINGLE_CMD_EN	0	Issue single cmd.	
01h (2404h)	**REG2404**	**7:0**	**Default : 0x00**	**Access : R/W**
	CA_SIZE[1:0]	7:6	00: 8col, 01: 9col, 10: 10col, 11: reserved.	
	BA_SIZE[1:0]	5:4	00: 2ba, 01: 4ba, 10: 8ba, 11: reserved.	
	DRAM_BUS[1:0]	3:2	00: 16bit, 01: 32bit, 10: 64bit, 11: reserved.	
	DRAM_TYPE[1:0]	1:0	00: Sdr, 01: ddr, 10: ddr2, 11: ddr3.	
01h (2405h)	**REG2405**	**7:0**	**Default : 0xF0**	**Access : R/W**
	CKO_OENZ	7	Ck output enable.	
	ADR_OENZ	6	Address output enable.	
	DQ_OENZ	5	Data output enable.	
	CKE_OENZ	4	Cke output enable.	
	DATA_SWAP[1:0]	3:2	01: [15:0], 10: [31:16].	
	DATA_RATIO[1:0]	1:0	00: 1x, 01: 2x, 10: 4x, 11: 8x.	
02h (2408h)	**REG2408**	**7:0**	**Default : 0x09**	**Access : R/W**
	I64_MODE	7	0: All 128 internal bus, 1: support 64 internal bus (only 4x mode).	
	FORCE_DDR_RD_ACT	6	Force the access status to read, for analog design reference.	

MIU_DIG Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
	-	5	Reserved.	
	RD_TIMING[4:0]	4:0	Read back data delay timing.	
02h (2409h)	**REG2409**	**7:0**	**Default : 0x00**	**Access : R/W**
	SRC_MCLK_DLY[1:0]	7:6	Select clock delay path.	
	SRC_MCLK_INV	5	Select inversed clock source.	
	SRC_MCLK_SEL	4	Clock source select.	
	MCP_TYPE	3	Internal MCP sdram type select.	
	MCP_EN	2	Internal MCP sdram enable.	
	RD_MCK_SEL	1	Feedback mclk/internal mclk.	
	RD_IN_PHASE	0	Read timing phase.	
03h (240Ch)	**REG240C**	**7:0**	**Default : 0x08**	**Access : R/W**
	TREFPERIOD[7:0]	7:0	Refresh cycle period, unit 16 mclk.	
03h (240Dh)	**REG240D**	**7:0**	**Default : 0x04**	**Access : R/W**
	SCRAMBLE_EN	7	Enable scramble function.	
	MOBILE_DRAM	6	Dram type is mobile dram.	
	ODT_ALWAYS_ON	5	Odt always on.	
	CKE_ALWAYS_ON	4	Cke always on.	
	I32_MODE	3	Support 32 internal bus.	
	TCKE[2:0]	2:0	Dram TCKE timing.	
04h (2410h)	**REG2410**	**7:0**	**Default : 0x33**	**Access : R/W**
	TRP[3:0]	7:4	Dram TRP timing.	
	TRCD[3:0]	3:0	Dram TRCD timing.	
04h (2411h)	**REG2411**	**7:0**	**Default : 0x08**	**Access : R/W**
	TRP_4	7	Dram tRP timing counter bit4.	
	TRCD_4	6	Dram tRCD timing counter bit4.	
	TRAS[5:0]	5:0	Dram TRAS timing.	
05h (2414h)	**REG2414**	**7:0**	**Default : 0x12**	**Access : R/W**
	TRTP[3:0]	7:4	Dram TRTP timing.	
	TRRD[3:0]	3:0	Dram TRRD timing.	
05h (2415h)	**REG2415**	**7:0**	**Default : 0x0C**	**Access : R/W**
	-	7:6	Reserved.	
	TRC[5:0]	5:0	Dram TRC timing.	
06h	**REG2418**	**7:0**	**Default : 0x61**	**Access : R/W**

MIU_DIG Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
(2418h)	TWR[3:0]	7:4	Dram TWR timing: write recovery time.	
	TWL[3:0]	3:0	Dram TWL timing: write latency.	
06h (2419h)	**REG2419**	**7:0**	**Default : 0x63**	**Access : R/W**
	TRTW[3:0]	7:4	Read to write delay.	
	TWTR[3:0]	3:0	Dram TWTR timing: write to read delay.	
07h (241Ch)	**REG241C**	**7:0**	**Default : 0x0E**	**Access : R/W**
	TRFC[7:0]	7:0	Dram TRFC timing.	
07h (241Dh)	**REG241D**	**7:0**	**Default : 0x10**	**Access : R/W**
	TWR_4	7	Dram tWR timing counter bit4: write recovery time.	
	TCCD[2:0]	6:4	Dram TCCD timing.	
	-	3:0	Reserved.	
08h (2420h)	**REG2420**	**7:0**	**Default : 0x00**	**Access : R/W**
	MR0[7:0]	7:0	Mode register 0.	
08h (2421h)	**REG2421**	**7:0**	**Default : 0x00**	**Access : R/W**
	MR0[15:8]	7:0	See description of '2420h'.	
09h (2424h)	**REG2424**	**7:0**	**Default : 0x00**	**Access : R/W**
	MR1[7:0]	7:0	Mode register 1.	
09h (2425h)	**REG2425**	**7:0**	**Default : 0x40**	**Access : R/W**
	MR1[15:8]	7:0	See description of '2424h'.	
0Ah (2428h)	**REG2428**	**7:0**	**Default : 0x00**	**Access : R/W**
	MR2[7:0]	7:0	Mode register 2.	
0Ah (2429h)	**REG2429**	**7:0**	**Default : 0x80**	**Access : R/W**
	MR2[15:8]	7:0	See description of '2428h'.	
0Bh (242Ch)	**REG242C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MR3[7:0]	7:0	Mode register 3.	
0Bh (242Dh)	**REG242D**	**7:0**	**Default : 0xC0**	**Access : R/W**
	MR3[15:8]	7:0	See description of '242Ch'.	
0Ch (2430h)	**REG2430**	**7:0**	**Default : 0x00**	**Access : R/W**
	MRX[7:0]	7:0	Single command mode register.	
0Ch (2431h)	**REG2431**	**7:0**	**Default : 0x00**	**Access : R/W**
	MRX[15:8]	7:0	See description of '2430h'.	
0Dh (2434h)	**REG2434**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEB_SEL[7:0]	7:0	For internal test only, select debug result.	

MIU_DIG Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
0Dh (2435h)	**REG2435**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEB_SEL[15:8]	7:0	See description of '2434h'.	
0Eh (2438h)	**REG2438**	**7:0**	**Default : 0x00**	**Access : RO**
	R_DEB_BUS[7:0]	7:0	Debug port.	
0Eh (2439h)	**REG2439**	**7:0**	**Default : 0x00**	**Access : RO**
	R_DEB_BUS[15:8]	7:0	See description of '2438h'.	
0Fh (243Ch)	**REG243C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_RST_G3	7	Miu arbiter group 3 software reset.	
	SW_RST_G2	6	Miu arbiter group 2 software reset.	
	SW_RST_G1	5	Miu arbiter group 1 software reset.	
	SW_RST_G0	4	Miu arbiter group 0 software reset.	
	SW_INIT_DONE	3	Sw initial done and turn on arbiter.	
	-	2	Reserved.	
	DFT_ADRMD	1	For internal test only.	
	SW_RST_MIU	0	Miu software reset.	
0Fh (243Dh)	**REG243D**	**7:0**	**Default : 0x0C**	**Access : R/W**
	NO_RQ_CTRL_EN	7	Turn on the function of when there is no any other request to MIU, let MIU keep servicing the client which is timeouted.	
	CMD_FIFO_4_STAGE	6	Control command fifo to 4 stage (default 8 stage).	
	SYNC_IN_16_STAGE	5	Control sync fifo to 16 stage (default 8 stage).	
	SYNC_OUT_THRESHOLD[4:0]	4:0	Sync out FIFO full threshold.	
10h (2440h)	**REG2440**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_ORDER_CTRL_EN[7:0]	7:0	Request group 0 order control.	
10h (2441h)	**REG2441**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_ORDER_CTRL_EN[15:8]	7:0	See description of '2440h'.	
11h (2444h)	**REG2444**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_ORDER_CTRL_EN[7:0]	7:0	Request group 1 order control.	
11h (2445h)	**REG2445**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_ORDER_CTRL_EN[15:8]	7:0	See description of '2444h'.	
12h (2448h)	**REG2448**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ2_ORDER_CTRL_EN[7:0]	7:0	Request group 2 order control.	
12h	**REG2449**	**7:0**	**Default : 0x00**	**Access : R/W**

MIU_DIG Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
(2449h)	RQ2_ORDER_CTRL_EN[15:8]	7:0	See description of '2448h'.	
13h (244Ch)	**REG244C**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ3_ORDER_CTRL_EN[7:0]	7:0	Request group 3 order control.	
13h (244Dh)	**REG244D**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ3_ORDER_CTRL_EN[15:8]	7:0	See description of '244Ch'.	
14h (2450h)	**REG2450**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_14_0[3:0]	7:4	Reserved.	
	MULTI_ACT_CTRL_EN2	3	Id3 act 2 ba enable.	
	MULTI_ACT_CTRL_EN1	2	Id2 act 2 ba enable.	
	MULTI_ACT_CTRL_EN0	1	Id1 act 2 ba enable.	
	MULTI_ACT_CTRL_EN	0	All client act 2 ba enable.	
14h (2451h)	**REG2451**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_14_1[1:0]	7:6	Reserved.	
	MULTI_ACT_CTRL_ID0[5:0]	5:0	Id1 for act 2 ba.	
15h (2454h)	**REG2454**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_15_0[1:0]	7:6	Reserved.	
	MULTI_ACT_CTRL_ID1[5:0]	5:0	Id2 for act 2 ba.	
15h (2455h)	**REG2455**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_15_1[1:0]	7:6	Reserved.	
	MULTI_ACT_CTRL_ID2[5:0]	5:0	Id3 for act 2 ba.	
16h (2458h)	**REG2458**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADDR_BALANCE_SEL[7:0]	7:0	Address switch control.	
16h (2459h)	**REG2459**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADDR_BALANCE_SEL[15:8]	7:0	See description of '2458h'.	
17h (245Ch)	**REG245C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GROUP_DATA_MASK[7:0]	7:0	For internal test.	
17h (245Dh)	**REG245D**	**7:0**	**Default : 0x00**	**Access : R/W**
	GROUP_DATA_MASK[15:8]	7:0	See description of '245Ch'.	
18h (2460h)	**REG2460**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	RO_PROTECT2_EN	2	Read only protect 2 enable.	
	RO_PROTECT1_EN	1	Read only protect 1 enable.	
	RO_PROTECT0_EN	0	Read only protect 0 enable.	

MIU_DIG Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
18h (2461h)	**REG2461**	**7:0**	**Default : 0x00**	**Access : R/W**
	ANA_BIST_EN	7	For internal test only.	
	ADC_TEST_EN	6	For internal test only.	
	-	5:0	Reserved.	
19h (2464h)	**REG2464**	**7:0**	**Default : 0x00**	**Access : R/W**
	RO_PROTECT0_START[7:0]	7:0	Read only protect 0 start address unit 4kb.	
19h (2465h)	**REG2465**	**7:0**	**Default : 0x00**	**Access : R/W**
	RO_PROTECT0_START[15:8]	7:0	See description of '2464h'.	
1Ah (2468h)	**REG2468**	**7:0**	**Default : 0x00**	**Access : R/W**
	RO_PROTECT0_END[7:0]	7:0	Read only protect 0 end address unit 4kb.	
1Ah (2469h)	**REG2469**	**7:0**	**Default : 0x00**	**Access : R/W**
	RO_PROTECT0_END[15:8]	7:0	See description of '2468h'.	
1Bh (246Ch)	**REG246C**	**7:0**	**Default : 0x00**	**Access : R/W**
	RO_PROTECT1_START[7:0]	7:0	Read only protect 1 start address unit 4kb.	
1Bh (246Dh)	**REG246D**	**7:0**	**Default : 0x00**	**Access : R/W**
	RO_PROTECT1_START[15:8]	7:0	See description of '246Ch'.	
1Ch (2470h)	**REG2470**	**7:0**	**Default : 0x00**	**Access : R/W**
	RO_PROTECT1_END[7:0]	7:0	Read only protect 1 end address unit 4kb.	
1Ch (2471h)	**REG2471**	**7:0**	**Default : 0x00**	**Access : R/W**
	RO_PROTECT1_END[15:8]	7:0	See description of '2470h'.	
1Dh (2474h)	**REG2474**	**7:0**	**Default : 0x00**	**Access : R/W**
	RO_PROTECT2_START[7:0]	7:0	Read only protect 2 start address unit 4kb.	
1Dh (2475h)	**REG2475**	**7:0**	**Default : 0x00**	**Access : R/W**
	RO_PROTECT2_START[15:8]	7:0	See description of '2474h'.	
1Eh (2478h)	**REG2478**	**7:0**	**Default : 0x00**	**Access : R/W**
	RO_PROTECT2_END[7:0]	7:0	Read only protect 2 start address unit 4kb.	
1Eh (2479h)	**REG2479**	**7:0**	**Default : 0x00**	**Access : R/W**
	RO_PROTECT2_END[15:8]	7:0	See description of '2478h'.	
1Fh (247Ch)	**REG247C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GATED_CONTROL[7:0]	7:0	For power saving gated control.	
1Fh (247Dh)	**REG247D**	**7:0**	**Default : 0x00**	**Access : R/W**
	GATED_CONTROL[15:8]	7:0	See description of '247Ch'.	
20h	**REG2480**	**7:0**	**Default : 0x00**	**Access : R/W**

MIU_DIG Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
(2480h)	-	7	Reserved.	
	RQ0_CEASELESS_EN	6	Group 0 ceaseless enable.	
	RQ0_GROUP_DEADLINE_EN	5	Group 0 deadline enable.	
	RQ0_TIMEOUT_EN	4	Group 0 timeout enable.	
	RQ0_GROUP_LIMIT_EN	3	Group 0 group limit enable.	
	RQ0_MEMBER_LIMIT_EN	2	Group 0 member limit enable.	
	RQ0_SET_PRIORITY	1	Group 0 set priority pulse.	
	RQ0_ROUND_ROBIN	0	Group 0 round robin enable.	
20h (2481h)	**REG2481**	**7:0**	**Default : 0x80**	**Access : R/W**
	RQ0_ARBITER_SKIP_ON	7	Group 0 skip empty ready on.	
	RQ0_GROUP_CUT_IN_EN	6	Group 0 group cut in enable.	
	RQ0_MEMBER_CUT_IN_EN	5	Group 0 pre-arbiter cut in enable.	
	RQ0_LAST_DONE_Z_OFF	4	Group 0 last_done_z off.	
	RQ0_CNT3_CTRL_EN	3	Group 0 flow control 3 enable.	
	RQ0_CNT2_CTRL_EN	2	Group 0 flow control 2 enable.	
	RQ0_CNT1_CTRL_EN	1	Group 0 flow control 1 enable.	
	RQ0_CNT0_CTRL_EN	0	Group 0 flow control 0 enable.	
21h (2484h)	**REG2484**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_MEMBER_MAX[7:0]	7:0	Group 0 member max service number, unit 4.	
21h (2485h)	**REG2485**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_GROUP_MAX[7:0]	7:0	Group 0 group max service number, unit 4.	
22h (2488h)	**REG2488**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_TIMEOUT[7:0]	7:0	Group 0 time out number.	
22h (2489h)	**REG2489**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_TIMEOUT[15:8]	7:0	See description of '2488h'.	
23h (248Ch)	**REG248C**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_MASK[7:0]	7:0	Group 0 request mask.	
23h (248Dh)	**REG248D**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_MASK[15:8]	7:0	See description of '248Ch'.	
24h (2490h)	**REG2490**	**7:0**	**Default : 0xFF**	**Access : R/W**
	RQ0_HPMASK[7:0]	7:0	Group 0 high priority mask.	
24h (2491h)	**REG2491**	**7:0**	**Default : 0xFF**	**Access : R/W**
	RQ0_HPMASK[15:8]	7:0	See description of '2490h'.	

MIU_DIG Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
25h (2494h)	**REG2494**	**7:0**	**Default : 0x10**	**Access : R/W**
	RQ01_PRIORITY[3:0]	7:4	Group0 2nd priority id.	
	RQ00_PRIORITY[3:0]	3:0	Group0 1st priority id.	
25h (2495h)	**REG2495**	**7:0**	**Default : 0x32**	**Access : R/W**
	RQ03_PRIORITY[3:0]	7:4	Group0 4th priority id.	
	RQ02_PRIORITY[3:0]	3:0	Group0 3rd priority id.	
26h (2498h)	**REG2498**	**7:0**	**Default : 0x54**	**Access : R/W**
	RQ05_PRIORITY[3:0]	7:4	Group0 6th priority id.	
	RQ04_PRIORITY[3:0]	3:0	Group0 5th priority id.	
26h (2499h)	**REG2499**	**7:0**	**Default : 0x76**	**Access : R/W**
	RQ07_PRIORITY[3:0]	7:4	Group0 8th priority id.	
	RQ06_PRIORITY[3:0]	3:0	Group0 7th priority id.	
27h (249Ch)	**REG249C**	**7:0**	**Default : 0x98**	**Access : R/W**
	RQ09_PRIORITY[3:0]	7:4	Group0 10th priority id.	
	RQ08_PRIORITY[3:0]	3:0	Group0 9th priority id.	
27h (249Dh)	**REG249D**	**7:0**	**Default : 0xBA**	**Access : R/W**
	RQ0B_PRIORITY[3:0]	7:4	Group0 12th priority id.	
	RQ0A_PRIORITY[3:0]	3:0	Group0 11th priority id.	
28h (24A0h)	**REG24A0**	**7:0**	**Default : 0xDC**	**Access : R/W**
	RQ0D_PRIORITY[3:0]	7:4	Group0 14th priority id.	
	RQ0C_PRIORITY[3:0]	3:0	Group0 13th priority id.	
28h (24A1h)	**REG24A1**	**7:0**	**Default : 0xFE**	**Access : R/W**
	RQ0F_PRIORITY[3:0]	7:4	Group0 16th priority id.	
	RQ0E_PRIORITY[3:0]	3:0	Group0 15th priority id.	
29h (24A5h)	**REG24A5**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_GROUP_DEADLINE[7:0]	7:0	Group 0 deadline timer number.	
2Ah (24A8h)	**REG24A8**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_CNT0_ID1[3:0]	7:4	Group 0 flow control 0 id1.	
	RQ0_CNT0_ID0[3:0]	3:0	Group 0 flow control 0 id0.	
2Ah (24A9h)	**REG24A9**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_CNT0_PERIOD[7:0]	7:0	Group 0 flow control 0 period number.	
2Bh (24ACh)	**REG24AC**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_CNT1_ID1[3:0]	7:4	Group 0 flow control 1 id1.	

MIU_DIG Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
	RQ0_CNT1_ID0[3:0]	3:0	Group 0 flow control 1 id0.	
2Bh (24ADh)	**REG24AD**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_CNT1_PERIOD[7:0]	7:0	Group 0 flow control 1 period number.	
2Ch (24B0h)	**REG24B0**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_CNT2_ID1[3:0]	7:4	Group 0 flow control 2 id1.	
	RQ0_CNT2_ID0[3:0]	3:0	Group 0 flow control 2 id0.	
2Ch (24B1h)	**REG24B1**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_CNT2_PERIOD[7:0]	7:0	Group 0 flow control 2 period number.	
2Dh (24B4h)	**REG24B4**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_CNT3_ID1[3:0]	7:4	Group 0 flow control 3 id1.	
	RQ0_CNT3_ID0[3:0]	3:0	Group 0 flow control 3 id0.	
2Dh (24B5h)	**REG24B5**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_CNT3_PERIOD[7:0]	7:0	Group 0 flow control 3 period number.	
2Eh (24B8h)	**REG24B8**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_LIMIT_MASK[7:0]	7:0	Group 0 client limit mask.	
2Eh (24B9h)	**REG24B9**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_LIMIT_MASK[15:8]	7:0	See description of '24B8h'.	
2Fh (24BCh)	**REG24BC**	**7:0**	**Default : 0x00**	**Access : RO**
	R_RQ0_LAST_DONE_Z[7:0]	7:0	Group 0 last done flag.	
2Fh (24BDh)	**REG24BD**	**7:0**	**Default : 0x00**	**Access : RO**
	R_RQ0_LAST_DONE_Z[15:8]	7:0	See description of '24BCh'.	
30h (24C0h)	**REG24C0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	RQ1_CEASELESS_EN	6	Group 1 ceaseless enable.	
	RQ1_GROUP_DEADLINE_EN	5	Group 1 deadline enable.	
	RQ1_TIMEOUT_EN	4	Group 1 timeout enable.	
	RQ1_GROUP_LIMIT_EN	3	Group 1 group limit enable.	
	RQ1_MEMBER_LIMIT_EN	2	Group 1 member limit enable.	
	RQ1_SET_PRIORITY	1	Group 1 set priority pulse.	
	RQ1_ROUND_ROBIN	0	Group 1 round robin enable.	
30h (24C1h)	**REG24C1**	**7:0**	**Default : 0x80**	**Access : R/W**
	RQ1_ARBITER_SKIP_ON	7	Group 1 skip empty ready on.	
	RQ1_GROUP_CUT_IN_EN	6	Group 1 group cut in enable.	

MIU_DIG Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
	RQ1_MEMBER_CUT_IN_EN	5	Group 1 pre-arbiter cut in enable.	
	RQ1_LAST_DONE_Z_OFF	4	Group 1 last_done_z off.	
	RQ1_CNT3_CTRL_EN	3	Group 1 flow control 3 enable.	
	RQ1_CNT2_CTRL_EN	2	Group 1 flow control 2 enable.	
	RQ1_CNT1_CTRL_EN	1	Group 1 flow control 1 enable.	
	RQ1_CNT0_CTRL_EN	0	Group 1 flow control 0 enable.	
31h (24C4h)	**REG24C4**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_MEMBER_MAX[7:0]	7:0	Group 1 member max service number, unit 4.	
31h (24C5h)	**REG24C5**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_GROUP_MAX[7:0]	7:0	Group 1 group max service number, unit 4.	
32h (24C8h)	**REG24C8**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_TIMEOUT[7:0]	7:0	Group 1 time out number.	
32h (24C9h)	**REG24C9**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_TIMEOUT[15:8]	7:0	See description of '24C8h'.	
33h (24CCh)	**REG24CC**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_MASK[7:0]	7:0	Group 1 request mask.	
33h (24CDh)	**REG24CD**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_MASK[15:8]	7:0	See description of '24CCh'.	
34h (24D0h)	**REG24D0**	**7:0**	**Default : 0xFF**	**Access : R/W**
	RQ1_HPMASK[7:0]	7:0	Group 1 high priority mask.	
34h (24D1h)	**REG24D1**	**7:0**	**Default : 0xFF**	**Access : R/W**
	RQ1_HPMASK[15:8]	7:0	See description of '24D0h'.	
35h (24D4h)	**REG24D4**	**7:0**	**Default : 0x10**	**Access : R/W**
	RQ11_PRIORITY[3:0]	7:4	Group1 2nd priority id.	
	RQ10_PRIORITY[3:0]	3:0	Group1 1st priority id.	
35h (24D5h)	**REG24D5**	**7:0**	**Default : 0x32**	**Access : R/W**
	RQ13_PRIORITY[3:0]	7:4	Group1 4th priority id.	
	RQ12_PRIORITY[3:0]	3:0	Group1 3rd priority id.	
36h (24D8h)	**REG24D8**	**7:0**	**Default : 0x54**	**Access : R/W**
	RQ15_PRIORITY[3:0]	7:4	Group1 6th priority id.	
	RQ14_PRIORITY[3:0]	3:0	Group1 5th priority id.	
36h (24D9h)	**REG24D9**	**7:0**	**Default : 0x76**	**Access : R/W**
	RQ17_PRIORITY[3:0]	7:4	Group1 8th priority id.	

MIU_DIG Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
	RQ16_PRIORITY[3:0]	3:0	Group1 7th priority id.	
37h (24DCh)	**REG24DC**	**7:0**	**Default : 0x98**	**Access : R/W**
	RQ19_PRIORITY[3:0]	7:4	Group1 10th priority id.	
	RQ18_PRIORITY[3:0]	3:0	Group1 9th priority id.	
37h (24DDh)	**REG24DD**	**7:0**	**Default : 0xBA**	**Access : R/W**
	RQ1B_PRIORITY[3:0]	7:4	Group1 12th priority id.	
	RQ1A_PRIORITY[3:0]	3:0	Group1 11th priority id.	
38h (24E0h)	**REG24E0**	**7:0**	**Default : 0xDC**	**Access : R/W**
	RQ1D_PRIORITY[3:0]	7:4	Group1 14th priority id.	
	RQ1C_PRIORITY[3:0]	3:0	Group1 13th priority id.	
38h (24E1h)	**REG24E1**	**7:0**	**Default : 0xFE**	**Access : R/W**
	RQ1F_PRIORITY[3:0]	7:4	Group1 16th priority id.	
	RQ1E_PRIORITY[3:0]	3:0	Group1 15th priority id.	
39h (24E5h)	**REG24E5**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_GROUP_DEADLINE[7:0]	7:0	Group 1 deadline timer number.	
3Ah (24E8h)	**REG24E8**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_CNT0_ID1[3:0]	7:4	Group 1 flow control 0 id1.	
	RQ1_CNT0_ID0[3:0]	3:0	Group 1 flow control 0 id0.	
3Ah (24E9h)	**REG24E9**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_CNT0_PERIOD[7:0]	7:0	Group 1 flow control 0 period number.	
3Bh (24ECh)	**REG24EC**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_CNT1_ID1[3:0]	7:4	Group 1 flow control 1 id1.	
	RQ1_CNT1_ID0[3:0]	3:0	Group 1 flow control 1 id0.	
3Bh (24EDh)	**REG24ED**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_CNT1_PERIOD[7:0]	7:0	Group 1 flow control 1 period number.	
3Ch (24F0h)	**REG24F0**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_CNT2_ID1[3:0]	7:4	Group 1 flow control 2 id1.	
	RQ1_CNT2_ID0[3:0]	3:0	Group 1 flow control 2 id0.	
3Ch (24F1h)	**REG24F1**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_CNT2_PERIOD[7:0]	7:0	Group 1 flow control 2 period number.	
3Dh (24F4h)	**REG24F4**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_CNT3_ID1[3:0]	7:4	Group 1 flow control 3 id1.	
	RQ1_CNT3_ID0[3:0]	3:0	Group 1 flow control 3 id0.	

MIU_DIG Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
3Dh (24F5h)	**REG24F5**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_CNT3_PERIOD[7:0]	7:0	Group 1 flow control 3 period number.	
3Eh (24F8h)	**REG24F8**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_LIMIT_MASK[7:0]	7:0	Group 1 client limit mask.	
3Eh (24F9h)	**REG24F9**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_LIMIT_MASK[15:8]	7:0	See description of '24F8h'.	
3Fh (24FCh)	**REG24FC**	**7:0**	**Default : 0x00**	**Access : RO**
	R_RQ1_LAST_DONE_Z[7:0]	7:0	Group 1 last done flag.	
3Fh (24FDh)	**REG24FD**	**7:0**	**Default : 0x00**	**Access : RO**
	R_RQ1_LAST_DONE_Z[15:8]	7:0	See description of '24FCh'.	
40h (2500h)	**REG2500**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	RQ2_CEASELESS_EN	6	Group 2 ceaseless enable.	
	RQ2_GROUP_DEADLINE_EN	5	Group 2 deadline enable.	
	RQ2_TIMEOUT_EN	4	Group 2 timeout enable.	
	RQ2_GROUP_LIMIT_EN	3	Group 2 group limit enable.	
	RQ2_MEMBER_LIMIT_EN	2	Group 2 member limit enable.	
	RQ2_SET_PRIORITY	1	Group 2 set priority pulse.	
	RQ2_ROUND_ROBIN	0	Group 2 round robin enable.	
40h (2501h)	**REG2501**	**7:0**	**Default : 0x80**	**Access : R/W**
	RQ2_ARBITER_SKIP_ON	7	Group 2 skip empty ready on.	
	RQ2_GROUP_CUT_IN_EN	6	Group 2 group cut in enable.	
	RQ2_MEMBER_CUT_IN_EN	5	Group 2 pre-arbiter cut in enable.	
	RQ2_LAST_DONE_Z_OFF	4	Group 2 last_done_z off.	
	RQ2_CNT3_CTRL_EN	3	Group 2 flow control 3 enable.	
	RQ2_CNT2_CTRL_EN	2	Group 2 flow control 2 enable.	
	RQ2_CNT1_CTRL_EN	1	Group 2 flow control 1 enable.	
	RQ2_CNT0_CTRL_EN	0	Group 2 flow control 0 enable.	
41h (2504h)	**REG2504**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ2_MEMBER_MAX[7:0]	7:0	Group 2 member max service number, unit 4.	
41h (2505h)	**REG2505**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ2_GROUP_MAX[7:0]	7:0	Group 2 group max service number, unit 4.	
42h	**REG2508**	**7:0**	**Default : 0x00**	**Access : R/W**

MIU_DIG Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
(2508h)	RQ2_TIMEOUT[7:0]	7:0	Group 2 time out number.	
42h (2509h)	**REG2509**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ2_TIMEOUT[15:8]	7:0	See description of '2508h'.	
43h (250Ch)	**REG250C**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ2_MASK[7:0]	7:0	Group 2 request mask.	
43h (250Dh)	**REG250D**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ2_MASK[15:8]	7:0	See description of '250Ch'.	
44h (2510h)	**REG2510**	**7:0**	**Default : 0xFF**	**Access : R/W**
	RQ2_HPMASK[7:0]	7:0	Group 2 high priority mask.	
44h (2511h)	**REG2511**	**7:0**	**Default : 0xFF**	**Access : R/W**
	RQ2_HPMASK[15:8]	7:0	See description of '2510h'.	
45h (2514h)	**REG2514**	**7:0**	**Default : 0x10**	**Access : R/W**
	RQ21_PRIORITY[3:0]	7:4	Group2 2nd priority id.	
	RQ20_PRIORITY[3:0]	3:0	Group2 1st priority id.	
45h (2515h)	**REG2515**	**7:0**	**Default : 0x32**	**Access : R/W**
	RQ23_PRIORITY[3:0]	7:4	Group2 4th priority id.	
	RQ22_PRIORITY[3:0]	3:0	Group2 3rd priority id.	
46h (2518h)	**REG2518**	**7:0**	**Default : 0x54**	**Access : R/W**
	RQ25_PRIORITY[3:0]	7:4	Group2 6th priority id.	
	RQ24_PRIORITY[3:0]	3:0	Group2 5th priority id.	
46h (2519h)	**REG2519**	**7:0**	**Default : 0x76**	**Access : R/W**
	RQ27_PRIORITY[3:0]	7:4	Group2 8th priority id.	
	RQ26_PRIORITY[3:0]	3:0	Group2 7th priority id.	
47h (251Ch)	**REG251C**	**7:0**	**Default : 0x98**	**Access : R/W**
	RQ29_PRIORITY[3:0]	7:4	Group2 10th priority id.	
	RQ28_PRIORITY[3:0]	3:0	Group2 9th priority id.	
47h (251Dh)	**REG251D**	**7:0**	**Default : 0xBA**	**Access : R/W**
	RQ2B_PRIORITY[3:0]	7:4	Group2 12th priority id.	
	RQ2A_PRIORITY[3:0]	3:0	Group2 11th priority id.	
48h (2520h)	**REG2520**	**7:0**	**Default : 0xDC**	**Access : R/W**
	RQ2D_PRIORITY[3:0]	7:4	Group2 14th priority id.	
	RQ2C_PRIORITY[3:0]	3:0	Group2 13th priority id.	
48h	**REG2521**	**7:0**	**Default : 0xFE**	**Access : R/W**

MIU_DIG Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
(2521h)	RQ2F_PRIORITY[3:0]	7:4	Group2 16th priority id.	
	RQ2E_PRIORITY[3:0]	3:0	Group2 15th priority id.	
49h (2525h)	**REG2525**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ2_GROUP_DEADLINE[7:0]	7:0	Group 2 deadline timer number.	
4Ah (2528h)	**REG2528**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ2_CNT0_ID1[3:0]	7:4	Group 2 flow control 0 id1.	
	RQ2_CNT0_ID0[3:0]	3:0	Group 2 flow control 0 id0.	
4Ah (2529h)	**REG2529**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ2_CNT0_PERIOD[7:0]	7:0	Group 2 flow control 0 period number.	
4Bh (252Ch)	**REG252C**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ2_CNT1_ID1[3:0]	7:4	Group 2 flow control 1 id1.	
	RQ2_CNT1_ID0[3:0]	3:0	Group 2 flow control 1 id0.	
4Bh (252Dh)	**REG252D**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ2_CNT1_PERIOD[7:0]	7:0	Group 2 flow control 1 period number.	
4Ch (2530h)	**REG2530**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ2_CNT2_ID1[3:0]	7:4	Group 2 flow control 2 id1.	
	RQ2_CNT2_ID0[3:0]	3:0	Group 2 flow control 2 id0.	
4Ch (2531h)	**REG2531**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ2_CNT2_PERIOD[7:0]	7:0	Group 2 flow control 2 period number.	
4Dh (2534h)	**REG2534**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ2_CNT3_ID1[3:0]	7:4	Group 2 flow control 3 id1.	
	RQ2_CNT3_ID0[3:0]	3:0	Group 2 flow control 3 id0.	
4Dh (2535h)	**REG2535**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ2_CNT3_PERIOD[7:0]	7:0	Group 2 flow control 3 period number.	
4Eh (2538h)	**REG2538**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ2_LIMIT_MASK[7:0]	7:0	Group 2 client limit mask.	
4Eh (2539h)	**REG2539**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ2_LIMIT_MASK[15:8]	7:0	See description of '2538h'.	
4Fh (253Ch)	**REG253C**	**7:0**	**Default : 0x00**	**Access : RO**
	R_RQ2_LAST_DONE_Z[7:0]	7:0	Group 2 last done flag.	
4Fh (253Dh)	**REG253D**	**7:0**	**Default : 0x00**	**Access : RO**
	R_RQ2_LAST_DONE_Z[15:8]	7:0	See description of '253Ch'.	
50h	**REG2540**	**7:0**	**Default : 0x00**	**Access : R/W**

MIU_DIG Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
(2540h)	-	7	Reserved.	
	RQ3_CEASELESS_EN	6	Group 3 ceaseless enable.	
	RQ3_GROUP_DEADLINE_EN	5	Group 3 deadline enable.	
	RQ3_TIMEOUT_EN	4	Group 3 timeout enable.	
	RQ3_GROUP_LIMIT_EN	3	Group 3 group limit enable.	
	RQ3_MEMBER_LIMIT_EN	2	Group 3 member limit enable.	
	RQ3_SET_PRIORITY	1	Group 3 set priority pulse.	
	RQ3_ROUND_ROBIN	0	Group 3 round robin enable.	
50h (2541h)	**REG2541**	**7:0**	**Default : 0x80**	**Access : R/W**
	RQ3_ARBITER_SKIP_ON	7	Group 3 skip empty ready on.	
	RQ3_GROUP_CUT_IN_EN	6	Group 3 group cut in enable.	
	RQ3_MEMBER_CUT_IN_EN	5	Group 3 pre-arbiter cut in enable.	
	RQ3_LAST_DONE_Z_OFF	4	Group 3 last_done_z off.	
	RQ3_CNT3_CTRL_EN	3	Group 3 flow control 3 enable.	
	RQ3_CNT2_CTRL_EN	2	Group 3 flow control 2 enable.	
	RQ3_CNT1_CTRL_EN	1	Group 3 flow control 1 enable.	
	RQ3_CNT0_CTRL_EN	0	Group 3 flow control 0 enable.	
51h (2544h)	**REG2544**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ3_MEMBER_MAX[7:0]	7:0	Group 3 member max service number, unit 4.	
51h (2545h)	**REG2545**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ3_GROUP_MAX[7:0]	7:0	Group 3 group max service number, unit 4.	
52h (2548h)	**REG2548**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ3_TIMEOUT[7:0]	7:0	Group 3 time out number.	
52h (2549h)	**REG2549**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ3_TIMEOUT[15:8]	7:0	See description of '2548h'.	
53h (254Ch)	**REG254C**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ3_MASK[7:0]	7:0	Group 3 request mask.	
53h (254Dh)	**REG254D**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ3_MASK[15:8]	7:0	See description of '254Ch'.	
54h (2550h)	**REG2550**	**7:0**	**Default : 0xFF**	**Access : R/W**
	RQ3_HPMASK[7:0]	7:0	Group 3 high priority mask.	
54h (2551h)	**REG2551**	**7:0**	**Default : 0xFF**	**Access : R/W**
	RQ3_HPMASK[15:8]	7:0	See description of '2550h'.	

MIU_DIG Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
55h (2554h)	**REG2554**	**7:0**	**Default : 0x10**	**Access : R/W**
	RQ31_PRIORITY[3:0]	7:4	Group3 2nd priority id.	
	RQ30_PRIORITY[3:0]	3:0	Group3 1st priority id.	
55h (2555h)	**REG2555**	**7:0**	**Default : 0x32**	**Access : R/W**
	RQ33_PRIORITY[3:0]	7:4	Group3 4th priority id.	
	RQ32_PRIORITY[3:0]	3:0	Group3 3rd priority id.	
56h (2558h)	**REG2558**	**7:0**	**Default : 0x54**	**Access : R/W**
	RQ35_PRIORITY[3:0]	7:4	Group3 6th priority id.	
	RQ34_PRIORITY[3:0]	3:0	Group3 5th priority id.	
56h (2559h)	**REG2559**	**7:0**	**Default : 0x76**	**Access : R/W**
	RQ37_PRIORITY[3:0]	7:4	Group3 8th priority id.	
	RQ36_PRIORITY[3:0]	3:0	Group3 7th priority id.	
57h (255Ch)	**REG255C**	**7:0**	**Default : 0x98**	**Access : R/W**
	RQ39_PRIORITY[3:0]	7:4	Group3 10th priority id.	
	RQ38_PRIORITY[3:0]	3:0	Group3 9th priority id.	
57h (255Dh)	**REG255D**	**7:0**	**Default : 0xBA**	**Access : R/W**
	RQ3B_PRIORITY[3:0]	7:4	Group3 12th priority id.	
	RQ3A_PRIORITY[3:0]	3:0	Group3 11th priority id.	
58h (2560h)	**REG2560**	**7:0**	**Default : 0xDC**	**Access : R/W**
	RQ3D_PRIORITY[3:0]	7:4	Group3 14th priority id.	
	RQ3C_PRIORITY[3:0]	3:0	Group3 13th priority id.	
58h (2561h)	**REG2561**	**7:0**	**Default : 0xFE**	**Access : R/W**
	RQ3F_PRIORITY[3:0]	7:4	Group3 16th priority id.	
	RQ3E_PRIORITY[3:0]	3:0	Group3 15th priority id.	
59h (2565h)	**REG2565**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ3_GROUP_DEADLINE[7:0]	7:0	Group 3 deadline timer number.	
5Ah (2568h)	**REG2568**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ3_CNT0_ID1[3:0]	7:4	Group 3 flow control 0 id1.	
	RQ3_CNT0_ID0[3:0]	3:0	Group 3 flow control 0 id0.	
5Ah (2569h)	**REG2569**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ3_CNT0_PERIOD[7:0]	7:0	Group 3 flow control 0 period number.	
5Bh (256Ch)	**REG256C**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ3_CNT1_ID1[3:0]	7:4	Group 3 flow control 1 id1.	

MIU_DIG Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
	RQ3_CNT1_ID0[3:0]	3:0	Group 3 flow control 1 id0.	
5Bh (256Dh)	**REG256D**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ3_CNT1_PERIOD[7:0]	7:0	Group 3 flow control 1 period number.	
5Ch (2570h)	**REG2570**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ3_CNT2_ID1[3:0]	7:4	Group 3 flow control 2 id1.	
	RQ3_CNT2_ID0[3:0]	3:0	Group 3 flow control 2 id0.	
5Ch (2571h)	**REG2571**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ3_CNT2_PERIOD[7:0]	7:0	Group 3 flow control 2 period number.	
5Dh (2574h)	**REG2574**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ3_CNT3_ID1[3:0]	7:4	Group 3 flow control 3 id1.	
	RQ3_CNT3_ID0[3:0]	3:0	Group 3 flow control 3 id0.	
5Dh (2575h)	**REG2575**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ3_CNT3_PERIOD[7:0]	7:0	Group 3 flow control 3 period number.	
5Eh (2578h)	**REG2578**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ3_LIMIT_MASK[7:0]	7:0	Group 3 client limit mask.	
5Eh (2579h)	**REG2579**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ3_LIMIT_MASK[15:8]	7:0	See description of '2578h'.	
5Fh (257Ch)	**REG257C**	**7:0**	**Default : 0x00**	**Access : RO**
	R_RQ3_LAST_DONE_Z[7:0]	7:0	Group 3 last done flag.	
5Fh (257Dh)	**REG257D**	**7:0**	**Default : 0x00**	**Access : RO**
	R_RQ3_LAST_DONE_Z[15:8]	7:0	See description of '257Ch'.	
60h (2580h)	**REG2580**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT3_INV	7	Protection 3 function invert.	
	PROTECT2_INV	6	Protection 2 function invert.	
	PROTECT1_INV	5	Protection 1 function invert.	
	PROTECT0_INV	4	Protection 0 function invert.	
	PROTECT3_EN	3	Protection 3 enable.	
	PROTECT2_EN	2	Protection 2 enable.	
	PROTECT1_EN	1	Protection 1 enable.	
	PROTECT0_EN	0	Protection 0 enable.	
60h (2581h)	**REG2581**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

MIU_DIG Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
	DRAM_SIZE[3:0]	3:0	0: For test, 1:2MB, 2:4MB, 3:8MB, 4:16MB, 5:32MB, 6:64MB, 7:128MB, 8:256MB.	
61h (2584h)	**REG2584**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PROTECT0_ID0[5:0]	5:0	Protection client ID.	
61h (2585h)	**REG2585**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PROTECT0_ID1[5:0]	5:0	Protection client ID.	
62h (2588h)	**REG2588**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PROTECT0_ID2[5:0]	5:0	Protection client ID.	
62h (2589h)	**REG2589**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PROTECT0_ID3[5:0]	5:0	Protection client ID.	
63h (258Ch)	**REG258C**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT0_START[7:0]	7:0	Protect start address unit 4kb.	
63h (258Dh)	**REG258D**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT0_START[15:8]	7:0	See description of '258Ch'.	
64h (2590h)	**REG2590**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT0_END[7:0]	7:0	Protect end address unit 4kb.	
64h (2591h)	**REG2591**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT0_END[15:8]	7:0	See description of '2590h'.	
65h (2594h)	**REG2594**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PROTECT1_ID0[5:0]	5:0	Protection client ID.	
65h (2595h)	**REG2595**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PROTECT1_ID1[5:0]	5:0	Protection client ID.	
66h (2598h)	**REG2598**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT1_START[7:0]	7:0	Protect start address unit 4kb.	
66h (2599h)	**REG2599**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT1_START[15:8]	7:0	See description of '2598h'.	
67h	**REG259C**	**7:0**	**Default : 0x00**	**Access : R/W**

MIU_DIG Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
(259Ch)	PROTECT1_END[7:0]	7:0	Protect end address unit 4kb.	
67h (259Dh)	**REG259D**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT1_END[15:8]	7:0	See description of '259Ch'.	
68h (25A0h)	**REG25A0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PROTECT2_ID0[5:0]	5:0	Protection client ID.	
68h (25A1h)	**REG25A1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PROTECT2_ID1[5:0]	5:0	Protection client ID.	
69h (25A4h)	**REG25A4**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT2_START[7:0]	7:0	Protect start address unit 4kb.	
69h (25A5h)	**REG25A5**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT2_START[15:8]	7:0	See description of '25A4h'.	
6Ah (25A8h)	**REG25A8**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT2_END[7:0]	7:0	Protect end address unit 4kb.	
6Ah (25A9h)	**REG25A9**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT2_END[15:8]	7:0	See description of '25A8h'.	
6Bh (25ACh)	**REG25AC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PROTECT3_ID0[5:0]	5:0	Protection client ID.	
6Bh (25ADh)	**REG25AD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PROTECT3_ID1[5:0]	5:0	Protection client ID.	
6Ch (25B0h)	**REG25B0**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT3_START[7:0]	7:0	Protect start address unit 4kb.	
6Ch (25B1h)	**REG25B1**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT3_START[15:8]	7:0	See description of '25B0h'.	
6Dh (25B4h)	**REG25B4**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT3_END[7:0]	7:0	Protect end address unit 4kb.	
6Dh (25B5h)	**REG25B5**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT3_END[15:8]	7:0	See description of '25B4h'.	
6Eh (25B8h)	**REG25B8**	**7:0**	**Default : 0xE4**	**Access : R/W**
	GROUP_PRIORITY3_ID[1:0]	7:6	4th priority group id.	

MIU_DIG Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
	GROUP_PRIORITY2_ID[1:0]	5:4	3rd priority group id.	
	GROUP_PRIORITY1_ID[1:0]	3:2	2nd priority group id.	
	GROUP_PRIORITY0_ID[1:0]	1:0	1st priority group id.	
6Eh (25B9h)	**REG25B9**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	R_MIU_SYNCO_BIST_FAIL[1:0]	7:6		
	R_MIU_SYNCI_BIST_FAIL[1:0]	5:4		
	RESERVED_6E[2:0]	3:1		
	SET_GROUP_PRIORITY	0	Set group fix priority.	
6Fh (25BCh)	**REG25BC**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	R_HIT_PROTECT_NO[2:0]	7:5		
	R_HIT_PROTECT_FLAG	4		
	-	3:2	Reserved.	
	PROTECT_IRQ_MASK	1	1: Turn on the log of protection function.	
	PROTECT_LOG_CLR	0	1: Turn on the log of protection function.	
6Fh (25BDh)	**REG25BD**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	R_HIT_PROTECT_ID[5:0]	5:0		
70h (25C0h)	**REG25C0**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADDR_TOGGLE_MODE	7	For internal test only.	
	FORCE_IN	6	Force read data.	
	FORCE_OUT	5	Force write data.	
	TEST_LOOP	4	Test loop mode.	
	INV_DATA	3	Inver data for test.	
	TEST_MODE[1:0]	2:1	Test mode.	
	TEST_EN	0	Test enable.	
70h (25C1h)	**REG25C1**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	R_TEST_FINISH	7	Test finish report.	
	R_TEST_FAIL	6	Test fail report.	
	R_TEST_FLAG	5	Test fail flag.	
	TEST_BYTE[2:0]	4:2	Test data byte select.	
	WRITE_ONLY	1	Only write command is accepted.	
	READ_ONLY	0	Only read command is accepted.	
71h	**REG25C4**	**7:0**	**Default : 0x00**	**Access : R/W**

MIU_DIG Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
(25C4h)	TEST_BASE[7:0]	7:0	Test base address.	
71h (25C5h)	**REG25C5**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_BASE[15:8]	7:0	See description of '25C4h'.	
72h (25C8h)	**REG25C8**	**7:0**	**Default : 0x08**	**Access : R/W**
	TEST_LENGTH_L[7:0]	7:0	Test length [15:0].	
72h (25C9h)	**REG25C9**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_LENGTH_L[15:8]	7:0	See description of '25C8h'.	
73h (25CCh)	**REG25CC**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_LENGTH_H[7:0]	7:0	Test length [27:16].	
73h (25CDh)	**REG25CD**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_MASK[3:0]	7:4	For internal test only.	
	TEST_LENGTH_H[11:8]	3:0	See description of '25CCh'.	
74h (25D0h)	**REG25D0**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_DATA[7:0]	7:0	Test data.	
74h (25D1h)	**REG25D1**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_DATA[15:8]	7:0	See description of '25D0h'.	
75h (25D4h)	**REG25D4**	**7:0**	**Default : 0x00**	**Access : RO**
	R_TEST_STATUS[7:0]	7:0	For internal test only.	
75h (25D5h)	**REG25D5**	**7:0**	**Default : 0x00**	**Access : RO**
	R_TEST_STATUS[15:8]	7:0	See description of '25D4h'.	
76h (25D8h)	**REG25D8**	**7:0**	**Default : 0x00**	**Access : RO**
	R_TEST_BYTE_FAIL[7:0]	7:0	For internal test only.	
76h (25D9h)	**REG25D9**	**7:0**	**Default : 0x00**	**Access : RO**
	R_TEST_BYTE_FAIL[15:8]	7:0	See description of '25D8h'.	
77h (25DCh)	**REG25DC**	**7:0**	**Default : 0x00**	**Access : RO**
	R_TEST_BIT_FAIL[7:0]	7:0	For internal test only.	
77h (25DDh)	**REG25DD**	**7:0**	**Default : 0x00**	**Access : RO**
	R_TEST_BIT_FAIL[15:8]	7:0	See description of '25DCh'.	
78h (25E0h)	**REG25E0**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_SEL0[7:0]	7:0	For internal test only.	
78h (25E1h)	**REG25E1**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_SEL0[15:8]	7:0	See description of '25E0h'.	
79h	**REG25E4**	**7:0**	**Default : 0x00**	**Access : R/W**

MIU_DIG Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
(25E4h)	MIU_SEL1[7:0]	7:0	For internal test only.	
79h (25E5h)	**REG25E5**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_SEL1[15:8]	7:0	See description of '25E4h'.	
7Ah (25E8h)	**REG25E8**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_SEL2[7:0]	7:0	For internal test only.	
7Ah (25E9h)	**REG25E9**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_SEL2[15:8]	7:0	See description of '25E8h'.	
7Bh (25ECh)	**REG25EC**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_SEL3[7:0]	7:0	For internal test only.	
7Bh (25EDh)	**REG25ED**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_SEL3[15:8]	7:0	See description of '25ECh'.	
7Ch (25F0h)	**REG25F0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	RDCRC_DATA_SEL[2:0]	6:4	For internal test only.	
	RDPTG_EN	3	For internal test only.	
	WDCRC_STOP	2	For internal test only.	
	WDCRC_START	1	For internal test only.	
	WDCRC_RST	0	For internal test only.	
7Ch (25F1h)	**REG25F1**	**7:0**	**Default : 0x00**	**Access : R/W**
	CMD_LFSR_EN	7	For internal test only.	
	-	6:0	Reserved.	
7Dh (25F4h)	**REG25F4**	**7:0**	**Default : 0x00**	**Access : R/W**
	PTN_MODE[7:0]	7:0	For internal test only.	
7Dh (25F5h)	**REG25F5**	**7:0**	**Default : 0x00**	**Access : R/W**
	PTN_MODE[15:8]	7:0	See description of '25F4h'.	
7Eh (25F8h)	**REG25F8**	**7:0**	**Default : 0x00**	**Access : R/W**
	PTN_DATA[7:0]	7:0	For internal test only.	
7Eh (25F9h)	**REG25F9**	**7:0**	**Default : 0x00**	**Access : R/W**
	PTN_DATA[15:8]	7:0	See description of '25F8h'.	
7Fh (25FCh)	**REG25FC**	**7:0**	**Default : 0x00**	**Access : RO**
	R_READ_CRC[7:0]	7:0	For internal test only.	
7Fh (25FDh)	**REG25FD**	**7:0**	**Default : 0x00**	**Access : RO**
	R_READ_CRC[15:8]	7:0	See description of '25FCh'.	

MPLL Register (Bank = 13)

MPLL Register (Bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2600h)	**REG2600**	**7:0**	**Default : 0xE7**	**Access : R/W**
	CPUPLL_ICP_ICTRL[1:0]	7:6	CPUPLL Charge-Pump current control. 2'h00: Icp x 4. 2'h01: Icp x 3. 2'h10: Icp x 2. 2'h11: Icp x1.	
	CPUPLL_IBIAS_ICTRL[1:0]	5:4	CPUPLL Ibias output current control. 2'h00: Iout x 1. 2'h01: Iout x 0.75. 2'h10: Iout x 0.5. 2'h11: Iout x0.25.	
	CPUPLL_ENFRUN	3	Enable CPUPLL VCO free eun.	
	CPUPLL_CLK33_IN_DIV2_EN	2	CPUPLL 3.3V input reference clock div2 or not.	
	CPUPLL_CLK_ADC432M_PD	1	Disable "CPUPLL_CLK_ADC432M" output.	
	CPUPLL_CLK_ADC216M_PD	0	Disable "CPUPLL_CLK_ADC216M" output.	
00h (2601h)	**REG2601**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:5	Reserved.	
	CPUPLL_LOOP_DIV_FIRST[1:0]	4:3	CPUPLL first loop-divider control. 2'b00: /1. 2'b01: /2 <-- default. 2'b10: /4 2'b11: /8	
	CPUPLL_INPUT_DIV_FIRST[1:0]	2:1	CPUPLL input-divider control:. 2'b00: /1 <-- default. 2'b01: /2 2'b10: /4 2'b11: /8	
	CPUPLL_IN_SELECT	0	CPUPLL input clock selection, while TEST[5]=1'b1,. 1'b0 1.2V clock input. 1'b1 3.3V clock input after internal level shift to 1.0V.	
01h	**REG2604**	**7:0**	**Default : 0x2E**	**Access : R/W**

MPLL Register (Bank = 13)

Index (Absolute)	Mnemonic	Bit	Description	
(2604h)	CPUPLL_LOOP_DIV_SECOND[7:0]	7:0	CPUPLL second loop-divider control. 8'h00: /1. 8'h01: /1. 8'h02: /2. 8'h03: /3. 8'h7F: /127. Others are not acceptable.	
01h (2605h)	**REG2605**	**7:0**	**Default : 0x05**	**Access : R/W**
	-	7:4	Reserved.	
	CPUPLL_RES_SEL	3	CPUPLL Loop Filter Resistance Selection. 1'b0: res=7k Ohm. 1'b1: res=14k Ohm. *for stability consideration. In DSP mode, please set 1'b1.	
	CPUPLL_PD	2	Power down CPUPLL.	
	CPUPLL_OUTPUT_DIV_FIRST[1:0]	1:0	CPUPLL output-divider control. 2'b00: /1 <-- default. 2'b01: /2. 2'b10: /4. 2'b11: /8.	
02h (2608h)	**REG2608**	**7:0**	**Default : 0x00**	**Access : R/W**
	CPUPLL_TEST[7:0]	7:0	CPUPLL test control for test mode.	
02h (2609h)	**REG2609**	**7:0**	**Default : 0x00**	**Access : R/W**
	CPUPLL_TEST[15:8]	7:0	See description of '2608h'.	
03h (260Ch)	**REG260C**	**7:0**	**Default : 0x3E**	**Access : R/W**
	MPLL_IBIAS_ICTRL[0]	7	MPLL Ibias output current control. 2'h00: Iout x 1. 2'h01: Iout x 0.75. 2'h10: Iout x 0.5. 2'h11: Iout x0.25.	
	MPLL_ENFRUN	6	Enable MPLL VCO free eun.	
	MPLL_CLK33_IN_DIV2_EN	5	MPLL 3.3V input reference clock div2 or not.	
	MPLL_CLK_ADC432M_PD	4	Disable "MPLL_CLK_ADC432M" output.	
	MPLL_CLK_ADC216M_PD	3	Disable "MPLL_CLK_ADC216M" output.	
	FRSEL	2	Select feedback resistor. 1'b0: external resistor. 1'b1: internal resistor.	

MPLL Register (Bank = 13)

Index (Absolute)	Mnemonic	Bit	Description	
	CPUPLL_VCO_DIV2_DISABLE	1	DIV2 before CPUPLL output divider.	
	CPUPLL_TEST_EN	0	Enable CPUPLL test clock output function.	
03h (260Dh)	**REG260D**	**7:0**	**Default : 0xC7**	**Access : R/W**
	MPLL_LOOP_DIV_FIRST[1:0]	7:6	MPLL first loop-divider control. 2'b00: /1. 2'b01: /2. 2'b10: /4 <-- default. 2'b11: /8.	
	MPLL_INPUT_DIV_FIRST[1:0]	5:4	MPLL input-divider control: 2'b00: /1 <-- default. 2'b01: /2. 2'b10: /4. 2'b11: /8.	
	MPLL_IN_SELECT	3	MPLL input clock selection, while TEST[5]=1'b1, 1'b0 1.2V clock input. 1'b1 3.3V clock input after internal level shift to 1.0V.	
	MPLL_ICP_ICTRL[1:0]	2:1	MPLL Charge-Pump current control. 2'h00: Icp x 4. 2'h01: Icp x 3. 2'h10: Icp x 2. 2'h11: Icp x1.	
	MPLL_IBIAS_ICTRL[1]	0	See description of '260Ch'.	
04h (2610h)	**REG2610**	**7:0**	**Default : 0x09**	**Access : R/W**
	MPLL_LOOP_DIV_SECOND[7:0]	7:0	MPLL second loop-divider control:. 8'h00: /1. 8'h01: /1. 8'h02: /2. 8'h03: /3. 8'h7F: /127. Others are not acceptable.	
04h (2611h)	**REG2611**	**7:0**	**Default : 0x05**	**Access : R/W**
	-	7:4	Reserved.	
	MPLL_RES_SEL	3	MPLL Loop Filter Resistance Selection. 1'b0: res=7k Ohm. 1'b1: res=14k Ohm. *for stability consideration. In DSP mode, please set 1'b1.	

MPLL Register (Bank = 13)

Index (Absolute)	Mnemonic	Bit	Description	
	MPLL_PD	2	Power down MPLL.	
	MPLL_OUTPUT_DIV_FIRST[1:0]	1:0	MPLL output-divider control. 2'b00: /1. 2'b01: /2 <-- default. 2'b10: /4. 2'b11: /8.	
05h (2614h)	**REG2614**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPLL_TEST[7:0]	7:0	MPLL test control for test mode.	
05h (2615h)	**REG2615**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPLL_TEST[15:8]	7:0	See description of '2614h'.	
06h (2618h)	**REG2618**	**7:0**	**Default : 0x0C**	**Access : RO, R/W**
	MPLL_LOCK	7	MPLL Lock signal. (Enable by MPLL_TEST[6]=1).	
	MPLL_HIGH_FLAG	6	MPLL High signal. (Enable by MPLL_TEST[13]=1).	
	CPUPLL_LOCK	5	CPUPLL Lock signal. (Enable by CPUPLL_TEST[6]=1).	
	CPUPLL_HIGH_FLAG	4	CPUPLL High signal. (Enable by CPUPLL_TEST[13]=1).	
	-	3:2	Reserved.	
	MPLL_VCO_DIV2_DISABLE	1	DIV2 before MPLL output divider.	
	MPLL_TEST_EN	0	Enable MPLL test clock output function.	
06h (2619h)	**REG2619**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MPLL_PD_CLK_USB	7	Disable "MPLL_CLK_USB" output.	
	MPLL_PD_DVB_DIV3	6	Disable "MPLL_DVB_DIV3" output.	
	MPLL_PD_DVB_DIV2	5	Disable "MPLL_DVB_DIV2" output.	
	MPLL_PD_CLK_DP432M	4	Disable "MPLL_CLK_DP432M" output.	
	MPLL_PD_CLK_DIV	3	Disable "MPLL_CLK_DIV" output.	
	MPLL_PD_CLK_AUDIO_USB	2	Disable the source of "MPLL_CLK_AUDIO" & "MPLL_CLK_USB".	
	MPLL_PD_CLK_AUDIO	1	Disable "MPLL_CLK_AUDIO" output.	
	CPUPLL_PD_CLK_OUT	0	Disable "CPUPLL_CLK_OUT" output.	
07h~08h (261Ch~2621h)		**7:0**	**Default : -**	**Access : -**
		7:0	Reserved	

SDIO0 Register (Bank = 14)

SDIO0 Register (Bank = 14)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2800h)	**REG2800**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_INT	7	SDIO interrupt event.	
	-	6:3	Reserved.	
	SD_DATA_END	2	SD/MMC data transaction complete event.	
	SD_CMD_END	1	SD/MMC card command and response transaction complete event.	
	MMA_DATA_END	0	MMA data transaction complete event.	
00h (2801h)	**REG2801**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MMA_LAST_DONE_INT	6	MMA Last Done interrupt event.	
	POWER_SAVE_INT	5	Power saving mode complete interrupt event.	
	-	4	Reserved.	
	CARD_DMA_END	3	Card interface DMA end interrupt.	
	-	2:1	Reserved.	
	MIU_WR_RANGE_ERR	0	MIU write protection out of range event.	
01h (2804h)	**REG2804**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_INT_EN	7	SDIO_INT interrupt enable.	
	-	6:3	Reserved.	
	SD_DATA_END_EN	2	SD_DATA_END interrupt enable.	
	SD_CMD_END_EN	1	SD_CMD_END interrupt enable.	
	MMA_DATA_EN	0	MMA_DATA_END interrupt enable.	
01h (2805h)	**REG2805**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MMA_LAST_DONE_INT_EN	6	MMA Last Done interrupt enable.	
	-	5:4	Reserved.	
	CARD_DMA_END_EN	3	Card interface DMA end interrupt enable.	
	-	2:1	Reserved.	
	MIU_WR_RANGE_ERR_EN	0	MIU write protection range interrupt enable.	
02h (2808h)	**REG2808**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:6	Reserved.	
	FIFO_CLKRDY	5	Data fifo clock ready.	
	MIU_REQUEST_RST	4	Mask MIU interface request, high active.	

SDIO0 Register (Bank = 14)

Index (Absolute)	Mnemonic	Bit	Description	
	DATA_SCRAMBLE_EN	3	MIU data scramble function enable.	
	JOB_RW_DIR	2	Specify whether this DMA cycle is Read or Write. 0: Read from card (data write to DRAM). 1: Write to card (data read from DRAM).	
	MMA_W_PRIORITY	1	MIU write request priority. 0: Low priority. 1: High priority.	
	MMA_R_PRIORITY	0	MIU read request priority. 0: Low priority. 1: High priority.	
02h (2809h)	**REG2809**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MIU_BUS_CTRL	2	MIU bus burst length selection enable. 0: Disable, length= 512-byte/MIU bus width. 1: Enable, length= reg_miu_bus_type.	
	MIU_BUS_TYPE[1:0]	1:0	MIU bus burst length. 0: 8 burst. 1: 16 burst. 2: 32 burst.	
03h (280Ch)	**REG280C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_26_16[7:0]	7:0	DMA Address[26:16].	
03h (280Dh)	**REG280D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_SELECT	7	MIU0/MIU1 selection, default 0 = MIU0.	
	-	6:3	Reserved.	
	DMA_ADDR_26_16[10:8]	2:0	See description of '280Ch'.	
04h (2810h)	**REG2810**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_15_0[7:0]	7:0	DMA Address[15:0].	
04h (2811h)	**REG2811**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_15_0[15:8]	7:0	See description of '2810h'.	
05h (2814h)	**REG2814**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_STS_CHG	7	SDIO card plug-in or remove status change.	
	-	6:0	Reserved.	
05h (2815h)	**REG2815**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SDIO2_STS_CHG	0	SDIO2 card plug-in or remove status change.	

SDIO0 Register (Bank = 14)

Index (Absolute)	Mnemonic	Bit	Description	
06h (2819h)	**REG2819**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SDIO2_CARD_DET_SRC	3	SDIO2 card detect pin select. 0: SDIO_CDZ. 1: SDIO_DAT3.	
	SDIO2_STS_EN	2	SDIO2 card status change interrupt enable.	
	SDIO_CARD_DET_SRC	1	SDIO card detect pin select. 0: SDIO_CDZ. 1: SDIO_DAT3.	
	SDIO_STS_EN	0	SDIO card status change interrupt enable.	
07h (281Ch)	**REG281C**	**7:0**	**Default : 0x00**	**Access : RO**
	SDIO_DET_N	7	SDIO card detection status.	
	-	6:0	Reserved.	
07h (281Dh)	**REG281D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	SDIO2_DET_N	1	SDIO2 card detection status.	
	-	0	Reserved.	
0Ah (2828h)	**REG2828**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SD_EN	1	SD/MMC card interface enable.	
	MMA_ENABLE	0	MIU DMA enable, job finish auto clear. Note: Before setting this bit, make sure JOB_BL_CNT, MIU_DMA1, JOB_RW_DIR and MIU_DMA0 have been updated.	
0Bh (282Ch)	**REG282C**	**7:0**	**Default : 0x00**	**Access : R/W**
	JOB_BL_CNT[7:0]	7:0	Total block counts for this job. (Card unit: sector. SDIO & Nand unit: reg_sdio_blk_size9_0).	
0Bh (282Dh)	**REG282D**	**7:0**	**Default : 0x00**	**Access : R/W**
	TR_JOB_CNT_MANUAL	7	Manual mode for content of reg_tr_bk_cnt. 0: Hardware auto mode. 1: Manual mode.	
	TR_JOB_CNT_SRC	6	Select remainder job count of card or MIU. 0: Card remainder job count. 1: Miu remainder job count.	

SDIO0 Register (Bank = 14)

Index (Absolute)	Mnemonic	Bit	Description	
	-	5:4	Reserved.	
	JOB_BL_CNT[11:8]	3:0	See description of '282Ch'.	
0Ch (2830h)	**REG2830**	**7:0**	**Default : 0x00**	**Access : RO**
	TR_BK_CNT[7:0]	7:0	Real time number of remainder sectors to be transferred.	
0Ch (2831h)	**REG2831**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	TR_BK_CNT[11:8]	3:0	See description of '2830h'.	
0Dh (2834h)	**REG2834**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CIF_RSP_SIZE[6:0]	6:0	Expected response size (byte count) for SD/MMC card. Expected register read size (byte count) for MS/MSPro card. 01: 1 byte. 40: 64 bytes.	
0Dh (2835h)	**REG2835**	**7:0**	**Default : 0x00**	**Access : R/W**
	SD_DELAY_SEL_7_0[7:0]	7:0	SD delay cell selection 10 bits. [1:0]: select 4 delay cells on data bus [0], [4]. [3:2]: select 4 delay cells on data bus [1], [5]. [5:4]: select 4 delay cells on data bus [2], [6]. [7:6]: select 4 delay cells on data bus [3], [7].	
0Eh (2838h)	**REG2838**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CIF_CMD_SIZE[6:0]	6:0	Command transfer size (byte count) for SD/MMC and MS/MSPro card. 01: 1 byte. 40: 64 bytes.	
0Eh (2839h)	**REG2839**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SD_DELAY_EN	2	SD bus add delay cell for SSO issue,. Enable register.	
	SD_DELAY_SEL_9_8[1:0]	1:0	SD delay cell selection 10 bits. [9:8]: select 4 delay cells on command line.	
0Fh	**REG283C**	**7:0**	**Default : 0x00**	**Access : R/W**

SDIO0 Register (Bank = 14)

Index (Absolute)	Mnemonic	Bit	Description	
(283Ch)	CARD_WD_CNT[7:0]	7:0	Expected data word count transferred through CIF FIFO. 0x00 represents 256 words. (CMD6 for SD card, CMD8/14/19 for MMC card).	
10h (2840h)	**REG2840**	**7:0**	**Default : 0x00**	**Access : R/W**
	MMC_BUS_TEST	7	Test MMC bus type through CIF Data FIFO.	
	SD_DATSYNC	6	Synchronize data bus, for SD1.1 specification.	
	SD_DEST	5	SD/MMC data transfer destination. 0: Data FIFO. 1: CIF FIFO.	
	SD_CS_EN	4	Set to enable clock auto-stop feature, which will stop CLK between read blocks when Data FIFO is full. 0: Auto-stop is disabled. 1: Auto-stop is enabled.	
	SDDRL	3	Firmware writes 1 to drive SD interface, data bus and command line low.	
	SD_DAT_LINE1	2	10: Use DAT7-0 line.	
	SD_DAT_LINE0	1	00: Use DAT0 line. 01: Use DAT3-0 line.	
	SD_CLK_EN	0	SD MIF output clock enable.	
10h (2841h)	**REG2841**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_PORT_SEL	4	SDIO port selection, 0-SDIO port1, 1-SDIO port2.	
	SD_DMA_RD_CLK_STOP	3	SD read DMA stop clock when DMA end.	
	2SD_1CLK_SRC	2	Clock control of card port, when SDIO port active. 0: Clock off. 1: Clock on.	
	SDIO_SD_BUS_SW	1	SDIO interface and SD/MMC card interface select. Default is SD/MMC card interface active and SDIO interface idle. Set 1 to have SDIO interface go active, and SD/MMC card interface stay idle.	
	SDIO_RDWAIT	0	When reading block data while Data FIFO is busy, hardware will drive SD_DAT1 to low, to inform card controller that host is busy. Active high.	

SDIO0 Register (Bank = 14)

Index (Absolute)	Mnemonic	Bit	Description	
11h (2844h)	**REG2844**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SD_DTRX_DIR	4	SD/MMC data transfer direction. 0: Read from card. 1: Write to card.	
	SD_DTRX_EN	3	SD/MMC data transmit/receive enable (job finish auto clear).	
	SD_CMD_EN	2	SD/MMC transmit command enable (job finish auto clear).	
	SD_RSP_EN	1	SD/MMC receive command response enable.	
	SD_RSPR2_EN	0	SD/MMC receive command response for R2 type.	
11h (2845h)	**REG2845**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SDIO_DET_INT_SRC	3	SDIO interrupt source selection in sdio_int_mod=0 or 1. 0-edge trigger, 1-level trigger.	
	SDIO_DET_ON	2	SDIO interrupt detect function switch, active high.	
	SDIO_INT_MOD1	1	SDIO_INT_MOD= 10: Single block read/write interrupt detect. SDIO_INT_MOD= 11: Multi-block read/write interrupt detect.	
	SDIO_INT_MOD0	0	SDIO_INT_MOD= 00: Continuous interrupt detect. SDIO_INT_MOD= 01: CMD12 or IO Abort command interrupt detect.	
12h (2848h)	**REG2848**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	SD_CARD_BUSY	6	SD card busy status, 1-SD card busy.	
	SD_WR_PRO_N	5	SD card write protect.	
	SD_CMDRSP_CERR	4	Received command phase. Response CRC error event.	
	SD_CMD_NORSP	3	Transmitted command phase. Response timeout event (time out = 64 clocks), which means there is no response on CMD line.	

SDIO0 Register (Bank = 14)

Index (Absolute)	Mnemonic	Bit	Description	
	SD_DAT_STSNEG	2	Transmitted data phase. "CRC status = negative" from SD/MMC card, which means a transmission error has occurred, and host needs to resend data.	
	SD_DAT_STSERR	1	Transmitted data phase. "CRC status = error" from SD/MMC card, which means SD/MMC card has encountered a flash program error.	
	SD_DAT_CERR	0	Received data phase CRC error event.	
12h (2849h)	**REG2849**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SD_DAT3	3	SD DATA Line 3.	
	SD_DAT2	2	SD DATA Line 2.	
	SD_DAT1	1	SD DATA Line 1.	
	SD_DAT0	0	SD DATA Line 0.	
1Bh (286Ch)	**REG286C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_BLK_SIZE12_0[7:0]	7:0	SDIO block size[12:0] (1~2047 bytes). 13'h001: 1 byte. 13'h200: 512 bytes. 13'h400: 1024 bytes.	
1Bh (286Dh)	**REG286D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_BLK_MOD	7	SDIO block mode enable.	
	-	6:5	Reserved.	
	SDIO_BLK_SIZE12_0[12:8]	4:0	See description of '286Ch'.	
1Ch (2870h)	**REG2870**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR15_0[7:0]	7:0	SDIO memory address[15:0] (byte offset).	
1Ch (2871h)	**REG2871**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR15_0[15:8]	7:0	See description of '2870h'.	
1Dh (2874h)	**REG2874**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR28_16[7:0]	7:0	SDIO memory address[28:16] (byte offset).	
1Dh (2875h)	**REG2875**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SDIO_MEM_ADDR28_16[13:8]	5:0	See description of '2874h'.	
1Eh (2878h)	**REG2878**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	

SDIO0 Register (Bank = 14)

Index (Absolute)	Mnemonic	Bit	Description	
	SDIO_DAT3_0[3:0]	3:0	SDIO data lines 3-0.	
1Eh (2879h)	**REG2879**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SDIO2_DAT3_0[3:0]	3:0	SDIO2 data lines 3-0.	
2Dh (28B4h)	**REG28B4**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:5	Reserved.	
	SRAM_CGEN	4	SARM clock gating.	
	-	3:0	Reserved.	
2Eh (28B8h)	**REG28B8**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BYTE_VLD_7_0[7:0]	7:0	MIU bus width is 64-bit, SW can select byte offset position for DMA transmission. BYTE_VLD[7:0]: hFF, valid data start on bus [63:0]. BYTE_VLD[7:0]: hFE, valid data start on bus [63:8]. BYTE_VLD[7:0]: hFC, valid data start on bus [63:16]. BYTE_VLD[7:0]: hF8, valid data start on bus [63:24]. BYTE_VLD[7:0]: hF0, valid data start on bus [63:32]. BYTE_VLD[7:0]: hE0, valid data start on bus [63:40]. BYTE_VLD[7:0]: hC0, valid data start on bus [63:48]. BYTE_VLD[7:0]: h80, valid data start on bus [63:56].	
30h (28C0h)	**REG28C0**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	CF_PAD_SWAP	7	CF pad function swap.	
	SD_PAD_SWAP	6	SD pad function swap.	
	XD_BUS_PORT_SEL	5	XD pad function swap.	
	CMD_BISTFAIL	4	CMD FIFO 128-byte BIST Test Fail.	
	CIFD_BISTFAIL	3	CIF FIFO_D 512-byte BIST Test Fail.	
	CIFC_BISTFAIL	2	CIF FIFO_C 64-byte BIST Test Fail.	
	DBFB_BISTFAIL	1	Data FIFO_B 512-byte BIST Test Fail.	
	DBFA_BISTFAIL	0	Data FIFO_A 512-byte BIST Test Fail.	
30h (28C1h)	**REG28C1**	**7:0**	**Default : 0x58**	**Access : R/W**
	XD_NAND_COBUS	7	NAND and XD/SD interface shared bus, Active high.	
	PING_PONG_FIFO_CLK_EN	6	Ping pong fifo clock enable.	
	ENDIAN_SEL	5	Endian select. Low: Little endian. High: Big endian.	
	FCIE_SOFT_RST	4	FCIE module software reset, active low, uP program.	

SDIO0 Register (Bank = 14)

Index (Absolute)	Mnemonic	Bit	Description	
	SD_MS_COBUS	3	SD and MS interface shared bus, 4-bit mode bus. MS 4-bit data bus is shared with SD 4-bit bus, and MS_BS is shared with SD_CMD. Active high.	
	DEBUG_MOD[2:0]	2:0	DEBUG_MOD [2:0] definition. 1: SD. 5: MMA. 6: DFF.	
31h (28C4h)	**REG28C4**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_15_0[7:0]	7:0	Debug bus [15:0].	
31h (28C5h)	**REG28C5**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_15_0[15:8]	7:0	See description of '28C4h'.	
32h (28C9h)	**REG28C9**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_23_16[7:0]	7:0	Debug bus [23:16].	
34h (28D0h)	**REG28D0**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SD_POWER_RD_MASK[7:0]	7:0	Power save mode, read data mask bits, 0-mask, 1-valid.	
34h (28D1h)	**REG28D1**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SD_POWER_RD_MASK[15:8]	7:0	See description of '28D0h'.	
35h (28D4h)	**REG28D4**	**7:0**	**Default : 0x08**	**Access : RO, R/W**
	BAT_SAVE_EVENT	7	Power save mode status, Battery lost event occurred, clear by reg_sd_power_save_rst=0.	
	RST_SAVE_EVENT	6	Power save mode status, Reset event occurred, clear by reg_sd_power_save_rst=0.	
	RIU_SAVE_EVENT	5	Power save mode status, RIU emulation event occurred, clear by reg_sd_power_save_rst=0.	
	-	4	Reserved.	
	SD_POWER_SAVE_RST	3	Software reset Power Save HW, default is '1', set '0' to reset HW.	
	POWER_SAVE_MODE_INT_EN	2	Power Save interrupt enable, high active.	
	SD_POWER_SAVE_RIU	1	SW set register to emulate power lost event, high active.	
	POWER_SAVE_MODE	0	Power Save HW enable, high active.	
38h	**REG28E0**	**7:0**	**Default : 0x00**	**Access : R/W**

SDIO0 Register (Bank = 14)

Index (Absolute)	Mnemonic	Bit	Description	
(28E0h)	RANGE_MIN_BYTE_ADDRESS_26_16[7:0]	7:0	MIU write range protection, minimum address pointer 27 bits (MIU width is 32 bits), address[26:16].	
38h (28E1h)	**REG28E1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	FORCE_MIU_WR_RANGE_ERR	4	Force MIU write protection out of range event.	
	MIU_WR_RANGE_ENABLE	3	MIU write protection function enable.	
	RANGE_MIN_BYTE_ADDRESS_26_16[10:8]	2:0	See description of '28E0h'.	
39h (28E4h)	**REG28E4**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_15_0[7:0]	7:0	MIU write range protection, minimum address pointer 26 bits (MIU width is 32 bits), address[15:0].	
39h (28E5h)	**REG28E5**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_15_0[15:8]	7:0	See description of '28E4h'.	
3Ah (28E8h)	**REG28E8**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_26_16[7:0]	7:0	MIU write range protection, maximum address pointer 26 bits (MIU width is 32 bits), address[26:16].	
3Ah (28E9h)	**REG28E9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	RANGE_MAX_BYTE_ADDRESS_26_16[10:8]	2:0	See description of '28E8h'.	
3Bh (28ECh)	**REG28EC**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_15_0[7:0]	7:0	MIU write range protection, maximum address pointer 26 bits (MIU width is 32 bits), address[15:0].	
3Bh (28EDh)	**REG28ED**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_15_0[15:8]	7:0	See description of '28ECh'.	
3Ch (28F0h)	**REG28F0**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_26_16[7:0]	7:0	MIU write range protection error address. MIU_WRRANGE_ERR_ADDR_26_16.	
3Ch (28F1h)	**REG28F1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	MIU_WRRANGE_ERR_ADDR_26_16[10:8]	2:0	See description of '28F0h'.	
3Dh	**REG28F4**	**7:0**	**Default : 0x00**	**Access : RO**

SDIO0 Register (Bank = 14)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(28F4h)	MIU_WRRANGE_ERR_ADDR_15_0[7:0]	7:0	MIU write range protection error address. MIU_WRRANGE_ERR_ADDR_15_0.	
3Dh (28F5h)	**REG28F5**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_15_0[15:8]	7:0	See description of '28F4h'.	

EFUSE Register (Bank = 18)

EFUSE Register (Bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (3000h)	**REG3000**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_MUX_BIT[7:0]	7:0	Efuse bit [127:0] ; mux with overwrite.	
00h (3001h)	**REG3001**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_MUX_BIT[15:8]	7:0	See description of '3000h'.	
01h (3004h)	**REG3004**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_MUX_BIT[23:16]	7:0	See description of '3000h'.	
01h (3005h)	**REG3005**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_MUX_BIT[31:24]	7:0	See description of '3000h'.	
02h (3008h)	**REG3008**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_MUX_BIT[39:32]	7:0	See description of '3000h'.	
02h (3009h)	**REG3009**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_MUX_BIT[47:40]	7:0	See description of '3000h'.	
03h (300Ch)	**REG300C**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_MUX_BIT[55:48]	7:0	See description of '3000h'.	
03h (300Dh)	**REG300D**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_MUX_BIT[63:56]	7:0	See description of '3000h'.	
04h (3010h)	**REG3010**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_MUX_BIT[71:64]	7:0	See description of '3000h'.	
04h (3011h)	**REG3011**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_MUX_BIT[79:72]	7:0	See description of '3000h'.	
05h (3014h)	**REG3014**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_MUX_BIT[87:80]	7:0	See description of '3000h'.	
05h (3015h)	**REG3015**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_MUX_BIT[95:88]	7:0	See description of '3000h'.	
06h (3018h)	**REG3018**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_MUX_BIT[103:96]	7:0	See description of '3000h'.	
06h (3019h)	**REG3019**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_MUX_BIT[111:104]	7:0	See description of '3000h'.	
07h (301Ch)	**REG301C**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_MUX_BIT[119:112]	7:0	See description of '3000h'.	
07h	**REG301D**	**7:0**	**Default : 0x00**	**Access : RO**

EFUSE Register (Bank = 18)

Index (Absolute)	Mnemonic	Bit	Description	
(301Dh)	EFUSE_MUX_BIT[127:120]	7:0	See description of '3000h'.	
08h (3020h)	**REG3020**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_SEL[7:0]	7:0	Efuse overwrite select [127:0].	
08h (3021h)	**REG3021**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_SEL[15:8]	7:0	See description of '3020h'.	
09h (3024h)	**REG3024**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_SEL[23:16]	7:0	See description of '3020h'.	
09h (3025h)	**REG3025**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_SEL[31:24]	7:0	See description of '3020h'.	
0Ah (3028h)	**REG3028**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_SEL[39:32]	7:0	See description of '3020h'.	
0Ah (3029h)	**REG3029**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_SEL[47:40]	7:0	See description of '3020h'.	
0Bh (302Ch)	**REG302C**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_SEL[55:48]	7:0	See description of '3020h'.	
0Bh (302Dh)	**REG302D**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_SEL[63:56]	7:0	See description of '3020h'.	
0Ch (3030h)	**REG3030**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_SEL[71:64]	7:0	See description of '3020h'.	
0Ch (3031h)	**REG3031**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_SEL[79:72]	7:0	See description of '3020h'.	
0Dh (3034h)	**REG3034**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_SEL[87:80]	7:0	See description of '3020h'.	
0Dh (3035h)	**REG3035**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_SEL[95:88]	7:0	See description of '3020h'.	
0Eh (3038h)	**REG3038**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_SEL[103:96]	7:0	See description of '3020h'.	
0Eh (3039h)	**REG3039**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_SEL[111:104]	7:0	See description of '3020h'.	
0Fh (303Ch)	**REG303C**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_SEL[119:112]	7:0	See description of '3020h'.	
0Fh (303Dh)	**REG303D**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_SEL[127:120]	7:0	See description of '3020h'.	

EFUSE Register (Bank = 18)

Index (Absolute)	Mnemonic	Bit	Description	
10h (3040h)	**REG3040**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_VALUE[7:0]	7:0	Efuse overwrite value [127:0].	
10h (3041h)	**REG3041**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_VALUE[15:8]	7:0	See description of '3040h'.	
11h (3044h)	**REG3044**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_VALUE[23:16]	7:0	See description of '3040h'.	
11h (3045h)	**REG3045**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_VALUE[31:24]	7:0	See description of '3040h'.	
12h (3048h)	**REG3048**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_VALUE[39:32]	7:0	See description of '3040h'.	
12h (3049h)	**REG3049**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_VALUE[47:40]	7:0	See description of '3040h'.	
13h (304Ch)	**REG304C**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_VALUE[55:48]	7:0	See description of '3040h'.	
13h (304Dh)	**REG304D**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_VALUE[63:56]	7:0	See description of '3040h'.	
14h (3050h)	**REG3050**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_VALUE[71:64]	7:0	See description of '3040h'.	
14h (3051h)	**REG3051**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_VALUE[79:72]	7:0	See description of '3040h'.	
15h (3054h)	**REG3054**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_VALUE[87:80]	7:0	See description of '3040h'.	
15h (3055h)	**REG3055**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_VALUE[95:88]	7:0	See description of '3040h'.	
16h (3058h)	**REG3058**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_VALUE[103:96]	7:0	See description of '3040h'.	
16h (3059h)	**REG3059**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_VALUE[111:104]	7:0	See description of '3040h'.	
17h (305Ch)	**REG305C**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_VALUE[119:112]	7:0	See description of '3040h'.	
17h (305Dh)	**REG305D**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_OVERWRITE_VALUE[127:120]	7:0	See description of '3040h'.	
18h	**REG3060**	**7:0**	**Default : 0x00**	**Access : RO**

EFUSE Register (Bank = 18)

Index (Absolute)	Mnemonic	Bit	Description	
(3060h)	EFUSE_RAW_BIT[7:0]	7:0	Efuse raw bit [127:0].	
18h (3061h)	**REG3061**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_RAW_BIT[15:8]	7:0	See description of '3060h'.	
19h (3064h)	**REG3064**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_RAW_BIT[23:16]	7:0	See description of '3060h'.	
19h (3065h)	**REG3065**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_RAW_BIT[31:24]	7:0	See description of '3060h'.	
1Ah (3068h)	**REG3068**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_RAW_BIT[39:32]	7:0	See description of '3060h'.	
1Ah (3069h)	**REG3069**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_RAW_BIT[47:40]	7:0	See description of '3060h'.	
1Bh (306Ch)	**REG306C**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_RAW_BIT[55:48]	7:0	See description of '3060h'.	
1Bh (306Dh)	**REG306D**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_RAW_BIT[63:56]	7:0	See description of '3060h'.	
1Ch (3070h)	**REG3070**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_RAW_BIT[71:64]	7:0	See description of '3060h'.	
1Ch (3071h)	**REG3071**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_RAW_BIT[79:72]	7:0	See description of '3060h'.	
1Dh (3074h)	**REG3074**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_RAW_BIT[87:80]	7:0	See description of '3060h'.	
1Dh (3075h)	**REG3075**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_RAW_BIT[95:88]	7:0	See description of '3060h'.	
1Eh (3078h)	**REG3078**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_RAW_BIT[103:96]	7:0	See description of '3060h'.	
1Eh (3079h)	**REG3079**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_RAW_BIT[111:104]	7:0	See description of '3060h'.	
1Fh (307Ch)	**REG307C**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_RAW_BIT[119:112]	7:0	See description of '3060h'.	
1Fh (307Dh)	**REG307D**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_RAW_BIT[127:120]	7:0	See description of '3060h'.	
20h (3080h)	**REG3080**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	

EFUSE Register (Bank = 18)

Index (Absolute)	Mnemonic	Bit	Description	
	PROG_FU_EN	0	Efuse program enable bit.	
21h (3084h)	**REG3084**	**7:0**	**Default : 0x04**	**Access : R/W**
	PROG_FU_CNT[7:0]	7:0	Program cycle count by 26Mz (10us). 260 * 1/26M ~= 10us.	
21h (3085h)	**REG3085**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	PROG_FU_CNT[8]	0	See description of '3084h'.	
22h (3088h)	**REG3088**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	GADRR[5:0]	5:0	Efuse_bit_sel_address.	
22h (3089h)	**REG3089**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	GBANK_SEL[9:8]	1:0	Efuse_bank_sel_address;. 2'b01 bank0,. 2'b10 bank1.	
23h (308Ch)	**REG308C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	GMONGATE	1	Efuse gmgate input signal. Must be low when GPROG is high.	
	GMONSEL	0	Efuse GMONSEL input signal. Must be low when GPROG is high.	
26h (3098h)	**REG3098**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	GBANK_P[4:3]	4:3	Efuse_bank_sel_address; 2'b01 bank0, 2'b10 bank1.	
	GPRCHG_N	2	Read only flag; efuse GPRCHG_N.	
	GFSET_P	1	Read only flag; efuse GFSET_P.	
	GSIGDEV_P	0	Read only flag; efuse GSIGDEV_P.	
27h (309Ch)	**REG309C**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_STATE[7:0]	7:0	Efuse read FSM state.	
27h (309Dh)	**REG309D**	**7:0**	**Default : 0x00**	**Access : RO**
	EFUSE_STATE[15:8]	7:0	See description of '309Ch'.	
28h (30A0h)	**REG30A0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	EFUSE_READ	0	Efuse read trigger.	

DISP Register (Bank = 19)

DISP Register (Bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (3204h)	**REG3204**	**7:0**	**Default : 0x00**	**Access : R/W**
	TG_VS_ST[7:0]	7:0		
01h (3205h)	**REG3205**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	TG_VS_ST[10:8]	2:0	See description of '3204h'.	
02h (3208h)	**REG3208**	**7:0**	**Default : 0x03**	**Access : R/W**
	TG_VS_END[7:0]	7:0		
02h (3209h)	**REG3209**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	TG_VS_END[10:8]	2:0	See description of '3208h'.	
03h (320Ch)	**REG320C**	**7:0**	**Default : 0x05**	**Access : R/W**
	TG_VFDE_ST[7:0]	7:0		
03h (320Dh)	**REG320D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	TG_VFDE_ST[10:8]	2:0	See description of '320Ch'.	
04h (3210h)	**REG3210**	**7:0**	**Default : 0x5C**	**Access : R/W**
	TG_VFDE_END[7:0]	7:0		
04h (3211h)	**REG3211**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:3	Reserved.	
	TG_VFDE_END[10:8]	2:0	See description of '3210h'.	
05h (3214h)	**REG3214**	**7:0**	**Default : 0x05**	**Access : R/W**
	TG_VDE_ST[7:0]	7:0		
05h (3215h)	**REG3215**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	TG_VDE_ST[10:8]	2:0	See description of '3214h'.	
06h (3218h)	**REG3218**	**7:0**	**Default : 0x5C**	**Access : R/W**
	TG_VDE_END[7:0]	7:0		
06h (3219h)	**REG3219**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:3	Reserved.	
	TG_VDE_END[10:8]	2:0	See description of '3218h'.	
07h	**REG321C**	**7:0**	**Default : 0x73**	**Access : R/W**

DISP Register (Bank = 19)

Index (Absolute)	Mnemonic	Bit	Description	
(321Ch)	TG_VTT[7:0]	7:0		
07h (321Dh)	**REG321D**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:3	Reserved.	
	TG_VTT[10:8]	2:0	See description of '321Ch'.	
09h (3224h)	**REG3224**	**7:0**	**Default : 0x00**	**Access : R/W**
	TG_HS_ST[7:0]	7:0		
09h (3225h)	**REG3225**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	TG_HS_ST[10:8]	2:0	See description of '3224h'.	
0Ah (3228h)	**REG3228**	**7:0**	**Default : 0x7F**	**Access : R/W**
	TG_HS_END[7:0]	7:0		
0Ah (3229h)	**REG3229**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	TG_HS_END[10:8]	2:0	See description of '3228h'.	
0Bh (322Ch)	**REG322C**	**7:0**	**Default : 0xA8**	**Access : R/W**
	TG_HFDE_ST[7:0]	7:0		
0Bh (322Dh)	**REG322D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	TG_HFDE_ST[10:8]	2:0	See description of '322Ch'.	
0Ch (3230h)	**REG3230**	**7:0**	**Default : 0xC7**	**Access : R/W**
	TG_HFDE_END[7:0]	7:0		
0Ch (3231h)	**REG3231**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:3	Reserved.	
	TG_HFDE_END[10:8]	2:0	See description of '3230h'.	
0Dh (3234h)	**REG3234**	**7:0**	**Default : 0xA8**	**Access : R/W**
	TG_HDE_ST[7:0]	7:0		
0Dh (3235h)	**REG3235**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	TG_HDE_ST[10:8]	2:0	See description of '3234h'.	
0Eh (3238h)	**REG3238**	**7:0**	**Default : 0xC7**	**Access : R/W**
	TG_HDE_END[7:0]	7:0		
0Eh (3239h)	**REG3239**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:3	Reserved.	

DISP Register (Bank = 19)

Index (Absolute)	Mnemonic	Bit	Description	
	TG_HDE_END[10:8]	2:0	See description of '3238h'.	
0Fh (323Ch)	**REG323C**	**7:0**	**Default : 0x1F**	**Access : R/W**
	TG_HTT[7:0]	7:0		
0Fh (323Dh)	**REG323D**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:3	Reserved.	
	TG_HTT[10:8]	2:0	See description of '323Ch'.	
10h (3240h)	**REG3240**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	TG_DBF_EN	1		
	DISP_OSD_EN	0		
10h (3241h)	**REG3241**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	DISP_FORCE_FRAME_COLOR	0		
11h (3244h)	**REG3244**	**7:0**	**Default : 0x00**	**Access : R/W**
	DISP_FRAME_COLOR[7:0]	7:0		
11h (3245h)	**REG3245**	**7:0**	**Default : 0x00**	**Access : R/W**
	DISP_FRAME_COLOR[15:8]	7:0	See description of '3244h'.	
12h (3248h)	**REG3248**	**7:0**	**Default : 0Xff**	**Access : R/W**
	DISP_FRAME_COLOR[23:16]	7:0	See description of '3244h'.	
13h (324Ch)	**REG324C**	**7:0**	**Default : 0x40**	**Access : R/W**
	DISP_LB_DEPTH[7:0]	7:0		
14h (3250h)	**REG3250**	**7:0**	**Default : 0x0F**	**Access : R/W**
	TG_FRAME_PLL_REF_Y[7:0]	7:0		
14h (3251h)	**REG3251**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	TG_FRAME_PLL_REF_Y[10:8]	2:0	See description of '3250h'.	
15h (3254h)	**REG3254**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	TG_SW_CLR_VCNT_FREEZE_REGION	1		
	TG_VCNT_FREEZE	0		
15h (3255h)	**REG3255**	**7:0**	**Default : 0x00**	**Access : RO**
	TG_VCNT_FREEZE_REGION	7		

DISP Register (Bank = 19)

Index (Absolute)	Mnemonic	Bit	Description	
	-	6:0	Reserved.	
17h (325Ch)	**REG325C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	STATUS_CLR	0		
18h (3260h)	**REG3260**	**7:0**	**Default : 0x80**	**Access : R/W**
	CBS_BRI[7:0]	7:0		
18h (3261h)	**REG3261**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	CBS_CLAMP_MODE	0		
19h (3264h)	**REG3264**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	CSC_Y2R_EN	0		
19h (3265h)	**REG3265**	**7:0**	**Default : 0x00**	**Access : R/W**
	CSC_Y2R_Y_OFSET8[7:0]	7:0		
1Ah (3268h)	**REG3268**	**7:0**	**Default : 0x00**	**Access : R/W**
	CSC_Y2R_CB_OFSET8[7:0]	7:0		
1Ah (3269h)	**REG3269**	**7:0**	**Default : 0x00**	**Access : R/W**
	CSC_Y2R_CR_OFSET8[7:0]	7:0		
1Bh (326Ch)	**REG326C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CSC_Y2R_A11[7:0]	7:0		
1Bh (326Dh)	**REG326D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CSC_Y2R_A11[13:8]	5:0	See description of '326Ch'.	
1Ch (3270h)	**REG3270**	**7:0**	**Default : 0x00**	**Access : R/W**
	CSC_Y2R_A12[7:0]	7:0		
1Ch (3271h)	**REG3271**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CSC_Y2R_A12[13:8]	5:0	See description of '3270h'.	
1Dh (3274h)	**REG3274**	**7:0**	**Default : 0x00**	**Access : R/W**
	CSC_Y2R_A13[7:0]	7:0		
1Dh (3275h)	**REG3275**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CSC_Y2R_A13[13:8]	5:0	See description of '3274h'.	

DISP Register (Bank = 19)

Index (Absolute)	Mnemonic	Bit	Description	
1Eh (3278h)	**REG3278**	**7:0**	**Default : 0x00**	**Access : R/W**
	CSC_Y2R_A21[7:0]	7:0		
1Eh (3279h)	**REG3279**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CSC_Y2R_A21[13:8]	5:0	See description of '3278h'.	
1Fh (327Ch)	**REG327C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CSC_Y2R_A22[7:0]	7:0		
1Fh (327Dh)	**REG327D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CSC_Y2R_A22[13:8]	5:0	See description of '327Ch'.	
20h (3280h)	**REG3280**	**7:0**	**Default : 0x00**	**Access : R/W**
	CSC_Y2R_A23[7:0]	7:0		
20h (3281h)	**REG3281**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CSC_Y2R_A23[13:8]	5:0	See description of '3280h'.	
21h (3284h)	**REG3284**	**7:0**	**Default : 0x00**	**Access : R/W**
	CSC_Y2R_A31[7:0]	7:0		
21h (3285h)	**REG3285**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CSC_Y2R_A31[13:8]	5:0	See description of '3284h'.	
22h (3288h)	**REG3288**	**7:0**	**Default : 0x00**	**Access : R/W**
	CSC_Y2R_A32[7:0]	7:0		
22h (3289h)	**REG3289**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CSC_Y2R_A32[13:8]	5:0	See description of '3288h'.	
23h (328Ch)	**REG328C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CSC_Y2R_A33[7:0]	7:0		
23h (328Dh)	**REG328D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CSC_Y2R_A33[13:8]	5:0	See description of '328Ch'.	
28h (32A0h)	**REG32A0**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY_30[7:0]	7:0		
28h	**REG32A1**	**7:0**	**Default : 0x00**	**Access : R/W**

DISP Register (Bank = 19)

Index (Absolute)	Mnemonic	Bit	Description	
(32A1h)	DUMMY_30[15:8]	7:0	See description of '32A0h'.	
30h (32C0h)	**REG32C0**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	STATUS_LB_NOT_ENOUGH	0		
37h (32DCh)	**REG32DC**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	BIST_FAIL_DISP[1:0]	1:0		
68h (33A0h)	**REG33A0**	**7:0**	**Default : 0x19**	**Access : R/W**
	VIP_3D_DITHER_EN	7	3d dither enable.	
	-	6	Reserved.	
	VIP_3D_DITHER_MONO_EN	5	3d dither monochrome mode enable.	
	VIP_3D_DITHER_LSB_EN	4	3d dither LSB dither enable.	
	VIP_3D_DITHER_LSB_SEL[1:0]	3:2	3d dither LSB dither table select.	
	VIP_3D_DITHER_MSB_SEL[1:0]	1:0	3d dither MSB dither table select.	
68h (33A1h)	**REG33A1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	VIP_3D_DITHER_VCLR_EN	6	3d dither vertical dither enable.	
	VIP_3D_DITHER_VCLR_NO[1:0]	5:4	3d dither vertical dither table number.	
	VIP_3D_DITHER_LSB_VCLR_EN	3	3d dither LSB vertical dither enable.	
	VIP_3D_DITHER_10_MOD_EN	2	3d dither 10 modes detect enable.	
	VIP_3D_DITHER_LSB_VCLR_NO[1:0]	1:0	3d dither LSB vertical dither table number.	
69h (33A4h)	**REG33A4**	**7:0**	**Default : 0x99**	**Access : R/W**
	VIP_3D_DITHER_MSB_R_MASK[1:0]	7:6	3d dither MSB R channel mask.	
	VIP_3D_DITHER_MSB_B_MASK[1:0]	5:4	3d dither MSB B channel mask.	
	VIP_3D_DITHER_LSB_R_MASK[1:0]	3:2	3d dither LSB R channel mask.	
	VIP_3D_DITHER_LSB_B_MASK[1:0]	1:0	3d dither LSB B channel mask.	

DISP Register (Bank = 19)

Index (Absolute)	Mnemonic	Bit	Description	
69h (33A5h)	**REG33A5**	**7:0**	**Default : 0x27**	**Access : R/W**
	VIP_3D_DITHER_H_DITHER_TABLE0[7:0]	7:0	3d dither Horizontal dither table0.	
7Ah (33E8h)	**REG33E8**	**7:0**	**Default : 0x8D**	**Access : R/W**
	VIP_3D_DITHER_H_DITHER_TABLE1[7:0]	7:0	3d dither Horizontal dither table1.	
7Ah (33E9h)	**REG33E9**	**7:0**	**Default : 0x63**	**Access : R/W**
	VIP_3D_DITHER_H_DITHER_TABLE2[7:0]	7:0	3d dither Horizontal dither table2.	
7Bh (33ECh)	**REG33EC**	**7:0**	**Default : 0x9C**	**Access : R/W**
	VIP_3D_DITHER_H_DITHER_TABLE3[7:0]	7:0	3d dither Horizontal dither table3.	
7Bh (33EDh)	**REG33ED**	**7:0**	**Default : 0x4E**	**Access : R/W**
	VIP_3D_DITHER_V_DITHER_TABLE0[7:0]	7:0	3d dither Vertical dither table0.	
7Ch (33F0h)	**REG33F0**	**7:0**	**Default : 0x4B**	**Access : R/W**
	VIP_3D_DITHER_V_DITHER_TABLE1[7:0]	7:0	3d dither Vertical dither table1.	
7Ch (33F1h)	**REG33F1**	**7:0**	**Default : 0x93**	**Access : R/W**
	VIP_3D_DITHER_V_DITHER_TABLE2[7:0]	7:0	3d dither Vertical dither table2.	
7Dh (33F4h)	**REG33F4**	**7:0**	**Default : 0x39**	**Access : R/W**
	VIP_3D_DITHER_V_DITHER_TABLE3[7:0]	7:0	3d dither Vertical dither table3.	
7Dh (33F5h)	**REG33F5**	**7:0**	**Default : 0x0C**	**Access : R/W**
	VIP_3D_DITHER_DEBUG[7:0]	7:0	3d dither Debug Use.	
7Eh (33F8h)	**REG33F8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	VIP_3D_DITHER_OUT_FMT[1:0]	1:0	3d dither output format. 2'b00 bypass mode. 2'b01 565 mode. 2'b10 666 mode. 2'b11 bypass mode.	

DISP_LPLL Register (Bank = 1A)

DISP_LPLL Register (Bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h (3408h)	**REG3408**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:2	Reserved.	
	IP_NON_STABLE	1	IP non stable.	
	IP_NO_SIGNAL	0	IP no signal.	
05h (3414h)	**REG3414**	**7:0**	**Default : 0x22**	**Access : R/W**
	PRD_LOCK_THRESH[3:0]	7:4	Prd lock threshes.	
	PRD_STABLE_THRESH[3:0]	3:0	Clock stable thresh.	
05h (3415h)	**REG3415**	**7:0**	**Default : 0x02**	**Access : R/W**
	PHASE_LOCK_THRESH[7:0]	7:0	Phase lock threshes.	
06h (3418h)	**REG3418**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_D5D6D7[7:0]	7:0	Limit for clock freq correction modification.	
06h (3419h)	**REG3419**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_D5D6D7[15:8]	7:0	See description of '3418h'.	
07h (341Ch)	**REG341C**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_D5D6D7[23:16]	7:0	See description of '3418h'.	
08h (3420h)	**REG3420**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_D5D6D7_RK[7:0]	7:0	Limit for phase correction modification.	
08h (3421h)	**REG3421**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_D5D6D7_RK[15:8]	7:0	See description of '3420h'.	
09h (3424h)	**REG3424**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_D5D6D7_RK[23:16]	7:0	See description of '3420h'.	
0Ah (3428h)	**REG3428**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_LPLL_OFFSET[7:0]	7:0	Limit for lpll phase offset.	
0Ah (3429h)	**REG3429**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_LPLL_OFFSET[15:8]	7:0	See description of '3428h'.	
0Bh (342Ch)	**REG342C**	**7:0**	**Default : 0x10**	**Access : R/W**
	P_GAIN_PRD[3:0]	7:4	P_gain for prd_lock, gain setting is same as i_gain_prd.	

DISP_LPLL Register (Bank = 1A)

Index (Absolute)	Mnemonic	Bit	Description	
	I_GAIN_PRD[3:0]	3:0	I_gain for prd lock. 0: >> 5. 1: >> 4. 2: >> 3. 3: >> 2. 4: >> 1. 5: Same. 6: << 1. 7: << 2. 8: << 3. 9: << 4. 10: << 5. 11: << 6. 12: << 7. 13: << 8. 14: << 9. 15: << 10.	
0Bh (342Dh)	**REG342D**	**7:0**	**Default : 0x10**	**Access : R/W**
	P_GAIN_PHASE[3:0]	7:4	P_gain for phase lock, gain setting is same as i_gain_prd.	
	I_GAIN_PHASE[3:0]	3:0	I_gain for phase lock, game setting is same as i_gain_prd.	
0Ch (3430h)	**REG3430**	**7:0**	**Default : 0x00**	**Access : R/W**
	P_GAIN_PHASE_ZERO	7	Disable p_gain for lock phase.	
	I_GAIN_PHASE_ZERO	6	Disable i_gain for lock phase.	
	P_GAIN_PRD_ZERO	5	Disable p_gain for lock prd.	
	I_GAIN_PRD_ZERO	4	Disable i_gain for lock prd.	
	FRAME_LPLL_EN	3	Frame lpll enable.	
	-	2	Reserved.	
	FPLL_MODE[1:0]	1:0	FPLL Mode. 00: Lock phase mode.	
0Ch (3431h)	**REG3431**	**7:0**	**Default : 0x00**	**Access : R/W**
	OVS_FRAME_DIV[3:0]	7:4	Output fame div for frame sync.	
	IVS_FRAME_DIV[3:0]	3:0	Input frame div for frame sync.	
0Dh (3434h)	**REG3434**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

DISP_LPLL Register (Bank = 1A)

Index (Absolute)	Mnemonic	Bit	Description	
	EN_2_LIMIT	4	Enable 2 limits.	
	FORCE_PHASE_CLOSE_DONE	3	S.W. Force phase close done.	
	FORCE_PHASE_REDUCE_DONE	2	S.W. Force phase reduce done.	
	FORCE_PRD_LOCK_DONE	1	S.W. Force prd lock done.	
	FORCE_PRD_STABLE	0	S.W. Force prd stable check ok.	
0Dh (3435h)	**REG3435**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:4	Reserved.	
	SSC_EN	3	SSC mode enable.	
	PRD_SEL_ORI_VS	2	Select ori ovs as lock prd referene.	
	NON_STABLE_EN	1	Frame pll disable when non_stable flag high.	
	NO_SIGNAL_EN	0	Frame pll disable when no_signal flag high.	
0Fh (343Ch)	**REG343C**	**7:0**	**Default : 0x44**	**Access : R/W**
	LPLL_SET[7:0]	7:0	LPLL initial setting value.	
0Fh (343Dh)	**REG343D**	**7:0**	**Default : 0x55**	**Access : R/W**
	LPLL_SET[15:8]	7:0	See description of '343Ch'.	
10h (3440h)	**REG3440**	**7:0**	**Default : 0x24**	**Access : R/W**
	LPLL_SET[23:16]	7:0	See description of '343Ch'.	
11h (3444h)	**REG3444**	**7:0**	**Default : 0x00**	**Access : RO**
	PHASE_DIF[7:0]	7:0	Phase dif value.	
11h (3445h)	**REG3445**	**7:0**	**Default : 0x00**	**Access : RO**
	PHASE_DIF[15:8]	7:0	See description of '3444h'.	
12h (3448h)	**REG3448**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	PHASE_UP	0	Ovs leading or lagging related to ivs. 0: Leading. 1: Lagging.	
13h (344Ch)	**REG344C**	**7:0**	**Default : 0x00**	**Access : RO**
	PRD_DIF[7:0]	7:0	Reference signal prd difference value.	
13h (344Dh)	**REG344D**	**7:0**	**Default : 0x00**	**Access : RO**
	PRD_DIF[15:8]	7:0	See description of '344Ch'.	
14h (3450h)	**REG3450**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	

DISP_LPLL Register (Bank = 1A)

Index (Absolute)	Mnemonic	Bit	Description	
	PRD_UP	0	Ovs prd related to ivs prd. 0: Faster. 1: Slower.	
17h (345Ch)	**REG345C**	**7:0**	**Default : 0x20**	**Access : R/W**
	LPLL_STEP[7:0]	7:0	Output PLL spread spectrum step.	
17h (345Dh)	**REG345D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL_STEP[9:8]	1:0	See description of '345Ch'.	
18h (3460h)	**REG3460**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL_SPAN[7:0]	7:0	Output PLL spread spectrum span.	
18h (3461h)	**REG3461**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	LPLL_SPAN[13:8]	5:0	See description of '3460h'.	
1Fh (347Ch)	**REG347C**	**7:0**	**Default : 0x80**	**Access : R/W**
	PHASE_CLOSE_THRESH[7:0]	7:0	Phase close done thresh.	
1Fh (347Dh)	**REG347D**	**7:0**	**Default : 0x30**	**Access : R/W**
	REDUCE_DONE_THRESH[3:0]	7:4	Phase reduce done thresh.	
	PHASE_CLOSE_THRESH[11:8]	3:0	See description of '347Ch'.	
20h (3480h)	**REG3480**	**7:0**	**Default : 0x52**	**Access : R/W**
	-	7	Reserved.	
	HIS_CNT_HIGH_THRESH[2:0]	6:4	History counter high thresh.	
	-	3	Reserved.	
	HIS_CNT_LOW_THRESH[2:0]	2:0	History counter low thresh.	
21h (3484h)	**REG3484**	**7:0**	**Default : 0x00**	**Access : RO**
	IVS_PRD_VALUE[7:0]	7:0	Ivs prd value.	
21h (3485h)	**REG3485**	**7:0**	**Default : 0x00**	**Access : RO**
	IVS_PRD_VALUE[15:8]	7:0	See description of '3484h'.	
22h (3488h)	**REG3488**	**7:0**	**Default : 0x00**	**Access : RO**
	IVS_PRD_VALUE[23:16]	7:0	See description of '3484h'.	
23h (348Ch)	**REG348C**	**7:0**	**Default : 0x00**	**Access : RO**
	OVS_PRD_VALUE[7:0]	7:0	Ovs prd value.	
23h (348Dh)	**REG348D**	**7:0**	**Default : 0x00**	**Access : RO**
	OVS_PRD_VALUE[15:8]	7:0	See description of '348Ch'.	

DISP_LPLL Register (Bank = 1A)

Index (Absolute)	Mnemonic	Bit	Description	
24h (3490h)	**REG3490**	**7:0**	**Default : 0x00**	**Access : RO**
	OVS_PRD_VALUE[23:16]	7:0	See description of '348Ch'.	
28h (34A0h)	**REG34A0**	**7:0**	**Default : 0x00**	**Access : RO**
	LPLL_SET_USING[7:0]	7:0	Lpll_set value for using.	
28h (34A1h)	**REG34A1**	**7:0**	**Default : 0x00**	**Access : RO**
	LPLL_SET_USING[15:8]	7:0	See description of '34A0h'.	
29h (34A4h)	**REG34A4**	**7:0**	**Default : 0x00**	**Access : RO**
	LPLL_SET_USING[23:16]	7:0	See description of '34A0h'.	
2Ah (34A8h)	**REG34A8**	**7:0**	**Default : 0x00**	**Access : RO**
	PHASE_REDUCE_DONE	7	Phase reduce done flag.	
	PRD_LOCK_DONE	6	Prd lock done flag.	
	IVS_PRD_STABLE	5	Idclk stable flag.	
	OVS_PRD_STABLE	4	Odclk stable flag.	
	-	3	Reserved.	
	CS_STATE[2:0]	2:0	Frame pll FSM state. 3'h0: free run. 3'h1: lock_freq. 3'h2: reduce_phase. 3'h3: wait phase_close. 3'h4: lock_phase. others: Reserved.	
2Ah (34A9h)	**REG34A9**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	PHASE_LOCK_DONE	0	Phase lock done flag.	
2Eh (34B8h)	**REG34B8**	**7:0**	**Default : 0xC3**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL_PDREG	1	Lpll reg power down.	
	LPL_PDBG	0	Lpll bg power down.	
33h (34CCh)	**REG34CC**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL2_SKEW_DIVIDER_DIV2_SEL	7		
	LPLL2_2CHIP_SYN_EN	6		
	-	5	Reserved.	
	LPLL2_EN_HFLVDS	4	Reset digital circuit in LPLL.	
	-	3:0	Reserved.	

DISP_LPLL Register (Bank = 1A)

Index (Absolute)	Mnemonic	Bit	Description	
33h (34CDh)	**REG34CD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	LPLL2_SCALAR_DIV_SEL[2:0]	4:2		
	LPLL2_EN_SKEW_DIVIDER	1		
	-	0	Reserved.	
34h (34D0h)	**REG34D0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	LPLL2_SKEW_CLKP_PHASE_SEL[4:0]	4:0		
34h (34D1h)	**REG34D1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	LPLL2_SKEW_CLKM_PHASE_SEL[4:0]	4:0		
38h (34E0h)	**REG34E0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL_SCALAR_FB_DIV2_EN	1		
	-	0	Reserved.	
3Ah (34E8h)	**REG34E8**	**7:0**	**Default : 0x0C**	**Access : R/W**
	-	7:4	Reserved.	
	OEN_FBIN	3		
	OEN_REFIN	2		
	-	1:0	Reserved.	
3Fh (34FCh)	**REG34FC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	LPLL_RESET	0	Lpll software reset, high active.	
40h (3500h)	**REG3500**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	LPLL_LOCK	5	PLL Lock status, 1=Lock.	
	LPLL_HIGH_FLAG	4	VCO Vring too high flag. 1=too high.	
	-	3:0	Reserved.	
40h (3501h)	**REG3501**	**7:0**	**Default : 0x61**	**Access : R/W**
	-	7	Reserved.	

DISP_LPLL Register (Bank = 1A)

Index (Absolute)	Mnemonic	Bit	Description	
	LPLL_ICTRL[2:0]	6:4	PLL Charge Pump control current. 000: 1uA, 001: 2uA, 010:4uA, 011:8uA. 100: 2uA, 101: 4uA, 110:8uA, 111:16uA.	
	-	3:2	Reserved.	
	LPLL_VCO_OFFSET	1	PLL offset frequency enable, active high.	
	LPLL_PD	0	PLL power down, High=Power down.	
41h (3504h)	**REG3504**	**7:0**	**Default : 0x1F**	**Access : R/W**
	-	7:5	Reserved.	
	LPLL_ANA_RESETP	4		
	LPLL_ANA_RESETI	3		
	LPLL_ANA_RESETF	2		
	LPLL_ANA_RESET	1		
	LPLL_ANA_PORST	0		
42h (3508h)	**REG3508**	**7:0**	**Default : 0x30**	**Access : R/W**
	LPLL_FBDIV[3:0]	7:4		
	LPLL_DDIV[3:0]	3:0		
42h (3509h)	**REG3509**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:6	Reserved.	
	LPLL_KN[1:0]	5:4		
	LPLL_KM[3:0]	3:0		
43h (350Ch)	**REG350C**	**7:0**	**Default : 0x05**	**Access : R/W**
	-	7:4	Reserved.	
	LPLL_KP[3:0]	3:0		
44h (3510h)	**REG3510**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL_TEST[7:0]	7:0	PLL test register.	
44h (3511h)	**REG3511**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL_TEST[15:8]	7:0	See description of '3510h'.	
7Fh (35FCh)	**REG35FC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SW_TRIG_DB_LOAD	1	Trig to load double buffer register.	
	DB_EN	0	Enable lpll register double.	

AUX Register (Bank = 1B)

AUX Register (Bank = 1B)				
Index	**Mnemonic**	**Bit**	**Description**	
00h	**ADC_CONFIG**	**15:0**	**Default : 16'h0000**	**Access : R/W**
	EN_PEN_INTERRUPT	15	Enable Touch Screen's pen interrupt. 0: Enable. 1: Disable (default).	
	EN_TOUCH_SCREEN	14	Enable Touch screen. 0: No ADC conversion for touch screen jobs even if they are written in the job list (default). 1: Enable touch screen jobs if they are in the job list.	
	AUXADC3_VOL	13:12	AUXADC3 voltage. 00: 1.2V. 01: 1.5V. 10: 2.0V. 11: 2.5V.	
	AUXADC2_VOL	11:10	AUXADC2 voltage. 00: 1.2V. 01: 1.5V. 10: 2.0V. 11: 2.5V.	
	AUXADC1_VOL	9:8	AUXADC1 voltage. 00: 1.2V. 01: 1.5V. 10: 2.0V. 11: 2.5V.	
	AUXADC0_VOL	7:6	AUXADC0 voltage. 00: 1.2V. 01: 1.5V. 10: 2.0V. 11: 2.5V.	
	AUX_ADC_PD	5	0: Power down Aux ADC. 1: Power up Aux ADC.	
	TOUCHSCREEN_INT_DELAY_ENABLE	4	Enable bit for Touch Screen inter delay. 1: Wait for inter delay after touch screen channel conversion. 0: Do not wait for inter delay after touch screen channel conversion.	
	CTN_INT_DELAY_ENABLE	3	Enable bit for CTN inter delay. 1: Wait for inter delay after CNT channel conversion. 0: Do not wait for inter delay after CNT channel conversion.	

AUX Register (Bank = 1B)

Index	Mnemonic	Bit	Description	
	NORMAL_DELAY_ENABLE	2	Inter delay of normal channel enable, active high.	
	ADCSTARTEN	1	Enable bit for ADCSTART bit. 1: Start conversion on ADCSTART bit setting. 0: Start conversion immediately.	
	ADCSTART	0	Start bit for ADC conversion sequence. 1: Start a conversion sequence. 0: No conversion.	
02h	**ADCTEST**	**15:0**	**Default : 16'h0000**	**Access : R/W**
	AUX_TEST	15:12	[0]: SADC_REF_OP switch select. 0: Switch positive. 1: Switch negative. [2:1]: SADC_REF_IBIAS current select. 00: 5uA. 01: 4uA. 10: 7uA. 11: 6uA. [3]: Reserved.	
	FREE_RUN_REF2_SEL	11:10	AUX_ADC_REFN: Auxiliary ADC negative reference voltage in FREERUN mode. 00: ADC reference ground (default). 01: AUXADC2 (XN in touch screen application). 10: AUXADC3 (YN in touch screen application). 11: Reserved.	
	FREE_RUN_REF1_SEL	9:7	AUX_ADC_REFP: Auxiliary ADC positive reference voltage in FREERUN mode. 000: 1.2V. 001: 1.5V. 010: 1.714V. 011: 2.0V. 100: 2.4V. 101: 3.2V (VABB) (default). 110: XP (pulled up X panel positive voltage, this is to calibrate out switch resistance). 111: YP (pulled up Y panel positive voltage, this is to calibrate out switch resistance).	
	FREE_RUN_MUX_SEL	6:4	AD_MUX_SEL: Auxiliary ADC input select in FREERUN mode. 000: AUXADC0 input pin. 001: AUXADC1 input pin. 010: AUXADC2 input pin. 011: AUXADC3 input pin.	

AUX Register (Bank = 1B)

Index	Mnemonic	Bit	Description	
			100: PM channel, see PM_MUX_SEL bits. 101: PA temperature. Others: Reserved.	
	FREE_RUN_PM_MUX_SEL	3:1	PM_MUX_SEL: Select which PM channel to measure, only effective in FREERUN test mode. 000: Zero input. 001: Battery voltage, measured voltage is VBAT*1.8/4.2. 010: Charging current, measured voltage is ISENSE*REXT_SEN*10. 011: 2.1uA BANDGAP_ATOP PTAT current. 100: 2.0uA BANDGAP_ATOP source current. 101: 2.0uA BANDGAP_ATOP sink current. 110: 2.0uA REFGEN_STOP source current. 111: 0.25uA REFGEN_ATOP sink current.	
	FREE_RUN_TEST	0	ADC_FREERUN_TEST: 0: One shot mode selected (default). 1: Enable ADC freerun test.	
04h	**ADC_TIMING_CFG1**	**15:0**	**Default : 16'h0000**	**Access : R/W**
	AD_CONV_DELAY	15:8	CTNADCONVDELAY: ADC conversion CNT job pre delay register for temperature channel measurement with CTN.32K domain. Delay time = 10*AD_CONV_DELAY*CLK_32K.	
	AD_CONV_INTER	7:0	ADCONVINTER: ADC conversion interval register, 32K domain.	
06h	**ADC_TIMING_CFG2**	**15:0**	**Default : 12'h0000**	**Access : R/W**
	-	15:12	Reserved.	
	PAL_CFG	11:10	AUXADC PAL channel REF configuration. 00: 1.2. 01: 1.5. 10: 2.0. 11: VAUX2.5V.	
	REPEAT_CFG	9:8	Repeat times for ADC_JOBS, the result is the average. 00: 1. 01: 32. 10: 64. 11: 128.	
	NORMAL_DELAY	7:0	Normal pre delay for ADC jobs expected TS and BATTEMP/BATTYPE, 32K domain.	

AUX Register (Bank = 1B)

Index	Mnemonic	Bit	Description	
08h	**ADC_TIMING_CFG_ADC_JOB_LIST**	**15:0**	**Default : 16'h0000**	**Access : R/W**
	-	15	Reserved.	
	ADCJOB0	14:10	ADCJOB0: First ADC JOB channel selection: 00000: No channel selected. 00001: Battery Voltage. 00010: Charge Current. 00011: VCS_SENSE. 00100: Battery temperature (CTN channel). 00101: Battery type. 00110: Charge Voltage sense. 00111: AUXADC0. 01000: AUXADC1. 01001: AUXADC2. 01010: AUXADC3. 01011: Touch Screen's X resistance. 01100: Touch Screen's Y resistance. 01101: Touch Screen's X location. 01110: Touch Screen's Y location. 01111: Touch Screen's Z1 location. 10000: Touch Screen's Z2 location. 10001: PA_TMP job.	
	TOUCH_SCREEN_DELAY	9:0	TOUCHSCREENDELAY: ADC pre delay register for touch screen channel, AUX_CLK domain.	
0Ah	**ADC_JOB_LIST**	**15:0**	**Default : 16'h0000**	**Access : R/W**
	-	15	Reserved.	
	ADCJOB3	14:10	ADCJOB3: Fourth ADC JOB channel selection. Same channel mapping as ADCJOB0.	
	ADCJOB2	9:5	ADCJOB2: Third ADC JOB channel selection. Same channel mapping as ADCJOB0.	
	ADCJOB1	4:0	ADCJOB1: Second ADC JOB channel selection. Same channel mapping as ADCJOB0.	
0Ch	**ADCRES0**	**15:0**	**Default :**	**Access : RO**
	-	15:10	Reserved.	
	RESULT0_REG	9:0	Result register for ADC job0.	
0Eh	**ADCRES1**	**15:0**	**Default :**	**Access : RO**
	-	15:10	Reserved.	
	RESULT1_REG	9:0	Result register for ADC job1.	

AUX Register (Bank = 1B)

Index	Mnemonic	Bit	Description	
10h	**ADCRES2**	**15:0**	**Default :**	**Access : RO**
	-	15:10	Reserved.	
	RESULT2_REG	9:0	Result register for ADC job2.	
12h	**ADCRES3**	**15:0**	**Default :**	**Access : RO**
	-	15:10	Reserved.	
	RESULT3_REG	9:0	Result register for ADC job3.	
14h	**CYCLE_CONTROL**	**15:0**	**Default : 7'h0**	**Access : R/W**
	-	15:7	Reserved.	
	PD_TSI	6	Touch screen power down. 0: Power down TS. 1: Power up TS.	
	TSI_IS	5	Touch screen current select. 0: 1.56mA (default). 1: 1.17mA.	
	AUX_CLK_SEL	4:3	AUX clock frequency. 00: 100k. 01: 200k. 10: 400k. 11: 2.6M.	
	ONE_SHOT_CYCLE	2:0	Each one shot pulse will keep (ONE_SHOT_CYCLE +1) AUX_CLKS.	
16h	**TS_REFSEL1**	**15:0**	**Default : 15'h5299**	**Access : R/W**
	-	15	Reserved.	
	TS_X_RES_REF	14:10	Touch screen's X resistance {REF1_SEL, REF2_SEL}. [14:12]: AUX ADC positive reference voltage level. 000: 1.2V. 001: 1.5V. 010: 1.714V. 011: 2.0V. 100: 2.4V. 101: 2.5V (VAUX) (default). 110: XP (pulled up X panel positive voltage, this is to calibrate out switch resistance). 111: YP (pulled up Y panel positive voltage, this is to calibrate out switch resistance). [11:10]: AUX ADC negative reference voltage level. 00: Ground (default). 01: XN (pulled down X panel voltage, this is to calibrate out	

AUX Register (Bank = 1B)

Index	Mnemonic	Bit	Description	
			switch resistance). 10: YN (pulled down Y panel voltage, this is to calibrate out switch resistance). 11: Reserved.	
	TS_Y_RES_REF	9:5	Touch screen's Y resistance {REF1_SEL, REF2_SEL}.	
	TS_X_LOC_REF	4:0	Touch screen's X location {REF1_SEL, REF2_SEL}.	
18h	**TS_REFSEL2**	**15:0**	**Default : 15'h7bbd**	**Access : R/W**
	-	15	Reserved.	
	TS_Y_LOC_REF	14:10	Touch screen's Y location {REF1_SEL, REF2_SEL}.	
	TS_Z1_LOC_REF	9:5	Touch screen's Z1 resistance {REF1_SEL, REF2_SEL}.	
	TS_Z2_LOC_REF	4:0	Touch screen's Z2 resistance {REF1_SEL, REF2_SEL}.	
1Ah	**FREERUN_TST**	**15:0**	**Default : 16'h01f9**	**Access : R/W**
	-	15:9	Reserved.	
	FREE_RUN_MUXN_SEL	8:7	Negative input to AUX ADC in free run mode. 00: Touch screen X panel pulled low. 01: Touch screen Y panel pulled low. 10: PM ground. 11: AUX ADC ground.	
	FREE_RUN_CFG	6:0	[6]: ENZXP: X panel pull up driver. 0: Enable. 1: Disable (default). [5]: ENZXR: X panel source current. 0: Enable. 1: Disable (default). [4]: ENZYP: Y panel pull up driver. 0: Enable. 1: Disable (default). [3]: ENZYR: Y panel source current. 0: Enable. 1: Disable (default). [2]: ENXN: X panel pull down driver. 0: Enable. 1: Disable (default). [1]: ENYN: Y panel pull down driver. 0: Enable. 1: Disable (default). [0]: ENZPOINT: pen detect driver. 0: Enable. 1: Disable (default).	

AUX Register (Bank = 1B)

Index	Mnemonic	Bit	Description	
1Ch	**INT_CLEAR**	**15:0**	**Default : 2'h0**	**Access : WO**
	-	15:2	Reserved.	
	INT_CLEAR_KEY0	1	Clear interrupt of the Key0 (Write only; Self-cleared until another arbitrary APB write).	
	INT_CLEAR_ADCDONE	1	Clear interrupt of the ADC done (Write only; Self-cleared until another arbitrary APB write).	
	INT_CLEAR_PENDET	0	Clear interrupt of the pen detection (Write only; Self-cleared until another arbitrary APB write).	
1Eh	**INT_MASK**	**15:0**	**Default : 2'h3**	**Access : R/W**
	-	15:2	Reserved.	
	INT_MASK_KEY0	1	Mask of the Key0 (High stands for enabling interrupt; Low stands for disabling).	
	INT_MASK_ADCDONE	1	Mask of the ADC done (High stands for enabling interrupt; Low stands for disabling).	
	INT_MASK_PENDET	0	Mask of the pen detection (High stands for enabling interrupt; Low stands for disabling).	
20h	**INT_FORCE**	**15:0**	**Default : 2'h0**	**Access : R/W**
	-	15:2	Reserved.	
	INT_FORCE_ KEY0	1	Forcing of the Key0 (High stands for enabling interrupt; Low stands for disabling).	
	INT_FORCE_ADCDONE	1	Forcing of the ADC done (High stands for enabling interrupt; Low stands for disabling).	
	INT_FORCE_PENDET	0	Forcing of the pen detection (High stands for enabling interrupt; Low stands for disabling).	
22h	**INT_SOURCE**	**15:0**	**Default :**	**Access : RO**
	-	15:2	Reserved.	
	INT_SOURCE_KEY0	1	Read the level int.	
	INT_SOURCE_ADCDONE	1	Read the level int.	
	INT_SOURCE_PENDET	0	Read the level int.	
24h	**INT_SENSE**	**15:0**	**Default :**	**Access : RO**
	-	15:2	Reserved.	
	INT_SENSE_KEY0	1	Read the edge int.	
	INT_SENSE_ADCDONE	1	Read the edge int.	
	INT_SENSE_PENDET	0	Read the edge int.	
26h	**GPIO_IN**	**15:0**	**Default :**	**Access : RO**

AUX Register (Bank = 1B)

Index	Mnemonic	Bit	Description	
	-	15:4	Reserved.	
	GPIO_IN	**3:0**	**Read the GPIO input.**	
3Ch	**SW_RESET**	**15:0**	**Default :**	**Access : WO**
	-	15:3	Reserved.	
	SW_RESET_ATOP	2	Reset AUX_ATOP.	
	-	1	Reserved.	
	SW_RESET_AUX	0	Reset aux digital part.	
3Eh	**GPIO_control**	**15:0**	**Default : 16'hFF0F**	**Access : RW**
	GPIO_OEN	**3:0**	GPIO Output enable	
	GPIO_O	**7:4**	GPIO Output value	
	PGE	**11:8**	PMOS gate enable: 1: push-pull GPIO (for general case) 0: open-drain GPIO.	
	AIE	**15:12**	Keypad [3:0] analog input to SARADC enable, high active	

CPUIF Register (Bank = 1B)

CPUIF Register (Bank = 1B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
60h (3780h)	**REG3780**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	I80_CSN	0	Chip select. 0: Enable. 1: Disable.	
60h (3781h)	**REG3781**	**7:0**	**Default : 0x00**	**Access : R/W**
	I80_B_OEN[7:0]	7:0	PAD_B OEN. 0: Output enable. 1: Disable.	
61h (3784h)	**REG3784**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	IMAGE_PHASE_AUTO_OFF	3	Write one frame only.	
	VSYNC_DONT_CARE	2	Don't care sync data with external signal.	
	IMAGE_PHASE	1	Image/command phase. 0: Command phase. 1: Image phase.	
	I80_DCN	0	Data/index select. 0: Index. 1: Data.	
61h (3785h)	**REG3785**	**7:0**	**Default : 0x00**	**Access : R/W**
	I80_G_OEN[7:0]	7:0	PAD_G OEN. 0: Output enable. 1: Disable.	
62h (3788h)	**REG3788**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:3	Reserved.	
	M68_EN_INV	2	Invert enable pulse for m68 mode. 0: Normal for i80 mode. 1: Inverse for m68 mode.	
	M68_RW_OPT	1	I80 system: set level high. 0: Forbidden. 1: Select i80 configuration. M68 system: read/ write option. 0: M68 write. 1: M68 read.	
	I80_RW_OPT	0	I80 system: read / write option.	

CPUIF Register (Bank = 1B)

Index (Absolute)	Mnemonic	Bit	Description	
			0: I80 write. 1: I80 read. M68 system: m68 configuration. 0: Forbidden. 1: Select m68 configuration.	
62h (3789h)	**REG3789**	**7:0**	**Default : 0x00**	**Access : R/W**
	I80_R_OEN[7:0]	7:0	PAD_R OEN. 0: Output enable. 1: Disable.	
63h (378Ch)	**REG378C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	LCD_BUS_FM[2:0]	2:0	Lcd bus format. RGB666 <18 bits per pixel>. 0 = transfer 18-bit data / cycle. 1 = transfer 9-bit data / cycle. 2 = transfer 6-bit data / cycle. RGB565 <16 bits per pixel>. 3 = transfer 16-bit data / cycle. 4 = transfer 8-bit data / cycle. RGB888 <24 bits per pixel>. 5 = transfer 24-bit data / cycle. 6 = transfer 8-bit data / cycle.	
64h (3790h)	**REG3790**	**7:0**	**Default : 0x00**	**Access : R/W**
	COMMAND[7:0]	7:0	COMMAND to panel.	
64h (3791h)	**REG3791**	**7:0**	**Default : 0x00**	**Access : R/W**
	COMMAND[15:8]	7:0	See description of '3790h'.	
65h (3794h)	**REG3794**	**7:0**	**Default : 0x00**	**Access : R/W**
	COMMAND[23:16]	7:0	See description of '3790h'.	
66h (3798h)	**REG3798**	**7:0**	**Default : 0x00**	**Access : R/W**
	DISP_WIDTH[7:0]	7:0	Display width.	
66h (3799h)	**REG3799**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DISP_WIDTH[10:8]	2:0	See description of '3798h'.	
67h (379Ch)	**REG379C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DISP_HEIGHT[7:0]	7:0	Display height.	
67h	**REG379D**	**7:0**	**Default : 0x00**	**Access : R/W**

CPUIF Register (Bank = 1B)

Index (Absolute)	Mnemonic	Bit	Description	
(379Dh)	-	7:3	Reserved.	
	DISP_HEIGHT[10:8]	2:0	See description of '379Ch'.	
68h (37A0h)	**REG37A0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	PATGEN_ON	4	Auto pattern gen switch.	
	PAT_TYPE[3:0]	3:0	Auto pattern gen type.	
69h (37A4h)	**REG37A4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	VSYNC_POL	1	Vsyn polarity.	
	EXT_TRIG	0	External trigger select. 0: Internal trigger. 1: External trigger.	
6Ah (37A8h)	**REG37A8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	INIT_TRIG	0	Initial trigger.	
6Bh (37ACh)	**REG37AC**	**7:0**	**Default : 0x24**	**Access : R/W**
	-	7	Reserved.	
	LCD_HB_1ST	6	Convey high byte data first.	
	LCD_C2[1:0]	5:4	C2 color representation. 0: R. 1: G. 2: B. 3: Reserved.	
	LCD_C1[1:0]	3:2	C1 color representation. 0: R. 1: G. 2: B. 3: Reserved.	
	LCD_C0[1:0]	1:0	C0 color representation. 0: R. 1: G. 2: B. 3: Reserved.	
6Ch (37B0h)	**REG37B0**	**7:0**	**Default : 0x00**	**Access : RO**
	PEL_HCNT[7:0]	7:0	Horizontal pixel count.	
6Ch (37B1h)	**REG37B1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	PEL_HCNT[10:8]	2:0	See description of '37B0h'.	
6Dh (37B4h)	**REG37B4**	**7:0**	**Default : 0x00**	**Access : RO**
	PEL_VCNT[7:0]	7:0	Vertical pixel count.	
6Dh (37B5h)	**REG37B5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	PEL_VCNT[10:8]	2:0	See description of '37B4h'.	

CPUIF Register (Bank = 1B)

Index (Absolute)	Mnemonic	Bit	Description	
6Eh (37B8h)	**REG37B8**	**7:0**	**Default : 0x00**	**Access : RO**
	8068_RD[7:0]	7:0	I80/m68 read data.	
6Eh (37B9h)	**REG37B9**	**7:0**	**Default : 0x00**	**Access : RO**
	8068_RD[15:8]	7:0	See description of '37B8h'.	
6Fh (37BCh)	**REG37BC**	**7:0**	**Default : 0x00**	**Access : RO**
	8068_RD[23:16]	7:0	See description of '37B8h'.	
7Fh (37FCh)	**REG37FC**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	CMD_DONE_STATUS	1	CMD done status.	
	DMA_STATUS	0	DMA status.	
7Fh (37FDh)	**REG37FD**	**7:0**	**Default : 0x00**	**Access : R/W**
	STATUS_CLR	7	Status clear.	
	-	6:0	Reserved.	

SC0 Register (Bank = 1C)

SC0 Register (Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h (3808h)	**REG3808**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SC_WM_SEL[1:0]	5:4	SC ipw data path mux: 2'd0: bt656 -> ipw. 2'd1: cpu interface -> ipw. 2'd2: hvsp -> ipw. 2'd3: hvsp (background) -> ipw.	
	-	3:1	Reserved.	
	SC_DM_SEL	0	SC display data path mux: 1'b0: hvsp -> display. 1'b1: ipm2 -> display.	
02h (3809h)	**REG3809**	**7:0**	**Default : 0x00**	**Access : R/W**
	BT_VS_INV	7	Bt656 decoder vsync inv.	
	BT_HS_INV	6	Bt656 decoder hsync inv.	
	BT_VS_SEL[1:0]	5:4	0: Vsync is sync to hsync dely 1 line 1: Vsync is sync to hsync dely 2 lines 2: Vsync is sync to hsync dely 0 line 3: Vsync is decoded by bt656 decoder.	
	-	3:0	Reserved.	
06h (3818h)	**REG3818**	**7:0**	**Default : 0x3F**	**Access : R/W**
	-	7:6	Reserved.	
	SC_CIF_GATE_EN	5	SC cpuif odclk gate enable.	
	SC_TC_GATE_EN	4	SC tcon odclk gate enable.	
	SC_VIP_GATE_EN	3	SC vip fclk gate enable.	
	SC_IPM2_GATE_EN	2	SC ipm2 gate enable.	
	SC_IPM_GATE_EN	1	SC ipm gate enable.	
	SC_IPW_GATE_EN	0	SC ipw gate enable.	
07h (381Ch)	**REG381C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SC_FIODCLK_SW_RST	4	SC fiodclk software reset.	
	SC_IDCLK_SW_RST	3	SC idclk software reset.	
	SC_FCLK_SW_RST	2	SC fclk software reset.	
	SC_MCLK_SW_RST	1	SC mclk software reset.	

SC0 Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description	
	SC_ODCLK_SW_RST	0	SC odclk software reset.	
0Fh (383Ch)	**REG383C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	BT_DET_STATUS1	1	Bt656 mode detection status 1.	
	BT_DET_STATUS0	0	Bt656 mode detection status 0.	
10h (3840h)	**REG3840**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SC_INT_CLR[3:0]	3:0	Read: SC IRQ status. Write: SC IRQ clear.	
10h (3841h)	**REG3841**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	SC_INT_MASK[3:0]	3:0	SC IRQ mask.	
11h (3844h)	**REG3844**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SC_INT_FORCE[3:0]	3:0	SC IRQ force.	
12h (3848h)	**REG3848**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	IPM_INT_CLR[2:0]	2:0	Read: IPM IRQ status. Write: IPM IRQ clear.	
12h (3849h)	**REG3849**	**7:0**	**Default : 0x07**	**Access : R/W**
	-	7:3	Reserved.	
	IPM_INT_MASK[2:0]	2:0	IPM IRQ mask.	
13h (384Ch)	**REG384C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	IPM_INT_FORCE[2:0]	2:0	IPM IRQ force.	
14h (3850h)	**REG3850**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CIF_INT_CLR[1:0]	1:0	Read: CPU interface IRQ status. Write: CPU interface IRQ clear.	
14h (3851h)	**REG3851**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	CIF_INT_MASK[1:0]	1:0	CPU interface IRQ status.	
15h	**REG3854**	**7:0**	**Default : 0x00**	**Access : R/W**

SC0 Register (Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(3854h)	-	7:2	Reserved.	
	CIF_INT_FORCE[1:0]	1:0	CPU interface in.	
3Eh ~ 3Eh	**-**	**7:0**	**Default : -**	**Access : -**
(38F8h ~ 38FDh)	-	-	Reserved.	

CHIPTOP Register (Bank = 1E)

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
05h (3C14h)	**REG3C14**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_PASSWD0[7:0]	7:0	System configuration overwrite password.	
05h (3C15h)	**REG3C15**	**7:0**	**Default : 0x00**	**Access : R/W**
	EFUSE_PASSWD1[7:0]	7:0	System configuration overwrite password.	
06h (3C18h)	**REG3C18**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOP_SW_RST[7:0]	7:0	Global software reset password (set h79 for software reset).	
07h (3C1Ch)	**REG3C1C**	**7:0**	**Default : 0x55**	**Access : R/W**
	RESET_CPU0[7:0]	7:0	CPU suicide register (set 829f for CPU self reset).	
07h (3C1Dh)	**REG3C1D**	**7:0**	**Default : 0x22**	**Access : R/W**
	RESET_CPU0[15:8]	7:0	See description of '3C1Ch'.	
0Bh (3C2Ch)	**REG3C2C**	**7:0**	**Default : 0x00**	**Access : RO**
	TRAP_STS[7:0]	7:0	Trapping status.	
0Bh (3C2Dh)	**REG3C2D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	TRAP_STS[11:8]	3:0	See description of '3C2Ch'.	
0Ch (3C30h)	**REG3C30**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRAP_OV[7:0]	7:0	Trapping option overwrite.	
0Ch (3C31h)	**REG3C31**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	TRAP_OV[11:8]	3:0	See description of '3C30h'.	
0Dh (3C34h)	**REG3C34**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRAP_OVEN[7:0]	7:0	Trapping option overwrite enable.	
0Dh (3C35h)	**REG3C35**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	TRAP_OVEN[11:8]	3:0	See description of '3C34h'.	
10h (3C40h)	**REG3C40**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MCU_QUICK_RST	2	MCU quick reset.	
	MCU_RESET	1	MCU reset.	
	-	0	Reserved.	
11h	**REG3C44**	**7:0**	**Default : 0x00**	**Access : R/W**

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
(3C44h)	-	7:3	Reserved.	
	CLK_SIGP_NORM_MODE	2	CLK_SIGP_NORM_MODE.	
	-	1	Reserved.	
	SW_MCU_CLK	0	MCU clock select. 0: 24 MHz. 1: CLK_MCU.	
1Ah (3C68h)	**REG3C68**	**7:0**	**Default : 0x00**	**Access : R/W**
	CKG_FCIE_CKGEN[7:0]	7:0	Control FCIE clock gen, spread clock frequency.	
1Ah (3C69h)	**REG3C69**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	CKG_FCIE_CKGEN[10:8]	2:0	See description of '3C68h'.	
1Bh (3C6Dh)	**REG3C6D**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:6	Reserved.	
	CKG_ODCLK[5:0]	5:0	CLK_ODCLK clock control. [0]: Disable clock (1: Disable (default)). [1]: Invert clock. [3:2]: Select clock source. 00: LPLL clock. 01: LPLL clock div 2. 10: LPLL clock div 3. 11: Reserved. [4]: Useless.	
1Ch (3C70h)	**REG3C70**	**7:0**	**Default : 0x61**	**Access : R/W**
	-	7:6	Reserved.	
	CKG_IDCLK[5:0]	5:0	CLK_IDCLK clock control (CCIR clock). [0]: Disable clock (1: Disable (default)). [1]: Invert clock. [5:2]: useless.	
1Dh (3C74h)	**REG3C74**	**7:0**	**Default : 0x61**	**Access : R/W**
	CKG_FCLK[1:0]	7:6	CLK_FCLK clock control. [0]: Disable clock (1: Disable (default)). [1]: Invert clock. [3:2]: Select clock source. 00: 160 MHz. 01: 144 MHz. 10: 108 MHz. 11: 54 MHz.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
			[5:4]: useless.	
	-	5:0	Reserved.	
1Dh (3C75h)	**REG3C75**	**7:0**	**Default : 0x18**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_FCLK[5:2]	3:0	See description of '3C74h'.	
1Eh (3C79h)	**REG3C79**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CKG_ARM[4:0]	6:2	CLK_ARM clock control. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: CPUPLL clock. 01: 432 MHz. 10: 216 MHz. 11: 192 MHz. [4]: Useless.	
	CKG_AUX[1:0]	1:0	CLK_AUX clock control (27 MHz). [0]: Disable clock. [1]: Invert clock.	
22h (3C88h)	**REG3C88**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_ARM_CLK	7	ARM clock select. 0: 24 MHz. 1: CLK_ARM.	
	-	6	Reserved.	
	CKG_LCDC[1:0]	5:4	CLK_LCDC clock control (LPLL clock). [0]: Disable clock. [1]: Invert clock.	
	CKG_RTC[1:0]	3:2	CLK_RTC clock control (32 KHz). [0]: Disable clock. [1]: Invert clock.	
	CKG_BIST[1:0]	1:0	CLK_BIST clock select. 00: 173 MHz. 01: 108 MHz. 10: 54 MHz. 11: 24 MHz.	
22h (3C89h)	**REG3C89**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
	CKG_MCU[4:0]	4:0	CLK_MCU clock control. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: 173 MHz. 01: 144 MHz. 10: 108 MHz. 11: 86.5 MHz. [4]: Useless.	
23h (3C8Ch)	**REG3C8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_XO_GPS[1:0]	3:2	CLK_xo_gps clock setting. [0]: Disable clock. [1]: Invert clock.	
	CKG_HAYDN2[1:0]	1:0	CLK_HAYDN2 clock control (144 MHz). [0]: Disable clock. [1]: Invert clock.	
23h (3C8Dh)	**REG3C8D**	**7:0**	**Default : 0x00**	**Access : R/W**
	CKG_AFE_GPS[1:0]	7:6	CLK_AFE_GPS clock control (AFE clock). [0]: Disable clock. [1]: Invert clock.	
	CKG_MIU[5:0]	5:0	CLK_MIU clock control (DPLL clock). [0]: Disable clock. [1]: Invert clock. [5:2]: useless.	
24h (3C90h)	**REG3C90**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:6	Reserved.	
	CKG_JPD[5:0]	5:0	CLK_JPD clock control. [0]: Disable clock (1: Disable (default)). [1]: Invert clock. [3:2]: Select clock source. 00: 144 MHz. 01: 120 MHz. 10: 108 MHz. 11: 86.5 MHz. [5:4]: useless.	
25h	**REG3C94**	**7:0**	**Default : 0x00**	**Access : R/W**

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
(3C94h)	CKG_SDIO[1:0]	7:6	CLK_SDIO clock control. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: 300 KHz. 001: 5.4 MHz. 010: 24 MHz. 011: 32 MHz. 100: 40 MHz. 101: 48 MHz. 110: Spread clock from 216MHz. 111: Reserved. [5]: Useless.	
	CKG_FCIE[5:0]	5:0	CLK_FCIE clock control. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: 300 KHz. 001: 5.4 MHz. 010: 24 MHz. 011: 32 MHz. 100: 40 MHz. 101: 48 MHz. 110: Spread clock from 216MHz. 111: 80 MHz. [5]: Useless.	
25h (3C95h)	**REG3C95**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_SDIO[5:2]	3:0	See description of '3C94h'.	
26h (3C98h)	**REG3C98**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7:3	Reserved.	
	CKG_TCK_R2[2:0]	2:0	CLK_TCK_R2 clock control. [0]: Disable clock. [1]: Invert clock. [2]: Don't use.	
27h (3C9Ch)	**REG3C9C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CKG_R2[2:0]	7:5	CLK_R2 clock control. [0]: Disable clock.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description
			[1]: Invert clock. [4:2]: Select clock source. 000: CLK_ARM div #. 001: 173 MHz. 010: 144 MHz. 011: 108 MHz. 100: 86.5 MHz. 101: 72 MHz. 110: 60 MHz. 111: 40 MHz.
	CKG_MPIF[4:0]	4:0	CLK_MPIF clock control. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: 120 MHz. 001: 108 MHz. 010: 86.5 MHz. 011: 72 MHz. 100: 60 MHz. 101: 40 MHz. 110: 24 MHz. 111: 12 MHz.
27h (3C9Dh)	**REG3C9D**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:2	Reserved.
	CKG_R2[4:3]	1:0	See description of '3C9Ch'.
28h (3CA0h)	**REG3CA0**	**7:0**	**Default : 0x01** **Access : R/W**
	CKG_FIODCLK[2:0]	7:5	CLK_FIODCLK clock control. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: CLK_FCLK. 01: CLK_IDCLK. 10: CLK_LCDC. 11: Reserved.
	CKG_GE[4:0]	4:0	CLK_GE clock control. [0]: Disable clock (1: Disable (default)). [1]: Invert clock. [3:2]: Select clock source. 00: 173 MHz.

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
			01: 144 MHz. 10: 108 MHz. 11: 86.5 MHz. [4]: Useless.	
28h (3CA1h)	**REG3CA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	CKG_SPI[3:0]	7:4	CLK_SPI clock control. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: 108 MHz. 01: 86.5 MHz. 10: 54 MHz. 11: 48 MHz.	
	CKG_MIIC[2:0]	3:1	CLK_MIIC clock control. [0]: Disable clock. [1]: Invert clock. [2]: Select clock source. 0: 24 MHz. 1: 12 MHz.	
	CKG_FIODCLK[3]	0	See description of '3CA0h'.	
29h (3CA4h)	**REG3CA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_SIGP[3:0]	3:0	CLK_SIGP clock control. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: 48 MHz. 01: 40 MHz. 10: 36 MHz. 11: 2 KHz.	
29h (3CA5h)	**REG3CA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	CKG_RFSPI[2:0]	7:5	CLK_RFSPI clock control. [0]: Disable clock. [1]: Invert clock. [2]: Select clock source. 0: 24 MHz. 1: 12 MHz.	
	CKG_TCK_ARM[2:0]	4:2	CLK_TCK_ARM clock control.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
			[0]: Disable clock. [1]: Invert clock. [2]: Don't use.	
	SW_SPI_CLK	1	SPI clock select. 0: 24 MHz. 1: CLK_SPI.	
	-	0	Reserved.	
2Ah (3CA8h)	**REG3CA8**	**7:0**	**Default : 0x89**	**Access : R/W**
	-	7	Reserved.	
	CKG_GOPG0[3:0]	6:3	CLK_GOPG0 clock control. [0]: Disable clock (1: Disable (default)). [1]: Invert clock. [3:2]: Select clock source. 00: Clk_odclk2 (odclk). 01: Clk_op_p. 10: Clk_op_p_gate.	
	-	2:0	Reserved.	
2Ah (3CA9h)	**REG3CA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SW_UART2_CLK	5	UART2 clock select. 0: 24 MHZ. 1: CLK_UART2.	
	SW_UART1_CLK	4	UART1 clock select. 0: 24 MHZ. 1: CLK_UART1.	
	SW_UART0_CLK	3	UART0 clock select. 0: 24 MHZ. 1: CLK_UART0.	
	-	2:0	Reserved.	
2Bh (3CACh)	**REG3CAC**	**7:0**	**Default : 0x21**	**Access : R/W**
	CKG_UART1[2:0]	7:5	CLK_UART1 clock control. [0]: Disable clock (1: Disable (default)). [1]: Invert clock. [3:2]: Select clock source. 00: 108 MHz. 01: 86.5 MHz. 10: 54 MHz.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description
			11: 48 MHz. [4]: Uselsess.
	CKG_UART0[4:0]	4:0	CLK_UART0 clock control. [0]: Disable clock (1: Disable (default)). [1]: Invert clock. [3:2]: Select clock source. 00: 108 MHz. 01: 86.5 MHz. 10: 54 MHz. 11: 48 MHz. [4]: Useless.
2Bh (3CADh)	**REG3CAD**	**7:0**	**Default : 0x04** **Access : R/W**
	-	7	Reserved.
	CKG_UART2[4:0]	6:2	CLK_UART2 clock control. [0]: Disable clock (1: Disable (default)). [1]: Invert clock. [3:2]: Select clock source. 00: 192 MHz. 01: 173 MHz. 10: 144 MHz. 11: 108 MHz. [4]: Useless.
	CKG_UART1[4:3]	1:0	See description of '3CACh'.
2Ch (3CB0h)	**REG3CB0**	**7:0**	**Default : 0x21** **Access : R/W**
	CKG_G3D_PLT[2:0]	7:5	CLK_G3D_PLT clock control. [0]: Disable clock (1: Disable (default)). [1]: Invert clock. [2]: Select clock source. 0: CLK_G3D. 1: CLK_MIU. [3]: Useless.
	CKG_G3D[4:0]	4:0	CLK_G3D clock control. [0]: Disable clock (1: Disable (default)). [1]: Invert clock. [3:2]: Select clock source. 00: 108 MHz. 01: 86.5 MHz. 10: 54 MHz.

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
			11: 48 MHz. [4]: Useless.	
2Ch (3CB1h)	**REG3CB1**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_G3D_GBL[3:0]	4:1	CLK_G3D_GBL clock control. [0]: Disable clock (1: Disable (default)). [1]: Invert clock. [3:2]: Select clock source. 0: CLK_G3D. 1: CLK_RIU. [3]: Useless.	
	CKG_G3D_PLT[3]	0	See description of '3CB0h'.	
2Dh (3CB4h)	**REG3CB4**	**7:0**	**Default : 0x09**	**Access : R/W**
	CKG_SIGP_DMA_RD[1:0]	7:6	CLK_SIGP_DMA_RD clock control. [0]: Disable clock. [1]: Invert clock. [2]: Select clock source. 0: CLK_SIGP_RAM. 1: CLK_SIGP.	
	-	5:0	Reserved.	
2Dh (3CB5h)	**REG3CB5**	**7:0**	**Default : 0x00**	**Access : R/W**
	CKG_SIGP_RAM[3:0]	7:4	CLK_SIGP_RAM clock control. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: CLK_ARM div #. 01: CLK_R2. 10: 173 MHz. 11: 108 MHz.	
	CKG_SIGP_DMA_WD[2:0]	3:1	CLK_SIGP_DMA_WD clock control. [0]: Disable clock. [1]: Invert clock. [2]: Select clock source. 0: CLK_SIGP_RAM. 1: CLK_SIGP.	
	CKG_SIGP_DMA_RD[2]	0	See description of '3CB4h'.	
2Eh	**REG3CB8**	**7:0**	**Default : 0x00**	**Access : R/W**

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
(3CB8h)	MCLK_MPIF_EN	7	MPIF MIU clock enable (0: enable; 1: disable).	
	MCLK_GE_EN	6	GE MIU clock enable (0: enable; 1: disable).	
	MCLK_FCIE_EN	5	FCIE MIU reader clock enable (0: enable; 1: disable).	
	MCLK_SDIO_EN	4	SDIO MIU clock enable (0: enable; 1: disable).	
	MCLK_OTG20_EN	3	OTG20 MIU clock enable (0: enable; 1: disable).	
	MCLK_SC_EN	2	SC MIU clock enable (0: enable; 1: disable).	
	MCLK_GOP_EN	1	GOP MIU clock enable (0: enable; 1: disable).	
	MCLK_JPD_EN	0	JPD MIU clock enable (0: enable; 1: disable).	
2Eh (3CB9h)	**REG3CB9**	**7:0**	**Default : 0x00**	**Access : R/W**
	MCLK_HAYDN2_EN	7	HAYDN2 clock enable (0: enable; 1: disable).	
	-	6:3	Reserved.	
	MCLK_PIU_EN	2	PIU MIU clock enable (0: enable; 1: disable).	
	SW_R2_CLK	1	R2 clock select. 0: 24 MHZ. 1: CLK_R2.	
	MCLK_G3D_EN	0	G3D MIU clock enable (0: enable; 1: disable).	
2Fh (3CBCh)	**REG3CBC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CKG_LPLL_SYN[1:0]	5:4	LPLL synthesizer clock selector (for DISP).	
	CKG_UPLL_SYN[1:0]	3:2	UPLL synthesizer clock selector (for UTMI).	
	CKG_DPLL_SYN[1:0]	1:0	DPLL synthesizer clock selector (for DDR).	
30h (3CC0h)	**REG3CC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	CKG_SDIO_CKGEN[7:0]	7:0	Control SDIO clock gen, spread clock frequency.	
30h (3CC1h)	**REG3CC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	CKG_SDIO_CKGEN[10:8]	2:0	See description of '3CC0h'.	
31h (3CC4h)	**REG3CC4**	**7:0**	**Default : 0xB6**	**Access : R/W**
	SD22_PE	7	Pull enable of PAD_F_CEZ.	
	SD22_DRV	6	Driving strength of PAD_F_CEZ.	
	SD21_PS	5	Pull select of PAD_F_CE1Z (0: down, 1: up).	
	SD21_PE	4	Pull enable of PAD_F_CE1Z.	
	SD21_DRV	3	Driving strength of PAD_F_CE1Z.	
	SD20_PS	2	Pull select of PAD_F_ALE (0: down, 1: up).	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
	SD20_PE	1	Pull enable of PAD_F_ALE.	
	SD20_DRV	0	Driving strength of PAD_F_ALE.	
31h (3CC5h)	**REG3CC5**	**7:0**	**Default : 0x65**	**Access : R/W**
	-	7	Reserved.	
	SD24_PS	6	Pull select of PAD_F_DA0 (0: down, 1: up).	
	SD24_PE	5	Pull enable of PAD_F_DA0.	
	SD24_DRV	4	Driving strength of PAD_F_DA0.	
	SD23_PS	3	Pull select of PAD_F_CLE (0: down, 1: up).	
	SD23_PE	2	Pull enable of PAD_F_CLE.	
	SD23_DRV	1	Driving strength of PAD_F_CLE.	
	SD22_PS	0	Pull select of PAD_F_CEZ (0: down, 1: up).	
32h (3CC8h)	**REG3CC8**	**7:0**	**Default : 0xB6**	**Access : R/W**
	SD27_PE	7	Pull enable of PAD_F_DA3.	
	SD27_DRV	6	Driving strength of PAD_F_DA3.	
	SD26_PS	5	Pull select of PAD_F_DA2 (0: down, 1: up).	
	SD26_PE	4	Pull enable of PAD_F_DA2.	
	SD26_DRV	3	Driving strength of PAD_F_DA2.	
	SD25_PS	2	Pull select of PAD_F_DA1 (0: down, 1: up).	
	SD25_PE	1	Pull enable of PAD_F_DA1.	
	SD25_DRV	0	Driving strength of PAD_F_DA1.	
32h (3CC9h)	**REG3CC9**	**7:0**	**Default : 0x6D**	**Access : R/W**
	-	7	Reserved.	
	SD29_PS	6	Pull select of PAD_F_DA5 (0: down, 1: up).	
	SD29_PE	5	Pull enable of PAD_F_DA5.	
	SD29_DRV	4	Driving strength of PAD_F_DA5.	
	SD28_PS	3	Pull select of PAD_F_DA4 (0: down, 1: up).	
	SD28_PE	2	Pull enable of PAD_F_DA4.	
	SD28_DRV	1	Driving strength of PAD_F_DA4.	
	SD27_PS	0	Pull select of PAD_F_DA3 (0: down, 1: up).	
33h (3CCCh)	**REG3CCC**	**7:0**	**Default : 0xB6**	**Access : R/W**
	SD2C_PE	7	Pull enable of PAD_F_RBZ.	
	SD2C_DRV	6	Driving strength of PAD_F_RBZ.	
	SD2B_PS	5	Pull select of PAD_F_DA7 (0: down, 1: up).	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
	SD2B_PE	4	Pull enable of PAD_F_DA7.	
	SD2B_DRV	3	Driving strength of PAD_F_DA7.	
	SD2A_PS	2	Pull select of PAD_F_DA6 (0: down, 1: up).	
	SD2A_PE	1	Pull enable of PAD_F_DA6.	
	SD2A_DRV	0	Driving strength of PAD_F_DA6.	
33h (3CCDh)	**REG3CCD**	**7:0**	**Default : 0x65**	**Access : R/W**
	-	7	Reserved.	
	SD2E_PS	6	Pull select of PAD_F_WEZ (0: down, 1: up).	
	SD2E_PE	5	Pull enable of PAD_F_WEZ.	
	SD2E_DRV	4	Driving strength of PAD_F_WEZ.	
	SD2D_PS	3	Pull select of PAD_F_REZ (0: down, 1: up).	
	SD2D_PE	2	Pull enable of PAD_F_REZ.	
	SD2D_DRV	1	Driving strength of PAD_F_REZ.	
	SD2C_PS	0	Pull select of PAD_F_RBZ (0: down, 1: up).	
34h (3CD0h)	**REG3CD0**	**7:0**	**Default : 0xB6**	**Access : R/W**
	SD31_PE	7	Pull enable of PAD_GPIO_G1.	
	SD31_DRV	6	Driving strength of PAD_GPIO_G17.	
	SD30_PS	5	Pull select of PAD_GPIO_G1 (0: down, 1: up).	
	SD30_PE	4	Pull enable of PAD_GPIO_G1.	
	SD30_DRV	3	Driving strength of PAD_GPIO_G16.	
	SD2F_PS	2	Pull select of PAD_F_WPZ (0: down, 1: up).	
	SD2F_PE	1	Pull enable of PAD_F_WPZ.	
	SD2F_DRV	0	Driving strength of PAD_F_WPZ.	
34h (3CD1h)	**REG3CD1**	**7:0**	**Default : 0x6D**	**Access : R/W**
	-	7	Reserved.	
	SD33_PS	6	Pull select of PAD_GPIO_G1 (0: down, 1: up).	
	SD33_PE	5	Pull enable of PAD_GPIO_G1.	
	SD33_DRV	4	Driving strength of PAD_GPIO_G19.	
	SD32_PS	3	Pull select of PAD_GPIO_G1 (0: down, 1: up).	
	SD32_PE	2	Pull enable of PAD_GPIO_G1.	
	SD32_DRV	1	Driving strength of PAD_GPIO_G18.	
	SD31_PS	0	Pull select of PAD_GPIO_G1 (0: down, 1: up).	
35h	**REG3CD4**	**7:0**	**Default : 0xB6**	**Access : R/W**

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description
(3CD4h)	SD36_PE	7	Pull enable of PAD_SPI_CK.
	SD36_DRV	6	Driving strength of PAD_SPI_CK.
	SD35_PS	5	Pull select of PAD_GPIO_G2 (0: down, 1: up).
	SD35_PE	4	Pull enable of PAD_GPIO_G2.
	SD35_DRV	3	Driving strength of PAD_GPIO_G21.
	SD34_PS	2	Pull select of PAD_GPIO_G2 (0: down, 1: up).
	SD34_PE	1	Pull enable of PAD_GPIO_G2.
	SD34_DRV	0	Driving strength of PAD_GPIO_G20.
35h (3CD5h)	**REG3CD5**	**7:0**	**Default : 0x6D** **Access : R/W**
	-	7	Reserved.
	SD38_PS	6	Pull select of PAD_SPI_CS1 (0: down, 1: up).
	SD38_PE	5	Pull enable of PAD_SPI_CS1.
	SD38_DRV	4	Driving strength of PAD_SPI_CS1Z.
	SD37_PS	3	Pull select of PAD_SPI_CS0 (0: down, 1: up).
	SD37_PE	2	Pull enable of PAD_SPI_CS0.
	SD37_DRV	1	Driving strength of PAD_SPI_CS0Z.
	SD36_PS	0	Pull select of PAD_SPI_CK (0: down, 1: up).
36h (3CD8h)	**REG3CD8**	**7:0**	**Default : 0xB6** **Access : R/W**
	SD10_PE	7	Pull enable of PAD_SD_CLK.
	SD10_DRV	6	Driving strength of PAD_SD_CLK.
	SD3A_PS	5	Pull select of PAD_SPI_DO (0: down, 1: up).
	SD3A_PE	4	Pull enable of PAD_SPI_DO.
	SD3A_DRV	3	Driving strength of PAD_SPI_DO.
	SD39_PS	2	Pull select of PAD_SPI_DI (0: down, 1: up).
	SD39_PE	1	Pull enable of PAD_SPI_DI.
	SD39_DRV	0	Driving strength of PAD_SPI_DI.
36h (3CD9h)	**REG3CD9**	**7:0**	**Default : 0x6C** **Access : R/W**
	-	7	Reserved.
	SD12_PS	6	Pull select of PAD_SD_D0 (0: down, 1: up).
	SD12_PE	5	Pull enable of PAD_SD_D0.
	SD12_DRV	4	Driving strength of PAD_SD_D0.
	SD11_PS	3	Pull select of PAD_SD_CMD (0: down, 1: up).
	SD11_PE	2	Pull enable of PAD_SD_CMD.

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
	SD11_DRV	1	Driving strength of PAD_SD_CMD.	
	SD10_PS	0	Pull select of PAD_SD_CLK (0: down, 1: up).	
37h (3CDCh)	**REG3CDC**	**7:0**	**Default : 0xB6**	**Access : R/W**
	SD15_PE	7	Pull enable of PAD_SD_D3.	
	SD15_DRV	6	Driving strength of PAD_SD_D3.	
	SD14_PS	5	Pull select of PAD_SD_D2 (0: down, 1: up).	
	SD14_PE	4	Pull enable of PAD_SD_D2.	
	SD14_DRV	3	Driving strength of PAD_SD_D2.	
	SD13_PS	2	Pull select of PAD_SD_D1 (0: down, 1: up).	
	SD13_PE	1	Pull enable of PAD_SD_D1.	
	SD13_DRV	0	Driving strength of PAD_SD_D1.	
37h (3CDDh)	**REG3CDD**	**7:0**	**Default : 0x6D**	**Access : R/W**
	-	7	Reserved.	
	SD17_PS	6	Pull select of PAD_SD_D5 (0: down, 1: up).	
	SD17_PE	5	Pull enable of PAD_SD_D5.	
	SD17_DRV	4	Driving strength of PAD_SD_D5.	
	SD16_PS	3	Pull select of PAD_SD_D4 (0: down, 1: up).	
	SD16_PE	2	Pull enable of PAD_SD_D4.	
	SD16_DRV	1	Driving strength of PAD_SD_D4.	
	SD15_PS	0	Pull select of PAD_SD_D3 (0: down, 1: up).	
38h (3CE0h)	**REG3CE0**	**7:0**	**Default : 0xB6**	**Access : R/W**
	SD1A_PE	7	Pull enable of PAD_SD_WPZ.	
	SD1A_DRV	6	Driving strength of PAD_SD_WPZ.	
	SD19_PS	5	Pull select of PAD_SD_D7 (0: down, 1: up).	
	SD19_PE	4	Pull enable of PAD_SD_D7.	
	SD19_DRV	3	Driving strength of PAD_SD_D7.	
	SD18_PS	2	Pull select of PAD_SD_D6 (0: down, 1: up).	
	SD18_PE	1	Pull enable of PAD_SD_D6.	
	SD18_DRV	0	Driving strength of PAD_SD_D6.	
38h (3CE1h)	**REG3CE1**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	SD1A_PS	0	Pull select of PAD_SD_WPZ (0: down, 1: up).	
40h	**REG3D00**	**7:0**	**Default : 0x00**	**Access : RO**

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
(3D00h)	-	7:6	Reserved.	
	GPIO_UART_IN[5:0]	5:0	Input of UART GPIO.	
40h (3D01h)	**REG3D01**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	GPIO_UART_OUT[5:0]	5:0	Output of UART GPIO.	
41h (3D04h)	**REG3D04**	**7:0**	**Default : 0x3F**	**Access : R/W**
	-	7:6	Reserved.	
	GPIO_UART_OEN[5:0]	5:0	Output enable of UART GPIO (0: output, 1: input).	
41h (3D05h)	**REG3D05**	**7:0**	**Default : 0x30**	**Access : RO, R/W**
	-	7:6	Reserved.	
	GPIO_I2CM_OEN[1:0]	5:4	Output enable of I2CM GPIO (0: output, 1: input).	
	GPIO_I2CM_OUT[1:0]	3:2	Output of I2CM GPIO.	
	GPIO_I2CM_IN[1:0]	1:0	Input of I2CM GPIO.	
42h (3D08h)	**REG3D08**	**7:0**	**Default : 0x00**	**Access : RO**
	GPIO_CCIR_IN[7:0]	7:0	Input of CCIR GPIO.	
42h (3D09h)	**REG3D09**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	GPIO_CCIR_IN[8]	0	See description of '3D08h'.	
43h (3D0Ch)	**REG3D0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIO_CCIR_OUT[7:0]	7:0	Output of CCIR GPIO.	
43h (3D0Dh)	**REG3D0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	GPIO_CCIR_OUT[8]	0	See description of '3D0Ch'.	
44h (3D10h)	**REG3D10**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GPIO_CCIR_OEN[7:0]	7:0	Output enable of CCIR GPIO (0: output, 1: input).	
44h (3D11h)	**REG3D11**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	GPIO_CCIR_OEN[8]	0	See description of '3D10h'.	
45h (3D14h)	**REG3D14**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GPIO_IIS_OUT[3:0]	7:4	Output of IIS GPIO.	
	GPIO_IIS_IN[3:0]	3:0	Input of IIS GPIO.	
45h (3D15h)	**REG3D15**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
	GPIO_IIS_OEN[3:0]	3:0	Output enable of IIS GPIO (0: output, 1: input).	
46h (3D18h)	**REG3D18**	**7:0**	**Default : 0x00**	**Access : RO**
	GPIO_MPIF_IN[7:0]	7:0	Input of MPIF GPIO.	
46h (3D19h)	**REG3D19**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIO_MPIF_OUT[7:0]	7:0	Output of MPIF GPIO.	
47h (3D1Ch)	**REG3D1C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GPIO_MPIF_OEN[7:0]	7:0	Output enable of MPIF GPIO (0: output, 1: input).	
48h (3D20h)	**REG3D20**	**7:0**	**Default : 0x00**	**Access : RO**
	GPIO_SD_IN[7:0]	7:0	Input of SD GPIO.	
48h (3D21h)	**REG3D21**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	GPIO_SD_IN[10:8]	2:0	See description of '3D20h'.	
49h (3D24h)	**REG3D24**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIO_SD_OUT[7:0]	7:0	Output of SD GPIO.	
49h (3D25h)	**REG3D25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GPIO_SD_OUT[10:8]	2:0	See description of '3D24h'.	
4Ah (3D28h)	**REG3D28**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GPIO_SD_OEN[7:0]	7:0	Output enable of SD GPIO (0: output, 1: input).	
4Ah (3D29h)	**REG3D29**	**7:0**	**Default : 0x07**	**Access : R/W**
	-	7:3	Reserved.	
	GPIO_SD_OEN[10:8]	2:0	See description of '3D28h'.	
4Bh (3D2Ch)	**REG3D2C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	GPIO_GPS_IN[5:0]	5:0	Input of GPS GPIO.	
4Bh (3D2Dh)	**REG3D2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	GPIO_GPS_OUT[5:0]	5:0	Output of GPS GPIO.	
4Ch (3D30h)	**REG3D30**	**7:0**	**Default : 0x3F**	**Access : R/W**
	-	7:6	Reserved.	
	GPIO_GPS_OEN[5:0]	5:0	Output enable of GPS GPIO (0: output, 1: input).	
4Dh (3D34h)	**REG3D34**	**7:0**	**Default : 0x00**	**Access : RO**
	GPIO_NF_IN[7:0]	7:0	Input of NF GPIO.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
4Dh (3D35h)	**REG3D35**	**7:0**	**Default : 0x00**	**Access : RO**
	GPIO_NF_IN[15:8]	7:0	See description of '3D34h'.	
4Eh (3D38h)	**REG3D38**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIO_NF_OUT[7:0]	7:0	Output of NF GPIO.	
4Eh (3D39h)	**REG3D39**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIO_NF_OUT[15:8]	7:0	See description of '3D38h'.	
4Fh (3D3Ch)	**REG3D3C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GPIO_NF_OEN[7:0]	7:0	Output enable of NF GPIO (0: output, 1: input).	
4Fh (3D3Dh)	**REG3D3D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GPIO_NF_OEN[15:8]	7:0	See description of '3D3Ch'.	
50h (3D40h)	**REG3D40**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GPIO_SPI_OUT[2:0]	7:5	Output of SPI GPIO.	
	GPIO_SPI_IN[4:0]	4:0	Input of SPI GPIO.	
50h (3D41h)	**REG3D41**	**7:0**	**Default : 0xFC**	**Access : R/W**
	ALLPAD_IN	7	1: Set all pads.	
	GPIO_SPI_OEN[4:0]	6:2	Output enable of SPI GPIO (0: output, 1: input).	
	GPIO_SPI_OUT[4:3]	1:0	See description of '3D40h'.	
51h (3D44h)	**REG3D44**	**7:0**	**Default : 0x00**	**Access : RO**
	GPIO_G_IN[7:0]	7:0	Input of dedicated GPIO.	
51h (3D45h)	**REG3D45**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	GPIO_G_IN[12:8]	4:0	See description of '3D44h'.	
52h (3D48h)	**REG3D48**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIO_G_OUT[7:0]	7:0	Output of dedicated GPIO.	
52h (3D49h)	**REG3D49**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	GPIO_G_OUT[12:8]	4:0	See description of '3D48h'.	
53h (3D4Ch)	**REG3D4C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GPIO_G_OEN[7:0]	7:0	Output enable of dedicated GPIO (0: output, 1: input).	
53h (3D4Dh)	**REG3D4D**	**7:0**	**Default : 0x1F**	**Access : R/W**
	-	7:5	Reserved.	
	GPIO_G_OEN[12:8]	4:0	See description of '3D4Ch'.	
59h	**REG3D64**	**7:0**	**Default : 0x01**	**Access : R/W**

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
(3D64h)	NF_MODE[0]	7	Refer to pad mux table.	
	-	6:0	Reserved.	
59h (3D65h)	**REG3D65**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	NF_MODE[2:1]	1:0	See description of '3D64h'.	
5Ah (3D68h)	**REG3D68**	**7:0**	**Default : 0x00**	**Access : RO**
	GPIO_TTL_IN[7:0]	7:0	Input of TTL GPIO.	
5Ah (3D69h)	**REG3D69**	**7:0**	**Default : 0x00**	**Access : RO**
	GPIO_TTL_IN[15:8]	7:0	See description of '3D68h'.	
5Bh (3D6Ch)	**REG3D6C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	GPIO_TTL_IN[16]	0	See description of '3D68h'.	
5Ch (3D70h)	**REG3D70**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIO_TTL_OUT[7:0]	7:0	Output of TTL GPIO.	
5Ch (3D71h)	**REG3D71**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIO_TTL_OUT[15:8]	7:0	See description of '3D70h'.	
5Dh (3D74h)	**REG3D74**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	GPIO_TTL_OUT[16]	0	See description of '3D70h'.	
5Eh (3D78h)	**REG3D78**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GPIO_TTL_OEN[7:0]	7:0	Output enable of TTL GPIO (0: output, 1: input).	
5Eh (3D79h)	**REG3D79**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GPIO_TTL_OEN[15:8]	7:0	See description of '3D78h'.	
5Fh (3D7Ch)	**REG3D7C**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	GPIO_TTL_OEN[16]	0	See description of '3D78h'.	
62h (3D89h)	**REG3D89**	**7:0**	**Default : 0x00**	**Access : R/W**
	SD3_MODE[1:0]	7:6	Refer to pad mux table.	
	R2JTAG_MODE[1:0]	5:4	Refer to pad mux table.	
	I8M6_MODE	3	Refer to pad mux table.	
	I80HRDY_MODE	2	Refer to pad mux table.	
	GPSPWM_MODE[1:0]	1:0	Refer to pad mux table.	
64h	**REG3D90**	**7:0**	**Default : 0x00**	**Access : R/W**

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
(3D90h)	SDIO_MODE[0]	7	Refer to pad mux table.	
	-	6:5	Reserved.	
	MPIF_MODE	4	Refer to pad mux table.	
	GPSBB_MODE	3	Refer to pad mux table.	
	CTSRTS_MODE	2	Refer to pad mux table.	
	CCIR_MODE	1	Refer to pad mux table.	
	-	0	Reserved.	
64h (3D91h)	**REG3D91**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	UART2_MODE	6	Refer to pad mux table.	
	UART1_MODE[1:0]	5:4	Refer to pad mux table.	
	UART0_MODE	3	Refer to pad mux table.	
	TEST_IN_MODE	2	Refer to pad mux table.	
	-	1	Reserved.	
	SDIO_MODE[1]	0	See description of '3D90h'.	
65h (3D94h)	**REG3D94**	**7:0**	**Default : 0x00**	**Access : RO**
	CHIP_CONFIG_STAT[7:0]	7:0	CHIP_CONFIG raw status.	
65h (3D95h)	**REG3D95**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	CHIP_CONFIG_STAT[11:8]	3:0	See description of '3D94h'.	
66h (3D98h)	**REG3D98**	**7:0**	**Default : 0x00**	**Access : RO**
	DEVICE_ID[7:0]	7:0	Device ID.	
66h (3D99h)	**REG3D99**	**7:0**	**Default : 0x00**	**Access : RO**
	DEVICE_ID[15:8]	7:0	See description of '3D98h'.	
67h (3D9Ch)	**REG3D9C**	**7:0**	**Default : 0x00**	**Access : RO**
	CHIP_VERSION[7:0]	7:0	Chip version.	
67h (3D9Dh)	**REG3D9D**	**7:0**	**Default : 0x00**	**Access : RO**
	CHIP_REVISION[7:0]	7:0	Chip revision.	
6Bh (3DACh)	**REG3DAC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_SAR[4:0]	4:0	CLK_SAR clock control. [0]: Disable clock. [1]: Invert clock.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
			[4:2]: Select clock source. 000: 2.4 MHz. 001: 1.2 MHz. 010: 600 KHz. 011: 300 KHz. 100: 150 KHz. others: Reserved.	
6Fh (3DBCh)	**REG3DBC**	**7:0**	**Default : 0x2D**	**Access : R/W**
	CKG_PMU_CKGEN[7:0]	7:0	Control PMU clock gen, spread clock frequency.	
6Fh (3DBDh)	**REG3DBD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CKG_PMU[2:0]	5:3	CLK_PMU clock control (spread clock from 216 MHz). [0]: Disable clock. [1]: Invert clock. [2]: Useless.	
	CKG_PMU_CKGEN[10:8]	2:0	See description of '3DBCh'.	
70h (3DC1h)	**REG3DC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	ROSC_OUT_SEL[1:0]	1:0	Ring OSC output select. 00: Select delay chain 0. 01: Select delay chain 1. 10: Select delay chain 2. 11: Select delay chain 3.	
75h (3DD4h)	**REG3DD4**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_RB	7	Setting for the data arrangement on test bus.	
	TEST_GB	6	Setting for the data arrangement on test bus.	
	TEST_RG	5	Setting for the data arrangement on test bus.	
	-	4	Reserved.	
	SWAPTEST12BIT	3	Swap MSB 12bits with LSB 12bits of test bus.	
	CLK_OUT_SEL[2:0]	2:0	Select TEST_CLK_OUT source. 000: TEST_CLK_OUT= TEST_BUS_GB[0]. 001: TEST_CLK_OUT= TEST_BUS_GB[1]. 010: TEST_CLK_OUT= TEST_BUS_GB[2]. 011: TEST_CLK_OUT= TEST_BUS_GB[3]. 100: TEST_CLK_OUT= TEST_BUS_GB[4]. 101: TEST_CLK_OUT= TEST_BUS_GB[5]. 110: TEST_CLK_OUT= TEST_BUS_GB[6].	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
			111: TEST_CLK_OUT= TEST_BUS_GB[7].	
75h (3DD5h)	**REG3DD5**	**7:0**	**Default : 0x00**	**Access : R/W**
	ROSC_IN_SEL	7	Select the input source of ring oscillator in CHIP_CONF. 1: Close-loop (enable ring oscillator). 0: Open-loop (input from external digital input).	
	TESTBUS_EN	6	Enable test bus output.	
	TESTCLK_MODE	5	TESTCLK_MODE used in TEST_CTRL.	
	-	4:2	Reserved.	
	SEL_CLK_TEST_OUT[1:0]	1:0	Select CLK_TEST_OUT. 2'b00: select CLK_TEST_OUT[47:0]. 2'b01: select CLK_TEST_OUT[95:48]. 2'b10: select CLK_TEST_OUT[143:96]. 2'b11: reserved.	
76h (3DD8h)	**REG3DD8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SINGLE_CLK_OUT_SEL[2:0]	2:0	Select single CLK_OUT. 001: TEST_BUS[11] = TEST_CLK_OUT_d2. TEST_BUS[10] = TEST_CLK_OUT. 010: TEST_BUS[11] = TEST_CLK_OUT_d2. TEST_BUS[10] = TEST_CLK_OUT_d4. 011: TEST_BUS[11] = TEST_CLK_OUT_d2. TEST_BUS[10] = TEST_CLK_OUT_d8. 100: TEST_BUS[11] = TEST_CLK_OUT_d2. TEST_BUS[10] = TEST_CLK_OUT_d16. Others: No TEST_CLK_OUT.	
77h (3DDCh)	**REG3DDC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	PIF_DRV	6	Driving strength of PAD_PIF.	
	TEST_BUS24B_SEL[5:0]	5:0	Select TEST_BUS[23:0] source. 6'd1: test_bus_case = clk_test_out[23:0]. 6'd2: test_bus_case = clk_test_out[47:24]. 6'd3: test_bus_case = {rosc_out,clk_test_out[70:48]}. 6'd4: test_bus_case = lpll_test_out. 6'd5: test_bus_case = aux_test_out. 6'd6: test_bus_case = sar_test_out. 6'd7: test_bus_case = pm_test_out. 6'd8: test_bus_case = rtc_test_out.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
			6'd9: test_bus_case = armbdg_test_out. 6'd10: test_bus_case = r2_test_out. 6'd11: test_bus_case = gps_test_out. 6'd12: test_bus_case = miu_test_out. 6'd13: test_bus_case = audio_test_out. 6'd14: test_bus_case = sc_test_out. 6'd15: test_bus_case = gop_test_out. 6'd16: test_bus_case = g3d_test_out. 6'd17: test_bus_case = ge_test_out. 6'd18: test_bus_case = jpd_test_out. 6'd19: test_bus_case = fcie_test_out. 6'd20: test_bus_case = sdio_test_out. 6'd21: test_bus_case = mpif_test_out. 6'd22: test_bus_case = uhc_test_out. 6'd23: test_bus_case = otg_test_out. 6'd24: test_bus_case = utmi_test_out. 6'd25: test_bus_case = piu_test_out. 6'd26: test_bus_case = bist_test_out[23:0]. 6'd27: test_bus_case = bist_test_out[47:24]. 6'd28: test_bus_case = {8'h0, bist_test_out[63:48]}. Default: Test_bus_case = 24'h0.	
78h (3DE0h)	**REG3DE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MIU_PDALL	6	Test MIU power down.	
	TEST_PADL	5	Test pad output low.	
	TEST_PADH	4	Test pad output high.	
	-	3:0	Reserved.	
78h (3DE1h)	**REG3DE1**	**7:0**	**Default : 0x00**	**Access : R/W**
	TTLGPIO6_MODE	7	Refer to pad mux table.	
	TTLGPIO5_MODE	6	Refer to pad mux table.	
	-	5	Reserved.	
	TTLGPIO4_MODE	4	Refer to pad mux table.	
	-	3:0	Reserved.	
7Bh (3DECh)	**REG3DEC**	**7:0**	**Default : 0x00**	**Access : R/W**
	DTON_MODE[2:0]	7:5	Refer to pad mux table.	
	-	4:0	Reserved.	
7Bh	**REG3DED**	**7:0**	**Default : 0x00**	**Access : R/W**

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
(3DEDh)	-	7:2	Reserved.	
	DTON2_MODE[1:0]	1:0	Refer to pad mux table.	
7Dh (3DF4h)	**REG3DF4**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXTI2S_MODE[1:0]	7:6	Refer to pad mux table.	
	MCLK_R2_EN	5	R2 MIU clock enable (0: enable; 1: disable).	
	-	4:0	Reserved.	
7Dh (3DF5h)	**REG3DF5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	BTI2S_MODE	6	Refer to pad mux table.	
	-	5:0	Reserved.	
7Eh (3DF8h)	**REG3DF8**	**7:0**	**Default : 0x00**	**Access : R/W**
	CKG_TMG[1:0]	7:6	CLK_TMG clock control (16 Hz). [0]: Disable clock. [1]: Invert clock.	
	32KOUT_MODE	5	Refer to pad mux table.	
	RSTOUT_MODE	4	Refer to pad mux table.	
	-	3	Reserved.	
	MIIC_MODE	2	Refer to pad mux table.	
	DIGMIC_MODE[1:0]	1:0	Refer to pad mux table.	
7Eh (3DF9h)	**REG3DF9**	**7:0**	**Default : 0x00**	**Access : R/W**
	MCLK_ARM_EN	7	ARM MIU clock enable (0: enable; 1: disable).	
	MCLK_UHC20_EN	6	UHC20 MIU clock enable (0: enable; 1: disable).	
	TTLGPIO3_MODE	5	Refer to pad mux table.	
	TTLGPIO2_MODE	4	Refer to pad mux table.	
	TTLGPIO1_MODE	3	Refer to pad mux table.	
	-	2	Reserved.	
	TEST_OUT_MODE[1:0]	1:0	Refer to pad mux table.	
7Fh (3DFCh)	**REG3DFC**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLASSD_EN	7	1: Enable Class-D.	
	PWM5_MODE	6	Refer to pad mux table.	
	PWM4_MODE	5	Refer to pad mux table.	
	PWM3_MODE	4	Refer to pad mux table.	
	PWM2_MODE	3	Refer to pad mux table.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description	
	PWM1_MODE	2	Refer to pad mux table.	
	PWM0_MODE[1:0]	1:0	Refer to pad mux table.	
7Fh (3DFDh)	**REG3DFD**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:6	Reserved.	
	CKG_BIST_EN	5	CLK_BIST clock enable.	
	BOOT_FROM_TCM	4	0: First fetch address is 0xFFFF0000. 1: First fetch address is 0x00000000.	
	RESET_CPU_DBG	3	ARM debug mode reset.	
	SPICS1_MODE	2	Refer to pad mux table.	
	MPIFSPI_MODE[1:0]	1:0	Refer to pad mux table.	

UTMI Register (Bank = 1F)

UTMI Register (Bank = 1F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (3E00h)	**REG3E00**	**7:0**	**Default : 0x01**	**Access : R/W**
	R_DM_PDEN	7	Override value to Enable FS/LS DM pull-down resistor. 0 = Normal. 1 = Pull down.	
	R_DP_PDEN	6	Override value to Enable FS/LS DP pull-down resistor. 0 = Normal. 1 = Pull down.	
	R_PUMODE	5	Override DP/DM pull-up resistor value control. 0 = Pull-up resistor ~ 900~1575 ohm. 1 = Pull-up resistor ~ 1425~3090 ohm.	
	DM_PUEN	4	Override value to Enable FS/LS DM pull-up resistor. 0 = Normal. 1 = Pull up.	
	DP_PUEN	3	Override value to Enable FS/LS DP pull-up resistor. 0 = Normal. 1 = Pull up.	
	REF_PDN	2	Override value to Power-down USB_XCVR reference block. 0 = Normal. 1 = Power down.	
	TERM_OVERRIDE	1	Enable FS/LS termination override mode. 0 = Disable. 1 = Enable override mode.	
	PDN_OVERRIDE	0	Enable USB_XCVR power-down control override mode. 0 = Disable. 1 = Enable override mode.	
00h (3E01h)	**REG3E01**	**7:0**	**Default : 0xDB**	**Access : R/W**
	REG_PDN	7	Override value to Power-down USB_XCVR build-in regulator block. 0 = Normal. 1 = Power down.	
	IREF_PDN	6	Override value to Power-down USB_XCVR HS current reference block. 0 = Normal. 1 = Power down.	
	VBUSDET_PDN	5	Override value to Power-down USB_XCVR VBUS detector block.	

UTMI Register (Bank = 1F)

Index (Absolute)	Mnemonic	Bit	Description
			0 = Normal. 1 = Power down.
	FL_XCVR_PDN	4	Override value to Power-down USB_XCVR FS/LS transceiver block. 0 = Normal. 1 = Power down.
	HS_PREAMP_PDN	3	Override value to Power-down USB_XCVR HS pre-amplifier block. 0 = Normal. 1 = Power down.
	HS_TED_PDN	2	Override value to Power-down USB_XCVR HS TED block. (squelch circuit). 0 = Normal. 1 = Power down.
	PLL_PDN	1	Override value to Power-down USB_XCVR PLL block. 0 = Normal. 1 = Power down.
	HS_DM_PDN	0	Override value to Power-down USB_XCVR HS de-serializer block. 0 = Normal. 1 = Power down.
01h (3E04h)	**REG3E04**	**7:0**	**Default : 0x80** **Access : R/W**
	BOND_SEL	7	Select internal regulator. 0 = Use external regulator. 1 = Use internal regulator.
	HS_TX_TEN	6	Force enable HS_TX analog Parallel-to-Serial function. (No use). 0 = Normal. 1 = Force enable current source.
	FL_LOWIMODE	5	Full/Low speed receiver power saving mode. 0 = Normal. 1 = Enable Low current mode.
	BITSTUFF_EN	4	Override value to control Bit-Stuff mode. 0 = Force Bit-Stuff disable. 1 = Force Bit-Stuff enable.
	NRZI_EN	3	Override value to control NRZI mode. 0 = Force NRZI disable. 1 = Force NRZI enable.

UTMI Register (Bank = 1F)

Index (Absolute)	Mnemonic	Bit	Description	
	CLK12_SEL	2	PLL 12MHz reference clock source select. 0 = From XTAL_IN. (12Mhz). 1 = From digital synthesizer. (48Mhz-N.f).	
	FSLS_SEL	1	Override value to select Full/Low speed USB_XCVR. 0 = Full speed mode. 1 = Low speed mode.	
	SEL_OVERRIDE	0	Source select and enable override control.(No use).	
01h (3E05h)	**REG3E05**	**7:0**	**Default : 0x10**	**Access : R/W**
	HS_RTERM_PDN	7	Power down option of high speed terminal resistor.	
	LINESTATE_SEL	6	Line state mode report selection in HS mode. 0 = Normal. 1 = Select RX_CHIRP as line state.	
	EOP40_DET_DELAY_CNT[2:0]	5:3	HS EOP_40 window delay for disconnect detection. (1T = 1/120 MHz). 00 = No delay. 01 = Delay 1T. 10 = Delay 2T. 11 = Delay 3T. (Default value is 2).	
	FL_SEL_OVERRIDE	2	Full/Low speed mode select override value. 0 = Normal. 1 = Controlled by register fs_ls_sel (bit-1).	
	NRZI_OVERRIDE	1	NRZI enable controlled by register. 0 = Normal. 1 = Controlled by nrzi_en (bit-3).	
	BITSTUFF_OVERRIDE	0	Bit-stuff enable controlled by register. 0 = Normal. 1 = Controlled by bitstuff_en (bit-4).	
02h (3E09h)	**REG3E09**	**7:0**	**Default : 0x30**	**Access : R/W**
	UTMI_TX_WAIT_CNT[3:0]	7:4	TX HS delay for min inter-packet 32 bit-time wait state. (1T = 1/120 MHz). 000 = zero wait state. 001 = 1T. … 101 = 6T. 111 = 7T. (Default is 3).	

UTMI Register (Bank = 1F)

Index (Absolute)	Mnemonic	Bit	Description
	TX_OUT_SEL_MULTI_PHASE[1:0]	3:2	UTMI TX OUT multi cycle phase selection. 00 = Phase 0. 01 = Phase 1. 10 = Phase 2. 11 = Phase 3.
	TX_IN_SEL_MULTI_PHASE[1:0]	1:0	UTMI TX IN Multi cycle phase selection. 00 = Phase 0. 01 = Phase 1. 10 = Phase 2. 11 = Phase 3.
03h (3E0Ch)	**REG3E0C**	**7:0**	**Default : 0x20** **Access : R/W**
	OTG_DUAL_ROLE	7	Enable OTG dual role mode. 0 = Register control. 1 = Normal function. (OTG mode).
	HS_STAGE_SELECT[1:0]	6:5	RX HS data recovery reference stage control. 00 = 1 stage. 01 = 2 stages. 00 = 3 stages. 01 = 4 stages. (Default is 1).
	TX_FL_LATENCY_DELAY_1	4	TX in Full/Low speed mode delay 1 DFF. 0 = Normal (combinational out to analog). 1 = Enable (DFF out to analog).
	TX_FL_EARLY_4	3	TX in fl mode 4 to 1 fifo bypass 1 DFF. (no use). 0 = Disable. 1 = Enable.
	TX_FORCE_HS_CURRENT_ENABLE	2	Force HS TX current source enable. 0 = Normal. 1 = Force current source.
	UTMI_TX_SW_RESET	1	UTMI TX software reset. 0 = Normal. 1 = Enable software reset.
	RX_SWRESET	0	UTMI RX software reset. 0 = Normal. 1 = Enable software reset.
03h (3E0Dh)	**REG3E0D**	**7:0**	**Default : 0x30** **Access : R/W**
	VBUSDET_TEST[1:0]	7:6	VBUS_VALID LEVEL SELECT.

UTMI Register (Bank = 1F)

Index (Absolute)	Mnemonic	Bit	Description	
	TX_RESERVED[3:0]	5:2	[1:0] = clock_switch_sel (Default is 2'b00). [2] = cid_over_dis (Default is 1). [3] = vbus_over_dis (Default is 1).	
	CDR_MODE_SEL	1	RX HS data recovery voting mode select. 0 = Old cdr mode. 1 = New cdr mode select to collect more RX edge information.	
	TX_RESET_FSM	0	Synchronous TX FSM software reset. 0 = Disable. 1 = Reset TX internal FSM engine.	
04h (3E10h)	**REG3E10**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLK_EXTRA_0_EN	7	pd_bg_current: Power down bandgap current.	
	CLKTEST_EN	6	Enable test clock output. 0 = Stop. 1 = Enable.	
	-	5:2	Reserved.	
	UTMI_CLK120_EN	1	Override value to enable UTMI 120M clock source. 0 = Stop. 1 = Enable.	
	UTMI_CLK_EN	0	Override value to enable UTMI 30M clock source. 0 = Stop. 1 = Enable.	
04h (3E11h)	**REG3E11**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_RX_ROBOUST_EN	7	Enable High speed Rx roboust feature.	
	-	6:5	Reserved.	
	CLK214_SYN_EN	4	Enable clock synthesizer.	
	FORCE_PLL_ON	3	Override enable to enable utmi pll by register. 0 = Normal. 1 = Force utmi pll always on.	
	CLK_CTL_OVERRIDE	2	Override enable to enable clock source by register. 0 = Normal. 1 = Force clock enable by register setting.	
	XTAL12_EN	1	Register to enable xtal clock. 0 = Stop. 1 = Enable.	
	CLK_EXTRA_1_EN	0	reg_all_pass: Enable ISI improvement.	
05h	**REG3E14**	**7:0**	**Default : 0x00**	**Access : R/W**

UTMI Register (Bank = 1F)

Index (Absolute)	Mnemonic	Bit	Description	
(3E14h)	CLK_EXTRA_0_INV	7	Inverse clock extra0. 0 = Normal. 1 = Inverse clock.	
	CLKTEST_INV	6	Inverse clock test. 0 = Normal. 1 = Inverse clock.	
	-	5:2	Reserved.	
	UTMI_CLK120_INV	1	Inverse 120MHz clock source. 0 = Normal. 1 = Inverse clock.	
	UTMI_CLK_INV	0	Inverse 30MHz clock source. 0 = Normal. 1 = Inverse clock.	
05h (3E15h)	**REG3E15**	**7:0**	**Default : 0x00**	**Access : R/W**
	CK_INV_RESERVED[6:0]	7:1	Reserved register for clock inverse.	
	CLK_EXTRA_1_INV	0	Inverse clock extra1. 0 = Normal. 1 = Inverse clock.	
06h (3E18h)	**REG3E18**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_CLOCK_DIV_SELECT[1:0]	7:6	UTMI test clock divider selection. 00 = /1. 01 = /2. 10 = /4. 11 = /8.	
	TEST_CLOCK_SELECT[5:0]	5:0	UTMI test clock selection. 00h = clk_120mhz_utmi_z. 01h = clk_30mhz_utmi_z. 02h = clk_120_12_1p5_mhz_tx_fsm_z. 03h = clk_120_48_6_mhz_rx_fsm_z. 04h = clk_48_6_mhz_fs_ls_rx_cdr_z. 05h = clk_120_12_1p5_mhz_rx_decoder_z. 06h = clk_10khz_power_on_fsm_z. 07h = clk_1khz_pll_clk_ready_timer_z. 08h = clk_extra_ref_0_z. 09h = clk_extra_ref_1_z. Other = N.A.	
06h	**REG3E19**	**7:0**	**Default : 0x00**	**Access : R/W**

UTMI Register (Bank = 1F)

Index (Absolute)	Mnemonic	Bit	Description
(3E19h)	UTMI_CKINV_EN_SEL [1:0]	7:6	UTMI 30MHz inverse clock enable generated by 120MHz. 00 = Select phase 0. 01 = Select phase 1. 10 = Select phase 2. 11 = Select phase 3. (Default is 1).
	UTMI_CK_EN_SEL[1:0]	5:4	UTMI 30MHz clock enable generated by 120MHz. 00 = Select phase 0. 01 = Select phase 1. 10 = Select phase 2. 11 = Select phase 3. (Default is 3). (Refer to UTMI_CKINV_EN_SEL offset is 2).
	CLK_EXTRA1_DIV_SELECT[1:0]	3:2	Extra clock 1 divider selection. 00 = 480MHz /2. 01 = 480MHz /3. 10 = 480MHz /4. 11 = 480MHz /5.
	CLK_EXTRA0_DIV_SELECT[1:0]	1:0	Extra clock 0 divider selection. 00 = 480MHz /2. 01 = 480MHz /3. 10 = 480MHz /4. 11 = 480MHz /5.
07h (3E1Ch)	**REG3E1C**	**7:0**	**Default : 0x00** **Access : RO**
	UTMI_DIGITAL_STATUS [7:0]	7:0	UTMI digital part status report. 1. Status [0]: Error flag in elasticity buffer. 0 = normal. 1 = elasticity buffer error. 2. Status [1]: Sync pattern error detected status. 0 = normal. 1 = sync strip error. 3. Status [2]: EOP error detected status. 0 = normal. 1 = EOP error. 4. Status [3]: Bit-stuffer error status in Full/Low speed mode. 0 = normal. 1 = bit stuff error. 5. Status [4]: Underflow status in elasticity buffer. 0 = not underflow.

UTMI Register (Bank = 1F)

Index (Absolute)	Mnemonic	Bit	Description	
			1 = underflow. 6. Status [5]: Overflow status in elasticity buffer. 0 = not overflow. 1 = overflow. 7. Status [6]: Reserved. 8. Status [7]: UTMI interrupt status. 0 = no IRQ. 1 = IRQ active. 9. Status [8]: Enable Chirp function while UTMI as a device. 0 = normal. 1 = chirp. 10. Status [9]: Enable Chirp function while UTMI as a host. 0 = normal. 1 = chirp. 11. Status [10]: Disconnect status in host mode. 0 = connected. 1 = disconnect. 12. Status [11]: TX FSM non-idle mode. 0 = idle. 1 = busy. 13. Status [12]: RX FSM non-idle mode. 0 = idle. 1 = busy. 14. Status [13]: Low speed mode enable status. 0 = unknown. 1 = low speed mode. 15. Status [14]: Full speed mode enable status. 0 = unknown. 1 = full speed mode. 16. Status [15]: High speed mode enable status. 0 = unknown. 1 = high speed mode.	
07h (3E1Dh)	**REG3E1D**	**7:0**	**Default : 0x00**	**Access : RO**
	UTMI_DIGITAL_STATUS [15:8]	7:0	See description of '3E1Ch'.	
08h (3E20h)	**REG3E20**	**7:0**	**Default : 0x00**	**Access : R/W**
	SE0_SET	7	Enable HS 45 ohm resistor on. 0 = Normal. 1 = Force 45 ohm resistor on.	

UTMI Register (Bank = 1F)

Index (Absolute)	Mnemonic	Bit	Description	
	UTMI_INT_CLR	6	Write 1 & write 0 will clear utmi interrupt. 0 = stand by. 1 = clear interrupt.	
	FORCE_TX_NONBUSY	5	Force UTMI RX side always input tx_busy signal control. 0 = Normal. 1 = Force tx_busy is 0.	
	FORCE_RX_NONBUSY	4	Force UTMI TX side always input rx_busy signal control. 0 = Normal. 1 = Force rx_busy is 0.	
	TEST_BUS_SELECT[3:0]	3:0	UTMI test bus selection for debugging. 0000 = select test 0. 0001 = select test 1. 0010 = select test 2. ... 1111 = select test 15. (Refer to note 1).	
08h (3E21h)	**REG3E21**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_TX_OVERRIDE	7	Enable HS tx controlled by register. 0 = Normal. 1 = Enable override mode.	
	ERROR_FLAG_CLR	6	Write 1 & write 0 to clear error flag in digital status (address 7). 0: Disable. 1: Enable clear error flag.	
	PHY_MODE_ENABLE	5	Enable UTMI in Phy mode. 0 = Normal. 1 = set UTMI in/out ports from pad.	
	POWER_GOOD_RST	4	SW reset for power good signal. 0 = Normal. 1 = Software reset instead of powergood reset.	
	TX_OVERRIDE	3	Enable FL tx controlled by register. 0 = Normal. 1 = Enable override mode.	
	TX_SE0	2	Override FL tx send SE0. 0 = Disable SE0. 1 = Force tx sending SE0.	
	TX_EN	1	Override FL tx enable. 0 = Disable tx.	

UTMI Register (Bank = 1F)

Index (Absolute)	Mnemonic	Bit	Description	
			1 = Force tx enable.	
	TX_DATA	0	Override FL tx data. 0 = transmit 0. 1 = transmit 0.	
09h (3E24h)	**REG3E24**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DEGLITCH_ENZ	7	Register to enable deglitch module. 0 = Enable vdd2low deglitch function. 1 = Disable.	
	VDD2LOW_RST_ENZ	6	Register to enable reset signal of vdd2low. 0 = Enable to output vdd2low_rst signal. 1 = Normal.	
	DEGLITCH_PRD[5:0]	5:0	Register to set vdd2low deglitch period.	
09h (3E25h)	**REG3E25**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_P1	7	Enable Port-1 debug port.	
	IB_RTERM_TEST[2:0]	6:4	HS RTERM current test.	
	REG_TEST[2:0]	3:1	REG_TEST_p1: Regulator test (port 1 only).	
	USBSYN_RST	0	SW reset for UTMI digital synthesizer. 0 = Normal. 1 = Software reset digital synthesizer module in UTMI.	
0Ah (3E28h)	**REG3E28**	**7:0**	**Default : 0x0B**	**Access : R/W**
	XCVRSEL[1:0]	7:6	Override value to set XCVRSEL value (MAC to UTMI). 00 = high speed. 01 = full speed. 10 = low speed. 11 = N.A.	
	OPMODE[1:0]	5:4	Override value to set OPMODE value. (MAC to UTMI). 00 = mode 0. 01 = mode 1. 10 = mode 2. 11 = mode 3.	
	IDDIG	3	Override value to set IDDIG value. (UTMI to MAC). 0 = Connected plug is a mini-A. 1 = Connected plug is a mini-B.	
	SESSEND	2	Override value to set SESSEND value. (UTMI to MAC). 0 = Vbus > 0.8 V.	

UTMI Register (Bank = 1F)

Index (Absolute)	Mnemonic	Bit	Description	
			1 = Vbus < 0.2 V.	
	AVALID	1	Override value to set A-port value. (UTMI to MAC). 0 = Vbus < 0.8 V. 1 = Vbus > 2.0 V.	
	VBUSVALID	0	Override value to set VBUS VALID value. (UTMI to MAC). 0 = Vbus < 4.4 V. 1 = Vbus > 4.75 V.	
0Ah (3E29h)	**REG3E29**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	HOST_CHIRP_DET	5	HOST_CHIRP_DET.	
	USB_BOND_SET	4	Override value for option USB_BOND. 0 = Two port UTMI settings. 1 = One port UTMI setting.	
	USB_BOND_OVD	3	Override bonding option USB_BOND. 0 = Normal. 1 = Bonding controlled by register.	
	SUSPENDM	2	Override value to control SUSPENDM. 0 = device in suspend mode. 1 = device in normal mode.	
	MACMODE_OVD	1	Override enable to control mac mode. 0 = Normal. 1 = Change Mac control signal from register.	
	TERMSEL	0	Override value to set TERMSEL value. (MAC to UTMI). 0 = high speed. 1 = full/low speed.	
0Bh (3E2Ch)	**REG3E2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SYNTHESIZE_NF[7:0]	7:0	Digital synthesizer clock frequency setting. MPLL clock divided by N.f setting. N = 5 bits. F = 27 bits.	
0Bh (3E2Dh)	**REG3E2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SYNTHESIZE_NF[15:8]	7:0	See description of '3E2Ch'.	
0Ch (3E30h)	**REG3E30**	**7:0**	**Default : 0xCC**	**Access : R/W**
	SYNTHESIZE_NF[23:16]	7:0	See description of '3E2Ch'.	

UTMI Register (Bank = 1F)

Index (Absolute)	Mnemonic	Bit	Description	
0Ch (3E31h)	**REG3E31**	**7:0**	**Default : 0x23**	**Access : R/W**
	SYNTHESIZE_NF[31:24]	7:0	See description of '3E2Ch'.	
10h (3E40h)	**REG3E40**	**7:0**	**Default : 0x00**	**Access : R/W**
	PLL_TEST[7:0]	7:0	1. PLL_TEST[0]: PLL reference input clock selection (accompanied with PLL_TEST[0]). {PLL_TEST[26], PLL_TEST[0]}. 00 = Naked crystal input. 01 = Reserved+K98. 10 = Synthesized clock. 11 = Buffered crystal input. 2. PLL_TEST[2:1]: PLL loop divider selection. 00 = / 40. 01 = / 20. 10 = / 10. 11 = / (PLL_TEST[7:3]) / 2. 3. PLL_TEST[7:3]: PLL loop divider control from 3 to 65 (N+1). 000000 = / 65. 000001 = NA. 000010 = / 3. 000011 = / 4. … 111111 = / 64. 4. PLL_TEST[9:8]: PLL test clock outputs, PLL_TCKOA and PLL_TCKOD, source select. 00 = FBCK33. 01 = REFCK33. 10 = FBCK18. 11 = CLK480 to digital. 5. PLL_TEST[11:10]:PLL test clock outputs, PLL_TCKOA and PLL_TCKOD, post-divider dividing ratio selection. 00 = /1. 01 = /2. 10 = /4. 11 = /8. 6.	

UTMI Register (Bank = 1F)

Index (Absolute)	Mnemonic	Bit	Description
			PLL_TEST[13:12]:CLK480 to digital output phase selection. 00 = A0. 01 = A90. 10 = A0B. 11 = A90B. 7. PLL_TEST[15:14]:HS transmitter serializer CLK480 phase selection. 00 = A0. 01 = A90. 10 = A0B. 11 = A90B. 8. PLL_TEST[16]:ENDISC. PLL charge pump control. When PLL_TEST[19], ENAUTO=0 and ENDISC=1, charge pump can pull up or down PLL VTRL by EXTDISC. 9. PLL_TEST[17]:EXTDISC. When PLL_TEST[19], ENAUTO=0 and PLL_TEST[16], ENDISC=1. 0 = Pull down PLL VCTL. 1 = Pull up PLL VCTL. 10. PLL_TEST[18]: ENLOCKZ. Disable PLL lock detector. 0 = PLL lock detector disabled. 1 = PLL lock detector enabled. 11. PLL_TEST[19]:ENAUTO. Enable PLL lock-up prevention. 0 = PLL lock-up prevention disabled. 1 = PLL lock-up prevention enabled. 12. PLL_TEST[20]:ENDCC. Enable VCO clock duty cycle correction. 0 = Duty cycle correction disabled. 1 = Duty cycle correction enabled. 13. PLL_TEST[22:21]:TVCO control.

UTMI Register (Bank = 1F)

Index (Absolute)	Mnemonic	Bit	Description
			00 = 0. 01 = 960MHz. 10 = 0. 11 = 480MHz. 14. PLL_TEST[23]:CLK480 to digital output source selection. 0 = Phase selected by PLL_TEST[13:12]. 1 = Phase fixed from TVCO. 15. PLL_TEST[24]:ENINV. CLK120 to HS transmitter serializer phase selection. 0 = CLK120 rising edge selected. 1 = CLK120 falling edge selected. 16. PLL_TEST[25]:ENINVENTMUX. Enable PLL test output clock. 0 = PLL_TCKOA and PLL_TCKOD disabled. 1 = PLL_TCKOA and PLL_TCKOD enabled. 17. PLL_TEST[26]:PLL input reference selection (accompanied with PLL_TEST[0]). {PLL_TEST[26], PLL_TEST[0]}. 00 = Naked crystal input. 01 = Reserved. 10 = Synthesized clock. 11 = Buffered crystal input. 18. PLL_TEST[31:27]: Reserved. 19. PLL_TEST[34:32]: ICTL33[2:0]. Charge pump current control. 000 = 100%. 001 = 200%. 010 = 50%. 011 = 150%. 100 = 75%. 101 = 175%. 110 = 25%. 111 = 125%. 20.

UTMI Register (Bank = 1F)

Index (Absolute)	Mnemonic	Bit	Description	
			PLL_TEST[35]: DIS_HVFLAG_DISC. Ring oscillator supply voltage sensor state discharge control. 0 = HV_FLAG state enabled. 1 = HV_FLAG state disabled. 21. PLL_TEST[36]: ENSYN33. Charge pump mode select for reference clock source. 0 = Reference clock source from crystal input mode. 1 = Reference clock source from synthesizer input mode. 22. PLL_TEST[38:37]:Regulated voltage select. 00 = 100% (1.8V). 01 = 90%. 10 = 83%. 11 = 110%. 23. PLL_TEST[39]:Regulator reference voltage source select. 0 = Reference from VBG. 1 = Reference from 3.3V supply / Res.	
10h (3E41h)	**REG3E41**	**7:0**	**Default : 0x00**	**Access : R/W**
	PLL_TEST[15:8]	7:0	See description of '3E40h'.	
11h (3E44h)	**REG3E44**	**7:0**	**Default : 0x00**	**Access : R/W**
	PLL_TEST[23:16]	7:0	See description of '3E40h'.	
11h (3E45h)	**REG3E45**	**7:0**	**Default : 0x00**	**Access : R/W**
	PLL_TEST[31:24]	7:0	See description of '3E40h'.	
12h (3E48h)	**REG3E48**	**7:0**	**Default : 0x00**	**Access : R/W**
	PLL_TEST[39:32]	7:0	See description of '3E40h'.	
13h (3E4Ch)	**REG3E4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_TED_TEST[7:0]	7:0	1. HS_TED_TEST[1:0] : De-glitch time setting for Squelch. 00 = 4 high-speed bit time. 01 = 6 high-speed bit time. 10 = 8 high-speed bit time. 11 = 2 high-speed bit time. 2. HS_TED_TEST[3:2] :Squelch detector input offset selection. 00 = 0mV. 01 = +12mV.	

UTMI Register (Bank = 1F)

Index (Absolute)	Mnemonic	Bit	Description	
			10 = -12mV. 11 = 0mV. 3. HS_TED_TEST[7:4] : Reserved.	
13h (3E4Dh)	**REG3E4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_PREAMP_TEST[7:0]	7:0	1. HS_PREAMP_TEST[1:0] : Reserved. 2. HS_PREAMP_TEST[3:2] : High-speed receiver bias current selection. 00 = 40u. 01 = 30u. 10 = 60u. 11 = 50u. 3. HS_PREAMP_TEST[7:4] : Reserved.	
14h (3E50h)	**REG3E50**	**7:0**	**Default : 0x00**	**Access : R/W**
	FL_XCVR_TEST[7:0]	7:0	1. FL_XCVR_TEST[2:0] : Full/low-speed slew rate control capacitor fine tune. 000 = 1.2p. 001 = 1.3p. 010 = 1.4p. 011 = 1.5p. 100 = 0.8p. 101 = 0.9p. 110 = 1.0p. 111 = 1.1p. 2. FL_XCVR_TEST[5:3] : High-speed pull-down resistor fine tune. 000 = 100%. 001 = 97.5%. 010 = 97.5%. 011 = 95%. 100~111 = 80%. 3. FL_XCVR_TEST[7:6] :Full/low-speed pull down resistor fine tune.	

UTMI Register (Bank = 1F)

Index (Absolute)	Mnemonic	Bit	Description	
			00 = 19.35k. 01 = 17.3k. 10 = 21.45k. 11 = 19.35k. 4. FL_XCVR_TEST[9:8] : Full/low-speed pull down resistor fine tune. 00 = 1.2k. 01 = 1.3k. 10 = 1.17k. 11 = 1.19k. 5. FL_XCVR_TEST[10] : Full/low speed slew rate control current fine tune. 0 = current 1X. 1 = current 0.8X. 6. FL_XCVR_TEST[11] : Disable Full/low speed data re-timing by CLK120. 0 = Enabled. 1 = Disabled. 7. FL_XCVR_TEST[12] : Enable analog test output to DM. 0 = Disabled. 1 = Enabled. 8. FL_XCVR_TEST[13] : Enable analog test input from DP. 0 = Disabled. 1 = Enabled. 9. FL_XCVR_TEST[15:14] : Reserved.	
14h (3E51h)	**REG3E51**	**7:0**	**Default : 0x00**	**Access : R/W**
	FL_XCVR_TEST[15:8]	7:0	See description of '3E50h'.	
15h (3E54h)	**REG3E54**	**7:0**	**Default : 0x00**	**Access : R/W**
	REF_TEST[7:0]	7:0	1. REF_TEST[1:0] : VSPOUT voltage control (for Squelch voltage threshold). 00 = 0.275V. 01 = 0.225V.	

UTMI Register (Bank = 1F)

Index (Absolute)	Mnemonic	Bit	Description
			10 = 0.250V. 11 = 0.300V. 2. REF_TEST[3:2] : VSMOUT voltage control (for Squelch voltage threshold). 00 = 0.150V. 01 = 0.100V. 10 = 0.125V. 11 = 0.175V. 3. REF_TEST[5:4] : VCPOUT voltage control (for Disconnect voltage threshold). 00 = 0.70V. 01 = 0.60V. 10 = 0.65V. 11 = 0.75V. 4. REF_TEST[7:6] : VCMOUT voltage control (for Disconnect voltage threshold). 00 = 0.15V. 01 = 0.05V. 10 = 0.10V. 11 = 0.20V. 5. REF_TEST[9:8] : PGD comparator voltage threshold select (with hysteresis=100mV). 1.8V Threshold Vthh Vthl. 00 1.30V 1.20V. 01 1.25V 1.15V. 10 1.20V 1.10V. 11 1.15V 1.05V. 3.3V Threshold Vthh Vthl. 00 2.87V 2.63V. 01 2.74V 2.52V. 10 2.82V 2.58V. 11 2.71V 2.46V. 6. REF_TEST[10] : Enable Power-Good Detector to detect USB phy 3.3V power supply. 0 = Disabled.

UTMI Register (Bank = 1F)

Index (Absolute)	Mnemonic	Bit	Description	
			1 = Enabled. 7. REF_TEST[11] : Enable Power-Good Detector. 0 = Disabled. 1 = Enabled. 8. REF_TEST[12] : Enable VBG to analog test output and reference from analog test input. 0 = Disabled. 1 = Enabled. 9. REF_TEST[13] : Enable VBG/R bias current test output (20uA to ground). 0 = Disabled. 1 = Enabled. 10. REF_TEST[14] : Reserved. 11. REF_TEST[15] : Enable Power-Good Detector to trigger POR. 0 = Disabled. 1 = Enabled.	
15h (3E55h)	**REG3E55**	**7:0**	**Default : 0x00**	**Access : R/W**
	REF_TEST[15:8]	7:0	See description of '3E54h'.	
16h (3E58h)	**REG3E58**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_TX_TEST[7:0]	7:0	1. HS_TX_TEST[2:0] : Reserved. 2. HS_TX_TEST[3] :Enable high-speed TX test clock output (accompanied with HS_TX_TEST[28]). 0 = Disable. 1 = Enable. 3. HS_TX_TEST[6:4] : High-speed TX output current adjust. 000 = 100%. 001 = 101.6%. 010 = 103.3%. 011 = 105.0%. 100 = 93.3%. 101 = 95.0%.	

UTMI Register (Bank = 1F)

Index (Absolute)	Mnemonic	Bit	Description
			110 = 96.7%. 111 = 98.3%. 4. HS_TX_TEST[8:7] : High-speed TX pre-emphasis adjust. 00 = 10.0%. 01 = 10.8%. 10 = 8.33%. 5. HS_TX_TEST[9] : Power-down High-speed TX pre-emphasis bias current. 0 = Enable. 1 = Power-down. 6. HS_TX_TEST[10] : Power-down high-speed TX current bias current. 0 = Enable. 1 = Power-down. 7. HS_TX_TEST[13:11] : HS_RTERM bias current adjust. 000 = 6/6. 001 = 7/6. 010 = 8/6. 011 = 9/6. 100 = 2/6. 101 = 3/6. 110 = 4/6. 111 = 5/6. 8. HS_TX_TEST[14] : Enable HS_TX test current output. 0 = Disable. 1 = Enable. 9. HS_TX_TEST[15] : Power-down VBUSDET_NC bias current. 0 = Enable. 1 = Power-down. 10. HS_TX_TEST[16] : Power-down HS_RX bias current. 0 = Enable. 1 = Power-down. 11.

UTMI Register (Bank = 1F)

Index (Absolute)	Mnemonic	Bit	Description
			HS_TX_TEST[17] : Power-down RTERM bias current. 0 = Enable. 1 = Power-down. 12. HS_TX_TEST[18] : Power-down HS_RTERM bias current. 0 = Enable. 1 = Power-Down. 13. HS_TX_TEST[19] : Power-down HS_RTERM/HS_RX/HS_TX_ITEST bias current. 0 = Enable. 1 = Power-down. 14. HS_TX_TEST[23:20] : Reserved. 15. HS_TX_TEST[24] : Mute high-speed TX input data. 0 = Normal Function. 1 = Mute. 16. HS_TX_TEST[25] : Enable pre-emphasis. 0 = Disable. 1 = Enable. 17. HS_TX_TEST[26] : Enable pre-emphasis at data transition edge. 0 = Disable. 1 = Enable. 18. HS_TX_TEST[27] : Enable pre-emphasis at data enable edge. 0 = Disable. 1 = Enable. 19. HS_TX_TEST[28] : Enable high-speed test clock output (accompanied with HS_TX_TEST[3]). 0 = Disable. 1 = Enable. 20. HS_TX_TEST[29] : High-speed test clock output source selection. 0 = PLL_TCKOA.

UTMI Register (Bank = 1F)

Index (Absolute)	Mnemonic	Bit	Description	
			1 = HS_TX_TCKI. 21. HS_TX_TEST[31:30] : Reserved.	
16h (3E59h)	**REG3E59**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_TX_TEST[15:8]	7:0	See description of '3E58h'.	
17h (3E5Ch)	**REG3E5C**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_TX_TEST[23:16]	7:0	See description of '3E58h'.	
17h (3E5Dh)	**REG3E5D**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_TX_TEST[31:24]	7:0	See description of '3E58h'.	
18h (3E60h)	**REG3E60**	**7:0**	**Default : 0x00**	**Access : RO**
	UTMI_ANALOG_STATUS [7:0]	7:0	Status report for utmi atop. Status [0]: UTMI pll lock status. Status [1]: UTMI pll flag. Status [2]: UTMI pll flag. Status [3]: UTMI pll clock test status. Status [4]: Power good status. Status [5]: Vbus voltage valid status. Status [6]: OTG session end status. Status [7]: Pad CID status. Status [8]: OTG connector Type-B valid status. Status [9]: OTG connector Type-A valid status. Status [13:10]: Reserved. Status [14]: loop back test failed. Status [15]: loop back test finish.	
18h (3E61h)	**REG3E61**	**7:0**	**Default : 0x00**	**Access : RO**
	UTMI_ANALOG_STATUS[15:8]	7:0	See description of '3E60h'.	
19h (3E64h)	**REG3E64**	**7:0**	**Default : 0x00**	**Access : R/W**
	PG_TX_LENGTH[7:0]	7:0	TX data length for internal pattern gen. (0~255 bytes).	
19h (3E65h)	**REG3E65**	**7:0**	**Default : 0x00**	**Access : R/W**
	PG_RESERVED[4:0]	7:3	Reserved register.	
	PG_TX_FIXED_DATA	2	Select fixed data to transmit. 0: Normal. 1: Enable to transmit random data.	
	PG_TX_MODE	1	Select random data to transmit. 0: Normal.	

UTMI Register (Bank = 1F)

Index (Absolute)	Mnemonic	Bit	Description	
			1: Enable to transmit random data.	
	PG_TX_GO	0	Tx data enable to transmit for internal pattern gen.	
1Ah (3E68h)	**REG3E68**	**7:0**	**Default : 0x00**	**Access : R/W**
	PG_TX_DATA[7:0]	7:0	Pattern Gen TX initial data setting.	
1Ah (3E69h)	**REG3E69**	**7:0**	**Default : 0x00**	**Access : R/W**
	PG_TX_DATA[15:8]	7:0	See description of '3E68h'.	
1Bh (3E6Ch)	**REG3E6C**	**7:0**	**Default : 0x01**	**Access : R/W**
	PG_TX_INC[7:0]	7:0	Pattern Gen TX data incremental value setting.	
1Bh (3E6Dh)	**REG3E6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	PG_TX_INC[15:8]	7:0	See description of '3E6Ch'.	
1Ch (3E70h)	**REG3E70**	**7:0**	**Default : 0x01**	**Access : RO, R/W**
	ASRST_ON	7	Asynchronous reset for new FL module.	
	DM1_STATUS	6	Port 1 DM line status.	
	DP1_STATUS	5	Port 1 DP line status.	
	DM_STATUS	4	Port 0 DM line status.	
	DP_STATUS	3	Port 0 DP line status.	
	SELPORT	2	Port select for usb_xcvr switch. 0: Selected port0. 1: Selected port1.	
	VIGEN_PDN	1	VIGEN_PDN.	
	EN_CK_192	0	Enable usb_xcvr 192MHz clock out.	
1Ch (3E71h)	**REG3E71**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED2[7:0]	7:0	Reserved register 2.	

FCIE3 Register (Bank = 20)

FCIE3 Register (Bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (4600h)	**REG4600**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_INT	7	SDIO interrupt event.	
	-	6:4	Reserved.	
	MS_DATA_END	3	MS/MSPro data transaction complete event.	
	SD_DATA_END	2	SD/MMC data transaction complete event.	
	SD_CMD_END	1	SD/MMC card command and response transaction complete event.	
	MMA_DATA_END	0	MMA data transaction complete event.	
00h (4601h)	**REG4601**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MMA_LAST_DONE_INT	6	MMA Last Done interrupt event.	
	POWER_SAVE_INT	5	Power saving mode complete interrupt event.	
	NC_R2N_ECCCOR_INT	4	Software correct ecc error in RIU2NAND mode interrupt event.	
	CARD_DMA_END	3	Card interface DMA end interrupt.	
	NC_R2N_RDY_INT	2	RIU2NAND job end interrupt event.	
	NC_JOB_END	1	NAND job end interrupt event.	
	MIU_WR_RANGE_ERR	0	MIU write protection out of range event.	
01h (4604h)	**REG4604**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_INT_EN	7	SDIO_INT interrupt enable.	
	-	6:4	Reserved.	
	MS_DATA_EN	3	MS_DATA_END interrupt enable.	
	SD_DATA_END_EN	2	SD_DATA_END interrupt enable.	
	SD_CMD_END_EN	1	SD_CMD_END interrupt enable.	
	MMA_DATA_EN	0	MMA_DATA_END interrupt enable.	
01h (4605h)	**REG4605**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MMA_LAST_DONE_INT_EN	6	MMA Last Done interrupt enable.	
	-	5	Reserved.	
	NC_R2N_ECCCOR_INT_EN	4	Software correct ecc error in RIU2NAND mode interrupt enable.	
	CARD_DMA_END_EN	3	Card interface DMA end interrupt enable.	

FCIE3 Register (Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
	NC_R2N_RDY_INT_EN	2	RIU2NAND job end interrupt enable.	
	NC_JOB_ENDEN	1	NAND job end interrupt enable.	
	MIU_WR_RANGE_ERR_EN	0	MIU write protection range interrupt enable.	
02h (4608h)	**REG4608**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:6	Reserved.	
	FIFO_CLKRDY	5	Data fifo clock ready.	
	MIU_REQUEST_RST	4	Mask MIU interface request, high active.	
	DATA_SCRAMBLE_EN	3	MIU data scramble function enable.	
	JOB_RW_DIR	2	Specify whether this DMA cycle is Read or Write. 0: Read from card (data write to DRAM). 1: Write to card (data read from DRAM).	
	MMA_W_PRIORITY	1	MIU write request priority. 0: Low priority. 1: High priority.	
	MMA_R_PRIORITY	0	MIU read request priority. 0: Low priority. 1: High priority.	
02h (4609h)	**REG4609**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MIU_BUS_CTRL	2	MIU bus burst length selection enable. 0: Disable, length = 512-byte/MIU bus width. 1: Enable, length = reg_miu_bus_type.	
	MIU_BUS_TYPE[1:0]	1:0	MIU bus burst length. 0: 8 burst. 1: 16 burst. 2: 32 burst.	
03h (460Ch)	**REG460C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_26_16[7:0]	7:0	DMA Address[26:16].	
03h (460Dh)	**REG460D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIU_SELECT	7	MIU0/MIU1 selection, default 0 = MIU0.	
	-	6:3	Reserved.	
	DMA_ADDR_26_16[10:8]	2:0	See description of '460Ch'.	
04h (4610h)	**REG4610**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_ADDR_15_0[7:0]	7:0	DMA Address[15:0].	
04h	**REG4611**	**7:0**	**Default : 0x00**	**Access : R/W**

FCIE3 Register (Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
(4611h)	DMA_ADDR_15_0[15:8]	7:0	See description of '4610h'.	
05h (4614h)	**REG4614**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_STS_CHG	7	SDIO card plug-in or remove status change.	
	-	6:2	Reserved.	
	MS_STS_CHG	1	MS/MSPro card plug-in or remove status change.	
	SD_STS_CHG	0	SD/MMC card plug-in or remove status change.	
06h (4618h)	**REG4618**	**7:0**	**Default : 0x00**	**Access : R/W**
	SD_CARD_DET_SRC	7	SD card-detect pin select. 0: SD_CDZ. 1: SD_DAT3.	
	-	6:2	Reserved.	
	MS_STS_EN	1	MS/MSPro card status change interrupt enable.	
	SD_STS_EN	0	SD card status change interrupt enable.	
06h (4619h)	**REG4619**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SDIO_CARD_DET_SRC	1	SDIO card detect pin select. 0: SDIO_CDZ. 1: SDIO_DAT3.	
	SDIO_STS_EN	0	SDIO card status change interrupt enable.	
07h (461Ch)	**REG461C**	**7:0**	**Default : 0x00**	**Access : RO**
	SDIO_DET_N	7	SDIO card detection status.	
	-	6:2	Reserved.	
	MS_DET_N	1	MS/MSPro card detection status.	
	SD_DET_N	0	SD/MMC card detection status.	
07h (461Dh)	**REG461D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	NF_RBZ_STS	0	Nand nf_rbz pin status.	
08h ~ 08h (4620h ~ 4621h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
09h ~ 09h (4624h ~ 4625h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
0Ah	**REG4628**	**7:0**	**Default : 0x00**	**Access : R/W**

FCIE3 Register (Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
(4628h)	-	7:6	Reserved.	
	NC_EN	5	NAND controller interface enable.	
	-	4:3	Reserved.	
	MS_EN	2	MS card interface enable.	
	SD_EN	1	SD/MMC card interface enable.	
	MMA_ENABLE	0	MIU DMA enable, job finish auto clear. Note: Before setting this bit, make sure JOB_BL_CNT, MIU_DMA1, JOB_RW_DIR and MIU_DMA0 have been updated.	
0Bh (462Ch)	**REG462C**	**7:0**	**Default : 0x00**	**Access : R/W**
	JOB_BL_CNT[7:0]	7:0	Total block counts for this job. (Card unit: sector. SDIO & Nand unit: reg_sdio_blk_size9_0).	
0Bh (462Dh)	**REG462D**	**7:0**	**Default : 0x00**	**Access : R/W**
	TR_JOB_CNT_MANUAL	7	Manual mode for content of reg_tr_bk_cnt. 0: Hardware auto mode. 1: Manual mode.	
	TR_JOB_CNT_SRC	6	Select remainder job count of card or MIU. 0: Card remainder job count. 1: Miu remainder job count.	
	-	5:4	Reserved.	
	JOB_BL_CNT[11:8]	3:0	See description of '462Ch'.	
0Ch (4630h)	**REG4630**	**7:0**	**Default : 0x00**	**Access : RO**
	TR_BK_CNT[7:0]	7:0	Real time number of remainder sectors to be transferred.	
0Ch (4631h)	**REG4631**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	TR_BK_CNT[11:8]	3:0	See description of '4630h'.	
0Dh (4634h)	**REG4634**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CIF_RSP_SIZE[6:0]	6:0	Expected response size (byte count) for SD/MMC card. Expected register read size (byte count) for MS/MSPro card. 01: 1 byte. 40: 64 bytes.	

FCIE3 Register (Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
0Dh (4635h)	**REG4635**	**7:0**	**Default : 0x00**	**Access : R/W**
	SD_DELAY_SEL_7_0[7:0]	7:0	SD delay cell selection 10 bits. [1:0]: select 4 delay cells on data bus [0], [4]. [3:2]: select 4 delay cells on data bus [1], [5]. [5:4]: select 4 delay cells on data bus [2], [6]. [7:6]: select 4 delay cells on data bus [3], [7].	
0Eh (4638h)	**REG4638**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CIF_CMD_SIZE[6:0]	6:0	Command transfer size (byte count) for SD/MMC and MS/MSPro card. 01: 1 byte. 40: 64 bytes.	
0Eh (4639h)	**REG4639**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SD_DELAY_EN	2	SD bus add delay cell for SSO issue,. Enable register.	
	SD_DELAY_SEL_9_8[1:0]	1:0	SD delay cell selection 10 bits. [9:8]: select 4 delay cells on command line.	
0Fh (463Ch)	**REG463C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CARD_WD_CNT[7:0]	7:0	Expected data word count transferred through CIF FIFO. 0x00 represents 256 words. (CMD6 for SD card, CMD8/14/19 for MMC card).	
10h (4640h)	**REG4640**	**7:0**	**Default : 0x00**	**Access : R/W**
	MMC_BUS_TEST	7	Test MMC bus type through CIF Data FIFO.	
	SD_DATSYNC	6	Synchronize data bus, for SD1.1 specification.	
	SD_DEST	5	SD/MMC data transfer destination. 0: Data FIFO. 1: CIF FIFO.	
	SD_CS_EN	4	Set to enable clock auto-stop feature, which will stop CLK between read blocks when Data FIFO is full. 0: Auto-stop is disabled. 1: Auto-stop is enabled.	
	SDDRL	3	Firmware writes 1 to drive SD interface, data bus and command line low.	

FCIE3 Register (Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
	SD_DAT_LINE1	2	10: Use DAT7-0 line.	
	SD_DAT_LINE0	1	00: Use DAT0 line. 01: Use DAT3-0 line.	
	SD_CLK_EN	0	SD MIF output clock enable.	
10h (4641h)	**REG4641**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_PORT_SEL	4	SDIO port selection, 0-SDIO port1, 1-SDIO port2.	
	SD_DMA_RD_CLK_STOP	3	SD read DMA stop clock when DMA end.	
	2SD_1CLK_SRC	2	Clock control of card port, when SDIO port active. 0: Clock off. 1: Clock on.	
	SDIO_SD_BUS_SW	1	SDIO interface and SD/MMC card interface select. Default is SD/MMC card interface active and SDIO interface idle. Set 1 to have SDIO interface go active, and SD/MMC card interface stay idle.	
	SDIO_RDWAIT	0	When reading block data while Data FIFO is busy, hardware will drive SD_DAT1 to low, to inform card controller that host is busy. Active high.	
11h (4644h)	**REG4644**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SD_DTRX_DIR	4	SD/MMC data transfer direction. 0: Read from card. 1: Write to card.	
	SD_DTRX_EN	3	SD/MMC data transmit/receive enable (job finish auto clear).	
	SD_CMD_EN	2	SD/MMC transmit command enable (job finish auto clear).	
	SD_RSP_EN	1	SD/MMC receive command response enable.	
	SD_RSPR2_EN	0	SD/MMC receive command response for R2 type.	
11h (4645h)	**REG4645**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

FCIE3 Register (Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
	SDIO_DET_INT_SRC	3	SDIO interrupt source selection in sdio_int_mod=0 or 1. 0-edge trigger, 1-level trigger.	
	SDIO_DET_ON	2	SDIO interrupt detect function switch, active high.	
	SDIO_INT_MOD1	1	SDIO_INT_MOD = 10: Single block read/write interrupt detect. SDIO_INT_MOD = 11: Multi-block read/write interrupt detect.	
	SDIO_INT_MOD0	0	SDIO_INT_MOD = 00: Continuous interrupt detect. SDIO_INT_MOD = 01: CMD12 or IO Abort command interrupt detect.	
12h (4648h)	**REG4648**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	SD_CARD_BUSY	6	SD card busy status, 1-SD card busy.	
	SD_WR_PRO_N	5	SD card write protect.	
	SD_CMDRSP_CERR	4	Received command phase: Response CRC error event.	
	SD_CMD_NORSP	3	Transmitted command phase: Response timeout event (time out = 64 clocks), which means there is no response on CMD line.	
	SD_DAT_STSNEG	2	Transmitted data phase: "CRC status = negative" from SD/MMC card, which means a transmission error has occurred, and host needs to resend data.	
	SD_DAT_STSERR	1	Transmitted data phase: "CRC status = error" from SD/MMC card, which means SD/MMC card has encountered a flash program error.	
	SD_DAT_CERR	0	Received data phase CRC error event.	
12h (4649h)	**REG4649**	**7:0**	**Default : 0x00**	**Access : RO**
	SD_DAT7	7	SD DATA Line 7.	
	SD_DAT6	6	SD DATA Line 6.	
	SD_DAT5	5	SD DATA Line 5.	
	SD_DAT4	4	SD DATA Line 4.	

FCIE3 Register (Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
	SD_DAT3	3	SD DATA Line 3.	
	SD_DAT2	2	SD DATA Line 2.	
	SD_DAT1	1	SD DATA Line 1.	
	SD_DAT0	0	SD DATA Line 0.	
13h (464Ch)	**REG464C**	**7:0**	**Default : 0x00**	**Access : R/W**
	BS_DLY2	7	MSPro BS line output delay select bit 2.	
	BS_DLY1	6	MSPro BS line output delay select bit 1.	
	BS_DLY0	5	MSPro BS line output delay select bit 0.	
	DAT_DLY2	4	MSPro data line output delay select bit 2.	
	DAT_DLY1	3	MSPro data line output delay select bit 1.	
	DAT_DLY0	2	MSPro data line output delay select bit 0.	
	MS_DAT_LINE1	1	01: Use DAT3-0 line.	
	MS_DAT_LINE0	0	00: Use DAT0 line.	
13h (464Dh)	**REG464D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	MSP_DELAY_EN	4	MSPro bus add delay cell enable.	
	TPC3	3	MS/MSPro Transfer Protocol Command register bit 3.	
	TPC2	2	MS/MSPro Transfer Protocol Command register bit 2.	
	TPC1	1	MS/MSPro Transfer Protocol Command register bit 1.	
	TPC0	0	MS/MSPro Transfer Protocol Command register bit 0.	
14h (4650h)	**REG4650**	**7:0**	**Default : 0x00**	**Access : R/W**
	MSP_CTL_DELAY_SEL_9_0[1:0]	7:6	MSPro control signal delay cell selection. [1:0]: select 4 delay cells on msp_dat0. [3:2]: select 4 delay cells on msp_dat1. [5:4]: select 4 delay cells on msp_dat2. [7:6]: select 4 delay cells on msp_dat3. [9:8]: select 4 delay cells on msp_bs.	
	MSP_CTL_DELAY_EN	5	MSPro control signal delay cell enable.	

FCIE3 Register (Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
	MS_DEST	4	Setting with MS_DTRX_EN. 0: Page data (512 bytes) transferred to Data FIFO. 1: Page data (512 bytes) transferred to CIF FIFO.	
	MS_BURST	3	MS/MSPro burst mode enable.	
	MS_BUS_DIR	2	MS/MSPro transfer bus direction. 0: Read from card. 1: Write to card (must be set along with MS_REGTRX_EN or MS_DTRX_EN).	
	MS_DTRX_EN	1	MS/MSPro data transfer enable. (job finish auto clear).	
	MS_REGTRX_EN	0	MS/MSPro register transfer enable. (Job finish auto clear).	
14h (4651h)	**REG4651**	**7:0**	**Default : 0x00**	**Access : R/W**
	MSP_CTL_DELAY_SEL_9_0[9:2]	7:0	See description of '4650h'.	
15h (4654h)	**REG4654**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:6	Reserved.	
	MS_CERR	5	MS/MSPro data bus CRC error.	
	MS_TOUT	4	MS/MSPro response handshaking timeout.	
	MS_DAT3	3	MSPro data line 3 status.	
	MS_DAT2	2	MSPro data line 2 status.	
	MS_DAT1	1	MSPro data line 1 status.	
	MS_DAT0	0	MS/MSPro data line 0 status.	
15h (4655h)	**REG4655**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	MS_CTL_DELAY_SEL_3_0[3:0]	4:1	MS control signal delay cell selection. [1:0]: select 4 delay cells on ms_dat0. [3:2]: select 4 delay cells on ms_bs.	
	MS_CTL_DELAY_EN	0	MS control signal delay cell enable.	
1Bh (466Ch)	**REG466C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_BLK_SIZE12_0[7:0]	7:0	SDIO block size[12:0] (1~2047 bytes). 13'h001: 1 byte. 13'h200: 512 bytes. 13'h400: 1024 bytes.	
1Bh	**REG466D**	**7:0**	**Default : 0x00**	**Access : R/W**

FCIE3 Register (Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
(466Dh)	SDIO_BLK_MOD	7	SDIO block mode enable.	
	-	6:5	Reserved.	
	SDIO_BLK_SIZE12_0[12:8]	4:0	See description of '466Ch'.	
1Ch (4670h)	**REG4670**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR15_0[7:0]	7:0	SDIO memory address[15:0] (byte offset).	
1Ch (4671h)	**REG4671**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR15_0[15:8]	7:0	See description of '4670h'.	
1Dh (4674h)	**REG4674**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MEM_ADDR28_16[7:0]	7:0	SDIO memory address[28:16] (byte offset).	
1Dh (4675h)	**REG4675**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SDIO_MEM_ADDR28_16[12:8]	4:0	See description of '4674h'.	
1Eh (4678h)	**REG4678**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SDIO_DAT3_0[3:0]	3:0	SDIO data lines 3-0.	
1Eh (4679h)	**REG4679**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SDIO2_DAT3_0[3:0]	3:0	SDIO2 data lines 3-0.	
1Fh (467Ch)	**REG467C**	**7:0**	**Default : 0x00**	**Access : RO**
	NC_R2N_COUNT_9_0[1:0]	7:6	RIU2NAND word counter[9:0].	
	NC_R2N_CS[3:0]	5:2	RIU2NAND state machine.	
	NFC2MI_RW	1	DMA read/write direction. 0: MIU/RIU to NAND. 1: NAND to MIU/RIU.	
	-	0	Reserved.	
1Fh (467Dh)	**REG467D**	**7:0**	**Default : 0x00**	**Access : RO**
	NC_R2N_COUNT_9_0[9:2]	7:0	See description of '467Ch'.	
20h (4680h)	**REG4680**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	R2N_DO_END	6	Assert a pulse to end RIU write to NAND. Set by SW, auto clear by HW.	
	R2N_DO_EN	5	Assert a pulse for RIU write each word to NAND. Set by SW, auto clear by HW.	

FCIE3 Register (Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
	R2N_DO_START	4	Assert a pulse to start RIU write to NAND. Set by SW, auto clear by HW.	
	R2N_DI_END	3	Assert a pulse to end RIU read from NAND. Set by SW, auto clear by HW.	
	R2N_DI_EN	2	Assert a pulse for RIU read each word from NAND. Set by SW, auto clear by HW.	
	R2N_DI_START	1	Assert a pulse to start RIU read from NAND. Set by SW, auto clear by HW.	
	R2N_MODE	0	Enable RIU directly access NAND instead of MIU.	
20h (4681h)	**REG4681**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	NC_R2N_COUNT_11_10[1:0]	7:6	RIU2NAND word counter[11:10].	
	NFIE_DOH4_DLY1	5	Delay type = 0, 1, 2, 3.	
	NFIE_DOH4_DLY0	4	MSB data bus 4 delay cells selection.	
	NFIE_DOL4_DLY1	3	Delay type = 0, 1, 2, 3.	
	NFIE_DOL4_DLY0	2	LSB data bus 4 delay cells selection.	
	NFIE_DO_DLY_EN	1	Enable nfie2pad_do[7:0] delay for SSO issue.	
	-	0	Reserved.	
21h (4684h)	**REG4684**	**7:0**	**Default : 0x00**	**Access : RO**
	NC_R2N_DI_DATA[7:0]	7:0	Data port for RIU read data from NAND.	
21h (4685h)	**REG4685**	**7:0**	**Default : 0x00**	**Access : RO**
	NC_R2N_DI_DATA[15:8]	7:0	See description of '4684h'.	
22h (4688h)	**REG4688**	**7:0**	**Default : 0x00**	**Access : R/W**
	R2N_DO_DATA[7:0]	7:0	Data port for RIU write data to NAND.	
22h (4689h)	**REG4689**	**7:0**	**Default : 0x00**	**Access : R/W**
	R2N_DO_DATA[15:8]	7:0	See description of '4688h'.	
25h (4694h)	**REG4694**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CIFD_RD_REQ	1	Force read CIF Data FIFO 512 bytes.	
	CIFC_RD_REQ	0	Force read function on CIF Command FIFO 64 bytes.	
25h (4695h)	**REG4695**	**7:0**	**Default : 0x00**	**Access : R/W**
	NFIE_DOH4_16B_DLY1	7	Delay type = 0, 1, 2, 3.	
	NFIE_DOH4_16B_DLY0	6	MSB data bus 4 delay cells selection.	

FCIE3 Register (Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
	NFIE_DOL4_16B_DLY1	5	Delay type = 0, 1, 2, 3.	
	NFIE_DOL4_16B_DLY0	4	LSB data bus 4 delay cells selection.	
	NFIE_DO_16B_DLY_EN	3	Enable nfie2pad_do[15:8] delay for SSO issue.	
	-	2:0	Reserved.	
2Dh (46B4h)	**REG46B4**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7	Reserved.	
	NAND_STOP_CE1Z_MASK	6	Mask nand ce1z inactive at read data phase while sharing data pad with DISP.	
	NAND_STOP_CEZ_MASK	5	Mask nand cez inactive at read data phase while sharing data pad with DISP.	
	SRAM_CGEN	4	SARM clock gating.	
	-	3:0	Reserved.	
2Dh (46B5h)	**REG46B5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	NAND_DATA_REORDER[1:0]	1:0	NAND data pin reordering:. 2'b00: 15~0;. 2'b01: 0~15;. 2'b10: 7~0, 8~15;. 2'b11: 8~15,0~7;.	
2Eh	**REG46B8**	**7:0**	**Default : 0xFF**	**Access : R/W**

FCIE3 Register (Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
(46B8h)	BYTE_VLD_7_0[7:0]	7:0	MIU bus width is 64-bit, SW can select byte offset position for DMA transmission. BYTE_VLD[7:0]: hFF, valid data start on bus [63:0]. BYTE_VLD[7:0]: hFE, valid data start on bus [63:8]. BYTE_VLD[7:0]: hFC, valid data start on bus [63:16]. BYTE_VLD[7:0]: hF8, valid data start on bus [63:24]. BYTE_VLD[7:0]: hF0, valid data start on bus [63:32]. BYTE_VLD[7:0]: hE0, valid data start on bus [63:40]. BYTE_VLD[7:0]: hC0, valid data start on bus [63:48]. BYTE_VLD[7:0]: h80, valid data start on bus [63:56].	
30h (46C0h)	**REG46C0**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	CF_PAD_SWAP	7	CF pad function swap.	
	SD_PAD_SWAP	6	SD pad function swap.	
	XD_BUS_PORT_SEL	5	XD pad function swap.	
	CMD_BISTFAIL	4	CMD FIFO 128-byte BIST Test Fail.	
	CIFD_BISTFAIL	3	CIF FIFO_D 512-byte BIST Test Fail.	
	CIFC_BISTFAIL	2	CIF FIFO_C 64-byte BIST Test Fail.	
	DBFB_BISTFAIL	1	Data FIFO_B 512-byte BIST Test Fail.	
	DBFA_BISTFAIL	0	Data FIFO_A 512-byte BIST Test Fail.	
30h (46C1h)	**REG46C1**	**7:0**	**Default : 0x58**	**Access : R/W**
	XD_NAND_COBUS	7	NAND and XD/SD interface shared bus, Active high.	
	PING_PONG_FIFO_CLK_EN	6	Ping pong fifo clock enable.	
	ENDIAN_SEL	5	Endian select. Low: Little endian. High: Big endian.	
	FCIE_SOFT_RST	4	FCIE module software reset, active low, uP program.	

FCIE3 Register (Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
	SD_MS_COBUS	3	SD and MS interface shared bus, 4-bit mode bus. MS 4-bit data bus is shared with SD 4-bit bus, and MS_BS is shared with SD_CMD. Active high.	
	DEBUG_MOD[2:0]	2:0	DEBUG_MOD [2:0] definition. 0: Disp_nand_padmux. 1: SD. 2: MS serial mode + SM. 3: MS parallel mode. 4: CF. 5: MMA. 6: DFF. 7: Nand.	
31h (46C4h)	**REG46C4**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_15_0[7:0]	7:0	Debug bus [15:0].	
31h (46C5h)	**REG46C5**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_15_0[15:8]	7:0	See description of '46C4h'.	
32h (46C9h)	**REG46C9**	**7:0**	**Default : 0x00**	**Access : RO**
	FCIE_DBUS_23_16[7:0]	7:0	Debug bus [23:16].	
34h (46D0h)	**REG46D0**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SD_POWER_RD_MASK[7:0]	7:0	Power save mode, read data mask bits, 0-mask, 1-valid.	
34h (46D1h)	**REG46D1**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SD_POWER_RD_MASK[15:8]	7:0	See description of '46D0h'.	
35h (46D4h)	**REG46D4**	**7:0**	**Default : 0x08**	**Access : RO, R/W**
	BAT_SAVE_EVENT	7	Power save mode status, Battery lost event occurred, clear by reg_sd_power_save_rst=0.	
	RST_SAVE_EVENT	6	Power save mode status, Reset event occurred, clear by reg_sd_power_save_rst=0.	
	RIU_SAVE_EVENT	5	Power save mode status, RIU emulation event occurred, clear by reg_sd_power_save_rst=0.	
	-	4	Reserved.	
	SD_POWER_SAVE_RST	3	Software reset Power Save HW, default is '1', set '0' to reset HW.	
	POWER_SAVE_MODE_INT_EN	2	Power Save interrupt enable, high active.	

FCIE3 Register (Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
	SD_POWER_SAVE_RIU	1	SW set register to emulate power lost event, high active.	
	POWER_SAVE_MODE	0	Power Save HW enable, high active.	
37h (46DCh)	**REG46DC**	**7:0**	**Default : 0x00**	**Access : R/W**
	NAND_CTL_DELAY_SEL_11_0[7:0]	7:0	Nand control signal delay cell selection. [2:0]: select 8 delay cells on nf_rez. [5:3]: select 8 delay cells on nf_wez. [8:6]: select 8 delay cells on nf_cle. [11:9]: select 8 delay cells on nf_ale.	
37h (46DDh)	**REG46DD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	NAND_CTL_DELAY_EN	4	Nand control signal delay cell enable.	
	NAND_CTL_DELAY_SEL_11_0[11:8]	3:0	See description of '46DCh'.	
38h (46E0h)	**REG46E0**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_26_16[7:0]	7:0	MIU write range protection, minimum address pointer 27 bits (MIU width is 32 bits), address[26:16].	
38h (46E1h)	**REG46E1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	FORCE_MIU_WR_RANGE_ERR	4	Force MIU write protection out of range event.	
	MIU_WR_RANGE_ENABLE	3	MIU write protection function enable.	
	RANGE_MIN_BYTE_ADDRESS_26_16[10:8]	2:0	See description of '46E0h'.	
39h (46E4h)	**REG46E4**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_15_0[7:0]	7:0	MIU write range protection, minimum address pointer 26 bits (MIU width is 32 bits), address[15:0].	
39h (46E5h)	**REG46E5**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MIN_BYTE_ADDRESS_15_0[15:8]	7:0	See description of '46E4h'.	
3Ah (46E8h)	**REG46E8**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_26_16[7:0]	7:0	MIU write range protection, maximum address pointer 26 bits (MIU width is 32 bits), address[26:16].	
3Ah (46E9h)	**REG46E9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	RANGE_MAX_BYTE_ADDRESS_26_16[10:8]	2:0	See description of '46E8h'.	

FCIE3 Register (Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
3Bh (46ECh)	**REG46EC**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_15_0[7:0]	7:0	MIU write range protection, maximum address pointer 26 bits (MIU width is 32 bits), address[15:0].	
3Bh (46EDh)	**REG46ED**	**7:0**	**Default : 0x00**	**Access : R/W**
	RANGE_MAX_BYTE_ADDRESS_15_0[15:8]	7:0	See description of '46ECh'.	
3Ch (46F0h)	**REG46F0**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_26_16[7:0]	7:0	MIU write range protection error address. MIU_WRRANGE_ERR_ADDR_26_16.	
3Ch (46F1h)	**REG46F1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	MIU_WRRANGE_ERR_ADDR_26_16[10:8]	2:0	See description of '46F0h'.	
3Dh (46F4h)	**REG46F4**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_15_0[7:0]	7:0	MIU write range protection error address,. MIU_WRRANGE_ERR_ADDR_15_0.	
3Dh (46F5h)	**REG46F5**	**7:0**	**Default : 0x00**	**Access : RO**
	MIU_WRRANGE_ERR_ADDR_15_0[15:8]	7:0	See description of '46F4h'.	
40h (4700h)	**REG4700**	**7:0**	**Default : 0x04**	**Access : R/W**
	NC_CHK_RB_STS_DIS	7	While executing wait_rb instruction, state machine checks R/B falling and rising edge status. 0: Enable. 1: Disable.	
	NC_CHK_RB_HIGH	6	While executing wait_rb instruction, state machine checks R/B high by delay 3 cycles instead of checking R/B low first. 0: Disable. 1: Enable.	
	NC_WP_AUTO	5	NAND WPZ controlled by hardware instead of firmware. 0: Software control. 1: Hardware auto mode.	
	NC_WP_EN	4	NAND WPZ controlled by software. 0: WPZ is Low. 1: WPZ is High.	

FCIE3 Register (Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
	NC_CE_AUTO	3	NAND CE controlled by hardware instead of firmware. 0: Software control. 1: Hardware auto mode.	
	NC_CE_EN	2	NAND CE controlled by software. 0: CEZ is Low. 1: CEZ is High.	
	NC_CE_SEL[1:0]	1:0	NAND Flash CE Chip Select 0/1/2/3. 00: Select CEZ. 01: Select CE1Z. 10: Select CE2Z. 11: Select CE3Z.	
40h (4701h)	**REG4701**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_BYTE0[3:0]	7:4	Reserved.	
	NC_INST_DELAY_NUM[3:0]	3:0	Cycle count for delay instruction execute.	
41h (4704h)	**REG4704**	**7:0**	**Default : 0x00**	**Access : R/W**
	NC_RD_HW[1:0]	7:6	Cycle count for RDJ high width.	
	NC_WR_LW[2:0]	5:3	Cycle count for WRJ low width.	
	NC_WR_HW[2:0]	2:0	Cycle count for WRJ high width. 000: 1 clock cycle. 001: 2 clock cycle. 010: 3 clock cycle. 011: 4 clock cycle. 100: 5 clock cycle. 101: 6 clock cycle. 110: 7 clock cycle. 111: 8 clock cycle.	
41h (4705h)	**REG4705**	**7:0**	**Default : 0x00**	**Access : R/W**
	NC_BCH_DEB_SEL	7	Debug mode signals mux out selection. 0: Ecc bch_top group0_dbus. 1: Ecc bch_top group1_dbus.	

FCIE3 Register (Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
	NC_DEB_SEL[2:0]	6:4	Debug mode signals mux out selection. 000: Disable. 001: Dpif_dbus. 010: Bramctrl_dbus. 011: Ecc_dbus. 100: Nfcas_dbus. 101: Instq_dbus.	
	NC_RD_LW[2:0]	3:1	Cycle count for RDJ low width.	
	NC_RD_HW[2]	0	See description of '4704h'.	
42h (4708h)	**REG4708**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	NC_STCHK_ERRH8	1	Status check for High 8 Data Bus. 0: OK. 1: Error.	
	NC_STCHK_ERRL8	0	Status check for Low 8 Data Bus. 0: OK. 1: Error.	
43h	**REG470C**	**7:0**	**Default : 0x00**	**Access : R/W**

FCIE3 Register (Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
(470Ch)	NC_AUXREG_ADR_WD[7:0]	7:0	Word address. 0x00 ~ 0x07 Command Registers (Hard Wired, Read Only). 0x08 ~ 0x0A Command Registers (R/W). 0x0B ~ 0x16 Address Register Sets (COL2+ROW4) x4. 0x18 Repeat count (10 bits). 0x19 Random data count. (10 bits, read data must be word alignment). ex: (1) read 6 bytes data => 0x44 should be 10h'006. ex: (2) read 7 bytes data => 0x44 should be 10h'008. ex: (3) write 6 bytes data => 0x44 should be 10h'006. ex: (4) write 7 bytes data => 0x44 should be 10h'007. 0x1A Random address offset. (8 bits, CIF_D address). 0x1B Status Check Mask(H8), Expect(L8). 0x1C Wait_Idle_Cnt (8 bits) for Wait_Idle_Inst. 0x20 ~ 0x2F Instruction Queue.	
44h (4710h)	**REG4710**	**7:0**	**Default : 0x00**	**Access : R/W**
	NC_AUXREG_DATA[7:0]	7:0	16 bit data port for Auxiliary Registers. 1. 0x44 Write can be consecutive once 0x43 set. 2. 0x44 Read CAN'T be consecutive due to riu_w as clock. Must write 0x43 first then read 0x44.	
44h (4711h)	**REG4711**	**7:0**	**Default : 0x00**	**Access : R/W**
	NC_AUXREG_DATA[15:8]	7:0	See description of '4710h'.	
45h (4714h)	**REG4714**	**7:0**	**Default : 0x00**	**Access : R/W**
	NC_INST_HB_SEL	7	Instruction Queue Address Higher Bank selection while job start. 0: 00~0F. 1: 10~1F.	

FCIE3 Register (Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
	NC_NONEFF_NUM[1:0]	6:5	Set the number of none "ECC_DI !=0Xffff " for skipping ECC check(treated as blank data). 00: Skip ECC when there is "ECC_DI !=0xFFFF". 01: Skip ECC when there is 2 "ECC_DI !=0xFFFF". 10: Skip ECC when there is 3 "ECC_DI !=0xFFFF". 11: Skip ECC when there is 4 "ECC_DI !=0xFFFF".	
	-	4	Reserved.	
	NC_DIR_DOWNSTREAM	3	NAND Flash data transfer direction for data FIFO (MIU). 0: Read from flash. 1: Write to flash.	
	NC_INST_HB_SEL_RPT	2	Instruction Queue Address Higher Bank selection while repeat. 0: 00~0F. 1: 10~1F.	
	NC_CIFC_ACCESS	1	NAND Controller directly access CIF_C. 0: Disable. 1: Enable.	
	NC_JOB_START	0	Start to execute instruction queue from 1st byte and exit until BREAK or error encountered.	
45h (4715h)	**REG4715**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	CHK_ALLONE	1	Check if all one when page read.	
	CHK_ALLZERO	0	Check if all zero when page read.	
46h (4718h)	**REG4718**	**7:0**	**Default : 0x00**	**Access : RO**
	NF_STCHK_DI_L8[7:0]	7:0	Low 8 Status Read from NAND Flash after issuing Check Status command "70".	
46h (4719h)	**REG4719**	**7:0**	**Default : 0x00**	**Access : RO**
	NF_STCHK_DI_H8[7:0]	7:0	High 8 Status Read from NAND Flash after issuing Check Status command "70".	
47h	**REG471C**	**7:0**	**Default : 0x00**	**Access : R/W**

FCIE3 Register (Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
(471Ch)	NC_SER_PART_START_INDEX[0]	7	The sector index which to start this serial partial transaction when NC_SER_PART_MODE = 1. 6'h00: start from 1st sector. 6'h01: start from 2nd sector. 6'h02: start from 3rd sector. 6'h03: start from 4th sector. ..... 6'h3F: start from 63rd sector.	
	NC_SER_PART_CNT[5:0]	6:1	Transfer sector count to hit when NC_SER_PART_MODE = 1. (Note: total sector size should be less than page size). 6'h00: 1 sector. 6'h01: 2 sectors. 6'h02: 3 sectors. 6'h03: 4 sectors. ..... 6'h3F: 63 sectors.	
	NC_SER_PART_MODE	0	Serial Partial Mode. If set, in action SER_DATA_IN/SER_DATA_OUT, data transferred are sector size bytes xN.	
47h (471Dh)	**REG471D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	NC_SER_PART_START_INDEX[5:1]	4:0	See description of '471Ch'.	
48h (4720h)	**REG4720**	**7:0**	**Default : 0x00**	**Access : R/W**
	SECTOR_SPARE_SIZE[7:0]	7:0	Spare area size of each sector in NAND FLASH. (Must be word alignment, bit[0] should be zero).	
48h (4721h)	**REG4721**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	NC_ONE_COL_ADR	5	Flash Address contains only one column address cycle. 0: 2 column address bytes. 1: 1 column address byte (use MSB of column address register).	
	NC_AUTO_RANDOM_DIS	4	Disable hardware auto support Nand flash random read/write command (Random Data Read 05-E0.Random Data Input 85).	

FCIE3 Register (Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
	NC_RANDOM_MODE	3	NAND random IN/OUT access enable. (Data transfer to CIFD or Spare MIU address, depend on reg_spare_dest).	
	NC_SPARE_ECC_BYPASS	2	Not protect ecc for spare data (only BCH used).	
	NC_SPARE_BYPASS	1	If set, don't write spare area to CIFD (nc_cifc_wen tied to 1).	
	SPARE_DEST	0	NAND spare area data destination/source. 0: Transfer spare data to/from CIFD. 1: Transfer spare data to/from Ping-pong FIFO (MIU).	
49h (4724h)	**REG4724**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPARE_SIZE[7:0]	7:0	Total spare area size of each page in NAND FLASH (must be word alignment, bit[0] should be zero).	
49h (4725h)	**REG4725**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SPARE_SIZE[10:8]	2:0	See description of '4724h'.	
4Ah (4728h)	**REG4728**	**7:0**	**Default : 0x00**	**Access : R/W**
	NC_RPT_ADR2_SEL[1:0]	7:6	Select NAND Address2 incremented unit while repeat. 000: 9'h001. 001: 9'h002. 010: 9'h004. 011: 9'h020. 100: 9'h040. 101: 9'h080. 110: 9'h100. 111: 9'h000.	
	NC_RPT_ADR1_SEL[2:0]	5:3	Select NAND Address1 incremented unit while repeat. 000: 9'h001. 001: 9'h002. 010: 9'h004. 011: 9'h020. 100: 9'h040. 101: 9'h080. 110: 9'h100. 111: 9'h000.	

FCIE3 Register (Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
	NC_RPT_ADR0_SEL[2:0]	2:0	Select NAND Address0 incremented unit while repeat. 000: 9'h001. 001: 9'h002. 010: 9'h004. 011: 9'h020. 100: 9'h040. 101: 9'h080. 110: 9'h100. 111: 9'h000.	
4Ah (4729h)	**REG4729**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	NC_RPT_ADR3_SEL[2:0]	3:1	Select NAND Address3 incremented unit while repeat. 000: 9'h001. 001: 9'h002. 010: 9'h004. 011: 9'h020. 100: 9'h040. 101: 9'h080. 110: 9'h100. 111: 9'h000.	
	NC_RPT_ADR2_SEL[2]	0	See description of '4728h'.	
4Bh (472Ch)	**REG472C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SIGN_EXPECT_DATA0[7:0]	7:0	NAND Signature check: expect data 0.	
4Bh (472Dh)	**REG472D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SIGN_EXPECT_DATA1[7:0]	7:0	NAND Signature check: expect data 1.	
4Ch (4730h)	**REG4730**	**7:0**	**Default : 0x00**	**Access : R/W**
	SIGN_COMP_ADDR0[7:0]	7:0	NAND Signature check: compare address 0.	
4Ch (4731h)	**REG4731**	**7:0**	**Default : 0x00**	**Access : R/W**
	SIGN_COMP_ADDR1[7:0]	7:0	NAND Signature check: compare address 1.	
4Dh (4734h)	**REG4734**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:5	Reserved.	
	SIGN_MISMATCH1_STS	4	NAND Signature check: Status check for data 1 (0: OK / 1: Mismatch).	
	SIGN_MISMATCH0_STS	3	NAND Signature check: Status check for data 0 (0: OK / 1: Mismatch).	

FCIE3 Register (Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
	SIGN_CLR_STS	2	NAND Signature check: clear mismatch status.	
	SIGN_STOP_RUN	1	NAND Signature check: when data mismatch, stop run.	
	SIGN_CHECK_EN	0	NAND Signature check: enable.	
4Eh (4738h)	**REG4738**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPARE_MEM_ADDR15_0[7:0]	7:0	NAND spare memory address[15:0] (byte offset).	
4Eh (4739h)	**REG4739**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPARE_MEM_ADDR15_0[15:8]	7:0	See description of '4738h'.	
4Fh (473Ch)	**REG473C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPARE_MEM_ADDR28_16[7:0]	7:0	NAND spare memory address[28:16] (byte offset).	
4Fh (473Dh)	**REG473D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPARE_MEM_ADDR28_16[12:8]	4:0	See description of '473Ch'.	
50h (4740h)	**REG4740**	**7:0**	**Default : 0x00**	**Access : R/W**
	NC_ECCERR_NSTOP	7	NAND Flash "ECC Uncorrectable Error None Stop" while upstream (NAND -> MIU). 0: Disable. 1: Enable.	

FCIE3 Register (Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description
	NC_ECC_MODE[3:0]	6:3	Select ecc algorithm mode. 4'b0000: 512 bytes, BCH code, 4-bit correct ability. 4'b0001: 512 bytes, BCH code, 8-bit correct ability. 4'b0010: 512 bytes, BCH code, 12-bit correct ability. 4'b0011: 512 bytes, BCH code, 16-bit correct ability. 4'b0100: 512 bytes, BCH code, 20-bit correct ability. 4'b0101: 512 bytes, BCH code, 24-bit correct ability. 4'b0110: 1K bytes, BCH code, 24-bit correct ability. 4'b0111: 1K bytes, BCH code, 32-bit correct ability. 4'b1000: 512 bytes, RS code, 4 symbol correct ability. 4'b1001 ~ 4'b1111: reserved.
	NC_PAGE_MODE[2:0]	2:0	Select nand page size. 3'b000: 512 bytes. 3'b001: 2K bytes. 3'b010: 4K bytes. 3'b011: 8K bytes. 3'b100: 16K bytes. 3'b101: 32K bytes. 3'b110 ~ 3'b111: reserved.
50h (4741h)	**REG4741**	**7:0**	**Default : 0x00** **Access : R/W**
	NC_WORD_MODE	7	NAND data bus width 0: 8 bits 1: 16 bits.
	NC_SHARE_PAD_EN	6	NAND share pad with DISP IP 0: disable 1: enable.
	-	5:3	Reserved.
	NC_ECC_BYPASS	2	Bypass ECC (skip ECC check/generate) while data transfer upstream or downstream (redundant area CIF_C being written for upstream but not for downstream). 0: Disable. 1: Enable.

FCIE3 Register (Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
	NC_ALLONE_ECC_CHECK	1	Enable NAND erase block ecc check.	
	NC_DYNGATED_EN	0	Dynamic Gated Clock enable. 0: Disable 1: enable.	
51h (4744h)	**REG4744**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	MAX_ECC_COR_NUM[5:0]	6:1	Maximum number of ECC correctable error bits in a sector during this DMA transaction.	
	ECC_ERROR_FLAG	0	ECC Uncorrectable error happened during this DMA transaction.	
51h (4745h)	**REG4745**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	NC_ECC_SEC_CNT[5:0]	5:0	Current sector count when ECC uncorrectable error (NC_ECC_FLAG = 0x10) happens.	
52h (4748h)	**REG4748**	**7:0**	**Default : 0x00**	**Access : RO**
	DMA_ECC_COR_NUM[7:0]	7:0	Total sector count of which has ECC correctable error happened during this DMA transaction.	
52h (4749h)	**REG4749**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DMA_ECC_COR_NUM[11:8]	3:0	See description of '4748h'.	
53h (474Ch)	**REG474C**	**7:0**	**Default : 0x00**	**Access : RO**
	ECC_ERROR_NUM[5:0]	7:2	Number of correctable error.	
	NC_ECC_FLAG[1:0]	1:0	ECC Flag. 2'b00: No error encountered. 2'b01: Correctable error encountered. 2'b10: Uncorrectable error encountered. 2'b11: ECC code error. (RS code only).	
53h (474Dh)	**REG474D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	NC_SEL_ECC_LOC[4:0]	4:0	Select ecc error location.	
54h (4750h)	**REG4750**	**7:0**	**Default : 0x00**	**Access : RO**
	ECC_ERROR_LOC[7:0]	7:0	ECC Error location.	
54h (4751h)	**REG4751**	**7:0**	**Default : 0x00**	**Access : RO**
	ECC_ERROR_LOC[15:8]	7:0	See description of '4750h'.	
55h	**REG4754**	**7:0**	**Default : 0x05**	**Access : R/W**

FCIE3 Register (Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
(4754h)	NF_READ_CMD0[7:0]	7:0	Configure command0 for auto random read.	
55h (4755h)	**REG4755**	**7:0**	**Default : 0xE0**	**Access : R/W**
	NF_READ_CMD1[7:0]	7:0	Configure command1 for auto random read.	
56h (4758h)	**REG4758**	**7:0**	**Default : 0x85**	**Access : R/W**
	NF_WRITE_CMD[7:0]	7:0	Configure command for auto random write.	
56h (4759h)	**REG4759**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	NC_HWCMD_DELAY_NUM[3:0]	3:0	Cycle count for delay auto random command execute.	

RTC Register (Bank = 24)

RTC Register (Bank = 24)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (4800h)	**REG4800**	**7:0**	**Default : 0x34**	**Access : RO, R/W**
	PG_VRTC	7	Power good of ldo vrtc.	
	VDD_RTC_STATUS	6	VDD_RTC power good status. Auto set to 1 when reg_load_en. Can be sw reset by reg_pg_rst.	
	EN_MSKCMP_SUBCNT	5	Enable mask compare subcnt. 0: Mask compare subcnt (default). 1: Unmask compare subcnt.	
	CNT_EN	4	Enable RTC count.	
	PG_RST	3	Reset power good register.	
	RTC_RST	2	Software reset // reset rtc_cal and rtc_irq.	
	LOAD_EN	1	Enable load for loading value into RTC counter.	
	VDD_RTC_GOOD	0	VDD_RTC power good status.	
00h (4801h)	**REG4801**	**7:0**	**Default : 0x00**	**Access : RO**
	BGOK_MUX	7	Bankgap mux ok flag; read only flag.	
	CHRG_PGIN	6	Charger plug-in flag; read only flag.	
	PG_STDLDO	5	Std ldo power good; read only flag.	
	REF_BKLDO_OK	4	Buck reference and std ldo ok flag; read only flag.	
	REF_OK	3	Reference gen ok flag; read only flag.	
	BG_OK	2	Bankgap ok flag; read only flag.	
	PG_VABB	1	Vabb power good flag; read only flag.	
	RTC_32K_OK	0	Rtc 32k ok flag.	
01h (4804h)	**REG4804**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOAD_VAL[7:0]	7:0	RTC counter load value.	
01h (4805h)	**REG4805**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOAD_VAL[15:8]	7:0	See description of '4804h'.	
02h (4808h)	**REG4808**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOAD_VAL[23:16]	7:0	See description of '4804h'.	
02h (4809h)	**REG4809**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOAD_VAL[31:24]	7:0	See description of '4804h'.	
03h (480Ch)	**REG480C**	**7:0**	**Default : 0x00**	**Access : RO**
	SEC_CNT[7:0]	7:0	Second counter; by snapshot.	

RTC Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description	
03h (480Dh)	**REG480D**	**7:0**	**Default : 0x00**	**Access : RO**
	SEC_CNT[15:8]	7:0	See description of '480Ch'.	
04h (4810h)	**REG4810**	**7:0**	**Default : 0x00**	**Access : RO**
	SEC_CNT[23:16]	7:0	See description of '480Ch'.	
04h (4811h)	**REG4811**	**7:0**	**Default : 0x00**	**Access : RO**
	SEC_CNT[31:24]	7:0	See description of '480Ch'.	
05h (4814h)	**REG4814**	**7:0**	**Default : 0x00**	**Access : RO**
	SUB_CNT[7:0]	7:0	Sub counter by snapshot (for dividing XTAL to 1 Hz).	
05h (4815h)	**REG4815**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	SUB_CNT[14:8]	6:0	See description of '4814h'.	
06h (4818h)	**REG4818**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MSKCMP_SUBCNT[7:0]	7:0	MSKCMP_SUBCNT[15:0], 1 to mask sub_cnt comapre.	
06h (4819h)	**REG4819**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MSKCMP_SUBCNT[15:8]	7:0	See description of '4818h'.	
07h (481Ch)	**REG481C**	**7:0**	**Default : 0x00**	**Access : R/W**
	FREQ_CW[7:0]	7:0	Frequency to add second counter (default is 1s).	
07h (481Dh)	**REG481D**	**7:0**	**Default : 0x80**	**Access : R/W**
	FREQ_CW[15:8]	7:0	See description of '481Ch'.	
08h (4820h)	**REG4820**	**7:0**	**Default : 0x00**	**Access : R/W**
	MATCH_VALUE[7:0]	7:0	Match value for alarm interrupt.	
08h (4821h)	**REG4821**	**7:0**	**Default : 0x00**	**Access : R/W**
	MATCH_VALUE[15:8]	7:0	See description of '4820h'.	
09h (4824h)	**REG4824**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MATCH_VALUE[23:16]	7:0	See description of '4820h'.	
09h (4825h)	**REG4825**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MATCH_VALUE[31:24]	7:0	See description of '4820h'.	
0Ah (4828h)	**REG4828**	**7:0**	**Default : 0x00**	**Access : RO**
	PMTEST	7	PMTEST flag; read only flag.	
	ONOFF	6	ONOFF flag; read only flag.	
	32K_FLAG	5	Rtc 32k flag; read only flag.	
	EN_STDLDO	4	Buck standby LDO enable; read only flag.	
	EN_BK_REFGEN	3	Buck reference gen enable; read only flag.	

RTC Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description	
	EN_REF	2	Reference gen enable; read only flag.	
	EN_BG	1	Bankgap enable; read only flag.	
	VABB_EN	0	Ldo vpm enable; read only flag.	
0Ah (4829h)	**REG4829**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	TESTBUS_SEL[3:0]	7:4	Select output testbus.	
	VABB_SET[1:0]	3:2	Select output voltage level,. [00]: 3.2V (default). [01]: 3.1V. [10]: 3.0V. [11]: 2.9V.	
	BAT_LOST_REBOOT_EN	1	Battery lost auto reboot enable. 0: Disable battery lost auto reboot. 1: Enable battery lost auto reboot.	
	ABBRESET	0	ABBRESET; read only flag.	
0Bh (482Ch)	**REG482C**	**7:0**	**Default : 0x00**	**Access : RO**
	RAW_SEC_CNT[7:0]	7:0	Raw second counter.	
0Bh (482Dh)	**REG482D**	**7:0**	**Default : 0x00**	**Access : RO**
	RAW_SEC_CNT[15:8]	7:0	See description of '482Ch'.	
0Ch (4830h)	**REG4830**	**7:0**	**Default : 0x00**	**Access : RO**
	RAW_SEC_CNT[23:16]	7:0	See description of '482Ch'.	
0Ch (4831h)	**REG4831**	**7:0**	**Default : 0x00**	**Access : RO**
	RAW_SEC_CNT[31:24]	7:0	See description of '482Ch'.	
0Dh (4834h)	**REG4834**	**7:0**	**Default : 0x00**	**Access : RO**
	RAW_SUB_CNT[7:0]	7:0	Raw sub counter (for dividing XTAL to 1 Hz).	
0Dh (4835h)	**REG4835**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	RAW_SUB_CNT[14:8]	6:0	See description of '4834h'.	
0Eh (4838h)	**REG4838**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	RTC_SNAPSHOT	0	Snapshot for real time clock. 0: No active. 1: Snapshot reg_sec_cnt and reg_sub_cnt.	
0Fh (483Ch)	**REG483C**	**7:0**	**Default : 0x00**	**Access : RO**
	RTC_FSM_STATE[7:0]	7:0	Rtc fsm state.	

RTC Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description	
0Fh (483Dh)	**REG483D**	**7:0**	**Default : 0x00**	**Access : RO**
	RTC_FSM_STATE[15:8]	7:0	See description of '483Ch'.	
10h (4840h)	**REG4840**	**7:0**	**Default : 0x00**	**Access : R/W**
	INITIAL_FLAG[7:0]	7:0	RTC initial current time.	
10h (4841h)	**REG4841**	**7:0**	**Default : 0x00**	**Access : R/W**
	INITIAL_FLAG[15:8]	7:0	See description of '4840h'.	
11h (4844h)	**REG4844**	**7:0**	**Default : 0x00**	**Access : R/W**
	INITIAL_FLAG[23:16]	7:0	See description of '4840h'.	
11h (4845h)	**REG4845**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	INITIAL_FLAG[30:24]	6:0	See description of '4840h'.	
12h (4848h)	**REG4848**	**7:0**	**Default : 0x00**	**Access : R/W**
	OFFSET_FLAG[7:0]	7:0	RTC offset time.	
12h (4849h)	**REG4849**	**7:0**	**Default : 0x00**	**Access : R/W**
	OFFSET_FLAG[15:8]	7:0	See description of '4848h'.	
13h (484Ch)	**REG484C**	**7:0**	**Default : 0x00**	**Access : R/W**
	OFFSET_FLAG[23:16]	7:0	See description of '4848h'.	
13h (484Dh)	**REG484D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	OFFSET_FLAG[30:24]	6:0	See description of '4848h'.	
14h (4850h)	**REG4850**	**7:0**	**Default : 0xFF**	**Access : R/W**
	ALARM_FLAG[7:0]	7:0	RTC alarm flag register.	
14h (4851h)	**REG4851**	**7:0**	**Default : 0xFF**	**Access : R/W**
	ALARM_FLAG[15:8]	7:0	See description of '4850h'.	
15h (4854h)	**REG4854**	**7:0**	**Default : 0xFF**	**Access : R/W**
	ALARM_FLAG[23:16]	7:0	See description of '4850h'.	
15h (4855h)	**REG4855**	**7:0**	**Default : 0x7F**	**Access : R/W**
	-	7	Reserved.	
	ALARM_FLAG[30:24]	6:0	See description of '4850h'.	
16h (4858h)	**REG4858**	**7:0**	**Default : 0xFF**	**Access : R/W**
	EVENT1_FLAG[7:0]	7:0	RTC interrupt event1 register.	
16h (4859h)	**REG4859**	**7:0**	**Default : 0xFF**	**Access : R/W**
	EVENT1_FLAG[15:8]	7:0	See description of '4858h'.	

RTC Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description	
17h (485Ch)	**REG485C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	EVENT1_FLAG[23:16]	7:0	See description of '4858h'.	
17h (485Dh)	**REG485D**	**7:0**	**Default : 0x7F**	**Access : R/W**
	-	7	Reserved.	
	EVENT1_FLAG[30:24]	6:0	See description of '4858h'.	
18h (4860h)	**REG4860**	**7:0**	**Default : 0xFF**	**Access : R/W**
	EVENT2_FLAG[7:0]	7:0	RTC interrupt event2 register.	
18h (4861h)	**REG4861**	**7:0**	**Default : 0xFF**	**Access : R/W**
	EVENT2_FLAG[15:8]	7:0	See description of '4860h'.	
19h (4864h)	**REG4864**	**7:0**	**Default : 0xFF**	**Access : R/W**
	EVENT2_FLAG[23:16]	7:0	See description of '4860h'.	
19h (4865h)	**REG4865**	**7:0**	**Default : 0x7F**	**Access : R/W**
	-	7	Reserved.	
	EVENT2_FLAG[30:24]	6:0	See description of '4860h'.	
1Ah (4868h)	**REG4868**	**7:0**	**Default : 0xFF**	**Access : R/W**
	EVENT3_FLAG[7:0]	7:0	RTC interrupt event3 register.	
1Ah (4869h)	**REG4869**	**7:0**	**Default : 0xFF**	**Access : R/W**
	EVENT3_FLAG[15:8]	7:0	See description of '4868h'.	
1Bh (486Ch)	**REG486C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	EVENT3_FLAG[23:16]	7:0	See description of '4868h'.	
1Bh (486Dh)	**REG486D**	**7:0**	**Default : 0x7F**	**Access : R/W**
	-	7	Reserved.	
	EVENT3_FLAG[30:24]	6:0	See description of '4868h'.	
1Ch (4870h)	**REG4870**	**7:0**	**Default : 0x00**	**Access : RO**
	CURRENT_FLAG[7:0]	7:0	RTC current flag.	
1Ch (4871h)	**REG4871**	**7:0**	**Default : 0x00**	**Access : RO**
	CURRENT_FLAG[15:8]	7:0	See description of '4870h'.	
1Dh (4874h)	**REG4874**	**7:0**	**Default : 0x00**	**Access : RO**
	CURRENT_FLAG[23:16]	7:0	See description of '4870h'.	
1Dh (4875h)	**REG4875**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	CURRENT_FLAG[30:24]	6:0	See description of '4870h'.	
1Eh	**REG4878**	**7:0**	**Default : 0x00**	**Access : R/W**

RTC Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description	
(4878h)	-	7:6	Reserved.	
	EVENT3_FLAG_UPDATE	5	Update RTC interrupt event3 register.	
	EVENT2_FLAG_UPDATE	4	Update RTC interrupt event2 register.	
	EVENT1_FLAG_UPDATE	3	Update RTC interrupt event1 register.	
	ALARM_FLAG_UPDATE	2	Update RTC alarm register.	
	OFFSET_FLAG_UPDATE	1	Update RTC offset time.	
	INITIAL_FLAG_UPDATE	0	Update RTC initial current time.	
1Fh (487Ch)	**REG487C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	EVENT3_INT_EN	3	RTC interrupt event3 interrupt enable.	
	EVENT2_INT_EN	2	RTC interrupt event2 interrupt enable.	
	EVENT1_INT_EN	1	RTC interrupt event1 interrupt enable.	
	ALARM_INT_EN	0	RTC alarm interrupt enable.	
20h (4880h)	**REG4880**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIFE[7:0]	7:0	RTC LIFE register.	
20h (4881h)	**REG4881**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIFE[15:8]	7:0	See description of '4880h'.	
21h (4884h)	**REG4884**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIFE[23:16]	7:0	See description of '4880h'.	
21h (4885h)	**REG4885**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIFE[31:24]	7:0	See description of '4880h'.	
22h (4888h)	**REG4888**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIFE[39:32]	7:0	See description of '4880h'.	
22h (4889h)	**REG4889**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIFE[47:40]	7:0	See description of '4880h'.	
23h (488Ch)	**REG488C**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIFE[55:48]	7:0	See description of '4880h'.	
23h (488Dh)	**REG488D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	LIFE[57:56]	1:0	See description of '4880h'.	
25h (4894h)	**REG4894**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	

RTC Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description	
	VABB_LQ_OV[1:0]	1:0	Overwrite control for VABB_LQ. [0]: VABB_LQ overwrite enable. [1]: VABB_LQ overwrite value.	
27h (489Ch)	**REG489C**	**7:0**	**Default : 0x00**	**Access : R/W**
	WD_EXPIRE[7:0]	7:0	Watch dog expired value (128hz). Need set this register at first, then set reg_watchdat_en.	
27h (489Dh)	**REG489D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	WATCHDOG_EN	4	Enable watch dog for !PAD_PWRHLD & !PMU_OFF 1second.	
	WD_EXPIRE[11:8]	3:0	See description of '489Ch'.	
28h (48A0h)	**REG48A0**	**7:0**	**Default : 0x03**	**Access : RO, R/W**
	-	7:5	Reserved.	
	ONOFF_SEL	4	On off PAD pull up/pull down selection. 0: PAD_ONOFF tie low; high level is turn-on event. 1: PAD_ONOFF tie high; low level is turn-on event.	
	SEL_STDLDO_VOUT_FLAG	3	STD LDO output voltage select.	
	ABB_REF_SEL_FLAG	2	VABB reference voltage select; real only flag.	
	SEL_STDLDO_VOUT	1	STD LDO. 0: 1.1V. 1: 1.2V (FSM set one before BUCK TRUN-ON).	
	ABB_REF_SEL	0	VABB reference voltage select. 0: Form VBG (RTC_FSM set 0 before ON_STATE). 1: From reference gen.	
29h (48A4h)	**REG48A4**	**7:0**	**Default : 0x1F**	**Access : R/W**
	-	7:5	Reserved.	
	SW_EN_STDLDO	4	Buck standby LDO enable.	
	SW_EN_BK_REFGEN	3	Buck reference gen enable.	
	SW_EN_REF	2	Reference gen enable.	
	SW_EN_BG	1	Bankgap enable.	
	SW_VABB_EN	0	Ldo vpm enable.	
29h (48A5h)	**REG48A5**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_PASSWD[7:0]	7:0	When SW_PASSWD = 8'hFF. D[4:0] will instead of RTC_FSM control.	
2Ah (48A8h)	**REG48A8**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	

RTC Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description	
	POWER_STATUS[1:0]	1:0	Keep the power status. 00: OFF mode. 01: SUSPEND mode. 10: Exhibited. 11: ON mode.	
2Bh (48ACh)	**REG48AC**	**7:0**	**Default : 0x7F**	**Access : R/W**
	RTC_IRQ_MASK[7:0]	7:0	Mask alarm interrupt.	
2Ch (48B0h)	**REG48B0**	**7:0**	**Default : 0x00**	**Access : R/W**
	RTC_IRQ_FORCE[7:0]	7:0	Force alarm interrupt to be 1.	
2Dh (48B4h)	**REG48B4**	**7:0**	**Default : 0x00**	**Access : R/W**
	RTC_IRQ_CLR[7:0]	7:0	Clear alarm interrupt.	
2Eh (48B8h)	**REG48B8**	**7:0**	**Default : 0x00**	**Access : RO**
	RTC_IRQ_RAW_STATUS[7:0]	7:0	RTC IRQ raw status: [7]: Reserved. [6]: Reg_event3_int, [5]: Reg_event2_int, [4]: Reg_event1_int, [3]: Reg_alarm_int, [2]: Rtc_match_int, [1]: Sub_cnt_match_int, [0]: ~reg_rtc_32k_ok.	
2Eh (48B9h)	**REG48B9**	**7:0**	**Default : 0x00**	**Access : RO**
	RTC_IRQ_FINAL_STATUS[7:0]	7:0	RTC IRQ final status.	
2Fh (48BCh)	**REG48BC**	**7:0**	**Default : 0x67**	**Access : R/W**
	RTC_INT_PASSWD[7:0]	7:0	RTC password.	
2Fh (48BDh)	**REG48BD**	**7:0**	**Default : 0x04**	**Access : R/W**
	RTC_INT_PASSWD[15:8]	7:0	See description of '48BCh'.	

USBC Register (Bank = 25)

USBC Register (Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2500h)	**RST_CTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved	
	OTG_XIU_ENABLE	6	The OTG XIU read and write operation are invalid if the bit is set to 1'b0.	
	UHC_XIU_ENABLE	5	The UHC XIU read and write operation are invalid if the bit is set to 1'b0.	
	-	4	Reserved for port1 in dual port design.	
	REG_SUSPEND_	3	Initial suspend control	
	OTG_RST	2	Write 1 to reset OTG controller.	
	UHC_RST	1	Write 1 to reset UHC controller.	
	USB_RST	0	Write 1 to reset USB controller.	
00h (2501h)	**-**	**7:0**	**Default : 0x02**	**Access : R/W**
		7:4	Reserved	
		3:2	Reserved for port1 in dual port design.	
	REG_VBUSVALID	1	Override vbusvalid value for port 0.	
	VBUS_SEL	0	The select option for vbusvalid in port 0. Default value is select to register value.	
01h (2502h)	**PORT_CTRL**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	HSIC_EN	5	UTMI select 0: Normal UTMI 1: HSIC UTMI (UIC)	
	IDPULLUP_CTRL	4	OTG idpullup control.	
	PME_POL	3	Power management event polarity select	
	INT_POL	2	Interrupt polarity select	
	PORT_CTRL	1:0	2'b00: UHC and OTG are both disable 2'b01: UHC enable 2'b10: OTG enable 2'b11: the setting is prohibited	
02h (2504h)	**INTERRUPT_ENABLE1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	ID_CHG_INTEN	3	The interrupt enable of status: ID state changed.	
	BVAL_CHG_INTEN	2	The interrupt enable of status: BVALID state changed.	

USBC Register (Bank = 25)

Index (Absolute)	Mnemonic	Bit	Description	
	AVAL_CHG_INTEN	1	The interrupt enable of status: AVALID state changed.	
	VBUS_CHG_INTEN	0	The interrupt enable of status: VBUSVALID state changed.	
03h (2506h)	**INTERRUPT_STATUS1**	**7:0**	**Default : 0x00**	**Access : R/W1C**
	-	7:4	Reserved.	
	ID_CHG_STS	3	The interrupt status: ID state changed.	
	BVAL_CHG_STS	2	The interrupt status: BVALID state changed.	
	AVAL_CHG_STS	1	The interrupt status: AVALID state changed.	
	VBUS_CHG_STS	0	The interrupt status: VBUSVALID state changed.	
04h (2508h)	**UTMI Signal Status**	**7:0**	**Default : 0x00**	**Access : RO**
	LINESTATE[1:0]	7:6	DM and DP single status.	
	SESSEND	5	UTMI status.	
	HOSTDISCON	4	Device disconnect in high speed mode.	
	IDDIG	3	PAD CID status.	
	BVALID	2	The status of Power detector.	
	AVALID	1	The status of Power detector.	
	VBUSVALID	0	The status of Power detector.	
04h (2509h)	**UTMI Signal Status**	**7:0**	**Default : 0x00**	**Access : RO**
	ID_DEB_CNT[2:0]	7:5	PAD CID debouncing counter	
	RXACTIVE	4	UTMI data interface.	
	RXVALID	3	UTMI data interface.	
	RXVALIDH	2	UTMI data interface.	
	RXERROR	1	UTMI data interface.	
	TXREADY	0	UTMI data interface.	
05h (250Ah)	**Power Management Event Enable**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved	
	CONN_BVAL_INTEN	6	The interrupt and PME enable CONN_BVAL_STS.	
	CONN_AVAL_INTEN	5	The interrupt and PME enable CONN_AVAL_STS.	
	CONN_VBUS_INTEN	4	The interrupt and PME enable CONN_VBUS_STS.	
	RESET_INTEN	3	The interrupt and PME enable RESET_STS.	
	RESUME_INTEN	2	The interrupt and PME enable RESUME_STS.	
	DEV_DET_INTEN	1	The interrupt and PME enable DEV_DET_STS.	

USBC Register (Bank = 25)

Index (Absolute)	Mnemonic	Bit	Description	
	WAKEUP_INTEN	0	The interrupt and PME enable WAKEUP_STS.	
06h (250Ch)	**Power Management Event Status**	**7:0**	**Default : 0x00**	**Access : R/W1C**
	-	7	Reserved.	
	CONN_BVAL_STS	6	OTG detect bvalid rising in the suspend mode. The status will both result interrupt and PME.	
	CONN_AVAL_STS	5	OTG detect avalid rising in the suspend mode. The status will both result interrupt and PME.	
	CONN_VBUS_STS	4	OTG detect PAD_VBUS rising in the suspend mode. The status will both result interrupt and PME.	
	RESET_STS	3	OTG detect host send USB bus reset in suspend mode. The status will both result interrupt and PME.	
	RESUME_STS	2	OTG detect host send USB bus resume signaling in suspend mode. The status will both result interrupt and PME.	
	DEV_DET_STS	1	UHC detect device plug-in in suspend mode. The status will both result interrupt and PME.	
	WAKEUP_STS	0	UHC detect device remote wakeup in suspend mode. The status will both result interrupt and PME.	

OTG Register (Bank = 26 ~ 29)

OTG Register (Bank = 26 ~ 29)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h	**FADDR**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	FUNCADDR	6:0	USB address.	
01h	**POWER**	**7:0**	**Default : 0x01**	**Access : R/W, RO**
	ISO_UPDATE	7	When set to '1', USB will wait for SOF token from the time TxPktRdy is set before sending a packet. If an IN token is received before an SOF token, a zero length data packet will be sent. Only Valid in isochronous mode (Access: R/W).	
	SOFT_CONN	6	Set '1' to pull up D+ (Access: R/W).	
	HS_EN	5	Set '1' to enable high speed mode (Access: R/W).	
	HS_MODE	4	Set '1' when in high speed mode (Access: RO).	
	RESET	3	Set '1' when USB bus is in USB reset state (Access: RO).	
	RESUME	2	Set '1' when to issue resume state (Access: R/W).	
	SUSPEND_MODE	1	Set '1' when in suspend state (Access: R/W).	
	EN_SUSPENDM	0	Enable SuspendM output (Access: R/W).	
02h	**INTRTX**	**7:0**	**Default : 0x00**	**Access : RO**
	EP7_TX	7	Endpoint7 TX interrupt.	
	EP6_TX	6	Endpoint6 TX interrupt.	
	EP5_TX	5	Endpoint5 TX interrupt.	
	EP4_TX	4	Endpoint4 TX interrupt.	
	EP3_TX	3	Endpoint3 TX interrupt.	
	EP2_TX	2	Endpoint2 TX interrupt.	
	EP1_TX	1	Endpoint1 TX interrupt.	
	EP0	0	Endpoint0 interrupt.	
04h	**INTRRX**	**7:0**	**Default : -**	**Access : RO**
	EP7_RX	7	Endpoint7 RX interrupt.	
	EP6_RX	6	Endpoint6 RX interrupt.	
	EP5_RX	5	Endpoint5 RX interrupt.	
	EP4_RX	4	Endpoint4 RX interrupt.	
	EP3_RX	3	Endpoint3 RX interrupt.	
	EP2_RX	2	Endpoint2 RX interrupt.	
	EP1_RX	1	Endpoint1 RX interrupt.	

OTG Register (Bank = 26 ~ 29)

Index (Absolute)	Mnemonic	Bit	Description	
	-	0	Reserved.	
06h	**INTRTXE**	**7:0**	**Default : 0x0F**	**Access : R/W**
	EP7_TXE	7	Endpoint7 TX interrupt enable.	
	EP6_TXE	6	Endpoint6 TX interrupt enable.	
	EP5_TXE	5	Endpoint5 TX interrupt enable.	
	EP4_TXE	4	Endpoint4 TX interrupt enable.	
	EP3_TXE	3	Endpoint3 TX interrupt enable.	
	EP2_TXE	2	Endpoint2 TX interrupt enable.	
	EP1_TXE	1	Endpoint1 TX interrupt enable.	
	EP0_TXE	0	Endpoint0 TX interrupt enable.	
08h	**INTRRXE**	**7:0**	**Default : 0x0E**	**Access : R/W**
	EP7_RXE	7	Endpoint7 RX interrupt enable.	
	EP6_RXE	6	Endpoint6 RX interrupt enable.	
	EP5_RXE	5	Endpoint5 RX interrupt enable.	
	EP4_RXE	4	Endpoint4 RX interrupt enable.	
	EP3_RXE	3	Endpoint3 RX interrupt enable.	
	EP2_RXE	2	Endpoint2 RX interrupt enable.	
	EP1_RXE	1	Endpoint1 RX interrupt enable.	
	-	0	Reserved.	
0Ah	**INTRUSB**	**7:0**	**Default : -**	**Access : RO**
	VBUS_ERROR	7	VBUS dropped below VBUS valid threshold interrupt. Only valid in A device.	
	SESS_REQ	6	Session request detected interrupt.	
	DISCON	5	Disconnection detected.	
	CONN	4	Connection detected; only valid in host mode.	
	SOF	3	SOF interrupt.	
	RESET_BABBLE	2	Reset/babble interrupt.	
	RESUME	1	Resume interrupt when in suspend mode.	
	SUSPEND	0	Suspend interrupt.	
0Bh	**INTRUSBE**	**7:0**	**Default : 0x06**	**Access : R/W**
	VBUS_ERROR	7	VBUS error interrupt enable.	
	SESS_REQ	6	SESSREQ interrupt enable.	
	DISCON	5	DISCON interrupt enable.	

OTG Register (Bank = 26 ~ 29)

Index (Absolute)	Mnemonic	Bit	Description	
	CONN	4	CONN interrupt enable.	
	SOF	3	SOF interrupt enable.	
	RST_BABBLE	2	Reset/babble interrupt enable.	
	RESUME	1	Resume interrupt enable.	
	SUSPEND	0	Suspend interrupt enable.	
0Ch	**FRAME_L**	**7:0**	**Default : -**	**Access : RO**
	FRAME[7:0]	7:0	The last Frame number received, low byte	
0Dh	**FRAME_H**	**7:0**	**Default : -**	**Access : RO**
	-	7:3	Reserved.	
	FRAME[10:8]	2:0	The last Frame number received, higher 3 bits.	
0Eh	**INDEX**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	EP_SEL	3:0	Before access EP1~EP3 registers, EP_SEL must be set to the corresponding endpoint (18h~27h).	
0Fh	**TESTMODE**	**7:0**	**Default : 0x00**	**Access : R/W**
	FORCE_HOST	7	Set to force entering host mode.	
	FIFO_ACCESS	6	Set to transfer EP0 TX to EP0 RX. Cleared automatically (Access: Self-clearing).	
	FORCE_FS	5	Set to force entering full speed.	
	FORCE_HS	4	Set to force entering high speed.	
	TEST_PACKET	3	Set to enter test packet defined in USB2.0 test mode.	
	TEST_K	2	Set to enter TEST_K defined in USB2.0 test mode.	
	TEST_J	1	Set to enter TEST_J defined in USB2.0 test mode.	
	TEST_SE0_NAK	0	Set to enter TEST_SE0_NAK defined in USB2.0 test mode.	
10h	**TXMAP_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXMAP[7:0]	7:0	Defines the max. Amount of the data that can be transferred through the select TX endpoint in a single operation; low byte.	
11h	**TXMAP_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	TXMAP[15:11]	7:3	Defines the multiplier for the max data bytes in a transaction. The maximum data transferred in a transaction is $(2^m)*$TXMAP; higher 5 bits.	
	TXMAP[10:8]	2:0	Defines the max. Amount of the data that can be transferred through the select TX endpoint in a single operation; middle 3	

OTG Register (Bank = 26 ~ 29)

Index (Absolute)	Mnemonic	Bit	Description	
			bits.	
For EP_SEL=0, 12h~1Fh				
12h	**CSR0**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	SERVICED_SETUPEND	7	Set to clear SETUPEND (Access: WO, auto-clear).	
	SERVICED_EXPKTRDY	6	Set to clear RXPKTRDY (Access: WO, auto-clear).	
	SENDSTALL	5	Set to terminate current transaction and transfer a stall packet (Access: WO, auto-clear).	
	SETUPEND	4	Set when a control transaction ends (Access: RO).	
	DATAEND	3	Set when loading the last transmit packet or unloading the last received packet (Access: WO, auto-clear).	
	SENTSTALL	2	EP0 send stall (Access: RO).	
	TXPKTRDY	1	EP0 transmit ready (Access: WO, auto-clear).	
	RXPKTRDY	0	EP0 receive packet ready (Access: RO).	
13h	**CSR0_FLSH**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	FLUSHFIFO	0	Set to flush the packet to be transmitted/read from the EP0 FIFO (Access: WO, auto-clear).	
18h	**COUNT0**	**7:0**	**Default : -**	**Access : RO**
	-	7	Reserved.	
	ENDPOINT0_EX_COUNT	6:0	Received endpoint 0 RX count.	
For EP_SEL≠0, 12h~1Fh: (EP1~EP3)				
12h	**TXCSR1**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	-	7	Reserved.	
	CLRDATATOG	6	Set to reset the data toggle of the corresponding endpoint to 0 (Access: WO).	
	SENTSTALL	5	Set when the stall is sent (Access: RO, auto-clear).	
	SENDSTALL	4	Set to send a stall for the IN packet of the corresponding TX endpoint (Access: R/W).	
	FLUSHFIFO	3	Set to flush the last packet in the corresponding TX FIFO (Access: R/W, auto-clear).	
	UNDERRUN	2	Set when transmitted data (TXPKTRDY) is not ready (Access: RO, auto-clear).	
	FIFONOTEMPTY	1	Set when at least 1 packet in the FIFO (Access: RO, auto-clear).	
	TXPKTRDY	0	Set when a packet is loaded to the TX FIFO (Access: R/W,	

OTG Register (Bank = 26 ~ 29)

Index (Absolute)	Mnemonic	Bit	Description	
			auto-clear).	
13h	**TXCSR2**	**7:0**	**Default : 0x00**	**Access : R/W**
	AUTOSET	7	Set '1' to make TXPKTRDY be auto-set.	
	-	6	Reserved.	
	MODE	5	0: Set as RX FIFO. 1: Set as TX FIFO.	
	DMAREQENAB	4	Set to enable DMA transfer for the corresponding TX endpoint.	
	FRCDATATOG	3	Set to force the data toggle switched for the TX endpoint.	
	DMAREQMODE	2	DMA mode.	
	-	1:0	Reserved.	
14h	**RXMAP_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	RXMAP[7:0]	7:0	Max packet size of RX packet for EP1~3, lower 8 bits.	
15h	**RXMAP_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	RXMAP[15:11]	7:3	Defines the multiplier for the max data bytes in a transaction. The maximum data transferred in a transaction is $(2^m)*$RXMAP.	
	RXMAP[10:8]	2:0	Max packet size of RX packet for EP1~3, middle 3 bits.	
16h	**RXCSR1**	**7:0**	**Default : 0x00**	**Access : R/W, RO**
	CLRDATATOG	7	Set to reset the RX data toggle to 0 for the corresponded endpoint (Access: R/W).	
	SENTSTALL	6	Set when the stall is transmitted (Access: RO).	
	SENDSTALL	5	Set to respond a stall for the OUT packet (Access: R/W).	
	FLUSHFIFO	4	Set to flush the data in the RX FIFO (Access: R/W).	
	DATAERROR	3	Set when received data has CRC or bit-stuffing error (Access: R/W).	
	OVERRUN	2	Set when out data packet can't be loaded to RX FIFO (Access: R/W, write for clear).	
	FIFOFULL	1	Set when FIFO is full (Access: RO).	
	RXPKTRDY	0	Set when a packet is received (Access: R/W, write for clear).	
17h	**RXCSR2**	**7:0**	**Default : 0x00**	**Access : R/W**
	AUTOCLR	7	Sign bit of blue color. 0: Increase. 1: Decrease.	

OTG Register (Bank = 26 ~ 29)

Index (Absolute)	Mnemonic	Bit	Description	
	-	6	Reserved.	
	DMAREQEN	5	DMA request enable for the RX FIFO.	
	DISNYET	4	Set to disable sending NYET for handshaking.	
	DMAREQMD	3	DMA mode setting.	
	-	2:0	Reserved.	
18h	**RXCOUNT_L**	**7:0**	**Default : -**	**Access : RO**
	RXCOUNT[7:0]	7:0	Received endpoint RX count, low byte.	
19h	**RXCOUNT_H**	**7:0**	**Default : -**	**Access : RO**
	-	7:5	Reserved.	
	RXCOUNT[12:8]	4:0	Received endpoint RX count, high byte.	
1Fh	**FIFOSIZE**	**7:0**	**Default : -**	**Access : RO**
	RXFIFOSIZE[3:0]	7:4	Size of the related RX FIFO (Default: Application Dependent).	
	TXFIFOSIZE[3:0]	3:0	Size of the related TX FIFO (Default: Application Dependent).	
20h	**EP0_FIFO_ACCESS_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP0_FIFO_ACCESS[7:0]	7:0	EP0 FIFO access port, low byte.	
21h	**EP0_FIFO_ACCESS_M1**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP0_FIFO_ACCESS[15:8]	7:0	EP0 FIFO access port, middle byte.	
22h	**EP0_FIFO_ACCESS_M2**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP0_FIFO_ACCESS[23:16]	7:0	EP0 FIFO access port, middle byte.	
23h	**EP0_FIFO_ACCESS_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP0_FIFO_ACCESS[31:24]	7:0	EP0 FIFO access port, high byte.	
24h	**EP1_FIFO_ACCESS_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP1_FIFO_ACCESS[7:0]	7:0	EP1 FIFO access port, low byte.	
25h	**EP1_FIFO_ACCESS_M1**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP1_FIFO_ACCESS[15:8]	7:0	EP1 FIFO access port, middle byte.	
26h	**EP1_FIFO_ACCESS_M2**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP1_FIFO_ACCESS[23:16]	7:0	EP1 FIFO access port, middle byte.	
27h	**EP1_FIFO_ACCESS_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP1_FIFO_ACCESS[31:24]	7:0	EP1 FIFO access port, high byte.	
28h	**EP2_FIFO_ACCESS_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP2_FIFO_ACCESS[7:0]	7:0	EP2 FIFO access port, low byte.	
29h	**EP2_FIFO_ACCESS_M1**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP2_FIFO_ACCESS[15:8]	7:0	EP2 FIFO access port, middle byte.	

OTG Register (Bank = 26 ~ 29)

Index (Absolute)	Mnemonic	Bit	Description	
2Ah	**EP2_FIFO_ACCESS_M2**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP2_FIFO_ACCESS[23:16]	7:0	EP2 FIFO access port, middle byte.	
2Bh	**EP2_FIFO_ACCESS_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP2_FIFO_ACCESS[31:24]	7:0	EP2 FIFO access port, high byte.	
2Ch	**EP3_FIFO_ACCESS_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP3_FIFO_ACCESS[7:0]	7:0	EP3 FIFO access port, low byte.	
2Dh	**EP3_FIFO_ACCESS_M1**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP3_FIFO_ACCESS[15:8]	7:0	EP3 FIFO access port, middle byte.	
2Eh	**EP3_FIFO_ACCESS_M2**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP3_FIFO_ACCESS[23:16]	7:0	EP3 FIFO access port, middle byte.	
2Fh	**EP3_FIFO_ACCESS_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP3_FIFO_ACCESS[31:24]	7:0	EP3 FIFO access port, high byte.	
30h	**EP4_FIFO_ACCESS_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP4_FIFO_ACCESS[7:0]	7:0	EP4 FIFO access port, low byte.	
31h	**EP4_FIFO_ACCESS_M1**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP4_FIFO_ACCESS[15:8]	7:0	EP4 FIFO access port, middle byte.	
32h	**EP4_FIFO_ACCESS_M2**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP4_FIFO_ACCESS[23:16]	7:0	EP4 FIFO access port, middle byte.	
33h	**EP4_FIFO_ACCESS_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP4_FIFO_ACCESS[31:24]	7:0	EP4 FIFO access port, high byte.	
34h	**EP5_FIFO_ACCESS_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP5_FIFO_ACCESS[7:0]	7:0	EP5 FIFO access port, low byte.	
35h	**EP5_FIFO_ACCESS_M1**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP5_FIFO_ACCESS[15:8]	7:0	EP5 FIFO access port, middle byte.	
36h	**EP5_FIFO_ACCESS_M2**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP5_FIFO_ACCESS[23:16]	7:0	EP5 FIFO access port, middle byte.	
37h	**EP5_FIFO_ACCESS_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP5_FIFO_ACCESS[31:24]	7:0	EP5 FIFO access port, high byte.	
38h	**EP6_FIFO_ACCESS_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP6_FIFO_ACCESS[7:0]	7:0	EP6 FIFO access port, low byte.	
39h	**EP6_FIFO_ACCESS_M1**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP6_FIFO_ACCESS[15:8]	7:0	EP6 FIFO access port, middle byte.	
3Ah	**EP6_FIFO_ACCESS_M2**	**7:0**	**Default : 0x00**	**Access : R/W**

OTG Register (Bank = 26 ~ 29)

Index (Absolute)	Mnemonic	Bit	Description	
	EP6_FIFO_ACCESS[23:16]	7:0	EP6 FIFO access port, middle byte.	
3Bh	**EP6_FIFO_ACCESS_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP6_FIFO_ACCESS[31:24]	7:0	EP6 FIFO access port, high byte.	
3Ch	**EP7_FIFO_ACCESS_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP7_FIFO_ACCESS[7:0]	7:0	EP7 FIFO access port, low byte.	
3Dh	**EP7_FIFO_ACCESS_M1**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP7_FIFO_ACCESS[15:8]	7:0	EP7 FIFO access port, middle byte.	
3Eh	**EP7_FIFO_ACCESS_M2**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP7_FIFO_ACCESS[23:16]	7:0	EP7 FIFO access port, middle byte.	
3Fh	**EP7_FIFO_ACCESS_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	EP7_FIFO_ACCESS[31:24]	7:0	EP7 FIFO access port, high byte.	
60h	**DEVCTL**	**7:0**	**Default : 0x00**	**Access : R/W, RO**
	B_DEVICE	7	0: A device. 1: B device. (Access: RO)	
	FSDEV	6	Set when high or full speed is attached. Only act in host mode (Access: RO).	
	LSDEV	5	Set when low speed device is attached. Only act in host mode (Access: RO).	
	VBUS[1:0]	4:3	00: VBUS power Below SESSIONEND. 01: VBUS power Above SESSIONEND, below AVALID. 10: VBUS power Above AVALID, below VBUSVALID. 11: VBUS power Above VBUSVALID. (Access: RO)	
	HOST_MD	2	Set when act as a host.	
	HOST_REQ	1	Set in initialize the host negotiation when suspend mode is entered. Cleared when host negotiation is completed (Access: R/W).	
	SESSION	0	Set/cleared when session starts/ends (Access: R/W).	
80h	**USB_CFG0_L**	**7:0**	**Default: 0x01**	**Access: R/W**
	MIU_PRIORITY	7	Set MIU priority	
	USBOTG	6	Force into device mode	
	DEBUG_SEL	5:2	Select Debug Group	
	OTG_TM1	1	Test Mode Enable	
	SRST_N	0	Soft Reset, Low Active (default set as 1)	

OTG Register (Bank = 26 ~ 29)

Index (Absolute)	Mnemonic	Bit	Description	
81h	**USB_CFG0_H**	**7:0**	**Default: 0x0f**	**Access: R/W**
	DMPULLDOWN	7	DM pull-down enable	
	SET_OK2RCV_1	6	2nd data phase enable for bulk out transfer	
	SET_ALLOW_ACK_1	5	2nd command phase enable for bulk out transfer	
	ECO4NAK_EN_1	4	2nd ECO enable for bulk out bug	
	EP_BULKOUT_1	3:0	2nd mode 1 send NAK endpoint number	
82h	**USB_CFG1_L**	**7:0**	**Default: 0x00**	**Access: R/W**
	Rx_Pkt_Cnt_1[7:0]	7:0	2nd mode 1 send NAK, RX packet count	
83h	**USB_CFG1_H**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	Rx_Pkt_Cnt_1[12:8]	4:0	2nd mode 1 send NAK, RX packet count	
84h	**USB_CFG2_L**	**7:0**	**Default: 0x00**	**Access: RO**
	DISCHGVBUS	7	OTG discharge vbus value	
	LINESTATE	6:5	UTMI linestate value	
	HOSTDISCONN	4	Host disconnect	
	AVALID	3	AVALID	
	VBUSVALID	2	VBUSVALID (VBUS > 4.4V)	
	SESSEND	1	Session end	
	IDDIG	0	Id value	
85h	**USB_CFG2_H**	**7:0**	**Default: 0x40**	**Access: RO**
	OPMODE	7:6	UTMI opmode	
	XCVRSEL	5:4	UTMI xcvrsel	
	TERMSEL	3	UTMI termsel	
	IDPULLUP	2	ID pull up enable	
	DRVVBUS	1	OTG drive vbus	
	CHRGVBUS	0	OTG charge vbus	
86h	**USB_CFG3_L**	**7:0**	**Default: 0x0f**	**Access: R/W**
	-	7:4	Reserved	
	EP_BULKOUT	3:0	Mode 1 send NAK endpoint number	
87h	**USB_CFG3_H**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUSPENDM	7	Low active, suspend status (R/O)	
	DPPULLDOWN	6	DP pull down status (R/O)	
	DMPULLDOWN	5	DM pull down status (R/O)	

OTG Register (Bank = 26 ~ 29)

Index (Absolute)	Mnemonic	Bit	Description	
	-	4:0	Reserved.	
88h	**USB_CFG4_L**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:0	Reserved.	
89h	**USB_CFG4_H**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
8Ah	**USB_CFG5_L**	**7:0**	**Default: 0x00**	**Access: R/W**
	Rx_Pkt_Cnt[7:0]	7:0	For mode 1 send NAK, RX packet count	
8Bh	**USB_CFG5_H**	**7:0**	**Default: 0x00**	**Access: R/W**
	SET_OK2RCV	7	Data phase enable for bulk out transfer	
	SET_ALLOW_ACK	6	command phase enable for bulk out transfer	
	ECO4NAK_EN	5	ECO enable for bulk out bug	
	Rx_Pkt_Cnt[12:8]	4:0	For mode 1 send NAK, RX packet count	
8Ch	**USB_CFG6_L**	**7:0**	**Default: 0x00**	**Access: R/W**
	Reg_hsic_en	7	HSIC mode enable	
	Reg_hst_en	6	Set as host mode while in HSIC mode	
	Reg_dev_en	5	Set as device mode while in HSIC mode	
	OVERWRITE_AVALID	4	Overwrite value of AVALID	
	OVERWRITE_VBUSVALID	3	Overwrite value of VBUSVALID	
	OVERWRITE_SESSEND	2	Overwrite value of SESSEND	
	OVERWRITE_IDDIG	1	Overwrite value of IDDIG	
	- (MIU_MODE)	0	Reserved (miu_mode for old project)	
8Dh	**USB_CFG6_H**	**7:0**	**Default: 0x00**	**Access: R/W**
	FLSH_WFIFO_DONE	7	0: Still in flush phase, 1: Flush write fifo done. (Read Only)	
	FLSH_AHB_WFIFO	6	1: write 1'b1 to flush write fifo in AHB2MIU wrapper.	
	Shortpkt_MODE	5	0: RxPktCnt set by CPU. 1: Real RcvPktCnt.	
	MCU_HLT_DMA_EN	4	0: Enable (Default), 1:Disable. When MCU Access(R/W) FIFO, will halt DMA CH transaction until MCU cycle finish.	
	INT_WR_CLR_EN	3	0: Interrupt Register Read clear(Default), 1: Interrupt Register Write clear.	
	DMAMCU_WR_FIX	2	0: Enable (Default), 1: Disable. MCU WR/DMA RD/USB WR bug fix.	

OTG Register (Bank = 26 ~ 29)

Index (Absolute)	Mnemonic	Bit	Description	
	DMAMCU_RD_FIX	1	0: Enable (Default), 1: Disable. MCU RD/DMA WR/USB RD bug fix.	
	DMACH_BUG_FIX	0	0: Enable (Default), 1: Disable. DMA Channel arbiter bug fix.	
8Eh	**USB_CFG7_L**	**7:0**	**Default: 0x00**	**Access: R/W**
	A2M_WAIT_TIME[2:0]	7:5	Timeout value for issue write at MIU port when AHB write fifo not empty	
	A2M_FIFO_THR[3:0]	4:1	Write FIFO threshold value to issue write plus at MIU port	
	A2M_FLW_CTRL	0	0: Disable AHB2MIU wrapper Flow control (Default), 1: Enable Flow control by register A2M_FIFO_THR and A2M_WAIT_TIM	
8Fh	**USB_CFG7_H**	**7:0**	**Default: 0x04**	**Access: R/W**
	-	7:6	Reserved.	
	A2M_WFF_FLH_DONE	5	Write one clear. When Enable A2M write fifo flush, this bit indicate write fifo was done when last DMA write cycle issued.	
	A2M_WFF_FLH_EN	4	AHB2MIU bridge 1: Enable write fifo flush when last dma write cycle, 0: Disable(default).	
	A2M_AHB_INCR_W	3:2	AHB2MIU parameter, INCR number 2'b01(default)	
	A2M_WAIT_TIME[4:3]	1:0	Timeout value for issue write at MIU port when AHB write fifo not empty	

OTG Register (Bank=28),(byte addr: 0x200)

Index (Absolute)	Mnemonic	Bits	Description	
00h	**DMA_INTR**	**7:0**	**Default : -**	**Access : RO**
	-	7:2	Reserved.	
	DMA_CH2_INTR	1	DMA Channel 2 interrupt.	
	DMA_CH1_INTR	0	DMA Channel 1 interrupt.	
04h	**CH1_DMA_CNTL**	**7:0**	**Default : 0x00**	**Access : R/W**
	ENDPOINT_NO	7:4	Endpoint number to be used in this DMA channel.	
	INTERRUPT_EN	3	DMA mode interrupt enable.	
	DMA_MODE	2	DMA mode setting. 0: DMA manual mode. 1: DMA auto mode.	

OTG Register (Bank=28),(byte addr: 0x200)

Index (Absolute)	Mnemonic	Bits	Description	
	DIRECTION	1	0: DMA RX direction. 1: DMA TX direction.	
	EN_DMA	0	Set to enable DMA channel 1.	
05h	**CH1_DMA_CNTL**	**7:0**	**Default : 0x00**	**Access : R/W, RO**
	-	7:3	Reserved.	
	BURST_MODE	2:1	00: Burst of unspecified length. 01: INCR4. 10: INCR8. 11: Burst of unspecified length. (Access: R/W)	
	BUS_ERROR	0	AHB bus error (Access: RO).	
08h	**CH1_DMA_ADDR_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH1_DMA_ADDR[7:0]	7:0	Start address of DMA channel 1, low byte.	
09h	**CH1_DMA_ADDR_M1**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH1_DMA_ADDR[15:8]	7:0	Start address of DMA channel 1, middle byte.	
0Ah	**CH1_DMA_ADDR_M2**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH1_DMA_ADDR[23:16]	7:0	Start address of DMA channel 1, middle byte.	
0Bh	**CH1_DMA_ADDR_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH1_DMA_ADDR[31:24]	7:0	Start address of DMA channel 1, high byte.	
0Ch	**CH1_DMA_CNT_L**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH1_DMA_CUNT[7:0]	7:0	Byte count of DMA channel 1, low byte.	
0Dh	**CH1_DMA_CNT_M1**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH1_DMA_CNT[15:8]	7:0	Byte count of DMA channel 1, middle byte.	
0Eh	**CH1_DMA_CNT_M2**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH1_DMA_CNT[23:16]	7:0	Byte count of DMA channel 1, middle byte.	
0Fh	**CH1_DMA_CNT_H**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH1_DMA_CNT[31:24]	7:0	Byte count of DMA channel 1, high byte.	
14h~3Fh		**7:0**	**Default : -**	**Access : -**
		7:0	Reserved	

UHC0 Register (Bank = 2A)

UHC0 Register (Bank = 2A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2400h)	**HCCAP**	**7:0**	**Default : 0x10**	**Access : RO**
	CAPLENGTH	7:0	Capability Register Length. This register is used as an offset to be added to register base to determine the beginning of the Operational Register Space.	
01h (2402h)	**HCCAP**	**7:0**	**Default : 0x00**	**Access : RO**
	HCIVERSION[7:0]	7:0	Host Controller Interface Version Number. This register is a two-byte register containing a BCD encoding of the EHCI revision number supported by the Host Controller.	
01h (2403h)	**HCCAP**	**7:0**	**Default : 0x01**	**Access : RO**
	HCIVERSION[15:8]	7:0	See description of '2402h'.	
02h (2404h)	**HCSPARAMS**	**7:0**	**Default : 0x01**	**Access : RO**
	-	7:4	Reserved.	
	N_PORTS	3:0	Number of Ports. This field specifies the number of physical downstream ports implemented on the Host Controller.	
04h (2408h)	**HCCPARAMS**	**7:0**	**Default : 0x06**	**Access : RO**
	-	7:3	Reserved.	
	ASYN_SCH_PARK_CAP	2	Asynchronous Schedule Park Capability. When this bit is set to '1', system software can specify and use a smaller frame list and configure the Host Controller via the Frame List Size field of USBCMD register. This requirement ensures the frame list is always physically contiguous.	
	PROG_FR_LIST_FLAG	1	Programmable Frame List Flag. When this bit is set to '1', system software can specify and use a smaller frame list and configure the Host Controller via Frame List Size Field of USBCMD register. This requirement ensures the frame list is always physically contiguous.	
	-	0	Reserved.	
08h (2410h)	**USBCMD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	INT_OAAD	6	Interrupt on Asynchronous Advance Doorbell.	

UHC0 Register (Bank = 2A)

Index (Absolute)	Mnemonic	Bit	Description
			This bit is used as a doorbell by software to ring the Host Controller to issue an interrupt at the next advance of Asynchronous Schedule.
	ASCH_EN	5	Asynchronous Schedule Enable. This bit controls whether the Host Controller skips the processing of Asynchronous Schedule. 0: Do not process Asynchronous Schedule. 1: Use the ASYNCLISTADDR register to access the Asynchronous Schedule.
	PSCH_EN	4	Periodic Schedule Enable. This bit controls whether the Host Controller skips the processing of Periodic Schedule. 0: Do not process Periodic Schedule. 1: Use the PERIODICKISTBASE register to access the Periodic Schedule.
	FRL_SIZE	3:2	Frame List Size. This field specifies the size of the frame list. 00: 1024 elements (4096 bytes; default value). 01: 512 elements (2048 bytes). 10: 256 elements (1024 bytes). 11: Reserved.
	HC_RESET	1	Host Controller Reset. This control bit is used by software to reset the Host Controller.
	RS	0	Run/Stop. When this bit is set to '1', the Host Controller proceeds with the execution of schedule. 0: Stop. 1: Run.
08h (2411h)	**USBCMD**	**7:0**	**Default : 0x0b** **Access : R/W**
	-	7:4	Reserved.
	ASYN_PK_EN	3	Asynchronous Schedule Park Mode Enable. Software uses this register to enable or disable the Park mode. When this register is set to 1, the Park mode is enabled.
	-	2	Reserved.
	ASYN_PK_CNT	1:0	Asynchronous Schedule Park Mode Count. This field contains a count for the number of

UHC0 Register (Bank = 2A)

Index (Absolute)	Mnemonic	Bit	Description	
			successive transactions that the Host Controller is allowed to execute from a high-speed queue head on Asynchronous Schedule.	
09h (2412h)	**USBCMD**	**7:0**	**Default : 0x08**	**Access : R/W**
	INT_THRC	7:0	Interrupt Threshold Control. This field is used by system software to select the maximum rate at which the Host Controller will issue interrupts. The only valid values are described below: Value Maximum Interrupt Interval for High Speed 00h Reserved. 01h 1 micro-frame. 02h 2 micro-frames. 04h 4 micro-frames. 08h 8 micro-frames (default, equals to 1ms). 10h 16 micro-frames (2 ms). 20h 32 micro-frames (4 ms). 40h 64 micro-frames (8 ms). Note: For Full Speed, these registers are reserved.	
0Ah (2414h)	**USBSTS**	**7:0**	**Default : 0x00**	**Access : R/WC**
	-	7:6	Reserved.	
	INT_OAA	5	Interrupt on Async Advance. This status bit indicates the assertion of interrupt on Async Advance Doorbell.	
	H_SYSERR	4	Host System Error. The Host Controller sets this bit to 1 when a serious error occurred during a host system access involving the Host Controller module.	
	FRL_ROL	3	Frame List Rollover. The Host Controller sets this bit to 1 when the Frame List Index rolls over from its maximum value to zero.	
	PO_CHG_DET	2	Port Change Detect. The Host Controller sets this bit to '1' when any port has a change bit transition from '0' to '1'. In addition, this bit is loaded with the OR of all of the PORTSC change bits.	
	USBERR_INT	1	USB Error Interrupt. The Host Controller sets this bit to '1' when the completion of a USB transaction results in an error	

UHC0 Register (Bank = 2A)

Index (Absolute)	Mnemonic	Bit	Description	
			condition.	
	USB_INT	0	USB Interrupt. The Host Controller sets this bit to '1' upon the completion of a USB transaction.	
0Ah (2415h)	**USBSTS**	**7:0**	**Default : 0x10**	**Access : RO**
	ASCH_STS	7	Asynchronous Schedule Status. This bit reports the actual status of Asynchronous Schedule.	
	PSCH_STS	6	Periodic Schedule Status. This bit reports the actual status of Periodic Schedule.	
	RECLAMATION	5	Reclamation. This is a read-only status bit, and is used to detect an empty of Asynchronous Schedule.	
	HCHALTED	4	Host Controller Halted. This bit is a zero whenever the Run/Stop bit is set to '1'. The Host Controller sets this bit to '1' after it has stopped the executing as a result of the Run/Stop bit being set to '0'.	
	-	3:0	Reserved.	
0Ch (2418h)	**USBINTR**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	INT_OAA_EN	5	Interrupt on Async Advance Enable. When this bit is set to '1', and the Interrupt on Async Advance bit in the USBSTS register is set to '1' also, the Host Controller will issue an interrupt at the next interrupt threshold.	
	H_SYSERR_EN	4	Host System Error Enable. When this bit is set to '1', and the Host System Error Status bit in the USBSTS register is set to '1' also, the Host Controller will issue an interrupt.	
	FRL_ROL_EN	3	Frame List Rollover Enable. When this bit is set to '1', and the Frame List Rollover bit in the USBSTS register is set to '1' also, the Host Controller will issue an interrupt.	
	PO_CHG_INT_EN	2	Port Change Interrupt Enable. When this bit is set to '1', and the Port Change Detect bit in the USBSTS register is set to '1' also, the Host	

UHC0 Register (Bank = 2A)

Index (Absolute)	Mnemonic	Bit	Description	
			Controller will issue an interrupt.	
	USBERR_INT_EN	1	USB Error Interrupt Enable. When this bit is set to '1', and the USBERRINT bit in the USBSTS register is set to '1' also, the Host Controller will issue an interrupt at the next interrupt threshold.	
	USB_INT_EN	0	USB Interrupt Enable. When this bit is set to '1', and the USBINT bit in the USBSTS register is set to '1' also, the Host Controller will issue an interrupt at the next interrupt threshold.	
0Eh (241Ch)	**FRINDEX**	**7:0**	**Default : 0x00**	**Access : R/W**
	FRINDEX[7:0]	7:0	Frame Index. This register is used by the Host Controller to index the frame into the Periodic Frame List. It updates every 125 microseconds. This register cannot be written unless the Host Controller is in the Halted state.	
0Eh (241Dh)	**FRINDEX**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	FRINDEX[13:8]	5:0	See description of '1Ch'.	
12h (2425h)	**PERIODICLISTBASE**	**7:0**	**Default : 0x00**	**Access : R/W**
	PERI_BASADR[15:12]	7:4	Periodic Frame List Base Address. This register contains the beginning address of the Periodic Frame List in the system memory. These bits correspond to memory address signals [31:12].	
	-	3:0	Reserved.	
13h (2426h)	**PERIODICLISTBASE**	**7:0**	**Default : 0x00**	**Access : R/W**
	PERI_BASADR[23:16]	7:0	See description of '25h'.	
13h (2427h)	**PERIODICLISTBASE**	**7:0**	**Default : 0x00**	**Access : R/W**
	PERI_BASADR[31:24]	7:0	See description of '25h'.	
14h (2428h)	**ASYNCLISTADDR**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASYNC_LADR[7:5]	7:5	Current Asynchronous List Address. This register contains the address of the next asynchronous queue head to be executed. These bits correspond to memory address signals [31:5].	
	-	4:0	Reserved.	
14h (2429h)	**ASYNCLISTADDR**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASYNC_LADR[15:8]	7:0	Please see description of '28h'.	

UHC0 Register (Bank = 2A)

Index (Absolute)	Mnemonic	Bit	Description	
15h (242Ah)	**ASYNCLISTADDR**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASYNC_LADR[23:16]	7:0	Please see description of '28h'.	
15h (242Bh)	**ASYNCLISTADDR**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASYNC_LADR[31:24]	7:0	Please see description of '28h'.	
16h ~ 17h (242Ch ~ 242Fh)		**7:0**	**Default : -**	**Access :-**
	Reserved	7:0	Reserved	
18h (2430h)	**PORTSC**	**7:0**	**Default : 0x00**	**Access : R/W, R/WC, RO**
	PO_SUSP	7	Port Suspend (R/W). 1: Port is in suspend state. 0: Port is not in suspend state. The Port Enable bit and Suspend bit of this register define the port state as follows: Bits [Port Enable, Suspend] — Port State 0X — Disable 10 — Enable 11 — Suspend During the suspend state, downstream propagation of data is blocked on this port, except for port reset. While in the suspend state, the port is sensitive to resume detection. Writing a zero to this bit is ignored by the Host Controller. The Host Controller will unconditionally set this bit to a zero when: • The software sets Force Port Resume bit to a zero (from a one) • The software sets Port Reset bit to a one (from a zero) Note: Before setting this bit, RUN/STOP bit should be set to 0.	
	F_PO_RESM	6	Force Port Resume (R/W). 1: Resume detected/driven on port. 0: No resume detected/driven on port. Software sets this bit to a one to resume signaling. The Host Controller sets this bit to a one if a J-to-K transition is detected while the port is in the suspend state. When this bit transits to a one for the detection of a J-to-K transition, the Port Change Detect bit in USBSTS register is also set to a one.	

UHC0 Register (Bank = 2A)

Index (Absolute)	Mnemonic	Bit	Description
	-	5:4	Reserved.
	PO_EN_CHG	3	Port Enable/Disable Change (R/WC). 1: Port enable/disable status has changed. 0: No change.
	PO_EN	2	Port Enable/Disable (R/W). 1: Enable. 0: Disable. Ports can only be enabled by the Host Controller as a part of the reset and enable. Software cannot enable a port by writing a one to this field.
	CONN_CHG	1	Connect Status Change (R/WC). 1: Change current connect status. 0: No change. This bit indicates a change has occurred in the port's current connect status.
	CONN_STS	0	Current Connect Status (RO). 1: Device is present on the port. 0: No device is present. This value reflects the current state of the port, and may not correspond directly to cause the Connect Status Change bit to be set. When TST_FORCEEN is set to '1', this signal is the output of U_HDISCON.
18h (2431h)	**PORTSC**	**7:0**	**Default : 0x00** **Access : R/W, RO**
	-	7:4	Reserved.
	LINE_STS	3:2	Line Status (RO). These bits reflect the current logical levels of the D+ and D- signal lines.
	-	1	Reserved.
	PO_RESET	0	Port Reset. 1: Port is in reset. 0: Port is not in reset. When the software writes a one to this bit, the bus reset sequence as defined in the USB spec will be started. Software writes a zero to this bit can terminate the bus reset sequence. Software must keep this bit at a one long enough to ensure the reset sequence. Note: Before setting this bit, RUN/STOP bit should be set to 0.

UHC0 Register (Bank = 2A)

Index (Absolute)	Mnemonic	Bit	Description	
19h 2432h	-	7:0	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	FORCE_TST_ENABLE	0	Force UHC enter test mode to issue test packet. The bit must set before clearing VBUS_OFF. Or it cannot enter test mode successfully.	
1Ah (2434h)	**HCMISC**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7	Reserved.	
	U_SUSP_N	6	Transceiver Suspend Mode. Active LOW places the transceiver in suspend mode that draws minimal power from power supplies. This is part of the power management.	
	EOF2_TIME	5:4	EOF 2 Timing Points, controlling EOF 2 timing point before next SOF. High-Speed EOF2 Time: 00: 2 clocks (30 MHz) = 66ns. 01: 4 clocks (30 MHz) = 133ns. 10: 8 clocks (30 MHz) = 266ns. 11: 16 clocks (30 MHz) = 533ns. Full-Speed EOF2 Time: 00: 20 clocks (30 MHz) = 666ns. 01: 40 clocks (30 MHz) = 1.333us. 10: 80 clocks (30 MHz) = 2.66us. 11: 160 clocks (30 MHz) = 5.3us. Low-Speed EOF2 Time: 00: 40 clocks (30 MHz) = 1.33us. 01: 80 clocks (30 MHz) = 2.66us. 10: 160 clocks (30 MHz) = 5.33us. 11: 320 clocks (30 MHz) = 10.66us.	
	EOF1_TIME	3:2	EOF 1 Timing Points, controlling EOF 1 timing point before next SOF. This value should be adjusted according to the maximum packet size. High-Speed EOF1 Time: 00: 540 clocks (30 MHz) = 18us. 01: 360 clocks (30 MHz) = 12us. 10: 180 clocks (30 MHz) = 6us. 11: 720 clocks (30 MHz) = 24us. Full-Speed EOF1 Time: 00: 1600 clocks (30 MHz) = 53.3us. 01: 1400 clocks (30 MHz) = 46.6us.	

UHC0 Register (Bank = 2A)

Index (Absolute)	Mnemonic	Bit	Description
			10: 1200 clocks (30 MHz) = 40us. 11: 21000 clocks (30 MHz) = 700us. Low-Speed EOF1 Time: 00: 3750 clocks (30 MHz) = 125us. 01: 3500 clocks (30 MHz) = 116us. 10: 3250 clocks (30 MHz) = 108us. 11: 4000 clocks (30 MHz) = 133us.
	ASYN_SCH_SLPT	1:0	Asynchronous Schedule Sleep Timer, controlling the Asynchronous Schedule sleep timer. 00: 5us. 01: 10us. 10: 15us. 11: 20us.
20h (2440h)	**BMCS**	**7:0**	**Default : 0x10** **Access : R/W**
	FORCE_NO_CHIRP	7	Force Full/Low speed mode
	-	6:5	Reserved (must be set to '0' at all times).
	VBUS_OFF	4	VBUS Off. This bit controls the voltage on VBUS ON/OFF (Default is OFF) or in other words, the signal U_DRVBUS. 0: VBUS On. 1: VBUS Off.
	INT_POLARITY	3	Control the polarity of system interrupt signal SYS_INT_N. 0: Active LOW (default). 1: Active HIGH.
	HALF_SPEED	2	Half Speed Enable. 1: FIFO controller asserts ACK to DMA once every two clock cycles. 0: FIFO controller asserts ACK to DMA continuously. This bit is set to '1' while implementing FPGA.
	HDISCON_FLT_SEL	1	Select a timer to filter out noise of HDISCON from UTMI+. 0: Approximated to 135 us. 1: Approximated to 270 us.
	VBUS_FLT_SEL	0	Select a timer to filter out noise of VBUS_VLD from UTMI+. This signal is valid when signal U_VBUSVLD is connected. 0: Approximated to 135 us.

UHC0 Register (Bank = 2A)

Index (Absolute)	Mnemonic	Bit	Description	
			1: Approximated to 472 us.	
20h (2441h)	**BMCS**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	HOST_SPD_TYP	2:1	Host Speed Type, indicating speed type of the attached device. 10: HS. 00: FS. 01: LS. 11: Reserved.	
	VBUS_VLD	0	VBUS Valid. When the voltage on VBUS is above the valid VBUS threshold, this signal is valid when U_VBUSVLD is connected.	
22h (2444h)	**BUSMONINTSTS**	**7:0**	**Default : 0x00**	**Access : R/WC**
	-	7:5	Reserved.	
	DMA_ERROR	4	DMA Error Interrupt. DMA operation cannot be finished normally, and an error signal is received. When CPU initiates DMA to fill up or read out device's FIFO, and DMA controller gets error response from system bus, this bit will be set. This bit can only be cleared by firmware. It is not affected by USB bus reset.	
	DMA_CMPLT	3	DMA Completion Interrupt. DMA operation is finished normally. When CPU initiates DMA to fill up or read out device's FIFO, this bit will be set after mission completion. This bit can only be cleared by firmware. It is not affected by USB bus reset.	
	DPLGRMV	2	Device Plug Remove. This register is set to '1' once the device plug is removed. Writing '1' clears this register and writing '0' takes no effect.	
	OVC	1	Over Current Detection. This register is set to '1' when the VBUS does not reach VBUS_VLD within the expected time. Writing '1' clears this register and writing '0' takes no effect. This signal is valid when signal U_VBUSVLD is connected.	
	VBUS_ERR	0	VBUS Error.	

UHC0 Register (Bank = 2A)

Index (Absolute)	Mnemonic	Bit	Description	
			This register is set to '1' when the Bus Monitor state machine moves to "VBUS_ERROR" state. Writing '1' clears this register and writing '0' takes no effect. This signal is valid when signal U_VBUSVLD is connected.	
24h (2448h)	**BUSMONINTEN**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DMA_ERROR_EN	4	DMA_ERROR interrupt enable.	
	DMA_CMPLT_EN	3	DMA_CMPLT interrupt enable.	
	BPLGRMV_EN	2	BPLGRMV interrupt enable.	
	OVC_EN	1	OVC interrupt enable.	
	A_VBUS_ERR_EN	0	A_VBUS_ERR interrupt enable.	
28h (2450h)	**TST**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	TST_LOOPBK	4	FIFO Loop Back Mode. A '1' turns on the loop-back mode. When this bit is set to '1', the Host Controller will enter the loop-back mode. During the loop-back mode, the Host Controller will use manual setting of DMA control to trigger DMA master.	
	TST_MOD	3	Test Mode. A '1' turns on the test mode. When this bit is set to '1', the Host Controller will enter the test mode. This test mode can save simulation time. In normal mode, the Host Controller uses a counter for 10 ms detection of USB reset. The count is a large number. In test mode, the Host Controller will use a smaller number counter for USB reset detection to save the test cycle on test machine.	
	TST_PKT	2	Test Mode for Packet. Upon writing a '1' to this bit, the Host Controller repetitively sends the packet defined in UTMI spec. to transceiver. Run/Stop bit should also be enabled to enable the function.	
	TST_KSTA	1	Upon writing a '1', the D+/D- is set to the high-speed K state.	
	TST_JSTA	0	Upon writing a '1', the D+/D- is set to the high-speed J	

UHC0 Register (Bank = 2A)

Index (Absolute)	Mnemonic	Bit	Description	
			state.	
38h (2470h)	**DMACTLPARA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DMA_IO	3	DMA IO to IO. Force DMA Controller not to toggle address. This bit is set when the DMA target is not a system memory but an IO device. If this register is set to '1', the 'DMA_LEN' must be an integer multiple of DWORD (4 byes), and the 'DMA_MADDR' must align to the boundary of DWORD (4 bytes).	
	-	2	Reserved.	
	DMA_TYPE	1	DMA Type, the transfer type of data moving. 0: FIFO to Memory. 1: Memory to FIFO.	
	DMA_START	0	DMA Start, informing DMA Controller to initiate DMA transfer. This bit is set to start the transfer and cleared when the DMA operation is completed. Note that this bit cannot be cleared by software; it can only be cleared by hardware in the case of either DMA completion or DMA error. Note that if DMA_LEN and DMA_START are set at the same time, the DMA_LEN will take effect immediately.	
38h (2471h)	**DMACTLPARA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_LEN[7:0]	7:0	DMA Length. The total bytes the DMA Controller will move. The unit is byte. The maximum length could be 1024B-1.	
39h (2472h)	**DMACTLPARA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_LEN[15:8]	7:0	See description of '71h'.	
39h (2473h)	**DMACTLPARA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	DMA_LEN[16]	0	See description of '71h'.	
3Ah (2474h)	**DMACTLPARA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_MADDR[7:0]	7:0	DMA Memory Address. The starting address of memory to request DMA transfer.	
3Ah	**DMACTLPARA2**	**7:0**	**Default : 0x00**	**Access : R/W**

UHC0 Register (Bank = 2A)

Index (Absolute)	Mnemonic	Bit	Description	
(2475h)	DMA_MADDR[15:8]	7:0	See description of '74h'.	
3Bh (2476h)	**DMACTLPARA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_MADDR[23:16]	7:0	See description of '74h'.	
3Bh (2477h)	**DMACTLPARA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_MADDR[31:24]	7:0	See description of '74h'.	
40h (2480h)	**PROJ_SPEC_REG0**	7:0	**Default: 0x00**	**Access: R/W, WO**
	DBUS_SELECT	7:5	Selects debug bus banks.	
	UTMI_SELECT	4	Selects external UTMI.	
	OLD_XI2PV	3	Enables old version XIU access.	
	CLK_STOP	2	Triggers the clock stop mechanism.	
	EN_RD_RD_SCRAMBLE	1	Enables memory inverted read.	
	EN_RD_WR_SCRAMBLE	0	Enables memory inverted write.	
40h (2481h)	**PROJ_SPEC_REG1**	**7:0**	**Default: 0x00**	**Access: R/W**
	SPLIT_SHORT_PKT_CLR_ACT	7	If the transfer is a periodic split transaction, the active status will be cleared when a short packet is received.	
	NON_ALIGN_EN	6	Enables MIU address non-alignment mode. It also means enabling new PV2MI bridge.	
	INVALID_MIU_ACS_INTEN	5	Enables interrupt when MIU invalid write occurs.	
	MIU_WR_PROTECT_EN	4	Enables MIU write protect.	
	DAT_RD_PRI_EN	3	The enable option (MIU priority access) of the "data read".	
	DAT_WR_PRI_EN	2	The enable option (MIU priority access) of the "data write".	
	QT_RD_PRI_EN	1	The enable option (MIU priority access) of the "q-table read".	
	QT_WR_PRI_EN	0	The enable option (MIU priority access) of the "q-table write".	
41h (2482h)	**PROJ_SPEC_REG2**	**7:0**	**Default: 0x00**	**Access: R/W**
	QT_RD_PRI_SEL	7:6	The select (delay time of MIU priority assert) of the "q-table read".	
	QT_WR_PRI_SEL	5:4	The select (delay time of MIU priority assert) of the "q-table write".	
	DAT_RD_PRI_SEL	3:2	The select (delay time of MIU priority assert) of the "data read".	

UHC0 Register (Bank = 2A)

Index (Absolute)	Mnemonic	Bit	Description	
	DAT_RD_PRI_SEL	1:0	The select (delay time of MIU priority assert) of the "data write".	
41h (2483h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	7:0	Reserved.	
42h (2484h)	**FDBUS_REG0**	**7:0**	**Default: 0x00**	**Access: RO**
	fusbh200_dbus[7:0]	7:0	Internal bus for debugging.	
42h (2485h)	**FDBUS_REG1**	**7:0**	**Default: 0x00**	**Access: RO**
	fusbh200_dbus[15:8]	7:0	Internal bus for debugging.	
43h (2486h)	**FDBUS_REG2**	**7:0**	**Default: 0x00**	**Access: RO**
	fusbh200_dbus[23:16]	7:0	Internal bus for debugging.	
43h (2487h)	**FDBUS_REG3**	**7:0**	**Default: 0x00**	**Access: RO**
	fusbh200_dbus[31:24]	7:0	Internal bus for debugging.	
44h (2488h)	**FDBUS_REG4**	**7:0**	**Default: 0x00**	**Access: RO**
	fusbh200_dbus[39:32]	7:0	Internal bus for debugging.	
44h (2489h)	**FDBUS_REG5**	**7:0**	**Default: 0x00**	**Access: RO**
	fusbh200_dbus[47:40]	7:0	Internal bus for debugging.	
45h (248Ah)	**STATUS_REG**	**7:0**	**Default: 0x00**	**Access: R/W1C**
	-	7:1	Reserved	
	INVALID_MIU_ACS	0	Interrupt status of invalid MIU write.	
45h (248B)	**-**	**7:0**	**Default: -**	**Access: -**
	-	7:0	Reserved	
46h (248Ch)	**MIU_WRITE_RANGE0**	**7:0**	**Default: 0x00**	**Access: R/W**
	LOWER_BOUND[7:0]	7:0	MIU write protect lower boundary address [7:0]: MIU write will be an invalid access if the write address is above the upper boundary address or below the lower boundary address.	
46h (248Dh)	**MIU_WRITE_RANGE1**	**7:0**	**Default: 0x00**	**Access: R/W**
	LOWER_BOUND[15:8]	7:0	MIU write protect lower boundary address [15:8]: MIU write will be an invalid access if the write address is above the upper boundary address or below the lower boundary address.	
47h (248Eh)	**MIU_WRITE_RANGE2**	**7:0**	**Default: 0x00**	**Access: R/W**
	LOWER_BOUND[23:16]	7:0	MIU write protect lower boundary address [23:16]: MIU write will be an invalid access if the write address	

UHC0 Register (Bank = 2A)

Index (Absolute)	Mnemonic	Bit	Description	
			is above the upper boundary address or below the lower boundary address.	
47h (248Fh)	**MIU_WRITE_RANGE3**	**7:0**	**Default: 0xFF**	**Access: R/W**
	UPPER_BOUND[7:0]	7:0	MIU write protect upper boundary address [7:0]: MIU write will be an invalid access if the write address is above the upper boundary address or below the lower boundary address.	
48h (2490h)	**MIU_WRITE_RANGE4**	**7:0**	**Default: 0xFF**	**Access: R/W**
	UPPER_BOUND[15:8]	7:0	MIU write protect upper boundary address [15:8]: MIU write will be an invalid access if the write address is above the upper boundary address or below the lower boundary address.	
48h (2491h)	**MIU_WRITE_RANGE5**	**7:0**	**Default: 0xFF**	**Access: R/W**
	UPPER_BOUND[23:16]	7:0	MIU write protect upper boundary address [23:16]: MIU write will be an invalid access if the write address is above the upper boundary address or below the lower boundary address.	

IRQ_0 Register (Bank = 2B)

IRQ_0 Register (Bank = 2B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (5600h)	**REG5600**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_FIQ_MASK[7:0]	7:0	Mask for FIQ, bit[31:0]. 1: Mask. 0: Not mask.	
00h (5601h)	**REG5601**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_FIQ_MASK[15:8]	7:0	See description of '5600h'.	
01h (5604h)	**REG5604**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_FIQ_MASK[23:16]	7:0	See description of '5600h'.	
01h (5605h)	**REG5605**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_FIQ_MASK[31:24]	7:0	See description of '5600h'.	
02h (5608h)	**REG5608**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_FORCE[7:0]	7:0	Force for FIQ, bit [31:0]. 1: Force. 0: Not force.	
02h (5609h)	**REG5609**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_FORCE[15:8]	7:0	See description of '5608h'.	
03h (560Ch)	**REG560C**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_FORCE[23:16]	7:0	See description of '5608h'.	
03h (560Dh)	**REG560D**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_FORCE[31:24]	7:0	See description of '5608h'.	
04h (5610h)	**REG5610**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_CLR7	7	Clear for FIQ, bit7.	
	C_FIQ_CLR6	6	Clear for FIQ, bit6.	
	C_FIQ_CLR5	5	Clear for FIQ, bit5.	
	C_FIQ_CLR4	4	Clear for FIQ, bit4.	
	C_FIQ_CLR3	3	Clear for FIQ, bit3.	
	C_FIQ_CLR2	2	Clear for FIQ, bit2.	
	C_FIQ_CLR1	1	Clear for FIQ, bit1.	
	C_FIQ_CLR0	0	Clear for FIQ, bit0.	
04h (5611h)	**REG5611**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_CLR15	7	Clear for FIQ, bit15.	
	C_FIQ_CLR14	6	Clear for FIQ, bit14.	

IRQ_0 Register (Bank = 2B)

Index (Absolute)	Mnemonic	Bit	Description	
	C_FIQ_CLR13	5	Clear for FIQ, bit13.	
	C_FIQ_CLR12	4	Clear for FIQ, bit12.	
	C_FIQ_CLR11	3	Clear for FIQ, bit11.	
	C_FIQ_CLR10	2	Clear for FIQ, bit10.	
	C_FIQ_CLR9	1	Clear for FIQ, bit9.	
	C_FIQ_CLR8	0	Clear for FIQ, bit8.	
05h (5614h)	**REG5614**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_CLR23	7	Clear for FIQ, bit23.	
	C_FIQ_CLR22	6	Clear for FIQ, bit22.	
	C_FIQ_CLR21	5	Clear for FIQ, bit21.	
	C_FIQ_CLR20	4	Clear for FIQ, bit20.	
	C_FIQ_CLR19	3	Clear for FIQ, bit19.	
	C_FIQ_CLR18	2	Clear for FIQ, bit18.	
	C_FIQ_CLR17	1	Clear for FIQ, bit17.	
	C_FIQ_CLR16	0	Clear for FIQ, bit16.	
05h (5615h)	**REG5615**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_CLR31	7	Clear for FIQ, bit31.	
	C_FIQ_CLR30	6	Clear for FIQ, bit30.	
	C_FIQ_CLR29	5	Clear for FIQ, bit29.	
	C_FIQ_CLR28	4	Clear for FIQ, bit28.	
	C_FIQ_CLR27	3	Clear for FIQ, bit27.	
	C_FIQ_CLR26	2	Clear for FIQ, bit26.	
	C_FIQ_CLR25	1	Clear for FIQ, bit25.	
	C_FIQ_CLR24	0	Clear for FIQ, bit24.	
06h (5618h)	**REG5618**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_RAW_STATUS[7:0]	7:0	FIQ Raw Status, bit [31:0]. Interrupt source status for FIQ.	
06h (5619h)	**REG5619**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_RAW_STATUS[15:8]	7:0	See description of '5618h'.	
07h (561Ch)	**REG561C**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_RAW_STATUS[23:16]	7:0	See description of '5618h'.	
07h (561Dh)	**REG561D**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_RAW_STATUS[31:24]	7:0	See description of '5618h'.	

IRQ_0 Register (Bank = 2B)

Index (Absolute)	Mnemonic	Bit	Description	
08h (5620h)	**REG5620**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_FINAL_STATUS[7:0]	7:0	FIQ Final Status, bit [31:0]. Final interrupt status for FIQ.	
08h (5621h)	**REG5621**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_FINAL_STATUS[15:8]	7:0	See description of '5620h'.	
09h (5624h)	**REG5624**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_FINAL_STATUS[23:16]	7:0	See description of '5620h'.	
09h (5625h)	**REG5625**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_FINAL_STATUS[31:24]	7:0	See description of '5620h'.	
0Ah (5628h)	**REG5628**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_SEL_HL_TRIGGER[7:0]	7:0	Select H or L trigger, bit[31:0]. Inverse source polarity for FIQ.	
0Ah (5629h)	**REG5629**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_SEL_HL_TRIGGER[15:8]	7:0	See description of '5628h'.	
0Bh (562Ch)	**REG562C**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_SEL_HL_TRIGGER[23:16]	7:0	See description of '5628h'.	
0Bh (562Dh)	**REG562D**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_SEL_HL_TRIGGER[31:24]	7:0	See description of '5628h'.	
0Ch (5630h)	**REG5630**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_IRQ_MASK[7:0]	7:0	Mask for IRQ, bit [31:0]. 1: Mask. 0: Not mask.	
0Ch (5631h)	**REG5631**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_IRQ_MASK[15:8]	7:0	See description of '5630h'.	
0Dh (5634h)	**REG5634**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_IRQ_MASK[23:16]	7:0	See description of '5630h'.	
0Dh (5635h)	**REG5635**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_IRQ_MASK[31:24]	7:0	See description of '5630h'.	
10h (5640h)	**REG5640**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_FORCE[7:0]	7:0	Force for IRQ, bit[31:0]. 1: Force. 0: Not force.	
10h (5641h)	**REG5641**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_FORCE[15:8]	7:0	See description of '5640h'.	

IRQ_0 Register (Bank = 2B)

Index (Absolute)	Mnemonic	Bit	Description	
11h (5644h)	**REG5644**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_FORCE[23:16]	7:0	See description of '5640h'.	
11h (5645h)	**REG5645**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_FORCE[31:24]	7:0	See description of '5640h'.	
14h (5650h)	**REG5650**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_SEL_HL_TRIGGER[7:0]	7:0	Select H or L trigger, bit[31:0]. Inverse source polarity for IRQ.	
14h (5651h)	**REG5651**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_SEL_HL_TRIGGER[15:8]	7:0	See description of '5650h'.	
15h (5654h)	**REG5654**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_SEL_HL_TRIGGER[23:16]	7:0	See description of '5650h'.	
15h (5655h)	**REG5655**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_SEL_HL_TRIGGER[31:24]	7:0	See description of '5650h'.	
18h (5660h)	**REG5660**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS[7:0]	7:0	IRQ Raw Status, bit[63:0]. Interrupt source status for IRQ.	
18h (5661h)	**REG5661**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS[15:8]	7:0	See description of '5660h'.	
19h (5664h)	**REG5664**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS[23:16]	7:0	See description of '5660h'.	
19h (5665h)	**REG5665**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS[31:24]	7:0	See description of '5660h'.	
1Ah (5668h)	**REG5668**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS[39:32]	7:0	See description of '5660h'.	
1Ah (5669h)	**REG5669**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS[47:40]	7:0	See description of '5660h'.	
1Bh (566Ch)	**REG566C**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS[55:48]	7:0	See description of '5660h'.	
1Bh (566Dh)	**REG566D**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS[63:56]	7:0	See description of '5660h'.	
1Ch (5670h)	**REG5670**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS[7:0]	7:0	IRQ Final Status, bit[63:0]. Final interrupt status for IRQ.	

IRQ_0 Register (Bank = 2B)

Index (Absolute)	Mnemonic	Bit	Description	
1Ch (5671h)	**REG5671**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS[15:8]	7:0	See description of '5670h'.	
1Dh (5674h)	**REG5674**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS[23:16]	7:0	See description of '5670h'.	
1Dh (5675h)	**REG5675**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS[31:24]	7:0	See description of '5670h'.	
1Eh (5678h)	**REG5678**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS[39:32]	7:0	See description of '5670h'.	
1Eh (5679h)	**REG5679**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS[47:40]	7:0	See description of '5670h'.	
1Fh (567Ch)	**REG567C**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS[55:48]	7:0	See description of '5670h'.	
1Fh (567Dh)	**REG567D**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS[63:56]	7:0	See description of '5670h'.	
20h (5680h)	**REG5680**	**7:0**	**Default : 0xFF**	**Access : R/W**
	FIQ2IRQOUT[7:0]	7:0	Select FIQ source output to IRQ.	
20h (5681h)	**REG5681**	**7:0**	**Default : 0xFF**	**Access : R/W**
	FIQ2IRQOUT[15:8]	7:0	See description of '5680h'.	
21h (5684h)	**REG5684**	**7:0**	**Default : 0xFF**	**Access : R/W**
	FIQ2IRQOUT[23:16]	7:0	See description of '5680h'.	
21h (5685h)	**REG5685**	**7:0**	**Default : 0xFF**	**Access : R/W**
	FIQ2IRQOUT[31:24]	7:0	See description of '5680h'.	
22h (5688h)	**REG5688**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_IDX[7:0]	7:0	FIQ index for first priority source.	
23h (568Ch)	**REG568C**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_IDX[7:0]	7:0	IRQ index for first priority source.	
24h (5690h)	**REG5690**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPARE0[7:0]	7:0	Spare register.	
24h (5691h)	**REG5691**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPARE1[7:0]	7:0	Spare register.	

XD2MIU Register (Bank = 2B)

XD2MIU Register (Bank = 2B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
60h (5780h)	**REG5780**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SOFTWARE_RST	0	Set 1 to reset HK_MCU XDATA2MIU.	
61h (5784h)	**REG5784**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED1[7:0]	7:0	RESERVED1.	
61h (5785h)	**REG5785**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED1[15:8]	7:0	See description of '5784h'.	
62h (5788h)	**REG5788**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	XB_SDR_MAP_EN	2	Set 1 to enable the mapping of HK_MCU XDATA to MIU.	
	XD2MIU_WPRI	1	XDATA2MIU write Priority.	
	XD2MIU_RPRI	0	XDATA2MIU read Priority.	
63h (578Ch)	**REG578C**	**7:0**	**Default : 0x00**	**Access : R/W**
	XB_ADDR[7:0]	7:0	The low bound address of MCU XDATA mapping to MIU. The unit is 1k bytes. The XDATA address is hit if (XB_ADDR[15:8] > xdata_addr[15:10] >= XB_ADDR[7:0]),.	
63h (578Dh)	**REG578D**	**7:0**	**Default : 0x00**	**Access : R/W**
	XB_ADDR[15:8]	7:0	See description of '578Ch'.	
64h (5790h)	**REG5790**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_XD_MAP[7:0]	7:0	The low byte address to access xdata from MIU. The granularity is 64k bytes. The actual address[23:0] to miu would be{SDR_XD_MAP[11:8], SDR_XD_MAP[7:0],xdata_addr[15:4]}, where xdata_addr[15:0] is mcu xdata address of 64k bytes.	
64h (5791h)	**REG5791**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_XD_MAP[15:8]	7:0	See description of '5790h'.	
65h (5794h)	**REG5794**	**7:0**	**Default : 0x00**	**Access : R/W**
	XB_ADDR_1[7:0]	7:0	The low bound address of MCU XDATA mapping to MIU. The unit is 1k bytes. The XDATA address is hit if (XB_ADDR_1[15:8] > xdata_addr[15:10] >= XB_ADDR_1[7:0]),.	
65h	**REG5795**	**7:0**	**Default : 0x00**	**Access : R/W**

XD2MIU Register (Bank = 2B)

Index (Absolute)	Mnemonic	Bit	Description	
(5795h)	XB_ADDR_1[15:8]	7:0	See description of '5794h'.	
66h (5798h)	**REG5798**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_XD_MAP_1_0[7:0]	7:0	The low byte address to access xdata from MIU. The granularity is 4k bytes. Where xdata_addr[15:0] is mcu xdata address of 64k bytes.	
66h (5799h)	**REG5799**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_XD_MAP_1_0[15:8]	7:0	See description of '5798h'.	
67h (579Ch)	**REG579C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_XD_MAP_1_1[7:0]	7:0	The actual byte address for SDRAM would be. {SDR_XD_MAP_1_1[3:0], reg_sdr_xd_map_1_0[15:0], xdata_addr[11:0]}. Note: Xdata_addr[11:0] comes from MCU51.	
67h (579Dh)	**REG579D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_XD_MAP_1_1[15:8]	7:0	See description of '579Ch'.	

HAYDN2_0 Register (Bank = 2C)

HAYDN2_0 Register (Bank = 2C)				
Index	**Mnemonic**	**Bit**	**Description**	
2C00h	**REG2C00**	**15:0**	**Default : 0x0000**	**Access : R/W**
	ENABLE_CTRL[15:0]	15:0	2C00. [15] REG_RESET_ALL. Audio reset. 0 = normal. 1 = reset. [14] REG_GATE_ALL_CLK. All audio clocks gated. 0 = normal. 1 = gated. [13] REG_MAP_NF_SYNTH_TRIG. Mmp nf synthesizer trigger. 0 = disable. 1 = enable. [12] REG_BT_NF_SYNTH_TRIG. Bt nf synthesizer trigger. 0 = disable. 1 = enable. [11:8] REG_INT_ENABLE. Enable DAC1~4 gating. 0 = disable. 1 = enable. [7:4] REG_CIC_ENABLE. Enable ADC1~4 gating. 0 = disable. 1 = enable. [3] reserved. [2] REG_INI_DATASRAM. Initialize sram. 0 = disable. 1 = enable. [1] EN_SDM. Enable SDM. 0 = disable. 1 = enable. [0] EN_TIME_GEN. Enalbe time gen. 0 = disable. 1 = enable.	

HAYDN2_0 Register (Bank = 2C)

Index	Mnemonic	Bit	Description	
2C02h	**REG2C02**	**15:0**	**Default : 0x0000**	**Access : R/W**
	MUX_CTRL[15:0]	15:0	2C02. [15:11] reserved. [10] BT_ULK_STEREO. Enable bt ulk stereo. 0 = BT_ULK_DPGA_DOUT. 1 = DEC_DATA. [9] REG_DIG_MIC_HPF_BPS_1. Bypass digital mic hpf1. 0 = normal. 1 = bypass. [8] REG_DIG_MIC_HPF_BPS_0. Bypass digital mic hpf0. 0 = normal. 1 = bypass. [7:6] reserved. [5] REG_DIG_MIC_128FS. Digital mic select 128fs. 0 = 64fs. 1 = 128fs. [4] REG_DMA_WR_SEL. Select DMA writer input. 0 = DEC_DATA_L/R. 1 = BT_I2S_RX_LDATA, DEC_DATA_M. [3:2] REG_DEC_S2M_SEL. Select S2M mode. 00 = 0.5*(L+R). 01 = L+R. 10 = L. 11 = R. [1:0] REG_MMP_MUX_SEL. Select MMP input. 00 = DMA1_RD_DATA_L/R. 01 = BT_I2S_RX_DOUT_L/R. 10 = DIG_MIC_DATA. 11 = 0.	
2C04h	**REG2C04**	**15:0**	**Default : 0x0000**	**Access : R/W**
	MIX_CTRL[15:0]	15:0	2C04. [15:12] reserved. [11:10] REG_DEC_MIX_SEL_L. Mix dec_mix input left channel.	

HAYDN2_0 Register (Bank = 2C)

Index	Mnemonic	Bit	Description	
			00 = 0. 01 = CH1_INT_OUT_L_SYNC. 10 = CH2_INT_OUT_L_SYNC. 11 = CH1_INT_OUT_L_SYNC + CH2_INT_OUT_L_SYNC. [9:8] REG_DEC_MIX_SEL_R. Mix dec_mix input right channel. 00 = 0. 01 = CH1_INT_OUT_R_SYNC. 10 = CH2_INT_OUT_L_SYNC. 11 = CH1_INT_OUT_R_SYNC + CH2_INT_OUT_L_SYNC. [7:6] REG_DAC_MIX_SEL_L. Mix dac_mix left channel. 00 = 0. 01 = CH1_ANA_OUT_L_SYNC. 10 = CH2_ANA_OUT_L_SYNC. 11 = CH1_ANA_OUT_L_SYNC + CH2_ANA_OUT_L_SYNC. [5:4] REG_DAC_MIX_SEL_R. Mix dac_mix input right channel. 00 = 0. 01 = CH1_ANA_OUT_R_SYNC. 10 = CH2_ANA_OUT_L_SYNC. 11 = CH1_IANA_OUT_R_SYNC + CH2_ANA_OUT_L_SYNC. [3:2] REG_SDM_L_SEL. Mix SDM_DWA_TOP left input. 00 = 0. 01 = DAC_MIX_OUT_L. 10 = DAC_MIX_OUT_R. 11 = 0.5*(DAC_MIX_OUT_L + DAC_MIX_OUT_R). [1:0] REG_SDM_R_SEL. Mix SDM_DWA_TOP right input. 00 = 0. 01 = DAC_MIX_OUT_R. 10 = DAC_MIX_OUT_L. 11 = 0.5*(DAC_MIX_OUT_L + DAC_MIX_OUT_R).	
2C06h	**REG2C06**	**15:0**	**Default : 0x05DC**	**Access : R/W**
	MMP_NF_SYNTH_H[15:0]	15:0	2C06. [15:14] reserved. [13:0]. MMP N.F synthesizer value high word. Dec2hex(round(CLK_AU_HIGH_FREQ/MMP_NF_SYNTH_256FS*2^20/128)).	

HAYDN2_0 Register (Bank = 2C)

Index	Mnemonic	Bit	Description	
2C08h	**REG2C08**	**15:0**	**Default : 0x0000**	**Access : R/W**
	MMP_NF_SYNTH_L[15:0]	15:0	2C08. [15:0]. MMP N.F synthesizer value low word. Dec2hex(round(CLK_AU_HIGH_FREQ/MMP_NF_SYNTH_256FS*2^20/128)).	
2C0Ah	**REG2C0A**	**15:0**	**Default : 0x05DC**	**Access : R/W**
	BT_NF_SYNTH_H[15:0]	15:0	2C0A. [15:14] reserved. [13:0]. BT N.F synthesizer value high word. Dec2hex(round(CLK_AU_HIGH_FREQ/BT_NF_SYNTH_256FS*2^20/128)).	
2C0Ch	**REG2C0C**	**15:0**	**Default : 0x0000**	**Access : R/W**
	BT_NF_SYNTH_L[15:0]	15:0	2C0C. [15:0]. BT N.F synthesizer value low word. Dec2hex(round(CLK_AU_HIGH_FREQ/BT_NF_SYNTH_256FS*2^20/128)).	
2C0Eh	**REG2C0E**	**15:0**	**Default : 0x0000**	**Access : R/W**
	SYNTH_BANDWIDTH[15:0]	15:0	2C0E. [15:8] reserved. [7] REG_MMP_FS_SYNTH_FF. MMP FS synthesizer force lock current frequency. 0 = unlock. 1 = lock. [6:4] REG_MMP_FS_SYNTH_BW. MMP FS synthesizer bandwidth selection. 0~7 (the higher the narrower). [3] REG_BT_FS_SYNTH_FF. BT FS synthesizer force lock current frequency. 0 = unlock. 1 = lock. [2:0] REG_BT_FS_SYNTH_BW. BT FS synthesizer bandwidth selection. 0~7 (the higher the narrower).	
2C10h	**REG2C10**	**15:0**	**Default : 0x0022**	**Access : R/W**
	MMP_INT_SYNTH[15:0]	15:0	2C10. [15:7] reserved.	

HAYDN2_0 Register (Bank = 2C)

Index	Mnemonic	Bit	Description	
			[6:0] MMP_INT_SYNTH.	
2C12h	**REG2C12**	**15:0**	**Default : 0x0001**	**Access : R/W**
	MAC_INT_SYNTH[15:0]	15:0	2C12. [15:7] reserved. [6:0] MAC_INT_SYNTH.	
2C14h	**REG2C14**	**15:0**	**Default : 0x0000**	**Access : R/W**
	BT_I2S_TRX_CTRL[15:0]	15:0	2C14. [15] RESETB_T/RX. Reset i2s tx and rx. 0 = reset. 1 = normal. [14] REG_I2S_T/RX_FMT. I2s format. 0 = i2s. 1 = left-justified. [13] REG_I2S_T/RX_FIFO_CLR. Clear tx/rx fifo. 0 = normal. 1 = clear. [12] REG_I2S_T/RX_MS. Master/slave mode seletion. 0 = slave. 1 = master. [11] REG_I2S_T/RX_BCK_INV. I2s bck invert. 0 = normal. 1 = invert. [10] REG_I2S_T/RX_PCM_MODE. I2s PCM mode. 0 = disable. 1 = enable. [9:8] REG_I2S_T/RX_BWH. I2sw bit width selection. 00 = 32. 01 = 48. 10 = 64. 11 = 50. [7:6] I2S_T/RX_MUX_SEL_R. Select right channel input. 00 = normal.	

HAYDN2_0 Register (Bank = 2C)

Index	Mnemonic	Bit	Description	
			01 = L. 10 = 0.5 (L+R). 11 = L+R. [5:4] I2S_T/RX_MUX_SEL_L. Select left channel input. 00 = normal. 01 = R. 10 = 0.5 (L+R). 11 = L+R. [3:0] resrved.	
2C16h	**REG2C16**	**15:0**	**Default : 0x0000**	**Access : R/W**
	EXT_I2S_RX_CTRL[15:0]	15:0	2C16. [15] RESETB_RX. Reset i2s rx. 0 = reset. 1 = normal. [14] REG_I2S_RX_FMT. I2s format. 0 = i2s. 1 = left-justified. [13] REG_I2S_RX_FIFO_CLR. Clear rx fifo. 0 = normal. 1 = clear. [12] REG_I2S_RX_MS. Master/slave mode selection. 0 = slave. 1 = master. [11] REG_I2S_RX_BCK_INV. I2s bck invert. 0 = normal. 1 = invert. [10] REG_I2S_RX_PCM_MODE. I2s PCM mode. 0 = disable. 1 = enable. [9:8] REG_I2S_RX_BWH. I2sw bit width selection. 00 = 32. 01 = 48. 10 = 64.	

HAYDN2_0 Register (Bank = 2C)

Index	Mnemonic	Bit	Description	
			11 = 50. [7:6] I2S_RX_MUX_SEL_R. Select right channel input. 00 = normal. 01 = L. 10 = 0.5 (L+R). 11 = L+R. [5:4] I2S_RX_MUX_SEL_L. Select left channel input. 00 = normal. 01 = R. 10 = 0.5 (L+R). 11 = L+R. [3:0] reserved.	
2C18h	**REG2C18**	**15:0**	**Default : 0x0000**	**Access : R/W**
	SDM_CTRL[15:0]	15:0	2C18. [15] REG_SDM_LOOP. Loop sdm input. 0 = disable. 1 = enable. [14] REG_CLR_MACOVL. Clear mac overflow flag. 0 = normal. 1 = clear. [13] REG_DAC_TEST_EN. Sdm quant output test mode enable. 0 = normal. 1 = test mode (REG_2C1A[15:10]). [12] REG_AU_TEST_CLK_INV. Audio test clock invert. 0 = normal. 1 = invert. [11] REG_DWA_TEST_EN. Dwa test mode enable, select audio test clock. 0 = normal (BT_NF_SYNTH_256FS. 1 = TEST_BUS[0]. [10:6] REG_FIX_MSB_SEL. DWA fix MSB selection. [5] REG_FIX_MSB_EN. Enable DWA fix MSB. 0 = disable.	

HAYDN2_0 Register (Bank = 2C)

Index	Mnemonic	Bit	Description	
			1 = enable. [4] REG_SHIFT_DIS. Disable dwa out bit shift. 0 = enable. 1 = disable. [3:1] REG_DITHER_SEL. SDM dither selection. [0] REG_DITHER_EN. SDM dither enable. 0 = disable. 1 = enable.	
2C1Ah	**REG2C1A**	**15:0**	**Default : 0x0000**	**Access : R/W**
	OFFSET_CTRL[15:0]	15:0	2C1A. [15:0] REG_OFFSET[17:2]. SDM input/ quant out offset.	
2C1Ch	**REG2C1C**	**15:0**	**Default : 0xB000**	**Access : R/W**
	PAD_BT_I2S_CTRL[15:0]	15:0	2C1C. [15] REG_BT_I2S_BCK_DG_EN. Bt i2s bck deglitch enable. 0 = disable. 1 = enable. [14] REG_BT_I2S_LOOP_INNER. Bt i2s sdo loop back to sdi enable. 0 = disable. 1 = enable. [13] REG_BT_I2S_WCK_OEN. [12] REG_BT_I2S_BCK_OEN. [11:10] reserved. [9:8] REG_BT_I2S_WCK_O_SEL. PAD_BT_I2S_TRX_WCK_O select. 01 = EXT_I2S_RX_WCK_O. Default = BT_I2S_TRX_WCK_O. [7:6] REG_BT_I2S_WCK_I_SEL. Bt i2s wck input pad select. 01 = PAD_EXT_I2S_RX_WCK_I. Default = PAD_BT_I2S_TRX_WCK_I. [5:4] REG_BT_I2S_BCK_O_SEL. PAD_BT_I2S_TRX_BCK_O select. 01 = EXT_I2S_RX_BCK_O. 10 = DIG_MIC_BCK_O.	

HAYDN2_0 Register (Bank = 2C)

Index	Mnemonic	Bit	Description
			Default = BT_I2S_TRX_BCK_O. [3:2] REG_BT_I2S_BCK_I_SEL. Bt i2s bck input pad select. 01 = PAD_EXT_I2S_RX_BCK_I. Default = PAD_BT_I2S_TRX_BCK_I. [1:0] REG_BT_I2S_SDI_I_SEL. Bt i2s sdi input pad select. 01 = PAD_EXT_I2S_RX_SDI_I. 10 = DIG_MIC_SDI_I. Default = PAD_BT_I2S_TRX_SDI_I.
2C1Eh	**REG2C1E**	**15:0**	**Default : 0xB000** **Access : R/W**
	PAD_EXT_I2S_CTRL[15:0]	15:0	2C1E. [15] REG_EXT_I2S_BCK_DG_EN. Extt i2s bck deglitch enable. 0 = disable. 1 = enable. [14] REG_EXT_I2S_LOOP_INNER. Ext i2s sdo loop back to sdi enable. 0 = disable. 1 = enable. [13] REG_EXT_I2S_WCK_OEN. [12] REG_EXT_I2S_BCK_OEN. [11:10] reserved. [9:8] REG_EXT_I2S_WCK_O_SEL. PAD_EXT_I2S_RX_WCK_O select. 01 = BT_I2S_TRX_WCK_O. Default = EXT_I2S_RX_WCK_O. [7:6] REG_EXT_I2S_WCK_I_SEL. Ext i2s wck input pad select. 01 = PAD_BT_I2S_TRX_WCK_I. Default = PAD_EXT_I2S_RX_WCK_I. [5:4] REG_EXT_I2S_BCK_O_SEL. PAD_EXT_I2S_RX_BCK_O select. 01 = BT_I2S_TRX_BCK_O. 10 = DIG_MIC_BCK_O. Default = EXT_I2S_RX_BCK_O. [3:2] REG_EXT_I2S_BCK_I_SEL. Ext i2s bck input pad select. 01 = PAD_BT_I2S_TRX_BCK_I. Default = PAD_EXT_I2S_RX_BCK_I. [1:0] REG_EXT_I2S_SDI_I_SEL.

HAYDN2_0 Register (Bank = 2C)

Index	Mnemonic	Bit	Description	
			Ext i2s sdi input pad select. 01 = PAD_BT_I2S_TRX_SDI_I. 10 = DIG_MIC_SDI_I. Default = PAD_EXT_I2S_RX_SDI_I.	
2C20h	**REG2C20**	**15:0**	**Default : 0x0000**	**Access : R/W**
	PAD_DIG_MIC_CTRL[15:0]	15:0	2C20. [15:12] REG_DIG_MIC_HPF_CORN. Digital mic high pass filter delay control? [11:4] reserved. [3:2] REG_DIG_MIC_BCK_O_SEL. PAD_DIG_MIC_BCK_O select input. 01 = BT_I2S_TRX_SDO_O. Default = DIG_MIC_BCK_O. [1:0] REG_DIG_MIC_SDI_I_SEL. DIG_MIC_SDI_I select input. 01 = PAD_BT_I2S_TRX_SDI_I. 02 = PAD_EXT_I2S_RX_SDI_I. Default = PAD_DIG_MIC_SDI_I.	
2C22h	**REG2C22**	**15:0**	**Default : 0x0000**	**Access : R/W**
	MAC_FIFO_RESET[15:0]	15:0	2C22. [15:8] reserved. [7:6] reserved. [5:4] REG_DAC_FIFO_RESET. Reset dac fifo in SRC_INT_TOP1~2. 0 = normal. 1 = reset. [3:2] reserved. [1:0] REG_ADC_FIFO_RESET. Reset adc fifo in SRC_INT_TOP1~2. 0 = normal. 1 = reset.	
2C24h	**REG2C24**	**15:0**	**Default : 0x000F**	**Access : R/W**
	FIR_INT_CMP0[15:0]	15:0	2C24. [15:0] REG_DAC_CMP0. Fir coefficient.	
2C26h	**REG2C26**	**15:0**	**Default : 0xFFA4**	**Access : R/W**
	FIR_INT_CMP1[15:0]	15:0	2C26. [15:0] REG_DAC_CMP1. Fir coefficient.	

HAYDN2_0 Register (Bank = 2C)

Index	Mnemonic	Bit	Description	
2C28h	**REG2C28**	**15:0**	**Default : 0x7F40**	**Access : R/W**
	FIR_INT_CMP2[15:0]	15:0	2C28. [15:0] REG_DAC_CMP2. Fir coefficient.	
2C2Ah	**REG2C2A**	**15:0**	**Default : 0x0022**	**Access : R/W**
	FIR_DEC_CMP0[15:0]	15:0	2C2A. [15:0] REG_ADC_CMP0. Fir coefficient.	
2C2Ch	**REG2C2C**	**15:0**	**Default : 0xFEF9**	**Access : R/W**
	FIR_DEC_CMP1[15:0]	15:0	2C2C. [15:0] REG_ADC_CMP1. Fir coefficient.	
2C2Eh	**REG2C2E**	**15:0**	**Default : 0x4461**	**Access : R/W**
	FIR_DEC_CMP2[15:0]	15:0	2C2E. [15:0] REG_ADC_CMP2. Fir coefficient.	
2C30h	**REG2C30**	**15:0**	**Default : 0x7334**	**Access : R/W**
	FIR_DEC_GAIN[15:0]	15:0	2C30. [15:0] REG_ADC_GAIN. Fir coefficient.	
2C32h	**REG2C32**	**15:0**	**Default : 0x0000**	**Access : R/W**
	BT_I2S_TEST_MD[15:0]	15:0	2C32. REG_I2S_TEST_MD. [15] REG_SINGEN_ENA. Singen enable. 0 = disable. 1 = enable. [14] REG_SINGEN_SEL. Singen select. 0 = TX. 1 = RX. [13:12]. I2s trx data select. 00 = I2S_TX_LDATA. 01 = I2S_TX_RDATA. 10 = I2X_RX_LDATA. 11 = I2S_RX_RDATA. [11:8] reserved. [7:4] REG_SINGEN_GAIN.	

HAYDN2_0 Register (Bank = 2C)

Index	Mnemonic	Bit	Description	
			Singen gain select. [3:0] REG_SINGEN_FREQ. Singen frequency select.	
2C34h	**REG2C34**	**15:0**	**Default : 0x0000**	**Access : R/W**
	CLK_INVT_CTRL[15:0]	15:0	2C34. CLK_INVT_CTRL. [15:9] reserved. [8] REG_AU_HIGH_FREQ_GATE. Clock AU_HIGH_FREQ invert. 0 = normal. 1 = invert. [7] REG_AU_MAC_INVT. Clock AU_MAC invert. 0 = normal. 1 = invert. [6] REG_AU_DAC_INVT. Clock AU_DAC invert. 0 = normal. 1 = invert. [5] REG_MMP_INT_256FS_INVT. Clock MMP_INT_256FS invert. 0 = normal. 1 = invert. [4] REG_BT_INT_256FS_INVT. Clock BT_INT_256FS invert. 0 = normal. 1 = invert. [3] REG_EXT_INT_RX_BCK_INVT. EXT_INT_RX_BCK invert. 0 = normal. 1 = invert. [2] REG_EXT_INT_RX_BCK_INV_INVT. EXT_INT_RX_BCK invert. 0 = normal. 1 = invert. [1] REG_VT_INT_TRX_BCK_INVT. BT_INT_TRX_BCK invert. 0 = normal. 1 = invert. [0] REG_BT_INT_TRX_BCK_INV_INVT. BT_INT_TRX_BCK invert.	

HAYDN2_0 Register (Bank = 2C)

Index	Mnemonic	Bit	Description	
			0 = normal. 1 = invert.	
2C36h	**REG2C36**	**15:0**	**Default : 0x0000**	**Access : R/W**
	CLK_GATE_CTRL[15:0]	15:0	2C36. CLK_GATE_CTRL. [15:9] reserved. [8] REG_AU_HIGH_FREQ_GATE. Clock AU_HIGH_FREQ gate. 0 = normal. 1 = gate. [7] REG_AU_MAC_GATE. Clock AU_MAC gate. 0 = normal. 1 =gate. [6] REG_AU_DAC_GATE. Clock AU_DAC gate. 0 = normal. 1 = gate. [5] REG_MMP_INT_256FS_GATE. Clock MMP_INT_256FS gate. 0 = normal. 1 = gate. [4] REG_BT_INT_256FS_GATE. Clock BT_INT_256FS gate. 0 = normal. 1 =gate. [3] REG_EXT_INT_RX_BCK_GATE. EXT_INT_RX_BCKgate. 0 = normal. 1 = gate. [2] REG_EXT_INT_RX_BCK_INV_GATE. EXT_INT_RX_BCK gate. 0 = normal. 1 = gate. [1] REG_VT_INT_TRX_BCK_GATE. BT_INT_TRX_BCKgate. 0 = normal. 1 = gate. [0] REG_BT_INT_TRX_BCK_INV_GATE. BT_INT_TRX_BCK gate. 0 = normal.	

HAYDN2_0 Register (Bank = 2C)

Index	Mnemonic	Bit	Description	
			1 = gate.	
2C38h	**REG2C38**	**15:0**	**Default : 0x0012**	**Access : R/W**
	DIG_MIC_CLK_PHASE[15:0]	15:0	2C38. [15:8] reserved. [7] REG_DIG_MIC_PHASE_INV. Digital mic phase invert. 0 = normal. 1 = invert. [6:0] REG_DIG_MIC_PHASE_SEL. Digital mic phase select.	
2C3Ah	**REG2C3A**	**15:0**	**Default : 0x0000**	**Access : R/W**
	RESERVED_1D[15:0]	15:0	2C3A. [15:0] reserved.	
2C3Ch	**REG2C3C**	**15:0**	**Default : 0x0000**	**Access : R/W**
	TEST_CTRL[15:0]	15:0	2C3C. [15:3] reserved. [2:0] REG_TEST_MUX_SEL. TEST_MUX_OUT select STATUS_0~7.	
2C3Eh	**REG2C3E**	**15:0**	**Default : 0x0000**	**Access : R/W**
	AU_PAD_CTRL[15:0]	15:0	2C3E.	
2C40h	**REG2C40**	**15:0**	**Default : 0x3803**	**Access : R/W**
	MMP_DPGA_CTRL[15:0]	15:0	2C40. [15:14] reserved. [13:11] REG_MMP_DPGA_STEP. DPGA sample number select. 0 = 128. 1 = 64. 2 = 32. 3 = 16. … 7 = 1. [10:4] REG_MMP_DPGA_OFFSET. DPGA gain offset. (+63 ~ -64) * 0.25dB. [3] REG_MMP_DPGA_STATUS_CLR. DPGA status clear. 0 = normal. 1 = clear. [2] REG_MMP_DPGA_GAIN_UPDATE.	

HAYDN2_0 Register (Bank = 2C)

Index	Mnemonic	Bit	Description	
			DPGA gain update. 0 = normal. 1 = update. [1] REG_MMP_DPGA_FADING. DPGA fading. 0 = disable. 1 = enable. [0] REG_MMP_DPGA_ENABLE. DPGE enable. 0 = disable. 1 = enable.	
2C42h	**REG2C42**	**15:0**	**Default : 0x0240**	**Access : R/W**
	MMP_DPGA_GAIN_L[15:0]	15:0	2C42. [15:10] reserved. [9:0] REG_MMP_GAIN_L. Left channel gain select. (+144 ~ -448) *0.25dB.	
2C44h	**REG2C44**	**15:0**	**Default : 0x0240**	**Access : R/W**
	MMP_DPGA_GAIN_R[15:0]	15:0	2C44. [15:10] reserved. [9:0] REG_MMP_GAIN_R. Right channel gain select. (+144 ~ -448) *0.25dB.	
2C46h	**REG2C46**	**15:0**	**Default : 0x3823**	**Access : R/W**
	BT_ULK_DPGA_CTRL[15:0]	15:0	2C46. [15:14] reserved. [13:11] REG_BT_ULK_DPGA_STEP. DPGA sample number select. 0 = 128. 1 = 64. 2 = 32. 3 = 16. … 7 = 1. [10:4] REG_BT_ULK_OFFSET. DPGA gain offset. (+63 ~ -64) * 0.25dB. [3] REG_BT_DPGA_STATUS_CLR. DPGA status clear. 0 = normal.	

HAYDN2_0 Register (Bank = 2C)

Index	Mnemonic	Bit	Description	
			1 = clear. [2] REG_BT_ULK_GAIN_UPDATE. DPGA gain update. 0 = normal. 1 = update. [1] REG_BT_ULK_DPGA_FADING. DPGA fading. 0 = disable. 1 = enable. [0] REG_BT_ULK_DPGA_ENABLE. DPGE enable. 0 = disable. 1 = enable.	
2C48h	**REG2C48**	**15:0**	**Default : 0x0240**	**Access : R/W**
	BT_ULK_DPGA_GAIN[15:0]	15:0	2C48. [15:10] reserved. [9:0] REG_BT_ULK_GAIN. Gain select. (+144 ~ -448) *0.25dB.	
2C4Ah	**REG2C4A**	**15:0**	**Default : 0x3803**	**Access : R/W**
	BT_DLK_DPGA_CTRL[15:0]	15:0	2C4A. [15:14] reserved. [13:11] REG_BT_DLK_DPGA_STEP. DPGA sample number select. 0 = 128. 1 = 64. 2 = 32. 3 = 16. .. 7 = 1. [10:4] REG_BT_DLK_OFFSET. DPGA gain offset. (+63 ~ -64) * 0.25dB. [3] reserved. [2] REG_BT_DLK_GAIN_UPDATE. DPGA gain update. 0 = normal. 1 = update. [1] REG_BT_DLK_DPGA_FADING. DPGA fading.	

HAYDN2_0 Register (Bank = 2C)

Index	Mnemonic	Bit	Description	
			0 = disable. 1 = enable. [0] REG_BT_DLK_DPGA_ENABLE. DPGE enable. 0 = disable. 1 = enable.	
2C4Ch	**REG2C4C**	**15:0**	**Default : 0x0240**	**Access : R/W**
	BT_DLK_DPGA_GAIN[15:0]	15:0	2C4C. [15:10] reserved. [9:0] REG_BT_DLK_GAIN. Gain select. (+144 ~ -448) *0.25dB.	
2C4Eh	**REG2C4E**	**15:0**	**Default : 0x0000**	**Access : R/W**
	RESERVED_27[15:0]	15:0	2C4E. [15:0] reserved.	
2C50h	**REG2C50**	**15:0**	**Default : 0x0000**	**Access : RO**
	STS_CLOCK[15:0]	15:0	2C50. TEST_CLK. [15:9] 0. [8] CKM_AU_HIGH_FREQ. [7] CKM_AU_MAC. [6] CKM_AU_DAC. [5] CKM_MMP_INT_256FS. [4] CKM_BT_INT_256FS. [3] CKM_EXT_I2S_RX_BCK. [2] CKM_EXT_I2S_RX_BCK_INV. [1] CKM_BT_I2S_TRX_BCK. [0] CKM_BT_I2S_TRX_BCK_INV.	
2C52h	**REG2C52**	**15:0**	**Default : 0x0000**	**Access : RO**
	STS_SYSTEM[15:0]	15:0	2C52. [15:12] REG_STS_DAC_FIFO_STATE. Dac fifo state. [11] REG_STS_MAC_IS_OVL. Mac overflow flag. [10:3] 0. [2] BIST_FAIL_SCALMECH. Scalmech bist fail flag. [1] BIST_FAIL_DAC1FIFO. Dac1 fifo bist fail flag.	

HAYDN2_0 Register (Bank = 2C)

Index	Mnemonic	Bit	Description	
			[0] BIST_FAIL_DAC2FIFO. Dac2 fifo bist fail flag.	
2C54h	**REG2C54**	**15:0**	**Default : 0x0000**	**Access : RO**
	STS_EXT_I2S_STATUS1[15:0]	15:0	2C54. In DFT mode, [15:0] = I2S_RX_LADATA[15:0]. Otherwise, [15:12] 0. [11] I2S_RX_FS_PULSE. [10] CKG_I2S_RX_BCK. [9] CLK_I2S_RX_BCK_INV. [8] PAD_I2S_RX_WCK_M. [7] CRT_I2S_RX_BCK. [6] PAD_I2S_RX_BCK_M. [5] PAD_I2S_RX_WCK_S. [4] PAD_I2S_RX_SDI. [3] I2S_RX_VALID. [2] RX_FIFO_STATUS. [1:0] REG_I2S_RX_WIDTH. I2s bit width select. 00 = 32. 01 = 48. 10 = 64. 11 = 50.	
2C56h	**REG2C56**	**15:0**	**Default : 0x0000**	**Access : RO**
	STS_BT_I2S_STATUS1[15:0]	15:0	2C56. In DFT mode, [15:0] = I2S_RX_LDATA[15:0]. Otherwise, [15] CLK_I2S_RX_BCK. [14] PAD_I2S_RX_WCK_M. [13] PAD_I2S_RX_WCK_S. [12] PAD_I2S_RX_SDI. [11] I2S_RX_VALID. [10] RX_FIFO_STATUS. [9:8] REG_I2S_RX_WIDTH. I2s bit width select. 00 = 32. 01 = 48. 10 = 64. 11 = 50. [7] CKG_I2S_TX_BCK.	

HAYDN2_0 Register (Bank = 2C)

Index	Mnemonic	Bit	Description	
			[6] PAD_I2S_TX_WCK_M. [5] PAD_I2S_TX_WCK_S. [4] PAD_I2S_TX_SDO. [3] I2S_TX_VALID. [2] TX_FIFO_STATUS. [1:0] REG_I2S_TX_WIDTH.	
2C58h	**REG2C58**	**15:0**	**Default : 0x0000**	**Access : RO**
	STS_BT_I2S_STATUS2[15:0]	15:0	2C58. [15:0] I2S_TRX_DATA_MUX, refer to REG2C32.	
2C5Ah	**REG2C5A**	**15:0**	**Default : 0x0000**	**Access : RO**
	STS_MMP_SYNTH_NF_H[15:0]	15:0	2C5A. [15] REG_STS_MMP_FS_SYNTH_NS. [14:0] = REG_STS_MMP_FS_SYNTH_NF[31:17]. High bits of status of mmp fs synth nf.	
2C5Ch	**REG2C5C**	**15:0**	**Default : 0x0000**	**Access : RO**
	STS_MMP_SYNTH_NF_L[15:0]	15:0	2C5C. [15:0] = REG_STS_MMP_FS_SYNTH_NF[16:1]. Low bits of status of mmp fs synth nf.	
2C5Eh	**REG2C5E**	**15:0**	**Default : 0x0000**	**Access : RO**
	STS_MMP_SYNTH_FC[15:0]	15:0	2C5E. [15:0] = free run counter value of SYNTH_MMP_FS.	
2C60h	**REG2C60**	**15:0**	**Default : 0x0000**	**Access : RO**
	STS_BT_SYNTH_NF_H[15:0]	15:0	2C60. [15] REG_STS_BT_FS_SYNTH_NS. [14:0] = REG_STS_BT_FS_SYNTH_NF [31:17]. High bits of status of bt fs synth nf.	
2C62h	**REG2C62**	**15:0**	**Default : 0x0000**	**Access : RO**
	STS_BT_SYNTH_NF_L[15:0]	15:0	2C62. [15:0] = REG_STS_BT_FS_SYNTH_NF[16:1]. Low bits of status of bt fs synth nf.	
2C64h	**REG2C64**	**15:0**	**Default : 0x0000**	**Access : RO**
	STS_BT_SYNTH_FC[15:0]	15:0	2C64. [15:0] = free run counter value of SYNTH_BT_FS.	
2C66h	**REG2C66**	**15:0**	**Default : 0x0000**	**Access : RO**
	STS_DPGA_STATUS[15:0]	15:0	2C66. [15:10] = REG_STS_BT_DPGA_STATUS {DPGA_VLD_ERR_FIRST, DPGA_ERR_CH_NUM}. Indicates dpga status, including valid error and error channel	

HAYDN2_0 Register (Bank = 2C)

Index	Mnemonic	Bit	Description	
			number. [9:4] = REG_STS_MMP_DPGA_STATUS. [3] = REG_STS_BT_ULK_MUTE_DONE. Bt uplink muted flag. 0 = normal. 1 = muted. [2] REG_STS_BT_DLK_MUTE_DONE. Bt downlink muted flag. 0 = normal. 1 = muted. [1] REG_STS_MMP_MUTE_DONE_L. Mmp left channel muted flag. 0 = normal. 1 = muted. [0] REG_STS_MMP_MUTE_DONE_R. Mmp right channel muted flag. 0 = normal. 1 = muted.	
2C68h	**REG2C68**	**15:0**	**Default : 0x0000**	**Access : RO**
	STS_TEST_MUX[15:0]	15:0	2C68. STS_TEST_MUX, refer to REG2C3C.	
2C6Ah	**REG2C6A**	**15:0**	**Default : 0x0000**	**Access : RO**
	STS_RESERVED_35[15:0]	15:0	2C6A.	
2C6Ch	**REG2C6C**	**15:0**	**Default : 0x0000**	**Access : RO**
	STS_RESERVED_36[15:0]	15:0	2C6C.	
2C6Eh	**REG2C6E**	**15:0**	**Default : 0x0000**	**Access : RO**
	STS_RESERVED_37[15:0]	15:0	2C6E.	
2C70h	**REG2C70**	**15:0**	**Default : 0x0000**	**Access : RO**
	STS_RESERVED_38[15:0]	15:0	2C70.	
2C72h	**REG2C72**	**15:0**	**Default : 0x0000**	**Access : RO**
	STS_RESERVED_39[15:0]	15:0	2C72.	
2C74h	**REG2C74**	**15:0**	**Default : 0x0000**	**Access : RO**
	STS_RESERVED_3A[15:0]	15:0	2C74.	
2C76h	**REG2C76**	**15:0**	**Default : 0x0000**	**Access : RO**
	STS_RESERVED_3B[15:0]	15:0	2C76.	
2C78h	**REG2C78**	**15:0**	**Default : 0x0000**	**Access : RO**
	STS_RESERVED_3C[15:0]	15:0	2C78.	

HAYDN2_0 Register (Bank = 2C)

Index	Mnemonic	Bit	Description	
2C7Ah	**REG2C7A**	**15:0**	**Default : 0x0000**	**Access : R/W**
	CTRL_RESERVED_3D[15:0]	15:0	2C7A.	
2C7Ch	**REG2C7C**	**15:0**	**Default : 0x0000**	**Access : R/W**
	CTRL_RESERVED_3E[15:0]	15:0	2C7C.	
2C7Eh	**REG2C7E**	**15:0**	**Default : 0x0000**	**Access : R/W**
	CTRL_RESERVED_3F[15:0]	15:0	2C7E.	
2C80h	**REG2C80**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA1_CTRL_0[15:0]	15:0	0x80 DMA1_CTRL_0. [15] REG_WR_UNDERRUN_INT_EN. DMA writer underrun threshold interrupt enable. 0 = disable. 1 = enable. [14] REG_WR_OVERRUN_INT_EN. DMA writer overrun threshold interrupt enable. 0 = disable. 1 = enable. [13] REG_RD_UNDERRUN_INT_EN. DMA reader underrun threshold interrupt enable. 0 = disable. 1 = enable. [12] REG_RD_OVERRUN_INT_EN. DMA reader overrun threshold interrupt enable. 0 = disable. 1 = enable. [11] REG_WR_FULL_INT_EN. DMA writer full interrupt enable. 0 = disable. 1 = enable. [10] REG_RD_EMPTY_INT_EN. DMA reader empty interrupt enable. 0 = disable. 1 = enable. [9] REG_WR_FULL_FLAG_CLR / REG_WR_LOCALBUF_FULL_CLR. DMA writer full flag clear / DMA writer local buffer full flag clear. 0 = normal. 1 = clear. [8] REG_RD_EMPTY_FLAG_CLR / REG_RD_LOCALBUF_EMPTY_CLR.	

HAYDN2_0 Register (Bank = 2C)

Index	Mnemonic	Bit	Description	
			DMA reader full flag clear / DMA reader local buffer full flag clear. 0 = normal. 1 = clear. [6] REG_SEL_TES_BUS. DMA test bus selection. 0: Select flag. 1: Select test bus. [5] REG_RD_LR_SWAP_EN. DMA reader left/right channel swap enable. 0 = normal. 1 = swap. [4] REG_PRIORITY_KEEP_HIGH. DMA reader priority keep high. 0 = normal. 1 = keep high priority. [3] REG_RD_BYTE_SWAP_EN. DMA reader byte swap enable. 0 = normal. 1 = swap. [2] REG_RD_LEVEL_CNT_LIVE_MASK. DMA reader level counter live mask. 0 = level counter free run mode. 1 = level counter will stop while buffer is empty. [1] REG_ENABLE. DMA enable. 0 = disable. 1 = enable. [0] REG_SW_RST_DMA. DMA software reset. 0 = normal. 1 = reset.	
2C82h	**REG2C82**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA1_CTRL_1[15:0]	15:0	0x82 DMA1_CTRL_1. [15] REG_RD_ENABLE. DMA reader enable. 0 = disable. 1 = enable. [14] REG_RD_INIT. DMA reader initial. 0 = normal.	

HAYDN2_0 Register (Bank = 2C)

Index	Mnemonic	Bit	Description	
			1 = initial. [13] REG_RD_TRIG. DMA reader trigger. 0 = normal. 1 = trigger. [12] REG_RD_LEVEL_CNT_MASK. DMA reader level counter mask. 0 = normal. 1 = mask. [11:0] REG_RD_BASE_ADDR[11:0]. DMA reader base address [11:0].	
2C84h	**REG2C84**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA1_CTRL_2[15:0]	15:0	0x84 DMA1_CTRL_2. [15] Reserved. [14:0] REG_RD_BASE_ADDR[14:0]. DMA reader base address [26:12].	
2C86h	**REG2C86**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA1_CTRL_3[15:0]	15:0	0x86 DMA1_CTRL_3. [15:0] REG_RD_BUFF_SIZE. DMA reader buffer size.	
2C88h	**REG2C88**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA1_CTRL_4[15:0]	15:0	0x88 DMA1_CTRL_4. [15:0] REG_RD_SIZE. DMA read size.	
2C8Ah	**REG2C8A**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA1_CTRL_5[15:0]	15:0	0x8A DMA1_CTRL_5. [15:0] REG_RD_OVERRUN_TH. DMA reader overrun threshold.	
2C8Ch	**REG2C8C**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA1_CTRL_6[15:0]	15:0	0x8C DMA1_CTRL_6. [15:0] REG_RD_UNDERRUN_TH. DMA reader underrun threshold.	
2C8Eh	**REG2C8E**	**15:0**	**Default : 0x0000**	**Access : RO**
	DMA1_CTRL_7[15:0]	15:0	0x8E DMA1_CTRL_7. [15:0] REG_RD_LEVEL_CNT. DMA reader level counter.	
2C90h	**REG2C90**	**15:0**	**Default : 0x0000**	**Access : RO**
	DMA1_CTRL_8[15:0]	15:0	0x90 DMA1_CTRL_8.	

HAYDN2_0 Register (Bank = 2C)

Index	Mnemonic	Bit	Description	
			[7] REG_RD_LOCALBUF_EMPTY. DMA reader local buffer empty flag. [6] REG_WR_LOCALBUF_FULL. DMA writer local buffer full flag. [5] REG_WR_FULL_FLAG. DMA writer full flag. [4] REG_RD_EMPTY_FLAG. DMA reader empty flag. [3] REG_RD_OVERRUN_FLAG. DMA reader overrun falg. [2] REG_RD_UNDERRUN_FLAG. DMA reader underrun flag. [1] REG_WR_OVERRUN_FLAG. DMA writer overrun flag. [0] REG_WR_UNDERRUN_FLAG. DMA writer underrun flag.	
2C92h	**REG2C92**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA1_CTRL_9[15:0]	15:0	0x92 DMA1_CTRL_9. [15] REG_WR_ENABLE. DMA writer enable. 0 = disable. 1 = enable. [14] REG_WR_INIT. DMA writer initial. 0 = normal. 1 = initial. [13] REG_WR_TRIG. DMA writer trigger. 0 = normal. 1 = trigger. [12] REG_WR_LEVEL_CNT_MASK. DMA writer level counter mask. 0 = normal. 1 = mask. [11:0] REG_WR_BASE_ADDR[11:0]. DMA writer base address [11:0].	
2C94h	**REG2C94**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA1_CTRL_10[15:0]	15:0	0x94 DMA1_CTRL_10. [15] Reserved. [14:0] REG_WR_BASE_ADDR[14:0].	

HAYDN2_0 Register (Bank = 2C)

Index	Mnemonic	Bit	Description	
			DMA writer base address [26:12].	
2C96h	**REG2C96**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA1_CTRL_11[15:0]	15:0	0x96 DMA1_CTRL_11. [15:0] REG_WR_BUFF_SIZE. DMA writer buffer size.	
2C98h	**REG2C98**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA1_CTRL_12[15:0]	15:0	0x98 DMA1_CTRL_12. [15:0] REG_WR_SIZE. DMA write size.	
2C9Ah	**REG2C9A**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA1_CTRL_13[15:0]	15:0	0x9A DMA1_CTRL_13. [15:0] REG_WR_OVERRUN_TH. DMA writer overrun threshold.	
2C9Ch	**REG2C9C**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA1_CTRL_14[15:0]	15:0	0x9C DMA1_CTRL_14. [15:0] REG_WR_UNDERRUN_TH. DMA writer underrun threshold.	
2C9Eh	**REG2C9E**	**15:0**	**Default : 0x0000**	**Access : RO**
	DMA1_CTRL_15[15:0]	15:0	0x9E DMA1_CTRL_15. [15:0] REG_WR_LEVEL_CNT. DMA writer level counter.	
2CE0h	**REG2CE0**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA_TEST_CTRL0[15:0]	15:0	0xE0 DMA_TEST_CTRL0. [0] DMA_TEST_WR_EN. DMA test wrtier enable. [1] DMA_TEST_WR. DMA test writer. [3:2] DMA_TEST_WR_SEL. DMA test writer selection. [4] DMA_TEST_RD_EN. DMA test reader enable. [5] DMA_TEST_RD. DMA test reader. [7:6] DMA_TEST_RD_SEL. DMA test reader selection.	
2CE2h	**REG2CE2**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA_TEST_CTRL1[15:0]	15:0	0xE2 DMA_TEST_CTRL1. [15:0] DMA_WR_DATA_L_MUX.	

HAYDN2_0 Register (Bank = 2C)

Index	Mnemonic	Bit	Description	
			DMA writer data left echannel value.	
2CE4h	**REG2CE4**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA_TEST_CTRL2[15:0]	15:0	0xE4 DMA_TEST_CTRL2. [15:0] DMA_WR_DATA_R_MUX. DMA writer data right echannel value.	
2CE6h	**REG2CE6**	**15:0**	**Default : 0x0000**	**Access : RO**
	DMA_TEST_CTRL3[15:0]	15:0	0xE6 DMA_TEST_CTRL3. [15:0] DMA_RD_DATA_L. DMA read DATA left channel.	
2CE8h	**REG2CE8**	**15:0**	**Default : 0x0000**	**Access : RO**
	DMA_TEST_CTRL4[15:0]	15:0	0xE8 DMA_TEST_CTRL4. [15:0] DMA_RD_DATA_R. DMA read DATA right channel.	
2CEAh	**REG2CEA**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA_TEST_CTRL5[15:0]	15:0	0xEA DMA_TEST_CTRL5. DMA1 sine generator setting. [15] REG_SINE_GEN_EN. Sine generator enable. [14] REG_SINE_GEN_RD_WR. Sine generator select reader or writer. 0 = reader. 1 = writer. [11] REG_DMA_TEST_SEL_H. DMA test bus select high word. 0 = low word. 1 = high word. [10:8] REG_DMA_TEST_SEL. DMA test bus selection. [3:0] REG_SINE_GEN_FREQ. Sine generator frequency selection. [7:4] REG_SINE_GEN_GAIN. Sine generator gain selection.	
2CECh	**REG2CEC**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DMA_TEST_CTRL6[15:0]	15:0	0xEC DMA_TEST_CTRL6. DMA2 sine generator setting. [15] REG_SINE_GEN_EN. Sine generator enable. [14] REG_SINE_GEN_RD_WR. Sine generator select reader or writer.	

HAYDN2_0 Register (Bank = 2C)

Index	Mnemonic	Bit	Description
			0 = reader. 1 = writer. [11] REG_DMA_TEST_SEL_H. DMA test bus select high word. 0 = low word. 1 = high word. [10:8] REG_DMA_TEST_SEL. DMA test bus selection. [3:0] REG_SINE_GEN_FREQ. Sine generator frequency selection. [7:4] REG_SINE_GEN_GAIN. Sine generator gain selection.
2CEEh	**REG2CEE**	**15:0**	**Default : 0x0000** **Access : R/W**
	DMA_TEST_CTRL7[15:0]	15:0	0xEE DMA_TEST_CTRL7. DMA3 sine generator setting. [15] REG_SINE_GEN_EN. Sine generator enable. [14] REG_SINE_GEN_RD_WR. Sine generator select reader or writer. 0 = reader. 1 = writer. [11] REG_DMA_TEST_SEL_H. DMA test bus select high word. 0 = low word. 1 = high word. [10:8] REG_DMA_TEST_SEL. DMA test bus selection. [3:0] REG_SINE_GEN_FREQ. Sine generator frequency selection. [7:4] REG_SINE_GEN_GAIN. Sine generator gain selection.

HAYDN2_1 Register (Bank = 2D)

HAYDN2_1 Register (Bank = 2D)				
Index	**Mnemonic**	**Bit**	**Description**	
2D00h	**REG2D00**	**15:0**	**Default : 0x0000**	**Access : R/W**
	ANALOG_CTRL00[15:0]	15:0	2D00. [14] INT_AU_DET_TEST_MODE. Interrupt audio detect test mode. [13] INT_AU_DET_TEST_VALUE. Interrupt audio detect test value. [12] REG_RSTZ_AU_DET. Rest audio detect.	
2D02h	**REG2D02**	**15:0**	**Default : 0x0000**	**Access : R/W**
	ANALOG_CTRL01[15:0]	15:0	2D02. [15] BG_LP_MODE_12. Bandgap Low power mode, 0: normal, 1: low power. [14] EN_AUDIO_IBIAS_12. Enable audio atop bias current, 0: disable, 1: enable. [13:12] IBSEL_AUDIO_12. "Select audio atop bias current, 00:5u,01:2.5u,10:10u,11:7.5u". [11] EN_BG_12. Enable bandgap, 0: disable, 1:enable. [10:8] TST_AUDIO_12. "Test audio current and voltage, use PAD_EARDET: 000: HiZ, 001: audio atop current. 010: DAC current, 011: driver IB. 100: Driver CTR_IPRTN, 101: driver CTR_IPRTP. 110: AVDD12, 111: AVSS". [7] EN_SPKDET_12. Enable speaker detect, 0:disable, 1:enable. [6:2] AUDIO_PORT_12. EN_VCM14, 0:disable, 1: enable driver VCM bufer. [1] DRV_REF_SEL_12 select driver reference, 0: avdd divided, 1: from bandgap. [0] reserved.	
2D04h	**REG2D04**	**15:0**	**Default : 0x0000**	**Access : R/W**
	ANALOG_CTRL02[15:0]	15:0	2D04. RIU_ANALOG_CTRL02[15] BG_LP_MODE_12. RIU_ANALOG_CTRL02[14] EN_AUDIO_IBIAS_12. RIU_ANALOG_CTRL02[13:12] IBSEL_AUDIO_12. RIU_ANALOG_CTRL02[11] EN_BG_12. RIU_ANALOG_CTRL02[10:8] TST_AUDIO_12.	

HAYDN2_1 Register (Bank = 2D)

Index	Mnemonic	Bit	Description	
			RIU_ANALOG_CTRL02[7] EN_SPKDET_12. RIU_ANALOG_CTRL02[6:2] AUDIO_PORT_12. RIU_ANALOG_CTRL02[1] DRV_REF_SEL_12. RIU_ANALOG_CTRL02[0] reserved.	
2D06h	**REG2D06**	**15:0**	**Default : 0x0004**	**Access : R/W**
	ANALOG_CTRL03[15:0]	15:0	2D06. [15:14] SEL_CK_12. "Selected audio input clock: 00: From crystal, 10: From crystal. 01: From digital clock, 11: From digital clock ". [13] POS_RL_12. "Audio DAC data latching mode select. 0: Negative edge select. 1: Positive edge select". [12] LDO12_VC_12. DAC 1.2V LDO voltage select 0:1.2V, 1:1.3V. [11] EN_DAC_L_12. Enable L channel DAC, 0:disable, 1:enable. [10] EN_DAC_R_12. Enable R channel DAC, 0:disable, 1:enable. [9] reserved. [8:6] GAIN_EAR_12. "Earphone gain control: 000: Gain=0.6; 001: Gain=0.4; 010: Gain=1.0; 011: Gain=1.2; 100: Gain=1.6, 101: Gain=2.0; 110: Gain=2.4". [5] EN_EAR_12. Enable earphone, 0: disable, 1:enable. [4] EN_STG2LP_12. "Earphone driver lower power stage enable, 0: Disable, 1:enable". [3] EN_STG2AB_12. "Earphone driver class AB drive stage enable, 0: Disable, 1:enable". [2] EN_OPLP_12.	

HAYDN2_1 Register (Bank = 2D)

Index	Mnemonic	Bit	Description	
			OPLP amp enable,0:disable, 1:enable. [1] EN_LT_12. Earphone driver left channel enable, 0: disable, 1:enable. [0] EN_RT_12. Earphone driver right channel enable, 0: disable, 1:enable.	
2D08h	**REG2D08**	**15:0**	**Default : 0x0000**	**Access : R/W**
	ANALOG_CTRL04[15:0]	15:0	2D08. [15:13] MX_ENL_12. "Earphone left channel MUX control: 000: DAC left channel output; 001: VMID; 010: AVSS_DRV; 011: DAC right channel output; 100: Linein1 differential input. 101: Linein2 differential input. 110: Linein1 P and VMID as stereo single end input. 111: Linein2 P and VMID as stereo single end input". [12:10] MX_ENR_12. "Earphone right channel MUX control: 000: DAC right channel output; 001: VMID; 010: AVSS_DRV; 011: DAC left channel output; 100: Linein1 differential input. 101: Linein2 differential input. 110: Linein1 N and VMID as stereo single end input. 111: Linein2 N and VMID as stereo single end input". [9] EAR_MUTE_12. Mute the earphone, 0: not mute, 1: mute. [8:7] ISEL_DRV_12. "Drive op bias current setting: 00: 5u, 01: 2.5u, 10: 10u, 11: 7.5u". [6:5] ISEL_PRTN_EAR_12. "OCP bias current select (NMOS). 00: 5u, 01: 2.5u, 10: 10u, 11: 7.5u". [4:3] ISEL_PRTP_EAR_12.	

HAYDN2_1 Register (Bank = 2D)

Index	Mnemonic	Bit	Description	
			"OCP bias current select (PMOS). 00: 5u, 01: 2.5u, 10: 10u, 11: 7.5u". [2:1] TCSEL_12. "Control the oplp output current to control the. Vcm set up time when audio power on. 00: 0.5s, 01: 1s, 10: 0.25s, 11: 0.125s". [0] EAR_POPRES_12. "Earphone depop res control: X0: AC mode(r=500); X1: DC mode.".	
2D0Ah	**REG2D0A**	**15:0**	**Default : 0x0000**	**Access : R/W**
	ANALOG_CTRL05[15:0]	15:0	2D0A reserved.	
2D14h	**REG2D14**	**15:0**	**Default : 0x0000**	**Access : R/W**
	ANALOG_CTRL10[15:0]	15:0	2D14. [15] SPK_PLGUIN_12. Plugin test.	
2D16h	**REG2D16**	**15:0**	**Default : 0x0000**	**Access : R/W**
	ANALOG_CTRL11[15:0]	15:0	2D16.	
2D18h	**REG2D18**	**15:0**	**Default : 0x0000**	**Access : RO**
	ANALOG_CTRL12[15:0]	15:0	2D18. [12] = REG_SPK_PLUGIN. [11] = REG_SPK_UNPLUG. [5] = INT_SPK_UNPLUG. [4] = INT_SPK_PLUGIN.	
2D1Ah	**REG2D1A**	**15:0**	**Default : 0x0000**	**Access : RO**
	ANALOG_CTRL13[15:0]	15:0	2D1A. [14] = INT_AUDIO_ATOP. [12] = OCP_DRV_12. [11] = DFT_ANALOG_INPUT. [5] = REG_SPK_STATE.	
2D1Ch	**REG2D1C**	**15:0**	**Default : 0x0000**	**Access : RO**
	ANALOG_CTRL14[15:0]	15:0	2D1C. Reserved.	

HAYDN2_1 Register (Bank = 2D)

Index	Mnemonic	Bit	Description	
2D1Eh	**REG2D1E**	**15:0**	**Default : 0x0000**	**Access : RO**
	ANALOG_CTRL15[15:0]	15:0	2D1E. [4] SPK_PLUGIN_12. [1] CRT_AU_DAC.	

HVSP Register (Bank = 2E)

HVSP Register (Bank = 2E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (5C04h)	**REG5C04**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	BYPASS_VSC	1	Bypass Vertical scaling.	
	SW_RST	0	Software reset, set "1" to reset.	
02h (5C08h)	**REG5C08**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSD_DST_HSIZE[7:0]	7:0	HSD_DST_HSIZE is HSD output pixel number -1.	
02h (5C09h)	**REG5C09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	HSD_DST_HSIZE[11:8]	3:0	See description of '5C08h'.	
03h (5C0Ch)	**REG5C0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSC_DST_HSIZE[7:0]	7:0	HSC_DST_HSIZE is horizontal output pixel number -1.	
03h (5C0Dh)	**REG5C0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	HSC_DST_HSIZE[11:8]	3:0	See description of '5C0Ch'.	
04h (5C10h)	**REG5C10**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSC_DST_VSIZE[7:0]	7:0	Vsc_dst_hsize is vertical output line number -1.	
04h (5C11h)	**REG5C11**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	VSC_DST_VSIZE[11:8]	3:0	See description of '5C10h'.	
05h (5C14h)	**REG5C14**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_INI_FAC[7:0]	7:0	Horizontal initial factor (s.20).	
05h (5C15h)	**REG5C15**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_INI_FAC[15:8]	7:0	See description of '5C14h'.	
06h (5C18h)	**REG5C18**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	H_INI_FAC[20:16]	4:0	See description of '5C14h'.	
07h (5C1Ch)	**REG5C1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_SCL_FAC[7:0]	7:0	Horizontal scaling factor (4.20).	
07h (5C1Dh)	**REG5C1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_SCL_FAC[15:8]	7:0	See description of '5C1Ch'.	
08h	**REG5C20**	**7:0**	**Default : 0x10**	**Access : R/W**

HVSP Register (Bank = 2E)

Index (Absolute)	Mnemonic	Bit	Description	
(5C20h)	H_SCL_FAC[23:16]	7:0	See description of '5C1Ch'.	
09h (5C24h)	**REG5C24**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_INI_FAC[7:0]	7:0	Vertical initial factor (s.20).	
09h (5C25h)	**REG5C25**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_INI_FAC[15:8]	7:0	See description of '5C24h'.	
0Ah (5C28h)	**REG5C28**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	V_INI_FAC[20:16]	4:0	See description of '5C24h'.	
0Bh (5C2Ch)	**REG5C2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_SCL_FAC[7:0]	7:0	Vertical scaling factor (4.20).	
0Bh (5C2Dh)	**REG5C2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_SCL_FAC[15:8]	7:0	See description of '5C2Ch'.	
0Ch (5C30h)	**REG5C30**	**7:0**	**Default : 0x10**	**Access : R/W**
	V_SCL_FAC[23:16]	7:0	See description of '5C2Ch'.	
0Ch (5C31h)	**REG5C31**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSC_MODE	7	Vsc mode 0: filt mode 1: CB mode.	
	VSP_DITH_EN	6	Enable vsc dith.	
	-	5:0	Reserved.	
0Dh (5C34h)	**REG5C34**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	RAM_W_FAST_MODE	1	Coefficient SRAM write fast mode. (Auto increase address after write reg_ram_wdat_h).	
	RAM_RW_EN	0	Coefficient SRAM read/write enable.	
0Eh (5C38h)	**REG5C38**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA_L[7:0]	7:0	Coefficient SRAM write data (low).	
0Eh (5C39h)	**REG5C39**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	RAM_WDATA_L[10:8]	2:0	See description of '5C38h'.	
0Fh (5C3Ch)	**REG5C3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA_H[7:0]	7:0	Coefficient SRAM write data (high).	
0Fh (5C3Dh)	**REG5C3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	RAM_WDATA_H[10:8]	2:0	See description of '5C3Ch'.	

HVSP Register (Bank = 2E)

Index (Absolute)	Mnemonic	Bit	Description	
10h (5C40h)	**REG5C40**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_ADDR[7:0]	7:0	Coefficient SRAM read/write address.	
10h (5C41h)	**REG5C41**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_W_PULSE	7	Coefficient SRAM write pulse.	
	-	6:0	Reserved.	
11h (5C44h)	**REG5C44**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA_L[7:0]	7:0	Coefficient SRAM read data (low).	
11h (5C45h)	**REG5C45**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	RAM_RDATA_L[10:8]	2:0	See description of '5C44h'.	
12h (5C48h)	**REG5C48**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA_H[7:0]	7:0	Coefficient SRAM read data (high).	
12h (5C49h)	**REG5C49**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	RAM_RDATA_H[10:8]	2:0	See description of '5C48h'.	
13h (5C4Ch)	**REG5C4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	V_CORING_Y_TH[5:0]	5:0	VSC Luma coring threshold.	
13h (5C4Dh)	**REG5C4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	H_CORING_Y_TH[5:0]	5:0	HSC Luma coring threshold.	
14h (5C50h)	**REG5C50**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSD_HFAC_INI[7:0]	7:0	Horizontal scaling down (CB) initial factor.	
14h (5C51h)	**REG5C51**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSD_HFAC_INI[15:8]	7:0	See description of '5C50h'.	
15h (5C54h)	**REG5C54**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	HSD_HFAC_INI[19:16]	3:0	See description of '5C50h'.	
16h (5C58h)	**REG5C58**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSD_HFACTOR[7:0]	7:0	Horizontal scaling down (CB) factor.	
16h (5C59h)	**REG5C59**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSD_HFACTOR[15:8]	7:0	See description of '5C58h'.	
17h	**REG5C5C**	**7:0**	**Default : 0x00**	**Access : R/W**

HVSP Register (Bank = 2E)

Index (Absolute)	Mnemonic	Bit	Description	
(5C5Ch)	-	7:4	Reserved.	
	HSD_HFACTOR[19:16]	3:0	See description of '5C58h'.	
17h (5C5Dh)	**REG5C5D**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSD_EN	7	HSD filter enable 0: disable 1: enable.	
	-	6:0	Reserved.	
18h (5C60h)	**REG5C60**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	H_FORCE_Y_BI	6	Force HSC luma bi-linear.	
	H_CHROMA_LP	5	HSC chroma low pass filter 0: disable 1: enable.	
	HFILT_MODE	4	HSC filter mode. 0: 2-tap. 1: 4-tap.	
	-	3:0	Reserved.	
19h (5C64h)	**REG5C64**	**7:0**	**Default : 0x03**	**Access : R/W**
	AVG_SHIFT_VFAC	7	Enable auto shift vertical scaling factor with vertical average.	
	-	6:5	Reserved.	
	V_COEF_SRAM_HI	4	VSC Use high 128 coefficient sram when reg_coef_mode=1.	
	H_COEF_SRAM_HI	3	HSC Use high 128 coefficient sram when reg_coef_mode=1.	
	COEF_MODE	2	Coefficient SRAM mode: 0: Use all 256 sram coefficients. 1: Use 128 sram coefficients.	
	V_COEF_LINEAR	1	VSC use linear coefficient (note: when enable linear coefficient reg_vfilt_mode should be 0).	
	H_COEF_LINEAR	0	HSC use linear coefficient (note: when enable linear coefficient reg_hfilt_mode should be 0).	
19h (5C65h)	**REG5C65**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	HSD_CR_LOAD_INI	3	HSD cr_load_ini: 0: Initial load cb. 1: Initial load cr.	
	HSD_422TO444_MODE[1:0]	2:1	HSD 422to444_mode mode: 0x: Duplicate. 3: Center. 2: YC co-sited.	
	-	0	Reserved.	

HVSP Register (Bank = 2E)

Index (Absolute)	Mnemonic	Bit	Description	
1Ah (5C68h)	**REG5C68**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	V_FORCE_Y_BI	5	Force VSC luma bi-linear.	
	V_CHROMA_LP	4	VSC chroma low-pass filter 0: disable 1: enable.	
	VFILT_MODE[1:0]	3:2	VSC filter mode: 0: 2-tap. 1: 4-tap. 2: 8-tap. 3: Reserved.	
	LINE_AVG[1:0]	1:0	VSC line average mode. 0: No average. 1: 2 lines average. 2: 4 lines average. 3: 8 lines average.	
1Ah (5C69h)	**REG5C69**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	VSC_INI_AVG[3:0]	3:0	VSC initial shift line (-7 ~ +7).	
1Bh (5C6Ch)	**REG5C6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	HSC_COEF_FORCE_Y	1	Force HSC Ccoef equal to Ycoef for RGB mode.	
	VSC_COEF_FORCE_Y	0	Force VSC Ccoef equal to Ycoef for RGB mode.	
1Ch (5C70h)	**REG5C70**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_INI_FAC_ODD[7:0]	7:0	Vertical initial factor (s.20).	
1Ch (5C71h)	**REG5C71**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_INI_FAC_ODD[15:8]	7:0	See description of '5C70h'.	
1Dh (5C74h)	**REG5C74**	**7:0**	**Default : 0x18**	**Access : R/W**
	-	7:5	Reserved.	
	V_INI_FAC_ODD[20:16]	4:0	See description of '5C70h'.	
1Dh (5C75h)	**REG5C75**	**7:0**	**Default : 0x00**	**Access : R/W**
	INTLAC_MODE	7	Enable interlace mode.	
	INTLAC_FLD_INV	6	When interlace mode inverse external field signal.	
	INTLAC_LOCAL	5	When interlace mode use local field signal.	
	-	4:0	Reserved.	
1Fh	**REG5C7C**	**7:0**	**Default : 0x41**	**Access : RO, R/W**

HVSP Register (Bank = 2E)

Index (Absolute)	Mnemonic	Bit	Description	
(5C7Ch)	CLR_AFTER_LAST_OUT	7	Enable clear all blocks after last pixel output to next IP.	
	MASK_BI_EXTRA	6	Enable masking duplicated write last line to LB at 2-tap filter mode.	
	-	5:4	Reserved.	
	BIST_FAIL[2:0]	3:1	BIST fail indicator.	
	SRAM_CG_EN	0	SRAM CG enable.	
1Fh (5C7Dh)	**REG5C7D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SC_DONE[3:0]	3:0	SC done status (hsd_done,vSC_DONE,hSC_DONE,pp_done).	
30h (5CC0h)	**REG5CC0**	**7:0**	**Default : 0x20**	**Access : R/W**
	H_TOTAL[7:0]	7:0	Patgen_H_TOTAL.	
30h (5CC1h)	**REG5CC1**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:4	Reserved.	
	H_TOTAL[11:8]	3:0	See description of '5CC0h'.	
31h (5CC4h)	**REG5CC4**	**7:0**	**Default : 0x58**	**Access : R/W**
	V_TOTAL[7:0]	7:0	Patgen_V_TOTAL.	
31h (5CC5h)	**REG5CC5**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	V_TOTAL[11:8]	3:0	See description of '5CC4h'.	
32h (5CC8h)	**REG5CC8**	**7:0**	**Default : 0x30**	**Access : R/W**
	H_BLOCK[7:0]	7:0	Patgen_H_BLOCK.	
32h (5CC9h)	**REG5CC9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	H_BLOCK[9:8]	1:0	See description of '5CC8h'.	
33h (5CCCh)	**REG5CCC**	**7:0**	**Default : 0x20**	**Access : R/W**
	V_BLOCK[7:0]	7:0	Patgen_V_BLOCK.	
33h (5CCDh)	**REG5CCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	V_BLOCK[9:8]	1:0	See description of '5CCCh'.	
34h (5CD0h)	**REG5CD0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PAT2SRC_RDY_SEL[1:0]	5:4	PAT2SRC_RDY_SEL.	
	RANDOM_SEL[1:0]	3:2	RANDOM_SEL.	

HVSP Register (Bank = 2E)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	PAT_DATA_SEL	1	PAT_DATA_SEL.
	PAT_TIMING_SEL	0	PAT_TIMING_SEL.

VPS Register (Bank =2E)

VPS Register (Bank = 2E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
40h (5D00h)	**REG5D00**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_Y_LPF_COEF[2:0]	6:4	Main window horizontal Y low pass filter coefficient.	
	-	3:1	Reserved.	
	MAIN_POST_PEAKING_EN	0	Main window 2D peaking enable.	
40h (5D01h)	**REG5D01**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_BAND4_PEAKING_EN	3	Main window band4 peaking enable.	
	MAIN_BAND3_PEAKING_EN	2	Main window band3 peaking enable.	
	MAIN_BAND2_PEAKING_EN	1	Main window band2 peaking enable.	
	MAIN_BAND1_PEAKING_EN	0	Main window band1 peaking enable.	
43h (5D0Ch)	**REG5D0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_CORING_THRD_2[3:0]	7:4	Main window coring threshold 2.	
	MAIN_CORING_THRD_1[3:0]	3:0	Main window coring threshold 1.	
43h (5D0Dh)	**REG5D0D**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_OSD_SHARPNESS_CTRL[5:0]	5:0	Main window user sharpness adjust.	
48h (5D20h)	**REG5D20**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_BAND1_COEF[5:0]	5:0	Main window band1 coefficient.	
48h (5D21h)	**REG5D21**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_BAND2_COEF[5:0]	5:0	Main window band2 coefficient.	
49h (5D24h)	**REG5D24**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_BAND3_COEF[5:0]	5:0	Main window band3 coefficient.	
49h (5D25h)	**REG5D25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_BAND4_COEF[5:0]	5:0	Main window band4 coefficient.	

IPM Register (Bank = 2F)

IPM Register (Bank = 2F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (5E00h)	**REG5E00**	**7:0**	**Default : 0x00**	**Access : R/W**
	INTERLACE_OUT	7	Interlace output.	
	-	6:2	Reserved.	
	EN_IPM	1	Enable IPM.	
	IPM_TRIG_SEL	0	IPM trigger method selection.	
00h (5E01h)	**REG5E01**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_2FB_EN	7	IPM 2 frame buffer mode.	
	-	6:3	Reserved.	
	422_YC_ORDER	2	YUV422 source data arrangement order: MSB<->LSB. 0: {Y1,Cr,Y0,Cb}. 1: {Cr,Y1,Cb,Y0}.	
	-	1	Reserved.	
	444_EN	0	YUV 444 data format.	
01h (5E04h)	**REG5E04**	**7:0**	**Default : 0x00**	**Access : R/W**
	PITCH[7:0]	7:0	Source frame buffer PITCH.	
01h (5E05h)	**REG5E05**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	PITCH[10:8]	2:0	See description of '5E04h'.	
04h (5E10h)	**REG5E10**	**7:0**	**Default : 0xCF**	**Access : R/W**
	PIC_WIDTH_M1[7:0]	7:0	Source image width minus one.	
04h (5E11h)	**REG5E11**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	PIC_WIDTH_M1[11:8]	3:0	See description of '5E10h'.	
05h (5E14h)	**REG5E14**	**7:0**	**Default : 0xDF**	**Access : R/W**
	PIC_HEIGHT_M1[7:0]	7:0	Source image height minus one.	
05h (5E15h)	**REG5E15**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	PIC_HEIGHT_M1[11:8]	3:0	See description of '5E14h'.	
06h (5E18h)	**REG5E18**	**7:0**	**Default : 0x00**	**Access : R/W**
	STARTX[7:0]	7:0	Horizontal start offset. (Unit: pixel).	

IPM Register (Bank = 2F)

Index (Absolute)	Mnemonic	Bit	Description	
06h (5E19h)	**REG5E19**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	STARTX[11:8]	3:0	See description of '5E18h'.	
07h (5E1Ch)	**REG5E1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	STARTY[7:0]	7:0	Vertical start offset. (unit: line).	
07h (5E1Dh)	**REG5E1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	STARTY[11:8]	3:0	See description of '5E1Ch'.	
08h (5E20h)	**REG5E20**	**7:0**	**Default : 0x00**	**Access : R/W**
	BASE_ADDR0[7:0]	7:0	Frame buffer base address.	
08h (5E21h)	**REG5E21**	**7:0**	**Default : 0x00**	**Access : R/W**
	BASE_ADDR0[15:8]	7:0	See description of '5E20h'.	
09h (5E24h)	**REG5E24**	**7:0**	**Default : 0x00**	**Access : R/W**
	BASE_ADDR0[23:16]	7:0	See description of '5E20h'.	
09h (5E25h)	**REG5E25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	BASE_ADDR0[25:24]	1:0	See description of '5E20h'.	
0Ah (5E28h)	**REG5E28**	**7:0**	**Default : 0x00**	**Access : R/W**
	BASE_ADDR1[7:0]	7:0	Frame buffer base address.	
0Ah (5E29h)	**REG5E29**	**7:0**	**Default : 0x00**	**Access : R/W**
	BASE_ADDR1[15:8]	7:0	See description of '5E28h'.	
0Bh (5E2Ch)	**REG5E2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	BASE_ADDR1[23:16]	7:0	See description of '5E28h'.	
0Bh (5E2Dh)	**REG5E2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	BASE_ADDR1[25:24]	1:0	See description of '5E28h'.	
0Ch (5E30h)	**REG5E30**	**7:0**	**Default : 0x00**	**Access : R/W**
	FIFO_RTHR_HP[3:0]	7:4	Trigger high priority read request threshold.	
	FIFO_RTHR[3:0]	3:0	Trigger read request threshold.	
0Ch (5E31h)	**REG5E31**	**7:0**	**Default : 0x07**	**Access : R/W**
	-	7:4	Reserved.	
	FIFO_RLEN[3:0]	3:0	Max read request length.	

IPM Register (Bank = 2F)

Index (Absolute)	Mnemonic	Bit	Description	
0Fh (5E3Ch)	**REG5E3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	JMD_BUFFER[1:0]	2:1	JMD temp buffer size. 0: 32 lines. 1: 64lines. 2: 8 lines. 3: 16 lines.	
	EN_SYNC_JMD	0	Enable synchronization mechanism with JMD.	
10h (5E40h)	**REG5E40**	**7:0**	**Default : 0x06**	**Access : R/W**
	-	7:4	Reserved.	
	TPAT_INIT_COLOR[2:0]	3:1	Select initial color.	
	EN_TESTPAT	0	Enable test pattern.	
11h (5E44h)	**REG5E44**	**7:0**	**Default : 0x76**	**Access : R/W**
	-	7	Reserved.	
	TPAT_BLKY[2:0]	6:4	Select block height.	
	-	3	Reserved.	
	TPAT_BLKX[2:0]	2:0	Select block width.	
11h (5E45h)	**REG5E45**	**7:0**	**Default : 0x11**	**Access : R/W**
	-	7	Reserved.	
	TPAT_DELTA_V[2:0]	6:4	Select block color changing by height.	
	-	3	Reserved.	
	TPAT_DELTA_H[2:0]	2:0	Select block color changing by widtht.	
18h (5E60h)	**REG5E60**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_LINE_CNT[7:0]	7:0	Software set ring buffer ready data line count.	
18h (5E61h)	**REG5E61**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SW_LINE_CNT[11:8]	3:0	See description of '5E60h'.	
19h (5E65h)	**REG5E65**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	EN_SW_SYNC	4	Enable Software synchronization mechanism.	
	-	3:2	Reserved.	
	CLR_EOF_STATUS	1	Read: End of frame status. Write: Clear end of frame status.	
	TRIG_MIF_RD	0	Trigger read request.	

IPM Register (Bank = 2F)

Index (Absolute)	Mnemonic	Bit	Description	
1Dh (5E74h)	**REG5E74**	**7:0**	**Default : 0x00**	**Access : RO**
	LINE_CNT[7:0]	7:0	Current process line count.	
1Dh (5E75h)	**REG5E75**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	LINE_CNT[11:8]	3:0	See description of '5E74h'.	
1Eh (5E78h)	**REG5E78**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS[7:0]	7:0	Internal STATUS for debug.	
1Eh (5E79h)	**REG5E79**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS[15:8]	7:0	See description of '5E78h'.	
1Fh (5E7Ch)	**REG5E7C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	IPM_BIST_FAIL	0	Fifo bist fail indicator.	

IPM2 Register (Bank = 2F)

IPM2 Register (Bank = 2F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
20h (5E80h)	**REG5E80**	**7:0**	**Default : 0x00**	**Access : R/W**
	INTERLACE_OUT	7	Interlace output.	
	-	6:2	Reserved.	
	EN_IPM	1	Enable IPM.	
	IPM_TRIG_SEL	0	IPM trigger method selection.	
20h (5E81h)	**REG5E81**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_2FB_EN	7	IPM 2 frame buffer mode.	
	-	6:3	Reserved.	
	422_YC_ORDER	2	YUV422 source data arrangement order: MSB<->LSB. 0: {Y1,Cr,Y0,Cb}. 1: {Cr,Y1,Cb,Y0}.	
	-	1	Reserved.	
	444_EN	0	YUV 444 data format.	
21h (5E84h)	**REG5E84**	**7:0**	**Default : 0x00**	**Access : R/W**
	PITCH[7:0]	7:0	Source frame buffer PITCH.	
21h (5E85h)	**REG5E85**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	PITCH[10:8]	2:0	See description of '5E84h'.	
24h (5E90h)	**REG5E90**	**7:0**	**Default : 0xCF**	**Access : R/W**
	PIC_WIDTH_M1[7:0]	7:0	Source image width minus one.	
24h (5E91h)	**REG5E91**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	PIC_WIDTH_M1[11:8]	3:0	See description of '5E90h'.	
25h (5E94h)	**REG5E94**	**7:0**	**Default : 0xDF**	**Access : R/W**
	PIC_HEIGHT_M1[7:0]	7:0	Source image height minus one.	
25h (5E95h)	**REG5E95**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	PIC_HEIGHT_M1[11:8]	3:0	See description of '5E94h'.	
26h (5E98h)	**REG5E98**	**7:0**	**Default : 0x00**	**Access : R/W**
	STARTX[7:0]	7:0	Horizontal start offset. (Unit: pixel).	
26h	**REG5E99**	**7:0**	**Default : 0x00**	**Access : R/W**

IPM2 Register (Bank = 2F)

Index (Absolute)	Mnemonic	Bit	Description	
(5E99h)	-	7:4	Reserved.	
	STARTX[11:8]	3:0	See description of '5E98h'.	
27h (5E9Ch)	**REG5E9C**	**7:0**	**Default : 0x00**	**Access : R/W**
	STARTY[7:0]	7:0	Vertical start offset. (Unit: line).	
27h (5E9Dh)	**REG5E9D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	STARTY[11:8]	3:0	See description of '5E9Ch'.	
28h (5EA0h)	**REG5EA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	BASE_ADDR0[7:0]	7:0	Frame buffer base address.	
28h (5EA1h)	**REG5EA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	BASE_ADDR0[15:8]	7:0	See description of '5EA0h'.	
29h (5EA4h)	**REG5EA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	BASE_ADDR0[23:16]	7:0	See description of '5EA0h'.	
29h (5EA5h)	**REG5EA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	BASE_ADDR0[25:24]	1:0	See description of '5EA0h'.	
2Ah (5EA8h)	**REG5EA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	BASE_ADDR1[7:0]	7:0	Frame buffer base address.	
2Ah (5EA9h)	**REG5EA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	BASE_ADDR1[15:8]	7:0	See description of '5EA8h'.	
2Bh (5EACh)	**REG5EAC**	**7:0**	**Default : 0x00**	**Access : R/W**
	BASE_ADDR1[23:16]	7:0	See description of '5EA8h'.	
2Bh (5EADh)	**REG5EAD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	BASE_ADDR1[25:24]	1:0	See description of '5EA8h'.	
2Ch (5EB0h)	**REG5EB0**	**7:0**	**Default : 0x00**	**Access : R/W**
	FIFO_RTHR_HP[3:0]	7:4	Trigger high priority read request threshold.	
	FIFO_RTHR[3:0]	3:0	Trigger read request threshold.	
2Ch (5EB1h)	**REG5EB1**	**7:0**	**Default : 0x07**	**Access : R/W**
	-	7:4	Reserved.	
	FIFO_RLEN[3:0]	3:0	Max read request length.	
2Fh (5EBCh)	**REG5EBC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	

IPM2 Register (Bank = 2F)

Index (Absolute)	Mnemonic	Bit	Description	
	JMD_BUFFER[1:0]	2:1	JMD temp buffer size. 0: 32 lines. 1: 64lines. 2: 8 lines. 3: 16 lines.	
	EN_SYNC_JMD	0	Enable synchronization mechanism with JMD.	
30h (5EC0h)	**REG5EC0**	**7:0**	**Default : 0x06**	**Access : R/W**
	-	7:4	Reserved.	
	TPAT_INIT_COLOR[2:0]	3:1	Select initial color.	
	EN_TESTPAT	0	Enable test pattern.	
31h (5EC4h)	**REG5EC4**	**7:0**	**Default : 0x76**	**Access : R/W**
	-	7	Reserved.	
	TPAT_BLKY[2:0]	6:4	Select block height.	
	-	3	Reserved.	
	TPAT_BLKX[2:0]	2:0	Select block width.	
31h (5EC5h)	**REG5EC5**	**7:0**	**Default : 0x11**	**Access : R/W**
	-	7	Reserved.	
	TPAT_DELTA_V[2:0]	6:4	Select block color changing by height.	
	-	3	Reserved.	
	TPAT_DELTA_H[2:0]	2:0	Select block color changing by widtht.	
38h (5EE0h)	**REG5EE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_LINE_CNT[7:0]	7:0	Software set ring buffer ready data line count.	
38h (5EE1h)	**REG5EE1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SW_LINE_CNT[11:8]	3:0	See description of '5EE0h'.	
39h (5EE5h)	**REG5EE5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	EN_SW_SYNC	4	Enable Software synchronization mechanism.	
	-	3:2	Reserved.	
	CLR_EOF_STATUS	1	Read: End of frame status. Write: Clear end of frame status.	
	TRIG_MIF_RD	0	Trigger read request.	
3Dh (5EF4h)	**REG5EF4**	**7:0**	**Default : 0x00**	**Access : RO**
	LINE_CNT[7:0]	7:0	Current process line count.	

IPM2 Register (Bank = 2F)

Index (Absolute)	Mnemonic	Bit	Description	
3Dh (5EF5h)	**REG5EF5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	LINE_CNT[11:8]	3:0	See description of '5EF4h'.	
3Eh (5EF8h)	**REG5EF8**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS[7:0]	7:0	Internal STATUS for debug.	
3Eh (5EF9h)	**REG5EF9**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS[15:8]	7:0	See description of '5EF8h'.	
3Fh (5EFCh)	**REG5EFC**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	IPM_BIST_FAIL	0	Fifo bist fail indicator.	

IPW Register (Bank = 2F)

IPW Register (Bank = 2F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
40h (5F00h)	**REG5F00**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPW_INTL_EN	7	IPW interlace mode enable.	
	-	6:4	Reserved.	
	IPW_WBE_MASK	3	IPW miu write byte enable mask.	
	IPW_WREQ_OFF	2	IPW force off.	
	-	1:0	Reserved.	
40h (5F01h)	**REG5F01**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPW_WREQ_RST	7	IPW write request reset.	
	-	6:3	Reserved.	
	IPW_DAT_ORDER	2	IPW data reorder.	
	-	1	Reserved.	
	IPW_444_EN	0	IPW 444 format.	
41h (5F04h)	**REG5F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPW_PITCH[7:0]	7:0	IPW frame buffer pitch.	
41h (5F05h)	**REG5F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	IPW_PITCH[10:8]	2:0	See description of '5F04h'.	
44h (5F10h)	**REG5F10**	**7:0**	**Default : 0xCF**	**Access : R/W**
	IPW_FETNUM_M1[7:0]	7:0	IPW source image width minus 1.	
44h (5F11h)	**REG5F11**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	IPW_FETNUM_M1[11:8]	3:0	See description of '5F10h'.	
45h (5F14h)	**REG5F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPW_VCNT_LIMIT_NUM_M1[7:0]	7:0	IPW vertical count limit max height minus1.	
45h (5F15h)	**REG5F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPW_VCNT_LIMIT_EN	7	IPW vertical count limit enable.	
	-	6:4	Reserved.	
	IPW_VCNT_LIMIT_NUM_M1[11:8]	3:0	See description of '5F14h'.	
48h (5F20h)	**REG5F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPW_BASE_ADDR0[7:0]	7:0	IPW frame buffer base address0.	
48h	**REG5F21**	**7:0**	**Default : 0x00**	**Access : R/W**

IPW Register (Bank = 2F)

Index (Absolute)	Mnemonic	Bit	Description	
(5F21h)	IPW_BASE_ADDR0[15:8]	7:0	See description of '5F20h'.	
49h (5F24h)	**REG5F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPW_BASE_ADDR0[23:16]	7:0	See description of '5F20h'.	
49h (5F25h)	**REG5F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	IPW_BASE_ADDR0[25:24]	1:0	See description of '5F20h'.	
4Ah (5F28h)	**REG5F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPW_BASE_ADDR1[7:0]	7:0	IPW frame buffer base address1.	
4Ah (5F29h)	**REG5F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPW_BASE_ADDR1[15:8]	7:0	See description of '5F28h'.	
4Bh (5F2Ch)	**REG5F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPW_BASE_ADDR1[23:16]	7:0	See description of '5F28h'.	
4Bh (5F2Dh)	**REG5F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	IPW_BASE_ADDR1[25:24]	1:0	See description of '5F28h'.	
4Ch (5F30h)	**REG5F30**	**7:0**	**Default : 0x94**	**Access : R/W**
	IPW_WREQ_HPRI[3:0]	7:4	IPW write request high priority threshold.	
	IPW_WREQ_THRD[3:0]	3:0	IPW write request trigger threshold.	
4Ch (5F31h)	**REG5F31**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	IPW_WREQ_MAX[3:0]	3:0	IPW max write request length.	
59h (5F65h)	**REG5F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	IPW_STATUS_CLR	0	IPW status clear.	
5Eh (5F78h)	**REG5F78**	**7:0**	**Default : 0x00**	**Access : RO**
	IPW_STATUS_LB_CNT[4:0]	7:3	IPW input source ready status.	
	IPW_STATUS_WM2_RDY	2	IPW input source ready status.	
	IPW_STATUS_2MI_RDY	1	IPW to miu ready status.	
	IPW_LB_STATUS	0	IPW LB full status.	
5Eh (5F79h)	**REG5F79**	**7:0**	**Default : 0x00**	**Access : RO**
	IPW_STATUS_VALID_CNT[3:0]	7:4	IPW MIU data valid count.	
	IPW_STATUS_VCNT[3:0]	3:0	IPW Vertical count status.	
5Fh	**REG5F7C**	**7:0**	**Default : 0x00**	**Access : RO**

IPW Register (Bank = 2F)

Index (Absolute)	Mnemonic	Bit	Description	
(5F7Ch)	-	7:1	Reserved.	
	IPW_BIST_FAIL	0	Fifo bist fail indicator.	
60h (5F80h)	**REG5F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MSYN_IPW_AUTO_FB_EN	2	Auto update write when ipw is done.	
	MSYN_2FB_FD_MD	1	FB sync 2 frame buffer field mode selection. 1'b0: toggle. 1'b1: by bt656_fd.	
	MSYN_2FB_EN	0	FB sync 2 frame buffer enable.	
60h (5F81h)	**REG5F81**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MSYN_RBK_MD[1:0]	5:4	Read/write bank map. 2'd0: rbk = wbk. 2'd1: rbk = ~wbk. 2'd2: rbk = ~rbk (toggle). 2'd3: reserved.	
	-	3:1	Reserved.	
	MSYN_2FB_FD_INV	0	Bt656_fd invert.	
61h (5F84h)	**REG5F84**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	MSYN_FORCE_WBK_EN	4	Force write bank enable.	
	-	3:1	Reserved.	
	MSYN_FORCE_WBK	0	Force write bank.	
61h (5F85h)	**REG5F85**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	MSYN_FORCE_RBK_EN	4	Force read bank enable.	
	-	3:1	Reserved.	
	MSYN_FORCE_RBK	0	Force read bank.	

VIP Register (Bank = 30)

VIP Register (Bank = 30)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
30h (60C0h)	**REG60C0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_ICC_EN	6	Main window ICC enable.	
	-	5:0	Reserved.	
31h (60C4h)	**REG60C4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_R[3:0]	3:0	Main window ICC saturation adjustment of R.	
31h (60C5h)	**REG60C5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_G[3:0]	3:0	Main window ICC saturation adjustment of G.	
32h (60C8h)	**REG60C8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_B[3:0]	3:0	Main window ICC saturation adjustment of B.	
32h (60C9h)	**REG60C9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_C[3:0]	3:0	Main window ICC saturation adjustment of C.	
33h (60CCh)	**REG60CC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_M[3:0]	3:0	Main window ICC saturation adjustment of M.	
33h (60CDh)	**REG60CD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_Y[3:0]	3:0	Main window ICC saturation adjustment of Y.	
34h (60D0h)	**REG60D0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_F[3:0]	3:0	Main window ICC saturation adjustment of F.	
35h (60D4h)	**REG60D4**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_SIGN_SA_USER[7:0]	7:0	Main window ICC decrease saturation.	
36h (60D8h)	**REG60D8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	COMMON_MINUS_GAIN[4:0]	4:0	ICC decrease saturation common gain.	
36h	**REG60D9**	**7:0**	**Default : 0x00**	**Access : R/W**

VIP Register (Bank = 30)

Index (Absolute)	Mnemonic	Bit	Description	
(60D9h)	-	7	Reserved.	
	SA_MIN[6:0]	6:0	ICC decrease saturation minimum threshold.	
40h (6100h)	**REG6100**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IBC_EN	7	Main window IBC enable.	
	-	6:0	Reserved.	
41h (6104h)	**REG6104**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YR_ADJ[5:0]	5:0	Main window IBC Y adjustment of R.	
41h (6105h)	**REG6105**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YG_ADJ[5:0]	5:0	Main window IBC Y adjustment of G.	
42h (6108h)	**REG6108**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YB_ADJ[5:0]	5:0	Main window IBC Y adjustment of B.	
42h (6109h)	**REG6109**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YC_ADJ[5:0]	5:0	Main window IBC Y adjustment of C.	
43h (610Ch)	**REG610C**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YM_ADJ[5:0]	5:0	Main window IBC Y adjustment of M.	
43h (610Dh)	**REG610D**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YY_ADJ[5:0]	5:0	Main window IBC Y adjustment of Y.	
44h (6110h)	**REG6110**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YF_ADJ[5:0]	5:0	Main window IBC Y adjustment of F.	
48h (6121h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
60h (6180h)	**REG6180**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_EN	7	Main window IHC enable.	
	-	6:0	Reserved.	
61h (6184h)	**REG6184**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

VIP Register (Bank = 30)

Index (Absolute)	Mnemonic	Bit	Description	
	MAIN_HUE_USER_R[6:0]	6:0	Main window IHC hue adjustment of R.	
61h (6185h)	**REG6185**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_G[6:0]	6:0	Main window IHC hue adjustment of G.	
62h (6188h)	**REG6188**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_B[6:0]	6:0	Main window IHC hue adjustment of B.	
62h (6189h)	**REG6189**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_C[6:0]	6:0	Main window IHC hue adjustment of C.	
63h (618Ch)	**REG618C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_M[6:0]	6:0	Main window IHC hue adjustment of M.	
63h (618Dh)	**REG618D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_Y[6:0]	6:0	Main window IHC hue adjustment of Y.	
64h (6190h)	**REG6190**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_F[6:0]	6:0	Main window IHC hue adjustment of F.	
65h (6194h)	**REG6194**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	R2Y_DITHER_EN	1	Main window RGB to YCbCr Dither Enable.	
	MAIN_R2Y_EN	0	Main window RGB to YCbCr Enable.	

DLC Register (Bank = 31)

DLC Register (Bank = 31)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Bh (622Ch)	**REG622C**	**7:0**	**Default : 0x00**	**Access : RO**
	MAIN_MAX_PIXEL[7:0]	7:0	Main window maximum pixel.	
0Bh (622Dh)	**REG622D**	**7:0**	**Default : 0x00**	**Access : RO**
	MAIN_MIN_PIXEL[7:0]	7:0	Main window minimum pixel.	
0Fh (623Ch)	**REG623C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BRI_ADJUST[7:0]	7:0	Main window Y adjust.	
10h (6240h)	**REG6240**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_BLACK_START[6:0]	6:0	Main window black start.	
10h (6241h)	**REG6241**	**7:0**	**Default : 0x80**	**Access : R/W**
	MAIN_BLACK_SLOP[7:0]	7:0	Main window black slope.	
11h (6244h)	**REG6244**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_WHITE_START[6:0]	6:0	Main window white start.	
11h (6245h)	**REG6245**	**7:0**	**Default : 0x80**	**Access : R/W**
	MAIN_WHITE_SLOP[7:0]	7:0	Main window white slope.	
14h (6251h)	**REG6251**	**7:0**	**Default : 0x40**	**Access : R/W**
	MAIN_C_GAIN[7:0]	7:0	Main window C gain.	
16h (6258h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
28h (62A0h)	**REG62A0**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_1F_00[7:0]	7:0	Histogram report section1.	
28h (62A1h)	**REG62A1**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_1F_00[15:8]	7:0	See description of '62A0h'.	
29h (62A4h)	**REG62A4**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_3F_20[7:0]	7:0	Histogram report section2.	
29h (62A5h)	**REG62A5**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_3F_20[15:8]	7:0	See description of '62A4h'.	
2Ah (62A8h)	**REG62A8**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_5F_40[7:0]	7:0	Histogram report section3.	
2Ah	**REG62A9**	**7:0**	**Default : 0x00**	**Access : RO**

(62A9h)	TOTAL_5F_40[15:8]	7:0	See description of '62A8h'.	
2Bh (62ACh)	**REG62AC**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_7F_60[7:0]	7:0	Histogram report section4.	
2Bh (62ADh)	**REG62AD**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_7F_60[15:8]	7:0	See description of '62ACh'.	
2Ch (62B0h)	**REG62B0**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_9F_80[7:0]	7:0	Histogram report section5.	
2Ch (62B1h)	**REG62B1**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_9F_80[15:8]	7:0	See description of '62B0h'.	
2Dh (62B4h)	**REG62B4**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_BF_A0[7:0]	7:0	Histogram report section6.	
2Dh (62B5h)	**REG62B5**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_BF_A0[15:8]	7:0	See description of '62B4h'.	
2Eh (62B8h)	**REG62B8**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_DF_C0[7:0]	7:0	Histogram report section7.	
2Eh (62B9h)	**REG62B9**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_DF_C0[15:8]	7:0	See description of '62B8h'.	
2Fh (62BCh)	**REG62BC**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_FF_E0[7:0]	7:0	Histogram report section8.	
2Fh (62BDh)	**REG62BD**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_FF_E0[15:8]	7:0	See description of '62BCh'.	
30h (62C0h)	**REG62C0**	**7:0**	**Default : 0x08**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_0[7:0]	7:0	Main window curve table 0.	
30h (62C1h)	**REG62C1**	**7:0**	**Default : 0x18**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_1[7:0]	7:0	Main window curve table 1.	
31h (62C4h)	**REG62C4**	**7:0**	**Default : 0x28**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_2[7:0]	7:0	Main window curve table 2.	
31h (62C5h)	**REG62C5**	**7:0**	**Default : 0x38**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_3[7:0]	7:0	Main window curve table 3.	
32h (62C8h)	**REG62C8**	**7:0**	**Default : 0x48**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_4[7:0]	7:0	Main window curve table 4.	
32h (62C9h)	**REG62C9**	**7:0**	**Default : 0x58**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_5[7:0]	7:0	Main window curve table 5.	
33h (62CCh)	**REG62CC**	**7:0**	**Default : 0x68**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_6[7:0]	7:0	Main window curve table 6.	
33h	**REG62CD**	**7:0**	**Default : 0x78**	**Access : R/W**

(62CDh)	MAIN_CURVE_FIT_TABLE_7[7:0]	7:0	Main window curve table 7.	
34h (62D0h)	**REG62D0**	**7:0**	**Default : 0x88**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_8[7:0]	7:0	Main window curve table 8.	
34h (62D1h)	**REG62D1**	**7:0**	**Default : 0x98**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_9[7:0]	7:0	Main window curve table 9.	
35h (62D4h)	**REG62D4**	**7:0**	**Default : 0xA8**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_10[7:0]	7:0	Main window curve table 10.	
35h (62D5h)	**REG62D5**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_11[7:0]	7:0	Main window curve table 11.	
36h (62D8h)	**REG62D8**	**7:0**	**Default : 0xC8**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_12[7:0]	7:0	Main window curve table 12.	
36h (62D9h)	**REG62D9**	**7:0**	**Default : 0xD8**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_13[7:0]	7:0	Main window curve table 13.	
37h (62DCh)	**REG62DC**	**7:0**	**Default : 0xE8**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_14[7:0]	7:0	Main window curve table 14.	
37h (62DDh)	**REG62DD**	**7:0**	**Default : 0xF8**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_15[7:0]	7:0	Main window curve table 15.	
61h (6384h)	**REG6384**	**7:0**	**Default : 0x00**	**Access : RO**
	MAIN_MAX_PIXEL_SAT[7:0]	7:0	Main window minimum pixel saturation.	
61h (6385h)	**REG6385**	**7:0**	**Default : 0x00**	**Access : RO**
	MAIN_MIN_PIXEL_SAT[7:0]	7:0	Main window maximum pixel saturation.	
76h (63D8h)	**REG63D8**	**7:0**	**Default : 0x08**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_N0[7:0]	7:0	Main window curve table left point.	
76h (63D9h)	**REG63D9**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	MAIN_CURVE_FIT_TABLE_N0[8]	0	See description of '63D8h'.	
77h (63DCh)	**REG63DC**	**7:0**	**Default : 0x08**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_16[7:0]	7:0	Main window curve table 16.	
77h (63DDh)	**REG63DD**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	MAIN_CURVE_FIT_TABLE_16[8]	0	See description of '63DCh'.	

TCON Register (Bank = 32)

TCON Register (Bank = 32)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
03h (640Ch)	**REG640C**	**7:0**	**Default: 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	EN_FCNT	0	Enable frame counter for power on sequence.	
04h (6410h)	**REG6410**	**7:0**	**Default: 0xFF**	**Access : R/W**
	TC_H1END_ODD[7:0]	7:0	The odd line HEND of GPO1 for Special Over Mode / 2nd horizontal end of GPO1.	
04h (6411h)	**REG6411**	**7:0**	**Default: 0x0F**	**Access : R/W**
	-	7	Reserved.	
	OVER_MODE_1	6	Special over mode enable of GPO1. 1: If the 1st GPO end position is at odd line, its horizontal end position will be determined by TC_H1END_ODD.	
	-	5:4	Reserved.	
	TC_H1END_ODD[11:8]	3:0	See description of '6410h'.	
05h (6414h)	**REG6414**	**7:0**	**Default: 0xFF**	**Access : R/W**
	TC_H2END_ODD[7:0]	7:0	The odd line HEND of GPO2 for Special Over Mode / 2nd horizontal end of GPO2.	
05h (6415h)	**REG6415**	**7:0**	**Default: 0x0F**	**Access : R/W**
	-	7	Reserved.	
	OVER_MODE_2	6	Special over mode enable of GPO2. 1: If the 1st GPO end position is at odd line, its horizontal end position will be determined by TC_H2END_ODD.	
	-	5:4	Reserved.	
	TC_H2END_ODD[11:8]	3:0	See description of '6414h'.	
06h (6418h)	**REG6418**	**7:0**	**Default: 0xFF**	**Access : R/W**
	TC_H3END_ODD[7:0]	7:0	The odd line HEND of GPO3 for Special Over Mode / 2nd horizontal end of GPO3.	
06h (6419h)	**REG6419**	**7:0**	**Default: 0x0F**	**Access : R/W**
	-	7	Reserved.	
	OVER_MODE_3	6	Special over mode enable of GPO3. 1: If the 1st GPO end position is at odd line, its horizontal end position will be determined by TC_H3END_ODD.	
	-	5:4	Reserved.	
	TC_H3END_ODD[11:8]	3:0	See description of '6418h'.	

TCON Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description	
07h (641Ch)	**REG641C**	**7:0**	**Default: 0xFF**	**Access : R/W**
	TC_H4END_ODD[7:0]	7:0	The odd line HEND of GPO4 for Special Over Mode / 2nd horizontal end of GPO4.	
07h (641Dh)	**REG641D**	**7:0**	**Default: 0x0F**	**Access : R/W**
	-	7	Reserved.	
	OVER_MODE_4	6	Special over mode enable of GPO4. 1: If the 1st GPO end position is at odd line, its horizontal end position will be determined by TC_H4END_ODD.	
	-	5:4	Reserved.	
	TC_H4END_ODD[11:8]	3:0	See description of '641Ch'.	
08h (6420h)	**REG6420**	**7:0**	**Default: 0xFF**	**Access : R/W**
	TC_H5END_ODD[7:0]	7:0	The odd line HEND of GPO5 for Special Over Mode / 2nd horizontal end of GPO5.	
08h (6421h)	**REG6421**	**7:0**	**Default: 0x0F**	**Access : R/W**
	-	7	Reserved.	
	OVER_MODE_5	6	Special over mode enable of GPO5. 1: If the 1st GPO end position is at odd line, its horizontal end position will be determined by TC_H5END_ODD.	
	-	5:4	Reserved.	
	TC_H5END_ODD[11:8]	3:0	See description of '6420h'.	
09h (6424h)	**REG6424**	**7:0**	**Default: 0xFF**	**Access : R/W**
	TC_H6END_ODD[7:0]	7:0	The odd line HEND of GPO6 for Special Over Mode / 2nd horizontal end of GPO9.	
09h (6425h)	**REG6425**	**7:0**	**Default: 0x0F**	**Access : R/W**
	-	7	Reserved.	
	OVER_MODE_6	6	Special over mode enable of GPO6. 1: If the 1st GPO end position is at odd line, its horizontal end position will be determined by TC_H6END_ODD.	
	-	5:4	Reserved.	
	TC_H6END_ODD[11:8]	3:0	See description of '6424h'.	
0Dh (6434h)	**REG6434**	**7:0**	**Default: 0x00**	**Access : R/W**
	TC_V0ST[7:0]	7:0	Vertical start of GPO0.	
0Dh (6435h)	**REG6435**	**7:0**	**Default: 0x00**	**Access : R/W**
	-	7:4	Reserved.	

TCON Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description	
	TC_V0ST[11:8]	3:0	See description of '6434h'.	
0Eh (6438h)	**REG6438**	**7:0**	**Default: 0x00**	**Access : R/W**
	TC_V0END[7:0]	7:0	Vertical end of GPO0.	
0Eh (6439h)	**REG6439**	**7:0**	**Default: 0x00**	**Access : R/W**
	FRAME_TOG0[3:0]	7:4	Frame tog number of GPO0. (If set 2, means 3 frame toggle once).	
	TC_V0END[11:8]	3:0	See description of '6438h'.	
0Fh (643Ch)	**REG643C**	**7:0**	**Default: 0x80**	**Access : R/W**
	TC_H0ST[7:0]	7:0	Horizontal start of GPO0.	
0Fh (643Dh)	**REG643D**	**7:0**	**Default: 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	TC_H0ST[11:8]	3:0	See description of '643Ch'.	
10h (6440h)	**REG6440**	**7:0**	**Default: 0x00**	**Access : R/W**
	TC_H0END[7:0]	7:0	Horizontal end of GPO0.	
10h (6441h)	**REG6441**	**7:0**	**Default: 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	TC_H0END[11:8]	3:0	See description of '6440h'.	
11h (6444h)	**REG6444**	**7:0**	**Default: 0x00**	**Access : R/W**
	TC_V1ST[7:0]	7:0	Vertical start of GPO1.	
11h (6445h)	**REG6445**	**7:0**	**Default: 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	TC_V1ST[11:8]	3:0	See description of '6444h'.	
12h (6448h)	**REG6448**	**7:0**	**Default: 0x00**	**Access : R/W**
	TC_V1END[7:0]	7:0	Vertical end of GPO1.	
12h (6449h)	**REG6449**	**7:0**	**Default: 0x00**	**Access : R/W**
	FRAME_TOG1[3:0]	7:4	Frame tog number of GPO1. (If set 2, means 3 frame toggle once).	
	TC_V1END[11:8]	3:0	See description of '6448h'.	
13h (644Ch)	**REG644C**	**7:0**	**Default: 0x0E**	**Access : R/W**
	TC_H1ST[7:0]	7:0	Horizontal start of GPO1.	
13h (644Dh)	**REG644D**	**7:0**	**Default: 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	TC_H1ST[11:8]	3:0	See description of '644Ch'.	

TCON Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description	
14h (6450h)	**REG6450**	**7:0**	**Default: 0x0F**	**Access : R/W**
	TC_H1END[7:0]	7:0	Horizontal end of GPO1.	
14h (6451h)	**REG6451**	**7:0**	**Default: 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	TC_H1END[11:8]	3:0	See description of '6450h'.	
15h (6454h)	**REG6454**	**7:0**	**Default: 0xA7**	**Access : R/W**
	TC_V2ST[7:0]	7:0	Vertical start of GPO2.	
15h (6455h)	**REG6455**	**7:0**	**Default: 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	TC_V2ST[11:8]	3:0	See description of '6454h'.	
16h (6458h)	**REG6458**	**7:0**	**Default: 0xA8**	**Access : R/W**
	TC_V2END[7:0]	7:0	Vertical end of GPO2.	
16h (6459h)	**REG6459**	**7:0**	**Default: 0x00**	**Access : R/W**
	FRAME_TOG2[3:0]	7:4	Frame tog number of GPO2. (If set 2, means 3 frame toggle once).	
	TC_V2END[11:8]	3:0	See description of '6458h'.	
17h (645Ch)	**REG645C**	**7:0**	**Default: 0xC0**	**Access : R/W**
	TC_H2ST[7:0]	7:0	Horizontal start of GPO2.	
17h (645Dh)	**REG645D**	**7:0**	**Default: 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	TC_H2ST[11:8]	3:0	See description of '645Ch'.	
18h (6460h)	**REG6460**	**7:0**	**Default: 0xC0**	**Access : R/W**
	TC_H2END[7:0]	7:0	Horizontal end of GPO2.	
18h (6461h)	**REG6461**	**7:0**	**Default: 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	TC_H2END[11:8]	3:0	See description of '6460h'.	
19h (6464h)	**REG6464**	**7:0**	**Default: 0x00**	**Access : R/W**
	TC_V3ST[7:0]	7:0	Vertical start of GPO3.	
19h (6465h)	**REG6465**	**7:0**	**Default: 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	TC_V3ST[11:8]	3:0	See description of '6464h'.	
1Ah (6468h)	**REG6468**	**7:0**	**Default: 0x00**	**Access : R/W**
	TC_V3END[7:0]	7:0	Vertical end of GPO3.	

TCON Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description	
1Ah (6469h)	**REG6469**	**7:0**	**Default: 0x00**	**Access : R/W**
	FRAME_TOG3[3:0]	7:4	Frame tog number of GPO3. (If set 2, means 3 frame toggle once).	
	TC_V3END[11:8]	3:0	See description of '6468h'.	
1Bh (646Ch)	**REG646C**	**7:0**	**Default: 0x78**	**Access : R/W**
	TC_H3ST[7:0]	7:0	Horizontal start of GPO3.	
1Bh (646Dh)	**REG646D**	**7:0**	**Default: 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	TC_H3ST[11:8]	3:0	See description of '646Ch'.	
1Ch (6470h)	**REG6470**	**7:0**	**Default: 0x60**	**Access : R/W**
	TC_H3END[7:0]	7:0	Horizontal end of GPO3.	
1Ch (6471h)	**REG6471**	**7:0**	**Default: 0x03**	**Access : R/W**
	-	7:4	Reserved.	
	TC_H3END[11:8]	3:0	See description of '6470h'.	
1Dh (6474h)	**REG6474**	**7:0**	**Default: 0x00**	**Access : R/W**
	TC_V4ST[7:0]	7:0	Vertical start of GPO4.	
1Dh (6475h)	**REG6475**	**7:0**	**Default: 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	TC_V4ST[11:8]	3:0	See description of '6474h'.	
1Eh (6478h)	**REG6478**	**7:0**	**Default: 0x00**	**Access : R/W**
	TC_V4END[7:0]	7:0	Vertical end of GPO4.	
1Eh (6479h)	**REG6479**	**7:0**	**Default: 0x00**	**Access : R/W**
	FRAME_TOG4[3:0]	7:4	Frame tog number of GPO4. (If set 2, means 3 frame toggle once).	
	TC_V4END[11:8]	3:0	See description of '6478h'.	
1Fh (647Ch)	**REG647C**	**7:0**	**Default: 0x40**	**Access : R/W**
	TC_H4ST[7:0]	7:0	Horizontal start of GPO4.	
1Fh (647Dh)	**REG647D**	**7:0**	**Default: 0x03**	**Access : R/W**
	-	7:4	Reserved.	
	TC_H4ST[11:8]	3:0	See description of '647Ch'.	
20h (6480h)	**REG6480**	**7:0**	**Default: 0x40**	**Access : R/W**
	TC_H4END[7:0]	7:0	Horizontal end of GPO4.	
20h	**REG6481**	**7:0**	**Default: 0x01**	**Access : R/W**

TCON Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description	
(6481h)	-	7:4	Reserved.	
	TC_H4END[11:8]	3:0	See description of '6480h'.	
21h (6484h)	**REG6484**	**7:0**	**Default: 0x00**	**Access : R/W**
	TC_V5ST[7:0]	7:0	Vertical start of GPO5.	
21h (6485h)	**REG6485**	**7:0**	**Default: 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	TC_V5ST[11:8]	3:0	See description of '6484h'.	
22h (6488h)	**REG6488**	**7:0**	**Default: 0x00**	**Access : R/W**
	TC_V5END[7:0]	7:0	Vertical end of GPO5.	
22h (6489h)	**REG6489**	**7:0**	**Default: 0x00**	**Access : R/W**
	FRAME_TOG5[3:0]	7:4	Frame tog number LSB of GPO5. (If set 2, means 3 frame toggle once).	
	TC_V5END[11:8]	3:0	See description of '6488h'.	
23h (648Ch)	**REG648C**	**7:0**	**Default: 0x34**	**Access : R/W**
	TC_H5ST[7:0]	7:0	Horizontal start of GPO5.	
23h (648Dh)	**REG648D**	**7:0**	**Default: 0x03**	**Access : R/W**
	-	7:4	Reserved.	
	TC_H5ST[11:8]	3:0	See description of '648Ch'.	
24h (6490h)	**REG6490**	**7:0**	**Default: 0x50**	**Access : R/W**
	TC_H5END[7:0]	7:0	Horizontal end of GPO5.	
24h (6491h)	**REG6491**	**7:0**	**Default: 0x03**	**Access : R/W**
	-	7:4	Reserved.	
	TC_H5END[11:8]	3:0	See description of '6490h'.	
25h (6494h)	**REG6494**	**7:0**	**Default: 0xFF**	**Access : R/W**
	TC_V6ST[7:0]	7:0	Vertical start of GPO6.	
25h (6495h)	**REG6495**	**7:0**	**Default: 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	TC_V6ST[11:8]	3:0	See description of '6494h'.	
26h (6498h)	**REG6498**	**7:0**	**Default: 0xFF**	**Access : R/W**
	TC_V6END[7:0]	7:0	Vertical end of GPO6.	
26h (6499h)	**REG6499**	**7:0**	**Default: 0x0F**	**Access : R/W**
	FRAME_TOG6[3:0]	7:4	Frame tog number of GPO6. (If set 2, means 3 frame toggle once).	

TCON Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description	
	TC_V6END[11:8]	3:0	See description of '6498h'.	
27h (649Ch)	**REG649C**	**7:0**	**Default: 0xFF**	**Access : R/W**
	TC_H6ST[7:0]	7:0	Horizontal start of GPO6.	
27h (649Dh)	**REG649D**	**7:0**	**Default: 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	TC_H6ST[11:8]	3:0	See description of '649Ch'.	
28h (64A0h)	**REG64A0**	**7:0**	**Default: 0xFF**	**Access : R/W**
	TC_H6END[7:0]	7:0	Horizontal end of GPO6.	
28h (64A1h)	**REG64A1**	**7:0**	**Default: 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	TC_H6END[11:8]	3:0	See description of '64A0h'.	
39h (64E4h)	**REG64E4**	**7:0**	**Default: 0x40**	**Access : R/W**
	G0OP	7	GPO0 Output Polarity. 0: Active high. 1: Active low.	
	G0TC	6	GPO0 Toggle Circuit enable. 0: Normal. 1: Toggle. Toggle mode is useful in POL generation when alternating polarity is required from line to line. Frame to frame polarity changes are made by programming an odd # in the vertical duration when in toggle mode.	
	-	5	Reserved.	
	G0TS[1:0]	4:3	GPO0 Type Select. When toggle mode=0:. 00: Normal. 01: Duration is greater than a line time (over 1 line). 10: Every two lines have one GPO pulse (skip 1 line). 11: Every three lines have one GPO pulse (skip 2 lines). When toggle mode=1: 00: One line toggle. 01: Reserved. 10: Two lines toggle. 11: Three lines toggle.	

TCON Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description	
	G0CS[2:0]	2:0	GPO0 Combination Select. 000: No combination. 001: AND. (GPO# & GPO#-1). 010: OR. (GPO# | GPO#-1). 011: Select GPO# and GPO#-1 on alternating frames. 1xx: XOR. (GPO# ^ GPO#-1).	
39h (64E5h)	**REG64E5**	**7:0**	**Default: 0x00**	**Access : R/W**
	G1OP	7	GPO1 Output Polarity. 0: Active high. 1: Active low.	
	G1TC	6	GPO1 Toggle Circuit enable. 0: Normal. 1: Toggle. Toggle mode is useful in POL generation when alternating polarity is required from line to line. Frame to frame polarity changes are made by programming an odd # in the vertical duration when in toggle mode.	
	-	5	Reserved.	
	G1TS[1:0]	4:3	GPO1 Type Select. When toggle mode=0. 00: Normal. 01: Duration is greater than a line time (over 1 line). 10: Every two lines have one GPO pulse (skip 1 line). 11: Every three lines have one GPO pulse (skip 2 lines). When toggle mode=1: 00: One line toggle. 01: Reserved. 10: Two lines toggle. 11: Three lines toggle.	
	G1CS[2:0]	2:0	GPO1 Combination Select. 000: No combination. 001: AND. (GPO# & GPO#-1). 010: OR. (GPO# | GPO#-1). 011: Select GPO# and GPO#-1 on alternating frames. 1xx: XOR. (GPO# ^ GPO#-1).	
3Ah	**REG64E8**	**7:0**	**Default: 0x00**	**Access : R/W**

TCON Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description
(64E8h)	G2OP	7	GPO2 Output Polarity. 0: Active high. 1: Active low.
	G2TC	6	GPO2 Toggle Circuit enable. 0: Normal. 1: Toggle. Toggle mode is useful in POL generation when alternating polarity is required from line to line. Frame to frame polarity changes are made by programming an odd # in the vertical duration when in toggle mode.
	-	5	Reserved.
	G2TS[1:0]	4:3	GPO2 Type Select. When toggle mode=0: 00: Normal. 01: Duration is greater than a line time (over 1 line). 10: Every two lines have one GPO pulse (skip 1 line). 11: Every three lines have one GPO pulse (skip 2 lines). When toggle mode=1: 00: One line toggle. 01: Reserved. 10: Two lines toggle. 11: Three lines toggle.
	G2CS[2:0]	2:0	GPO2 Combination Select. 000: No combination. 001: AND. (GPO# & GPO#-1). 010: OR. (GPO# | GPO#-1). 011: Select GPO# and GPO#-1 on alternating frames. 1xx: XOR. (GPO# ^ GPO#-1).
3Ah (64E9h)	**REG64E9**	**7:0**	**Default: 0x00** **Access : R/W**
	G3OP	7	GPO3 Output Polarity. 0: Active high. 1: Active low.
	G3TC	6	GPO3 Toggle Circuit enable. 0: Normal. 1: Toggle. Toggle mode is useful in POL generation when alternating polarity is required from line to line. Frame to frame polarity changes are made by programming an odd # in the vertical duration when in toggle mode.

TCON Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description
	-	5	Reserved.
	G3TS[1:0]	4:3	GPO3 Type Select. When toggle mode=0:. 00: Normal. 01: Duration is greater than a line time (over 1 line). 10: Every two lines have one GPO pulse (skip 1 line). 11: Every three lines have one GPO pulse (skip 2 lines). When toggle mode=1: 00: One line toggle. 01: Reserved. 10: Two lines toggle. 11: Three lines toggle.
	G3CS[2:0]	2:0	GPO3 Combination Select. 000: No combination. 001: AND. (GPO# & GPO#-1). 010: OR. (GPO# | GPO#-1). 011: Select GPO# and GPO#-1 on alternating frames. 1xx: XOR. (GPO# ^ GPO#-1).
3Bh (64ECh)	**REG64EC**	**7:0**	**Default: 0x00** **Access : R/W**
	G4OP	7	GPO4 Output Polarity. 0: Active high. 1: Active low.
	G4TC	6	GPO4 Toggle Circuit enable. 0: Normal. 1: Toggle. Toggle mode is useful in POL generation when alternating polarity is required from line to line. Frame to frame polarity changes are made by programming an odd # in the vertical duration when in toggle mode.
	-	5	Reserved.

TCON Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description	
	G4TS[1:0]	4:3	GPO4 Type Select. When toggle mode=0: 00: Normal. 01: Duration is greater than a line time (over 1 line). 10: Every two lines have one GPO pulse (skip 1 line). 11: Every three lines have one GPO pulse (skip 2 lines). When toggle mode=1: 00: One line toggle. 01: Reserved. 10: Two lines toggle. 11: Three lines toggle.	
	G4CS[2:0]	2:0	GPO4 Combination Select. 000: No combination. 001: AND. (GPO# & GPO#-1). 010: OR. (GPO# | GPO#-1). 011: Select GPO# and GPO#-1 on alternating frames. 1xx: XOR. (GPO# ^ GPO#-1).	
3Bh (64EDh)	**REG64ED**	**7:0**	**Default: 0x00**	**Access : R/W**
	G5OP	7	GPO5 Output Polarity. 0: Active high. 1: Active low.	
	G5TC	6	GPO5 Toggle Circuit enable. 0: Normal. 1: Toggle. Toggle mode is useful in POL generation when alternating polarity is required from line to line. Frame to frame polarity changes are made by programming an odd # in the vertical duration when in toggle mode.	
	-	5	Reserved.	

TCON Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description
	G5TS[1:0]	4:3	GPO5 Type Select. When toggle mode=0. 00: Normal. 01: Duration is greater than a line time (over 1 line). 10: Every two lines have one GPO pulse (skip 1 line). 11: Every three lines have one GPO pulse (skip 2 lines). When toggle mode=1: 00: One line toggle. 01: Reserved. 10: Two lines toggle. 11: Three lines toggle.
	G5CS[2:0]	2:0	GPO5 Combination Select. 000: No combination. 001: AND. (GPO# & GPO#-1). 010: OR. (GPO# | GPO#-1). 011: Select GPO# and GPO#-1 on alternating frames. 1xx: XOR. (GPO# ^ GPO#-1).
3Ch (64F0h)	**REG64F0**	**7:0**	**Default: 0x00** **Access : R/W**
	G6OP	7	GPO6 Output Polarity. 0: Active high. 1: Active low.
	G6TC	6	GPO6 Toggle Circuit enable. 0: Normal. 1: Toggle. Toggle mode is useful in POL generation when alternating polarity is required from line to line. Frame to frame polarity changes are made by programming an odd # in the vertical duration when in toggle mode.
	-	5	Reserved.

TCON Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description	
	G6TS[1:0]	4:3	GPO6 Type Select. When toggle mode=0. 00: Normal. 01: Duration is greater than a line time (over 1 line). 10: Every two lines have one GPO pulse (skip 1 line). 11: Every three lines have one GPO pulse (skip 2 lines). When toggle mode=1: 00: One line toggle. 01: Reserved. 10: Two lines toggle. 11: Three lines toggle.	
	G6CS[2:0]	2:0	GPO6 Combination Select. 000: No combination. 001: AND. (GPO# & GPO#-1). 010: OR. (GPO# | GPO#-1). 011: Select GPO# and GPO#-1 on alternating frames. 1xx: XOR. (GPO# ^ GPO#-1).	
3Fh (64FCh)	**REG64FC**	**7:0**	**Default: 0x04**	**Access : R/W**
	GPO5_EN	7	GPO5 enable of POL.	
	GPO4_EN	6	GPO4 enable of POL.	
	GPO3_EN	5	GPO3 enable of POL.	
	GPO2_EN	4	GPO2 enable of POL.	
	GPO1_EN	3	GPO1 enable of POL.	
	GPO0_EN	2	GPO0 enable of POL.	
	-	1:0	Reserved.	
3Fh (64FDh)	**REG64FD**	**7:0**	**Default: 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	GPO6_EN	0	GPO6 enable of POL.	
4Ch (6531h)	**REG6531**	**7:0**	**Default: 0xF0**	**Access : R/W**
	GPO0_PS[3:0]	7:4	Frame count for power sequence of gpo0. Only active with Frame counter enable (EN_FCNT=1).	
	-	3:0	Reserved.	
4Dh (6535h)	**REG6535**	**7:0**	**Default: 0xF0**	**Access : R/W**
	GPO1_PS[3:0]	7:4	Frame count for power sequence of gpo1. Only active with Frame counter enable (EN_FCNT=1).	
	-	3:0	Reserved.	

TCON Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description	
4Eh (6539h)	**REG6539**	**7:0**	**Default: 0xF0**	**Access : R/W**
	GPO2_PS[3:0]	7:4	Frame count for power sequence of gpo2. Only active with Frame counter enable (EN_FCNT=1).	
	-	3:0	Reserved.	
4Fh (653Dh)	**REG653D**	**7:0**	**Default: 0xF0**	**Access : R/W**
	GPO3_PS[3:0]	7:4	Frame count for power sequence of gpo3. Only active with Frame counter enable (EN_FCNT=1).	
	-	3:0	Reserved.	
50h (6541h)	**REG6541**	**7:0**	**Default: 0xF0**	**Access : R/W**
	GPO4_PS[3:0]	7:4	Frame count for power sequence of gpo4. Only active with Frame counter enable (EN_FCNT=1).	
	-	3:0	Reserved.	
51h (6545h)	**REG6545**	**7:0**	**Default: 0xF0**	**Access : R/W**
	GPO5_PS[3:0]	7:4	Frame count for power sequence of gpo5. Only active with Frame counter enable (EN_FCNT=1).	
	-	3:0	Reserved.	
5Bh (656Dh)	**REG656D**	**7:0**	**Default: 0xF0**	**Access : R/W**
	GPO6_PS[3:0]	7:4	Frame count for power sequence of gpo6. Only active with Frame counter enable (EN_FCNT=1).	
	-	3:0	Reserved.	
61h (6584h)	**REG6584**	**7:0**	**Default: 0x7F**	**Access : R/W**
	-	7	Reserved.	
	GPO6_FF_OEN	6	GPO6_FF output enable.	
	GPO5_FF_OEN	5	GPO5_FF output enable.	
	GPO4_FF_OEN	4	GPO4_FF output enable.	
	GPO3_FF_OEN	3	GPO3_FF output enable.	
	GPO2_FF_OEN	2	GPO2_FF output enable.	
	GPO1_FF_OEN	1	GPO1_FF output enable.	
	GPO0_FF_OEN	0	GPO0_FF output enable. 0: Output. 1: Close.	
6Eh (65B8h)	**REG65B8**	**7:0**	**Default: 0x00**	**Access : R/W**
	-	7	Reserved.	

TCON Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description
	GPO6_N_1_SEL	6	Select the signal which is used for GPO6 Combination Select (G6CS). (GPO6 n 1 select). 0: Use GPO5. 1: Use an always Low signal (1'b0).
	GPO5_N_1_SEL	5	Select the signal which is used for GPO5 Combination Select (G5CS). (GPO5 n 1 select). 0: Use GPO4. 1: Use an always Low signal (1'b0).
	GPO4_N_1_SEL	4	Select the signal which is used for GPO4 Combination Select (G4CS). (GPO4 n 1 select). 0: Use GPO3. 1: Use an always Low signal (1'b0).
	GPO3_N_1_SEL	3	Select the signal which is used for GPO3 Combination Select (G3CS). (GPO3 n 1 select). 0: Use GPO2. 1: Use an always Low signal (1'b0).
	GPO2_N_1_SEL	2	Select the signal which is used for GPO2 Combination Select (G2CS). (GPO2 n 1 select). 0: Use GPO1. 1: Use an always Low signal (1'b0).
	GPO1_N_1_SEL	1	Select the signal which is used for GPO1 Combination Select (G1CS). (GPO1 n 1 select). 0: Use GPO0. 1: Use an always Low signal (1'b0).
	GPO0_N_1_SEL	0	Select the signal which is used for GPO0 Combination Select (G0CS). (GPO0 n 1 select). 0: Use GPOD. 1: Use an always Low signal (1'b0).
76h (65D8h)	**REG65D8**	**7:0**	**Default: 0x00** **Access : R/W**
	GPO3_STH_SEL[1:0]	7:6	Gpo3 sth pulse width select.
	GPO2_STH_SEL[1:0]	5:4	Gpo2 sth pulse width select.

TCON Register (Bank = 32)

Index (Absolute)	Mnemonic	Bit	Description	
	GPO1_STH_SEL[1:0]	3:2	Gpo1 sth pulse width select.	
	GPO0_STH_SEL[1:0]	1:0	Gpo0 sth pulse width select. 00: 1T positive clock sample (gpo_pos). 01: 1T negative clock sample (gpo_neg). 10: 1.5T positive clock sample (gpo_pos | gpo_neg). 11: 1.5T negative clock sample (gpo_neg | gpo_2nd).	
76h (65D9h)	**REG65D9**	**7:0**	**Default: 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	GPO6_STH_SEL[1:0]	5:4	Gpo6 sth pulse width select.	
	GPO5_STH_SEL[1:0]	3:2	Gpo5 sth pulse width select.	
	GPO4_STH_SEL[1:0]	1:0	Gpo4 sth pulse width select.	
79h (65E4h)	**REG65E4**	**7:0**	**Default: 0x01**	**Access : R/W**
	-	7	Reserved.	
	G6AT	6	GPO6 Auto Toggle for POL. 0: Disable. 1: Enable.	
	G5AT	5	GPO5 Auto Toggle for POL. 0: Disable. 1: Enable.	
	G4AT	4	GPO4 Auto Toggle for POL. 0: Disable. 1: Enable.	
	G3AT	3	GPO3 Auto Toggle for POL. 0: Disable. 1: Enable.	
	G2AT	2	GPO2 Auto Toggle for POL. 0: Disable. 1: Enable.	
	G1AT	1	GPO1 Auto Toggle for POL. 0: Disable. 1: Enable.	
	G0AT	0	GPO0 Auto Toggle for POL. 0: Disable. 1: Enable.	
7Fh (65FCh)	**REG65FC**	**7:0**	**Default: 0x00**	**Access : R/W**
	TC_DUMMY0[7:0]	7:0	Dummy register.	

TCON Register (Bank = 32)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
7Fh (65FDh)	**REG65FD**	**7:0**	**Default: 0x00**	**Access : R/W**
	TC_DUMMY0[15:8]	7:0	See description of '65FCh'.	

MAILBOX Register (Bank = 33)

MAILBOX Register (Bank = 33)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
40h (6700h)	**REG6700**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_0[7:0]	7:0	MAILBOX_0.	
40h (6701h)	**REG6701**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_0[15:8]	7:0	See description of '6700h'.	
41h (6704h)	**REG6704**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_1[7:0]	7:0	MAILBOX_1.	
41h (6705h)	**REG6705**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_1[15:8]	7:0	See description of '6704h'.	
42h (6708h)	**REG6708**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_2[7:0]	7:0	MAILBOX_2.	
42h (6709h)	**REG6709**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_2[15:8]	7:0	See description of '6708h'.	
43h (670Ch)	**REG670C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_3[7:0]	7:0	MAILBOX_3.	
43h (670Dh)	**REG670D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_3[15:8]	7:0	See description of '670Ch'.	
44h (6710h)	**REG6710**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_4[7:0]	7:0	MAILBOX_4.	
44h (6711h)	**REG6711**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_4[15:8]	7:0	See description of '6710h'.	
45h (6714h)	**REG6714**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_5[7:0]	7:0	MAILBOX_5.	
45h (6715h)	**REG6715**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_5[15:8]	7:0	See description of '6714h'.	
46h (6718h)	**REG6718**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_6[7:0]	7:0	MAILBOX_6.	
46h (6719h)	**REG6719**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_6[15:8]	7:0	See description of '6718h'.	
47h (671Ch)	**REG671C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_7[7:0]	7:0	MAILBOX_7.	
47h	**REG671D**	**7:0**	**Default : 0x00**	**Access : R/W**

MAILBOX Register (Bank = 33)

Index (Absolute)	Mnemonic	Bit	Description	
(671Dh)	MB0_7[15:8]	7:0	See description of '671Ch'.	
48h (6720h)	**REG6720**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_8[7:0]	7:0	MAILBOX_8.	
48h (6721h)	**REG6721**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_8[15:8]	7:0	See description of '6720h'.	
49h (6724h)	**REG6724**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_9[7:0]	7:0	MAILBOX_9.	
49h (6725h)	**REG6725**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_9[15:8]	7:0	See description of '6724h'.	
4Ah (6728h)	**REG6728**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_A[7:0]	7:0	MAILBOX_10.	
4Ah (6729h)	**REG6729**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_A[15:8]	7:0	See description of '6728h'.	
4Bh (672Ch)	**REG672C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_B[7:0]	7:0	MAILBOX_11.	
4Bh (672Dh)	**REG672D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_B[15:8]	7:0	See description of '672Ch'.	
4Ch (6730h)	**REG6730**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_C[7:0]	7:0	MAILBOX_12.	
4Ch (6731h)	**REG6731**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_C[15:8]	7:0	See description of '6730h'.	
4Dh (6734h)	**REG6734**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_D[7:0]	7:0	MAILBOX_13.	
4Dh (6735h)	**REG6735**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_D[15:8]	7:0	See description of '6734h'.	
4Eh (6738h)	**REG6738**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_E[7:0]	7:0	MAILBOX_14.	
4Eh (6739h)	**REG6739**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_E[15:8]	7:0	See description of '6738h'.	
4Fh (673Ch)	**REG673C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_F[7:0]	7:0	MAILBOX_15.	
4Fh (673Dh)	**REG673D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_F[15:8]	7:0	See description of '673Ch'.	

MAILBOX Register (Bank = 33)

Index (Absolute)	Mnemonic	Bit	Description	
50h (6740h)	**REG6740**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_10[7:0]	7:0	MAILBOX_16.	
50h (6741h)	**REG6741**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_10[15:8]	7:0	See description of '6740h'.	
51h (6744h)	**REG6744**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_11[7:0]	7:0	MAILBOX_17.	
51h (6745h)	**REG6745**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_11[15:8]	7:0	See description of '6744h'.	
52h (6748h)	**REG6748**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_12[7:0]	7:0	MAILBOX_18.	
52h (6749h)	**REG6749**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_12[15:8]	7:0	See description of '6748h'.	
53h (674Ch)	**REG674C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_13[7:0]	7:0	MAILBOX_19.	
53h (674Dh)	**REG674D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_13[15:8]	7:0	See description of '674Ch'.	
54h (6750h)	**REG6750**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_14[7:0]	7:0	MAILBOX_20.	
54h (6751h)	**REG6751**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_14[15:8]	7:0	See description of '6750h'.	
55h (6754h)	**REG6754**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_15[7:0]	7:0	MAILBOX_21.	
55h (6755h)	**REG6755**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_15[15:8]	7:0	See description of '6754h'.	
56h (6758h)	**REG6758**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_16[7:0]	7:0	MAILBOX_22.	
56h (6759h)	**REG6759**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_16[15:8]	7:0	See description of '6758h'.	
57h (675Ch)	**REG675C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_17[7:0]	7:0	MAILBOX_23.	
57h (675Dh)	**REG675D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_17[15:8]	7:0	See description of '675Ch'.	
58h	**REG6760**	**7:0**	**Default : 0x00**	**Access : R/W**

MAILBOX Register (Bank = 33)

Index (Absolute)	Mnemonic	Bit	Description	
(6760h)	MB0_18[7:0]	7:0	MAILBOX_24.	
58h (6761h)	**REG6761**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_18[15:8]	7:0	See description of '6760h'.	
59h (6764h)	**REG6764**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_19[7:0]	7:0	MAILBOX_25.	
59h (6765h)	**REG6765**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_19[15:8]	7:0	See description of '6764h'.	
5Ah (6768h)	**REG6768**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_1A[7:0]	7:0	MAILBOX_26.	
5Ah (6769h)	**REG6769**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_1A[15:8]	7:0	See description of '6768h'.	
5Bh (676Ch)	**REG676C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_1B[7:0]	7:0	MAILBOX_27.	
5Bh (676Dh)	**REG676D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_1B[15:8]	7:0	See description of '676Ch'.	
5Ch (6770h)	**REG6770**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_1C[7:0]	7:0	MAILBOX_28.	
5Ch (6771h)	**REG6771**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_1C[15:8]	7:0	See description of '6770h'.	
5Dh (6774h)	**REG6774**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_1D[7:0]	7:0	MAILBOX_29.	
5Dh (6775h)	**REG6775**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_1D[15:8]	7:0	See description of '6774h'.	
5Eh (6778h)	**REG6778**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_1E[7:0]	7:0	MAILBOX_30.	
5Eh (6779h)	**REG6779**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_1E[15:8]	7:0	See description of '6778h'.	
5Fh (677Ch)	**REG677C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_1F[7:0]	7:0	MAILBOX_31.	
5Fh (677Dh)	**REG677D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_1F[15:8]	7:0	See description of '677Ch'.	
60h (6780h)	**REG6780**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_20[7:0]	7:0	MAILBOX_32.	

MAILBOX Register (Bank = 33)

Index (Absolute)	Mnemonic	Bit	Description	
60h (6781h)	**REG6781**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_20[15:8]	7:0	See description of '6780h'.	
61h (6784h)	**REG6784**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_21[7:0]	7:0	MAILBOX_33.	
61h (6785h)	**REG6785**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_21[15:8]	7:0	See description of '6784h'.	
62h (6788h)	**REG6788**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_22[7:0]	7:0	MAILBOX_34.	
62h (6789h)	**REG6789**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_22[15:8]	7:0	See description of '6788h'.	
63h (678Ch)	**REG678C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_23[7:0]	7:0	MAILBOX_35.	
63h (678Dh)	**REG678D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_23[15:8]	7:0	See description of '678Ch'.	
64h (6790h)	**REG6790**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_24[7:0]	7:0	MAILBOX_36.	
64h (6791h)	**REG6791**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_24[15:8]	7:0	See description of '6790h'.	
65h (6794h)	**REG6794**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_25[7:0]	7:0	MAILBOX_37.	
65h (6795h)	**REG6795**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_25[15:8]	7:0	See description of '6794h'.	
66h (6798h)	**REG6798**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_26[7:0]	7:0	MAILBOX_38.	
66h (6799h)	**REG6799**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_26[15:8]	7:0	See description of '6798h'.	
67h (679Ch)	**REG679C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_27[7:0]	7:0	MAILBOX_39.	
67h (679Dh)	**REG679D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_27[15:8]	7:0	See description of '679Ch'.	
68h (67A0h)	**REG67A0**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_28[7:0]	7:0	MAILBOX_40.	
68h	**REG67A1**	**7:0**	**Default : 0x00**	**Access : R/W**

MAILBOX Register (Bank = 33)

Index (Absolute)	Mnemonic	Bit	Description	
(67A1h)	MB0_28[15:8]	7:0	See description of '67A0h'.	
69h (67A4h)	**REG67A4**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_29[7:0]	7:0	MAILBOX_41.	
69h (67A5h)	**REG67A5**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_29[15:8]	7:0	See description of '67A4h'.	
6Ah (67A8h)	**REG67A8**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_2A[7:0]	7:0	MAILBOX_42.	
6Ah (67A9h)	**REG67A9**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_2A[15:8]	7:0	See description of '67A8h'.	
6Bh (67ACh)	**REG67AC**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_2B[7:0]	7:0	MAILBOX_43.	
6Bh (67ADh)	**REG67AD**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_2B[15:8]	7:0	See description of '67ACh'.	
6Ch (67B0h)	**REG67B0**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_2C[7:0]	7:0	MAILBOX_44.	
6Ch (67B1h)	**REG67B1**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_2C[15:8]	7:0	See description of '67B0h'.	
6Dh (67B4h)	**REG67B4**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_2D[7:0]	7:0	MAILBOX_45.	
6Dh (67B5h)	**REG67B5**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_2D[15:8]	7:0	See description of '67B4h'.	
6Eh (67B8h)	**REG67B8**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_2E[7:0]	7:0	MAILBOX_46.	
6Eh (67B9h)	**REG67B9**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_2E[15:8]	7:0	See description of '67B8h'.	
6Fh (67BCh)	**REG67BC**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_2F[7:0]	7:0	MAILBOX_47.	
6Fh (67BDh)	**REG67BD**	**7:0**	**Default : 0x00**	**Access : R/W**
	MB0_2F[15:8]	7:0	See description of '67BCh'.	

SEMAPHORE Register (Bank = 34)

SEMAPHORE Register (Bank = 34)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (6800h)	**REG6800**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEMA_0[7:0]	7:0	SEMA_0[15:2]. Reserve. SEMA_0[1:0]. 2'b00: clear. 2'b01: ID1. 2'b10: ID2. 2'b11: ID3.	
00h (6801h)	**REG6801**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEMA_0[15:8]	7:0	See description of '6800h'.	
01h (6804h)	**REG6804**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEMA_1[7:0]	7:0	SEMA_1[15:2]. Reserve. SEMA_1[1:0]. 2'b00: clear. 2'b01: ID1. 2'b10: ID2. 2'b11: ID3.	
01h (6805h)	**REG6805**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEMA_1[15:8]	7:0	See description of '6804h'.	
02h (6808h)	**REG6808**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEMA_2[7:0]	7:0	SEMA_2[15:2]. Reserve. SEMA_2[1:0]. 2'b00: clear. 2'b01: ID1. 2'b10: ID2. 2'b11: ID3.	
02h (6809h)	**REG6809**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEMA_2[15:8]	7:0	See description of '6808h'.	
03h	**REG680C**	**7:0**	**Default : 0x00**	**Access : R/W**

SEMAPHORE Register (Bank = 34)

Index (Absolute)	Mnemonic	Bit	Description	
(680Ch)	SEMA_3[7:0]	7:0	SEMA_3[15:2]. Reserve. SEMA_3[1:0]. 2'b00: clear. 2'b01: ID1. 2'b10: ID2. 2'b11: ID3.	
03h (680Dh)	**REG680D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEMA_3[15:8]	7:0	See description of '680Ch'.	
04h (6810h)	**REG6810**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEMA_4[7:0]	7:0	SEMA_4[15:2]. Reserve. SEMA_4[1:0]. 2'b00: clear. 2'b01: ID1. 2'b10: ID2. 2'b11: ID3.	
04h (6811h)	**REG6811**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEMA_4[15:8]	7:0	See description of '6810h'.	
05h (6814h)	**REG6814**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEMA_5[7:0]	7:0	SEMA_5[15:2]. Reserve. SEMA_5[1:0]. 2'b00: clear. 2'b01: ID1. 2'b10: ID2. 2'b11: ID3.	
05h (6815h)	**REG6815**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEMA_5[15:8]	7:0	See description of '6814h'.	
06h (6818h)	**REG6818**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEMA_6[7:0]	7:0	SEMA_6[15:2]. Reserve. SEMA_6[1:0]. 2'b00: clear. 2'b01: ID1. 2'b10: ID2. 2'b11: ID3.	

SEMAPHORE Register (Bank = 34)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
06h (6819h)	**REG6819**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEMA_6[15:8]	7:0	See description of '6818h'.	
07h (681Ch)	**REG681C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEMA_7[7:0]	7:0	SEMA_7[15:2]. Reserve. SEMA_7[1:0]. 2'b00: clear. 2'b01: ID1. 2'b10: ID2. 2'b11: ID3.	
07h (681Dh)	**REG681D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEMA_7[15:8]	7:0	See description of '681Ch'.	

MI2C Register (Bank = 34)

MI2C Register (Bank = 34)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (6840h)	**REG6840**	**7:0**	**Default : 0x01**	**Access : WO**
	-	7:1	Reserved.	
	MI2C_SW_RST	0	Master i2c software reset.	
1Dh (6874h)	**REG6874**	**7:0**	**Default : 0x00**	**Access : R/W**
	MI2C_DATA[7:0]	7:0	I2CDAT (I2C transmit data).	
1Dh (6875h)	**REG6875**	**7:0**	**Default : 0x00**	**Access : R/W**
	MI2C_ADDRESS[7:0]	7:0	I2CADR.	
1Eh (6878h)	**REG6878**	**7:0**	**Default : 0x00**	**Access : R/W**
	MI2C_COMMAND[7:0]	7:0	I2CCON (I2C command register). 0: Cr0. 1: Cr1. 2: Acknowledge bit. 3: Si (Interrupt flag). 4: 1->Stop. 5: 1->Start. 6: 1->i2c enable, 0->i2c disable. 7: Cr2.	
1Eh (6879h)	**REG6879**	**7:0**	**Default : 0x00**	**Access : RO**
	MI2C_STATE[7:0]	7:0	I2CSTA (I2C state register).	

PWM Register (Bank = 34)

PWM Register (Bank = 34)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
21h (6884h)	**REG6884**	**7:0**	**Default : 0xFF**	**Access : R/W**
	UNIT_DIV[7:0]	7:0	Pwm clock unit divider.	
21h (6885h)	**REG6885**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM_RST_CNT	7	Reset all pwm counters, high active.	
	PWM_CLR_ERR	6	Clear all pwm reset error flags.	
	-	5:1	Reserved.	
	SYNC_PULSE_SEL	0	Reset signal pulse selection 0: falling edge 1: rising edge.	
22h (6888h)	**REG6888**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM0_PERIOD[7:0]	7:0	Pwm0 period.	
22h (6889h)	**REG6889**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PWM0_PERIOD[9:8]	1:0	See description of '6888h'.	
23h (688Ch)	**REG688C**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM0_DUTY[7:0]	7:0	Pwm0 duty.	
23h (688Dh)	**REG688D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PWM0_DUTY[9:8]	1:0	See description of '688Ch'.	
24h (6890h)	**REG6890**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM0_DIV[7:0]	7:0	Pwm0 divider.	
24h (6891h)	**REG6891**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	PWM0_RST_DIV_ERR	7		
	PWM0_RST_PRD_ERR	6		
	PWM0_RST_PWM_ERR	5		
	PWM0_EN	4	Pwm0 enable.	
	PWM0_DBEN	3	Pwm0 double enable.	
	PWM0_RESET_EN	2	Pwm0 vsync reset0.	
	PWM0_VDBEN	1	Pwm0_vsync_double_enable.	
	PWM0_POLARITY	0	PWM0_POLARITY.	
25h (6894h)	**REG6894**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM1_PERIOD[7:0]	7:0	Pwm1 period.	
25h	**REG6895**	**7:0**	**Default : 0x00**	**Access : R/W**

PWM Register (Bank = 34)

Index (Absolute)	Mnemonic	Bit	Description	
(6895h)	-	7:2	Reserved.	
	PWM1_PERIOD[9:8]	1:0	See description of '6894h'.	
26h (6898h)	**REG6898**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM1_DUTY[7:0]	7:0	Pwm1 duty.	
26h (6899h)	**REG6899**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PWM1_DUTY[9:8]	1:0	See description of '6898h'.	
27h (689Ch)	**REG689C**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM1_DIV[7:0]	7:0	Pwm1 divider.	
27h (689Dh)	**REG689D**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	PWM1_RST_DIV_ERR	7		
	PWM1_RST_PRD_ERR	6		
	PWM1_RST_PWM_ERR	5		
	PWM1_EN	4	Pwm1 enable.	
	PWM1_DBEN	3	Pwm1 double enable.	
	PWM1_RESET_EN	2	Pwm1 vsync reset0.	
	PWM1_VDBEN	1	Pwm1_vsync_double_enable.	
	PWM1_POLARITY	0	PWM1_POLARITY.	
28h (68A0h)	**REG68A0**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM2_PERIOD[7:0]	7:0	Pwm2 period.	
28h (68A1h)	**REG68A1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PWM2_PERIOD[9:8]	1:0	See description of '68A0h'.	
29h (68A4h)	**REG68A4**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM2_DUTY[7:0]	7:0	Pwm2 duty.	
29h (68A5h)	**REG68A5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PWM2_DUTY[9:8]	1:0	See description of '68A4h'.	
2Ah (68A8h)	**REG68A8**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM2_DIV[7:0]	7:0	Pwm2 divider.	
2Ah (68A9h)	**REG68A9**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	PWM2_RST_DIV_ERR	7		
	PWM2_RST_PRD_ERR	6		

PWM Register (Bank = 34)

Index (Absolute)	Mnemonic	Bit	Description	
	PWM2_RST_PWM_ERR	5		
	PWM2_EN	4	Pwm2 enable.	
	PWM2_DBEN	3	Pwm2 double enable.	
	PWM2_RESET_EN	2	Pwm2 vsync reset0.	
	PWM2_VDBEN	1	Pwm2_vsync_double_enable.	
	PWM2_POLARITY	0	PWM2_POLARITY.	
2Bh (68ACh)	**REG68AC**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM3_PERIOD[7:0]	7:0	Pwm3 period.	
2Bh (68ADh)	**REG68AD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PWM3_PERIOD[9:8]	1:0	See description of '68ACh'.	
2Ch (68B0h)	**REG68B0**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM3_DUTY[7:0]	7:0	Pwm3 duty.	
2Ch (68B1h)	**REG68B1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PWM3_DUTY[9:8]	1:0	See description of '68B0h'.	
2Dh (68B4h)	**REG68B4**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM3_DIV[7:0]	7:0	Pwm3 divider.	
2Dh (68B5h)	**REG68B5**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	PWM3_RST_DIV_ERR	7		
	PWM3_RST_PRD_ERR	6		
	PWM3_RST_PWM_ERR	5		
	PWM3_EN	4	Pwm3 enable.	
	PWM3_DBEN	3	Pwm3 double enable.	
	PWM3_RESET_EN	2	Pwm3 vsync reset0.	
	PWM3_VDBEN	1	Pwm3_vsync_double_enable.	
	PWM3_POLARITY	0	PWM3_POLARITY.	
2Eh (68B8h)	**REG68B8**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM4_PERIOD[7:0]	7:0	Pwm4 period.	
2Eh (68B9h)	**REG68B9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PWM4_PERIOD[9:8]	1:0	See description of '68B8h'.	
2Fh	**REG68BC**	**7:0**	**Default : 0x00**	**Access : R/W**

PWM Register (Bank = 34)

Index (Absolute)	Mnemonic	Bit	Description	
(68BCh)	PWM4_DUTY[7:0]	7:0	Pwm4 duty.	
2Fh (68BDh)	**REG68BD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PWM4_DUTY[9:8]	1:0	See description of '68BCh'.	
30h (68C0h)	**REG68C0**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM4_DIV[7:0]	7:0	Pwm4 divider.	
30h (68C1h)	**REG68C1**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	PWM4_RST_DIV_ERR	7		
	PWM4_RST_PRD_ERR	6		
	PWM4_RST_PWM_ERR	5		
	PWM4_EN	4	Pwm4 enable.	
	PWM4_DBEN	3	Pwm4 double enable.	
	PWM4_RESET_EN	2	Pwm4 vsync reset0.	
	PWM4_VDBEN	1	Pwm4_vsync_double_enable.	
	PWM4_POLARITY	0	PWM4_POLARITY.	
31h (68C4h)	**REG68C4**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM5_PERIOD[7:0]	7:0	Pwm5 period.	
31h (68C5h)	**REG68C5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PWM5_PERIOD[9:8]	1:0	See description of '68C4h'.	
32h (68C8h)	**REG68C8**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM5_DUTY[7:0]	7:0	Pwm5 duty.	
32h (68C9h)	**REG68C9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PWM5_DUTY[9:8]	1:0	See description of '68C8h'.	
33h (68CCh)	**REG68CC**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM5_DIV[7:0]	7:0	Pwm5 divider.	
33h (68CDh)	**REG68CD**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	PWM5_RST_DIV_ERR	7		
	PWM5_RST_PRD_ERR	6		
	PWM5_RST_PWM_ERR	5		
	PWM5_EN	4	Pwm5 enable.	
	PWM5_DBEN	3	Pwm5 double enable.	

PWM Register (Bank = 34)

Index (Absolute)	Mnemonic	Bit	Description	
	PWM5_RESET_EN	2	Pwm5 vsync reset0.	
	PWM5_VDBEN	1	Pwm5_vsync_double_enable.	
	PWM5_POLARITY	0	PWM5_POLARITY.	
34h (68D0h)	**REG68D0**	**7:0**	**Default : 0x00**	**Access : R/W**
	RST_MUX1	7	Pwm1 reset mux.	
	-	6:4	Reserved.	
	HS_RST_CNT1[3:0]	3:0	Pwm1 hsync reset counter.	
34h (68D1h)	**REG68D1**	**7:0**	**Default : 0x00**	**Access : R/W**
	RST_MUX0	7	Pwm0 reset mux.	
	-	6:4	Reserved.	
	HS_RST_CNT0[3:0]	3:0	Pwm0 hsync reset counter.	
35h (68D4h)	**REG68D4**	**7:0**	**Default : 0x00**	**Access : R/W**
	RST_MUX3	7	Pwm3 reset mux.	
	-	6:4	Reserved.	
	HS_RST_CNT3[3:0]	3:0	Pwm3 hsync reset counter.	
35h (68D5h)	**REG68D5**	**7:0**	**Default : 0x00**	**Access : R/W**
	RST_MUX2	7	Pwm2 reset mux.	
	-	6:4	Reserved.	
	HS_RST_CNT2[3:0]	3:0	Pwm2 hsync reset counter.	
36h (68D8h)	**REG68D8**	**7:0**	**Default : 0x00**	**Access : R/W**
	RST_MUX5	7	Pwm5 reset mux.	
	-	6:4	Reserved.	
	HS_RST_CNT5[3:0]	3:0	Pwm5 hsync reset counter.	
36h (68D9h)	**REG68D9**	**7:0**	**Default : 0x00**	**Access : R/W**
	RST_MUX4	7	Pwm4 reset mux.	
	-	6:4	Reserved.	
	HS_RST_CNT4[3:0]	3:0	Pwm4 hsync reset counter.	

WDT Register (Bank = 34)

WDT Register (Bank = 34)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
60h (6980h)	**REG6980**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	WDT_CLR	0	Write "1' to re-start WDT.	
62h (6988h)	**REG6988**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	WDT_RST_FLAG	0	Assert: WDT reset has been occurred;. Write "1" to clear.	
62h (6989h)	**REG6989**	**7:0**	**Default : 0x09**	**Access : R/W**
	WDT_RST_LEN[7:0]	7:0	Length of WDT reset. 0: One xtal clock; 1: two xtal clock; 3.....	
63h (698Ch)	**REG698C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	WDT_INT[7:0]	7:0	WDT interrupt period;. Interrupt asserts when "WDT counter [31:16]" is equal to WDT_INT and "WDT counter [15:0]" is equal to 0x0000.	
63h (698Dh)	**REG698D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	WDT_INT[15:8]	7:0	See description of '698Ch'.	
64h (6990h)	**REG6990**	**7:0**	**Default : 0xFF**	**Access : R/W**
	WDT_MAX[7:0]	7:0	WDT period maximum value. WDT enable if WDT_MAX is not equal to 0x00000000.	
64h (6991h)	**REG6991**	**7:0**	**Default : 0xFF**	**Access : R/W**
	WDT_MAX[15:8]	7:0	See description of '6990h'.	
65h (6994h)	**REG6994**	**7:0**	**Default : 0xFF**	**Access : R/W**
	WDT_MAX[23:16]	7:0	See description of '6990h'.	
65h (6995h)	**REG6995**	**7:0**	**Default : 0xFF**	**Access : R/W**
	WDT_MAX[31:24]	7:0	See description of '6990h'.	

TIMER0 Register (Bank = 34)

TIMER0 Register (Bank = 34)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
70h (69C0h)	**REG69C0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	TIMER_TRIG	1	Set: Enable timer counting one time (from 0 to max, then stop). Clear: By reset itself OR set reg_timer_en.	
	TIMER_EN	0	Set: Enable timer counting rolled (from 0 to max, then rolled). Clear: By reset itself OR set reg_timer_trig.	
70h (69C1h)	**REG69C1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	TIMER_INT_EN	0	Set: Enable interrupt. Clear: By reset itself.	
71h (69C4h)	**REG69C4**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	TIMER_HIT	0	Assert: When counter enabled and matches reg_timer_max. Deassert: By write 1 OR set reg_timer_en, reg_timer_once, reg_timer_max.	
72h (69C8h)	**REG69C8**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TIMER_MAX[7:0]	7:0	Timer maximum value.	
72h (69C9h)	**REG69C9**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TIMER_MAX[15:8]	7:0	See description of '69C8h'.	
73h (69CCh)	**REG69CC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TIMER_MAX[23:16]	7:0	See description of '69C8h'.	
73h (69CDh)	**REG69CD**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TIMER_MAX[31:24]	7:0	See description of '69C8h'.	
74h (69D0h)	**REG69D0**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CAP[7:0]	7:0	Timer current value. Note: With non-32-bit-data system, please read from LSB.	
74h (69D1h)	**REG69D1**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CAP[15:8]	7:0	See description of '69D0h'.	
75h (69D4h)	**REG69D4**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CAP[23:16]	7:0	See description of '69D0h'.	

TIMER0 Register (Bank = 34)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
75h (69D5h)	**REG69D5**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CAP[31:24]	7:0	See description of '69D0h'.	

GOP Register (Bank = 35)

GOP2G_0 Register (Bank = 35, Sub-Bank = 03)

GOP2G_0 Register (Bank = 35, Sub-Bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (6A00h)	**REG6A00**	**7:0**	**Default : 0x09**	**Access : R/W**
	5541_EN	7	RGB5541 alpha mask mode enable, only for RGB1555 Data type.	
	-	6:5	Reserved.	
	GWIN_FLD_INV	4	Input Field inverse.	
	GWIN_PROG_MD	3	GWINs display mode. 0: Interlace. 1: Progress.	
	GWIN_HS_INV	2	Input Hsync inverse.	
	GWIN_VS_INV	1	Input Vsync inverse.	
	GWIN_RST	0	GOP soft reset.	
00h (6A01h)	**REG6A01**	**7:0**	**Default : 0x42**	**Access : R/W**
	ALPHA_INV	7	Alpha out inverse.	
	HS_MASK	6	1: Mask Hsync when VFDE is low. 0: No mask.	
	DISP_VBACK	5	V line read out direction 0: down 1:up.	
	DISP_HBACK	4	H pixel read out direction 0: forward 1:back.	
	TRS_EN	3	Transparent color enable.	
	GWIN_YUVOUT	2	GOP out format. 0: RGB 1: VYU.	
	GENSHOT_FAST	1	Genshot fast.	
	OUT_RDY	0	Output ready.	
01h (6A04h)	**REG6A04**	**7:0**	**Default : 0x14**	**Access : R/W**
	GWIN1_PINPON	7	GWIN1 PINPON mode (with G3D).	
	-	6	Reserved.	
	HI_TSH[1:0]	5:4	MIU access high priority threshold.	
	DMA_EXT[1:0]	3:2	GOP DMA Burst length. 0: 8 1: 16 2: 32 3: all.	
	GWIN_DEST[1:0]	1:0	GOP destination. 0: IP_0, 1: reserved, 2: OP, 3: MVOP.	
01h (6A05h)	**REG6A05**	**7:0**	**Default : 0xA0**	**Access : R/W**
	RI_END[3:0]	7:4	Regdma interval end.	

GOP2G_0 Register (Bank = 35, Sub-Bank = 03)

Index (Absolute)	Mnemonic	Bit	Description	
	RI_STR[3:0]	3:0	Regdma interval start.	
02h (6A08h)	**REG6A08**	**7:0**	**Default : 0x80**	**Access : R/W**
	DMA_THD[1:0]	7:6	DMA FIFO threshold. 0: 80, 1: 96, 2: 112, 3: 120.	
	-	5:0	Reserved.	
02h (6A09h)	**REG6A09**	**7:0**	**Default : 0x0F**	**Access : R/W**
	BLINK_EN	7	Blink enable.	
	BLINK_RATE[6:0]	6:0	Blink toggle duration.	
08h (6A20h)	**REG6A20**	**7:0**	**Default : 0x33**	**Access : R/W**
	-	7:2	Reserved.	
	VS1_INT_MASK	1	Vs1 interrupt mask.	
	VS0_INT_MASK	0	Vs0 interrupt mask.	
08h (6A21h)	**REG6A21**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	VS1_INT	1	Vs1 interrupt flag.	
	VS0_INT	0	Vs0 interrupt flag.	
09h (6A24h)	**REG6A24**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	RD_FLAG	3	PINPON flag.	
	RDMA_STATE[2:0]	2:0	RDMA state.	
09h (6A25h)	**REG6A25**	**7:0**	**Default : 0x00**	**Access : RO**
	LB1_BIST_FAIL	7	LB1 BIST.	
	LB0_BIST_FAIL	6	LB0 BIST.	
	-	5	Reserved.	
	GW_FF_BIST_FAIL	4	Buffer BIST.	
	LB_UF	3	Line buffer underflow.	
	LB_OF	2	Line buffer overflow.	
	GW_UF	1	Buffer underflow.	
	GW_OF	0	Buffer overflow.	
0Eh (6A38h)	**REG6A38**	**7:0**	**Default : 0x90**	**Access : R/W**
	RDMA_HT[7:0]	7:0	RDMA H total (unit: 2 pixels). RDMA_HT > MAX{GWINs_HEND}.	
0Eh	**REG6A39**	**7:0**	**Default : 0x00**	**Access : R/W**

GOP2G_0 Register (Bank = 35, Sub-Bank = 03)

Index (Absolute)	Mnemonic	Bit	Description	
(6A39h)	-	7:2	Reserved.	
	RDMA_HT[9:8]	1:0	See description of '6A38h'.	
0Fh (6A3Ch)	**REG6A3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	HS_PIPE[7:0]	7:0	Hsync input pipe delay.	
0Fh (6A3Dh)	**REG6A3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	HS_PIPE[9:8]	1:0	See description of '6A3Ch'.	
10h (6A40h)	**REG6A40**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SLOW_RATIO[5:0]	5:0	FIFO read out slow ratio.	
10h (6A41h)	**REG6A41**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SLOW_THD[6:0]	6:0	FIFO out speed slow down when data counts <= SLOW_THD.	
11h (6A44h)	**REG6A44**	**7:0**	**Default : 0x00**	**Access : R/W**
	BRI[7:0]	7:0	Brightness level: -256~255. BRI[8] is sign bit.	
11h (6A45h)	**REG6A45**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	BRI[8]	0	See description of '6A44h'.	
12h (6A48h)	**REG6A48**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	CON[5:0]	5:0	Contrast gain. Gain = CON / 16.	
13h (6A4Ch)	**REG6A4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_STR0[7:0]	7:0	Start address for pinpon buffer0.	
13h (6A4Dh)	**REG6A4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_STR0[15:8]	7:0	See description of '6A4Ch'.	
14h (6A50h)	**REG6A50**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_STR0[23:16]	7:0	See description of '6A4Ch'.	
14h (6A51h)	**REG6A51**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	DRAM_STR0[25:24]	1:0	See description of '6A4Ch'.	
15h	**REG6A54**	**7:0**	**Default : 0x00**	**Access : R/W**

GOP2G_0 Register (Bank = 35, Sub-Bank = 03)

Index (Absolute)	Mnemonic	Bit	Description	
(6A54h)	DRAM_STR1[7:0]	7:0	Start address for pinpon buffer1.	
15h (6A55h)	**REG6A55**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_STR1[15:8]	7:0	See description of '6A54h'.	
16h (6A58h)	**REG6A58**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_STR1[23:16]	7:0	See description of '6A54h'.	
16h (6A59h)	**REG6A59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	DRAM_STR1[25:24]	1:0	See description of '6A54h'.	
20h (6A80h)	**REG6A80**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	PRI0	0	1st priority GWIN number.	
24h (6A90h)	**REG6A90**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRS_CLR[7:0]	7:0	Transparent color key. For RGB domain only.	
24h (6A91h)	**REG6A91**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRS_CLR[15:8]	7:0	See description of '6A90h'.	
25h (6A94h)	**REG6A94**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRS_CLR[23:16]	7:0	See description of '6A90h'.	
30h (6AC0h)	**REG6AC0**	**7:0**	**Default : 0x40**	**Access : R/W**
	STRCH_HSIZE[7:0]	7:0	Stretch Window H size (unit: 2 pixel). When V stretch ratio=1, hsize has no size limit. When V stretch ratio !=1, the max hsize is limited by line buffer size.	
30h (6AC1h)	**REG6AC1**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:2	Reserved.	
	STRCH_HSIZE[9:8]	1:0	See description of '6AC0h'.	
31h (6AC4h)	**REG6AC4**	**7:0**	**Default : 0x68**	**Access : R/W**
	STRCH_VSIZE[7:0]	7:0	Stretch Window V size.	
31h (6AC5h)	**REG6AC5**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	STRCH_VSIZE[10:8]	2:0	See description of '6AC4h'.	
32h (6AC8h)	**REG6AC8**	**7:0**	**Default : 0x64**	**Access : R/W**
	STRCH_HST[7:0]	7:0	Stretch Window H coordinate.	

GOP2G_0 Register (Bank = 35, Sub-Bank = 03)

Index (Absolute)	Mnemonic	Bit	Description	
32h (6AC9h)	**REG6AC9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	STRCH_HST[11:8]	3:0	See description of '6AC8h'.	
34h (6AD0h)	**REG6AD0**	**7:0**	**Default : 0x00**	**Access : R/W**
	STRCH_VST[7:0]	7:0	Stretch Window V coordinate.	
34h (6AD1h)	**REG6AD1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	STRCH_VST[10:8]	2:0	See description of '6AD0h'.	
7Eh (6BF8h)	**REG6BF8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	GOPG0_MUX[1:0]	1:0	GOP GWIN output layer0 select. 1: GOP2G. Others: Reserved.	
7Fh (6BFCh)	**REG6BFC**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:6	Reserved.	
	GOP2G_INT	5	GOP2G INT FLAG.	
	-	4:3	Reserved.	
	GOP_BNK[2:0]	2:0	GOP BANK select. 3: GOP2G_0. 4: GOP2G_1. Others: Reserved.	
7Fh (6BFDh)	**REG6BFD**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:6	Reserved.	
	GOP2G_WR_ACK	5	GOP2G register write ACK.	
	-	4	Reserved.	
	GOP_FCLR	3	GOP FIFO flag clear.	
	GOP_BK_WR	2	GOP selected bank double buffer write (Sync. With Vsync).	
	GOP_FWR	1	GOP Registers force write in.	
	GOP_WR	0	GOP all banks double buffer write (Sync. With Vsync).	

GOP2G_1 Register (Bank = 35, Sub-Bank = 04)

GOP2G_1 Register (Bank = 35, Sub-Bank = 04)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (6A00h)	**REG6A00**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_DTYPE[3:0]	7:4	GWIN0 Source Data Type. 0: RGB1555 / Blink mode. 1: RGB565. 2: ARGB4444. 3: 2266. 4: 8- bit palette. 5: ARGB8888. 8: RGB1555/ YUV422. 9: YUV422. Each GWIN only one data type, the gwins with different Data wid.	
	-	3:1	Reserved.	
	GWIN0_EN	0	Graphic window 0 Enable.	
00h (6A01h)	**REG6A01**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_TILE_MD	7	Tile mode for GE3D and GE data format. 0: Linear; 1: Tile mode.	
	GWIN0_ALPHA_EN	6	GWIN0 alpha_enable. 1: Pixel alpha, 0: constant alpha.	
	GWIN0_ALPHA[5:0]	5:0	GWIN0 constant alpha. Img_Pix =Case. 0: SRC_PIX. 63: GWIN_PIX. Others :(alpha * GWIN_PIX + (64-alpha) * SRC_PIX)/64.	
01h (6A04h)	**REG6A04**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK0_STR[7:0]	7:0	Ring Block start address in dram for GWIN0 read out. Unit 1 word.	
01h (6A05h)	**REG6A05**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK0_STR[15:8]	7:0	See description of '6A04h'.	
02h (6A08h)	**REG6A08**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK0_STR[23:16]	7:0	See description of '6A04h'.	
02h (6A09h)	**REG6A09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	DRAM_RBLK0_STR[25:24]	1:0	See description of '6A04h'.	
04h	**REG6A10**	**7:0**	**Default : 0x00**	**Access : R/W**

GOP2G_1 Register (Bank = 35, Sub-Bank = 04)

Index (Absolute)	Mnemonic	Bit	Description	
(6A10h)	GWIN0_HSTR[7:0]	7:0	The horizontal start pixel of Display Image for. GWIN0. Unit: 1 word pixels.	
04h (6A11h)	**REG6A11**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	GWIN0_HSTR[9:8]	1:0	See description of '6A10h'.	
05h (6A14h)	**REG6A14**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_HEND[7:0]	7:0	The horizontal end pixel of Display Image for. GWIN0. Unit: 1 word pixels.	
05h (6A15h)	**REG6A15**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	GWIN0_HEND[9:8]	1:0	See description of '6A14h'.	
06h (6A18h)	**REG6A18**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_VSTR[7:0]	7:0	The vertical start line of Display Image for GWIN0 Unit: 1 line.	
06h (6A19h)	**REG6A19**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GWIN0_VSTR[10:8]	2:0	See description of '6A18h'.	
08h (6A20h)	**REG6A20**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN0_VEND[7:0]	7:0	The vertical end line of Display Image for GWIN0 Unit: 1 line.	
08h (6A21h)	**REG6A21**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GWIN0_VEND[10:8]	2:0	See description of '6A20h'.	
09h (6A24h)	**REG6A24**	**7:0**	**Default : 0x00**	**Access : R/W**
	RBLK0_HSIZE[7:0]	7:0	Ring Block0 line size.	
09h (6A25h)	**REG6A25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	RBLK0_HSIZE[9:8]	1:0	See description of '6A24h'.	
16h (6A58h)	**REG6A58**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	GWIN0_FADE_INC	6	FADE IN/OUT 1: stronger; 0: weaker.	
	GWIN0_FADE_INI	5	FADE Initial.	

GOP2G_1 Register (Bank = 35, Sub-Bank = 04)

Index (Absolute)	Mnemonic	Bit	Description	
	GWIN0_FADE_EN	4	FADE enable.	
	GWIN0_FADE0_RATE[3:0]	3:0	FADE frame rate for GWIN0.	
20h (6A80h)	**REG6A80**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN1_DTYPE[3:0]	7:4	GWIN1 Source Data Type.	
	-	3:1	Reserved.	
	GWIN1_EN	0	Graphic window 1 Enable.	
20h (6A81h)	**REG6A81**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN1_TILE_MD	7	Tile mode for GE3D and GE data format.	
	GWIN1_ALPHA_EN	6	GWIN1 alpha_enable. 1: Pixel alpha 0: constant alpha.	
	GWIN1_ALPHA[5:0]	5:0	GWIN1 constant alpha.	
21h (6A84h)	**REG6A84**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK1_STR[7:0]	7:0	Ring Block start address in dram for GWIN1 read out. Unit: 1 word.	
21h (6A85h)	**REG6A85**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK1_STR[15:8]	7:0	See description of '6A84h'.	
22h (6A88h)	**REG6A88**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_RBLK1_STR[23:16]	7:0	See description of '6A84h'.	
22h (6A89h)	**REG6A89**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	DRAM_RBLK1_STR[25:24]	1:0	See description of '6A84h'.	
24h (6A90h)	**REG6A90**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN1_HSTR[7:0]	7:0	The horizontal start pixel of Display Image for. GWIN1. Unit: 1 word pixels.	
24h (6A91h)	**REG6A91**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	GWIN1_HSTR[9:8]	1:0	See description of '6A90h'.	
25h (6A94h)	**REG6A94**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN1_HEND[7:0]	7:0	The horizontal end pixel of Display Image for. GWIN1. Unit: 1 word pixels.	
25h (6A95h)	**REG6A95**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	

GOP2G_1 Register (Bank = 35, Sub-Bank = 04)

Index (Absolute)	Mnemonic	Bit	Description	
	GWIN1_HEND[9:8]	1:0	See description of '6A94h'.	
26h (6A98h)	**REG6A98**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN1_VSTR[7:0]	7:0	The vertical start line of Display Image for GWIN1. Unit: 1 line.	
26h (6A99h)	**REG6A99**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GWIN1_VSTR[10:8]	2:0	See description of '6A98h'.	
28h (6AA0h)	**REG6AA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	GWIN1_VEND[7:0]	7:0	The vertical end line of Display Image for GWIN1 Unit: 1 line.	
28h (6AA1h)	**REG6AA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GWIN1_VEND[10:8]	2:0	See description of '6AA0h'.	
29h (6AA4h)	**REG6AA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	RBLK1_HSIZE[7:0]	7:0	Ring Block1 line size.	
29h (6AA5h)	**REG6AA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	RBLK1_HSIZE[9:8]	1:0	See description of '6AA4h'.	
36h (6AD8h)	**REG6AD8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	GWIN1_FADE_INC	6	FADE IN/OUT 1: stronger; 0: weaker.	
	GWIN1_FADE_INI	5	FADE Initial.	
	GWIN1_FADE_EN	4	FADE enable.	
	GWIN1_FADE_RATE[3:0]	3:0	FADE frame rate for GWIN1.	
7Eh (6BF8h)	**REG6BF8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	GOPG0_MUX[1:0]	1:0	GOP GWIN output layer0 select. 1: GOP2G. Others: Reserved.	
7Fh (6BFCh)	**REG6BFC**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:6	Reserved.	
	GOP2G_INT	5	GOP2G INT FLAG.	
	-	4:3	Reserved.	

GOP2G_1 Register (Bank = 35, Sub-Bank = 04)

Index (Absolute)	Mnemonic	Bit	Description	
	GOP_BNK[2:0]	2:0	GOP BANK select. 3: GOP2G_0. 4: GOP2G_1. Others: Reserved.	
7Fh (6BFDh)	**REG6BFD**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:6	Reserved.	
	GOP2G_WR_ACK	5	GOP2G register write ACK.	
	-	4	Reserved.	
	GOP_FCLR	3	GOP FIFO flag clear.	
	GOP_BK_WR	2	GOP selected bank double buffer write (Sync. With Vsync).	
	GOP_FWR	1	GOP Registers force write in.	
	GOP_WR	0	GOP all banks double buffer write (Sync. With Vsync).	

GE Register (Bank = 36)

GE Register (Bank = 36)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (6C00h)	**REG6C00**	**7:0**	**Default : 0x03**	**Access : R/W**
	EN_GE_DCK	7	Enable Destination Color Key. # 1'b0: Disable. # 1'b1: Enable.	
	EN_GE_SCK	6	Enable Source Color Key. # 1'b0: Disable. # 1'b1: Enable.	
	EN_GE_ROP	5	Enable ROP2. # 1'b0: Disable (This is equal to set reg_pe_rop2 = 4'hc). # 1'b1: Enable.	
	-	4:3	Reserved.	
	EN_GE_ABL	2	Enable Alpha Blending. # 1'b0: Disable. # 1'b1: Enable.	
	EN_GE_DITHER	1	Enable Dither. # 1'b0: Disable. # 1'b1: Enable.	
	EN_GE	0	Enable Pixel Engine. # 1 'b0: Disable and Reset to the Initial State. # 1 'b1: Enable.	
00h (6C01h)	**REG6C01**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	EN_GE_DSTAC	4	Enable Destination Alpha Comparison. # 1'b0: Disable. # 1'b1: Enable.	
	EN_GE_ALPHA_CMP	3	Enable Alpha Comparison. # 1'b0: Disable. # 1'b1: Enable.	
	-	2	Reserved.	
	EN_GE_RANDOM_NOISE	1	Enable Random Noise. # 1'b0: Disable. # 1'b1: Enable.	
	EN_GE_LPT	0	Enable Line Pattern Test. # 1'b0: Disable. # 1'b1: Enable.	

GE Register (Bank = 36)

Index (Absolute)	Mnemonic	Bit	Description	
01h (6C04h)	**REG6C04**	**7:0**	**Default : 0x01**	**Access : R/W**
	EN_GE_LENGTH_LIMIT	7	Enable Length Limitation. # 1'b0: Disable. # 1'b1: Enable.	
	EN_GE_ITC	6	Enable Italic Font. # 1'b0: Disable. # 1'b1: Enable.	
	EN_GE_CLIP_CHK	5	Enable Clipping Check. # 1'b0: Disable. # 1'b1: Enable.	
	-	4:1	Reserved.	
	EN_GE_CMQ	0	Enable Command Queue. # 1'b0: Disable Command Queue. # 1'b1: Enable.	
01h (6C05h)	**REG6C05**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	EN_GE_D_TILE_ADDR	1	Enable Destination Tile (Swizzle) Address Mode. # 1'b0: Disable. # 1'b1: Enable.	
	EN_GE_S_TILE_ADDR	0	Enable Source Tile (Swizzle) Address Mode. # 1'b0: Disable. # 1'b1: Enable.	
03h (6C0Ch)	**REG6C0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	GE_STBB_TH[4:0]	4:0	Reading Source Threshold.	
0Fh (6C3Ch)	**REG6C3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_TAG[7:0]	7:0	Tag Register.	
0Fh (6C3Dh)	**REG6C3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_TAG[15:8]	7:0	See description of '6C3Ch'.	
10h (6C40h)	**REG6C40**	**7:0**	**Default : 0x0C**	**Access : R/W**
	-	7:4	Reserved.	
	GE_ROP2[3:0]	3:0	Raster Operation ROP2.	
11h (6C44h)	**REG6C44**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

GE Register (Bank = 36)

Index (Absolute)	Mnemonic	Bit	Description	
	GE_ABL_COEF[3:0]	3:0	Source Coefficient of Alpha Blending. # Cout = Csrc * reg_pe_abl_coef OP Cdst * (1 - reg_pe_abl_coef). # Where Csrc is source color, Cdst is the destination or background color. # 4'h0: 1.0 (8'hff). # 4'h1: reg_pe_abl_const. # 4'h2: Asrc. # 4'h3: Adst. # 4'h4: ((Asrc * Acon) * Csrc + (1-(Asrc*Acon)) * Cdst) / 2. # 4'h5: ((Asrc * Acon) * Csrc + Adst * Cdst * (1-(Asrc*Acon))) / (Asrc*Acon) + Adst * (1-Asrc * Acon)). # 4'h6: ((Asrc * Acon) * Csrc * (1-Adst) + Adst * Cdst) / (Asrc * Acon) * (1-Adst) + Adst). # 4'h8: 0.0. # 4'h9: 1 - reg_pe_abl_const. # 4'hA: 1 - Asrc. # 4'hB: 1 - Adst. # 4'hC: 1 - Asrc * reg_pe_abl_const. # Others: Reserved.	
12h (6C49h)	**REG6C49**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GE_DB_ABL[2:0]	2:0	Alpha value of Writing to Destination After Alpha Color Key. # 3'b000: reg_pe_abl_const. # 3'b001: Asrc. # 3'b010: Adst. # 3'b011: Asrc * Acon. # 3'b100: Asrc * Acon * Adst. # 3'b101: Adst - Adst * Asrc * Acon. # 3'b110: Asrc * Acon - Adst * Asrc * Acon. # 3'b111: Asrc * Acon - Adst * Asrc * Acon + Adst. # Others: Reserved.	
13h (6C4Ch)	**REG6C4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_ABL_CONST[7:0]	7:0	Constant Color Register for Alpha Blending.	
14h	**REG6C50**	**7:0**	**Default : 0x00**	**Access : R/W**

GE Register (Bank = 36)

Index (Absolute)	Mnemonic	Bit	Description	
(6C50h)	GE_SCK_HTH[7:0]	7:0	Source Color Key High Threshold. The index mode of 8bit or 16bit, high threshold and low threshold must the same. # [7:0] 8bit Palette. # [15:0] 16bit Index Mode. # [31:0] ARGB8888.	
14h **(6C51h)**	**REG6C51**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SCK_HTH[15:8]	7:0	See description of '6C50h'.	
15h **(6C54h)**	**REG6C54**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SCK_HTH[23:16]	7:0	See description of '6C50h'.	
15h **(6C55h)**	**REG6C55**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SCK_HTH[31:24]	7:0	See description of '6C50h'.	
16h **(6C58h)**	**REG6C58**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SCK_LTH[7:0]	7:0	Source Color Key Low Threshold. The index mode of 8bit or 16bit, high threshold and low threshold must the same. # [7:0] 8bit Palette. # [15:0] 16bit Index Mode. # [31:0] ARGB8888.	
16h **(6C59h)**	**REG6C59**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SCK_LTH[15:8]	7:0	See description of '6C58h'.	
17h **(6C5Ch)**	**REG6C5C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SCK_LTH[23:16]	7:0	See description of '6C58h'.	
17h **(6C5Dh)**	**REG6C5D**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SCK_LTH[31:24]	7:0	See description of '6C58h'.	
18h **(6C60h)**	**REG6C60**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DCK_HTH[7:0]	7:0	Destination Color Key High Threshold. The index mode of 8bit or 16bit, high threshold and low threshold must the same. # [7:0] 8bit Palette. # [15:0] 16bit Index Mode. # [31:0] ARGB8888.	
18h **(6C61h)**	**REG6C61**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DCK_HTH[15:8]	7:0	See description of '6C60h'.	
19h **(6C64h)**	**REG6C64**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DCK_HTH[23:16]	7:0	See description of '6C60h'.	

GE Register (Bank = 36)

Index (Absolute)	Mnemonic	Bit	Description	
19h (6C65h)	**REG6C65**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DCK_HTH[31:24]	7:0	See description of '6C60h'.	
1Ah (6C68h)	**REG6C68**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DCK_LTH[7:0]	7:0	Destination Color Key Low Threshold. The index mode of 8bit or 16bit, high threshold and low threshold must the same. # [7:0] 8bit Palette. # [15:0] 16bit Index Mode. # [31:0] ARGB8888.	
1Ah (6C69h)	**REG6C69**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DCK_LTH[15:8]	7:0	See description of '6C68h'.	
1Bh (6C6Ch)	**REG6C6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DCK_LTH[23:16]	7:0	See description of '6C68h'.	
1Bh (6C6Dh)	**REG6C6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DCK_LTH[31:24]	7:0	See description of '6C68h'.	
1Ch (6C70h)	**REG6C70**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	GE_DSTAC_MODE	5	Destination Alpha Comparison Mode. # 1'b0: If the destination alpha is in the threshold and GE won't do the alpha operation. # 1'b1: If the destination isn't in the Threshold, GE won't do the alpha operation.	
	GE_ALPHA_CMP_MODE	4	Alpha Compare Mode. # 1'b0: Maximum Alpha of Source and Destination. # 1'b1: Minimum Alpha of Source and Destination.	
	-	3:2	Reserved.	
	GE_DCK_OP_MODE	1	Destination Color Key Operation Mode. # 1'b0: If the color didn't equal to the destination color key, the color will be replaced by source color. # 1'b1: If the color equal to the source color key, the color will replace by source color.	
	GE_SCK_OP_MODE	0	Source Color Key Operation Mode. # 1'b0: If the color equal to the source color key, the color will be replaced by destination color. # 1'b1: If the color didn't equal to the source color key, the color will replace by destination color.	

GE Register (Bank = 36)

Index (Absolute)	Mnemonic	Bit	Description	
1Dh (6C74h)	**REG6C74**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DSTAC_HTH[7:0]	7:0	Destination Alpha Comparison Value High Threshold.	
1Dh (6C75h)	**REG6C75**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DSTAC_LTH[7:0]	7:0	Destination Alpha Comparison Value Low Threshold.	
1Fh (6C7Ch)	**REG6C7C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DB_YUV_FM[1:0]	7:6	YUV destination 422 format. # 2'h0: CbY1CrY0. # 2'h1: CrY1CbY0. # 2'h2: Y1CbY0Cr. # 2'h3: Y1CrY0Cb.	
	GE_SB_YUV_FM[1:0]	5:4	YUV source 422 format. # 2'h0: CbY1CrY0. # 2'h1: CrY1CbY0. # 2'h2: Y1CbY0Cr. # 2'h3: Y1CrY0Cb.	
	GE_YUV_IN	3	UV input range. # 1'h0: UV 0~255. # 1'h1: UV -128~127.	
	GE_YUV_RANGE	2	YUV output range. # 1'h0: 0~255. # 1'h1: Y 16~235 UV 16~240.	
	GE_DC_CSC_FM[1:0]	1:0	Color Space Conversion Format for Decode (RGB to YUV). # 2'h0: Computer Mode (Y-> 16~235, UV -> 0~240). # 2'h1: CSC to 0~255. Color Space Conversion Format for Decode (YUV to RGB). # 2'h0: Computer Mode. # Others: Reserved.	
20h (6C80h)	**REG6C80**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SB_BASE[7:0]	7:0	Base Address of Graphics Engine Source Buffer. The Unit of Base Address is Byte. The start of Source Buffer storage must be 8bit alignment.	
20h (6C81h)	**REG6C81**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SB_BASE[15:8]	7:0	See description of '6C80h'.	
21h (6C84h)	**REG6C84**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SB_BASE[23:16]	7:0	See description of '6C80h'.	
21h	**REG6C85**	**7:0**	**Default : 0x00**	**Access : R/W**

GE Register (Bank = 36)

Index (Absolute)	Mnemonic	Bit	Description	
(6C85h)	-	7:3	Reserved.	
	GE_SB_BASE[26:24]	2:0	See description of '6C80h'.	
26h (6C98h)	**REG6C98**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DB_BASE[7:0]	7:0	Base Address of Graphics Engine Destination Buffer. The Unit of Base is Byte. The Destination Buffer storage must be 8bit alignment.	
26h (6C99h)	**REG6C99**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DB_BASE[15:8]	7:0	See description of '6C98h'.	
27h (6C9Ch)	**REG6C9C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DB_BASE[23:16]	7:0	See description of '6C98h'.	
27h (6C9Dh)	**REG6C9D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GE_DB_BASE[26:24]	2:0	See description of '6C98h'.	
30h (6CC0h)	**REG6CC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_SB_PIT[7:0]	7:0	Pitch of Graphics Engine Source Buffer. The Unit of Pitch is Byte. 1. In I1,I2,I4 modes, the pitch must be 8 bits alignment. 2. In other modes, the pitch must be 32bits alignment.	
30h (6CC1h)	**REG6CC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	GE_SB_PIT[13:8]	5:0	See description of '6CC0h'.	
33h (6CCCh)	**REG6CCC**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_DB_PIT[7:0]	7:0	Pitch of Graphics Engine Destination Buffer. The unit of pitch is byte, but the pitch must 32bits alignment.	
33h (6CCDh)	**REG6CCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	GE_DB_PIT[13:8]	5:0	See description of '6CCCh'.	
34h (6CD0h)	**REG6CD0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

GE Register (Bank = 36)

Index (Absolute)	Mnemonic	Bit	Description	
	GE_SB_FM[3:0]	3:0	Format of Graphics Engine Source Buffer. # 4'h0: 1 bit Intensity 1. # 4'h1: 2 bits, Intensity 2. # 4'h2: 4 bits, Intensity 4. # 4'h4: 8 bits, Palette 8. # 4'h6: 16 bits, FaBaFgBg2266[15:0]. # 4'h7: 16 bits, 1ABFgBg12355[15:0]. # 4'h8: 16 bits, RGB565[15:0]. # 4'h9: 16 bits, ARGB1555[15:0]. # 4'ha: 16 bits, ARGB4444[15:0]. # 4'hb: 16 bits, 1BAAFgBg123433[15:0]. # 4'he: 16 bits, YUYV422[15:0]. # 4'hf: 32 bits, ARGB8888[31:0]. Others: Reserved.	
34h (6CD1h)	**REG6CD1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_DB_FM[3:0]	3:0	Format of Graphics Engine Destination Buffer. # 4'h4: 8 bits Palette 8. # 4'h6: 16 bits, FaBaFgBg2266[15:0]. # 4'h7: 16 bits, 1ABFgBg12355[15:0]. # 4'h8: 16 bits, RGB565[15:0]. # 4'h9: 16 bits, 0RGB1555[15:0]. # 4'ha: 16 bits, ARGB4444[15:0]. # 4'hb: 16 bits, 1BA1A2FgBg123433[15:0]. # 4'he: 16 bits, YUYV422[15:0]. # 4'hf: ARGB8888[31:0]. Others: Reserved.	
35h (6CD4h)	**REG6CD4**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I0_C[7:0]	7:0	Intensity 0 color for ge source buffer in I format. # [31:0] ARGB8888. # [15:0] 1BA1A2FgBg (123433). # [15:0] 1ABFgBg (12355). # [15:0] FaBaFgBg (2266). # [7:0] 8bit Palette.	
35h (6CD5h)	**REG6CD5**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I0_C[15:8]	7:0	See description of '6CD4h'.	
36h (6CD8h)	**REG6CD8**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I0_C[23:16]	7:0	See description of '6CD4h'.	

GE Register (Bank = 36)

Index (Absolute)	Mnemonic	Bit	Description	
36h (6CD9h)	**REG6CD9**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I0_C[31:24]	7:0	See description of '6CD4h'.	
37h (6CDCh)	**REG6CDC**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I1_C[7:0]	7:0	Intensity 1 color for ge source buffer in I format. # [31:0] ARGB8888. # [15:0] 1BA1A2FgBg (123433). # [15:0] 1ABFgBg (12355). # [15:0] FaBaFgBg (2266). # [7:0] 8bit Palette.	
37h (6CDDh)	**REG6CDD**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I1_C[15:8]	7:0	See description of '6CDCh'.	
38h (6CE0h)	**REG6CE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I1_C[23:16]	7:0	See description of '6CDCh'.	
38h (6CE1h)	**REG6CE1**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I1_C[31:24]	7:0	See description of '6CDCh'.	
39h (6CE4h)	**REG6CE4**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I2_C[7:0]	7:0	Intensity 2 color for ge source buffer in I format. # [31:0] ARGB8888. # [15:0] 1BA1A2FgBg (123433). # [15:0] 1ABFgBg (12355). # [15:0] FaBaFgBg (2266). # [7:0] 8bit Palette.	
39h (6CE5h)	**REG6CE5**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I2_C[15:8]	7:0	See description of '6CE4h'.	
3Ah (6CE8h)	**REG6CE8**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I2_C[23:16]	7:0	See description of '6CE4h'.	
3Ah (6CE9h)	**REG6CE9**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I2_C[31:24]	7:0	See description of '6CE4h'.	
3Bh (6CECh)	**REG6CEC**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I3_C[7:0]	7:0	Intensity 3 color for ge source buffer in I format. # [31:0] ARGB8888. # [15:0] 1BA1A2FgBg (123433). # [15:0] 1ABFgBg (12355). # [15:0] FaBaFgBg (2266). # [7:0] 8bit Palette.	
3Bh	**REG6CED**	**7:0**	**Default : 0x00**	**Access : R/W**

GE Register (Bank = 36)

Index (Absolute)	Mnemonic	Bit	Description	
(6CEDh)	GE_I3_C[15:8]	7:0	See description of '6CECh'.	
3Ch (6CF0h)	**REG6CF0**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I3_C[23:16]	7:0	See description of '6CECh'.	
3Ch (6CF1h)	**REG6CF1**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I3_C[31:24]	7:0	See description of '6CECh'.	
3Dh (6CF4h)	**REG6CF4**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I4_C[7:0]	7:0	Intensity 4 color for ge source buffer in I format. # [31:0] ARGB8888. # [15:0] 1BA1A2FgBg (123433). # [15:0] 1ABFgBg (12355). # [15:0] FaBaFgBg (2266). # [7:0] 8bit Palette.	
3Dh (6CF5h)	**REG6CF5**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I4_C[15:8]	7:0	See description of '6CF4h'.	
3Eh (6CF8h)	**REG6CF8**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I4_C[23:16]	7:0	See description of '6CF4h'.	
3Eh (6CF9h)	**REG6CF9**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I4_C[31:24]	7:0	See description of '6CF4h'.	
3Fh (6CFCh)	**REG6CFC**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I5_C[7:0]	7:0	Intensity 5 color for ge source buffer in I format. # [31:0] ARGB8888. # [15:0] 1BA1A2FgBg (123433). # [15:0] 1ABFgBg (12355). # [15:0] FaBaFgBg (2266). # [7:0] 8bit Palette.	
3Fh (6CFDh)	**REG6CFD**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I5_C[15:8]	7:0	See description of '6CFCh'.	
40h (6D00h)	**REG6D00**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I5_C[23:16]	7:0	See description of '6CFCh'.	
40h (6D01h)	**REG6D01**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I5_C[31:24]	7:0	See description of '6CFCh'.	
41h	**REG6D04**	**7:0**	**Default : 0x00**	**Access : R/W**

GE Register (Bank = 36)

Index (Absolute)	Mnemonic	Bit	Description	
(6D04h)	GE_I6_C[7:0]	7:0	Intensity 6 color for ge source buffer in I format. # [31:0] ARGB8888. # [15:0] 1BA1A2FgBg (123433). # [15:0] 1ABFgBg (12355). # [15:0] FaBaFgBg (2266). # [7:0] 8bit Palette.	
41h (6D05h)	**REG6D05**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I6_C[15:8]	7:0	See description of '6D04h'.	
42h (6D08h)	**REG6D08**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I6_C[23:16]	7:0	See description of '6D04h'.	
42h (6D09h)	**REG6D09**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I6_C[31:24]	7:0	See description of '6D04h'.	
43h (6D0Ch)	**REG6D0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I7_C[7:0]	7:0	Intensity 7 color for ge source buffer in I format. # [31:0] ARGB8888. # [15:0] 1BA1A2FgBg (123433). # [15:0] 1ABFgBg (12355). # [15:0] FaBaFgBg (2266). # [7:0] 8bit Palette.	
43h (6D0Dh)	**REG6D0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I7_C[15:8]	7:0	See description of '6D0Ch'.	
44h (6D10h)	**REG6D10**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I7_C[23:16]	7:0	See description of '6D0Ch'.	
44h (6D11h)	**REG6D11**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I7_C[31:24]	7:0	See description of '6D0Ch'.	
45h (6D14h)	**REG6D14**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I8_C[7:0]	7:0	Intensity 8 color for ge source buffer in I format. # [31:0] ARGB8888. # [15:0] 1BA1A2FgBg (123433). # [15:0] 1ABFgBg (12355). # [15:0] FaBaFgBg (2266). # [7:0] 8bit Palette.	
45h (6D15h)	**REG6D15**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I8_C[15:8]	7:0	See description of '6D14h'.	
46h (6D18h)	**REG6D18**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I8_C[23:16]	7:0	See description of '6D14h'.	

GE Register (Bank = 36)

Index (Absolute)	Mnemonic	Bit	Description	
46h (6D19h)	**REG6D19**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I8_C[31:24]	7:0	See description of '6D14h'.	
47h (6D1Ch)	**REG6D1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I9_C[7:0]	7:0	Intensity 9 color for ge source buffer in I format. # [31:0] ARGB8888. # [15:0] 1BA1A2FgBg (123433). # [15:0] 1ABFgBg (12355). # [15:0] FaBaFgBg (2266). # [7:0] 8bit Palette.	
47h (6D1Dh)	**REG6D1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I9_C[15:8]	7:0	See description of '6D1Ch'.	
48h (6D20h)	**REG6D20**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I9_C[23:16]	7:0	See description of '6D1Ch'.	
48h (6D21h)	**REG6D21**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I9_C[31:24]	7:0	See description of '6D1Ch'.	
49h (6D24h)	**REG6D24**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I10_C[7:0]	7:0	Intensity 10 color for ge source buffer in I format. # [31:0] ARGB8888. # [15:0] 1BA1A2FgBg (123433). # [15:0] 1ABFgBg (12355). # [15:0] FaBaFgBg (2266). # [7:0] 8bit Palette.	
49h (6D25h)	**REG6D25**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I10_C[15:8]	7:0	See description of '6D24h'.	
4Ah (6D28h)	**REG6D28**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I10_C[23:16]	7:0	See description of '6D24h'.	
4Ah (6D29h)	**REG6D29**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I10_C[31:24]	7:0	See description of '6D24h'.	
4Bh (6D2Ch)	**REG6D2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I11_C[7:0]	7:0	Intensity 11 color for ge source buffer in I format. # [31:0] ARGB8888. # [15:0] 1BA1A2FgBg (123433). # [15:0] 1ABFgBg (12355). # [15:0] FaBaFgBg (2266). # [7:0] 8bit Palette.	
4Bh	**REG6D2D**	**7:0**	**Default : 0x00**	**Access : R/W**

GE Register (Bank = 36)

Index (Absolute)	Mnemonic	Bit	Description	
(6D2Dh)	GE_I11_C[15:8]	7:0	See description of '6D2Ch'.	
4Ch (6D30h)	**REG6D30**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I11_C[23:16]	7:0	See description of '6D2Ch'.	
4Ch (6D31h)	**REG6D31**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I11_C[31:24]	7:0	See description of '6D2Ch'.	
4Dh (6D34h)	**REG6D34**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I12_C[7:0]	7:0	Intensity 12 color for ge source buffer in I format. # [31:0] ARGB8888. # [15:0] 1BA1A2FgBg (123433). # [15:0] 1ABFgBg (12355). # [15:0] FaBaFgBg (2266). # [7:0] 8bit Palette.	
4Dh (6D35h)	**REG6D35**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I12_C[15:8]	7:0	See description of '6D34h'.	
4Eh (6D38h)	**REG6D38**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I12_C[23:16]	7:0	See description of '6D34h'.	
4Eh (6D39h)	**REG6D39**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I12_C[31:24]	7:0	See description of '6D34h'.	
4Fh (6D3Ch)	**REG6D3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I13_C[7:0]	7:0	Intensity 13 color for ge source buffer in I format. # [31:0] ARGB8888. # [15:0] 1BA1A2FgBg (123433). # [15:0] 1ABFgBg (12355). # [15:0] FaBaFgBg (2266). # [7:0] 8bit Palette.	
4Fh (6D3Dh)	**REG6D3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I13_C[15:8]	7:0	See description of '6D3Ch'.	
50h (6D40h)	**REG6D40**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I13_C[23:16]	7:0	See description of '6D3Ch'.	
50h (6D41h)	**REG6D41**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I13_C[31:24]	7:0	See description of '6D3Ch'.	
51h	**REG6D44**	**7:0**	**Default : 0x00**	**Access : R/W**

GE Register (Bank = 36)

Index (Absolute)	Mnemonic	Bit	Description	
(6D44h)	GE_I14_C[7:0]	7:0	Intensity 14 color for ge source buffer in I format. # [31:0] ARGB8888. # [15:0] 1BA1A2FgBg (123433). # [15:0] 1ABFgBg (12355). # [15:0] FaBaFgBg (2266). # [7:0] 8bit Palette.	
51h (6D45h)	**REG6D45**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I14_C[15:8]	7:0	See description of '6D44h'.	
52h (6D48h)	**REG6D48**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I14_C[23:16]	7:0	See description of '6D44h'.	
52h (6D49h)	**REG6D49**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I14_C[31:24]	7:0	See description of '6D44h'.	
53h (6D4Ch)	**REG6D4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I15_C[7:0]	7:0	Intensity 15 color for ge source buffer in I format. # [31:0] ARGB8888. # [15:0] 1BA1A2FgBg (123433). # [15:0] 1ABFgBg (12355). # [15:0] FaBaFgBg (2266). # [7:0] 8bit Palette.	
53h (6D4Dh)	**REG6D4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I15_C[15:8]	7:0	See description of '6D4Ch'.	
54h (6D50h)	**REG6D50**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I15_C[23:16]	7:0	See description of '6D4Ch'.	
54h (6D51h)	**REG6D51**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_I15_C[31:24]	7:0	See description of '6D4Ch'.	
55h (6D54h)	**REG6D54**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_CLIP_LEFT[7:0]	7:0	2D Clipping Window Left Setting.	
55h (6D55h)	**REG6D55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GE_CLIP_LEFT[10:8]	2:0	See description of '6D54h'.	
56h (6D58h)	**REG6D58**	**7:0**	**Default : 0xD0**	**Access : R/W**
	GE_CLIP_RIGHT[7:0]	7:0	2D Clipping Window Right Setting.	
56h (6D59h)	**REG6D59**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:3	Reserved.	
	GE_CLIP_RIGHT[10:8]	2:0	See description of '6D58h'.	

GE Register (Bank = 36)

Index (Absolute)	Mnemonic	Bit	Description	
57h (6D5Ch)	**REG6D5C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_CLIP_TOP[7:0]	7:0	2D Clipping Window Top Setting.	
57h (6D5Dh)	**REG6D5D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GE_CLIP_TOP[10:8]	2:0	See description of '6D5Ch'.	
58h (6D60h)	**REG6D60**	**7:0**	**Default : 0x40**	**Access : R/W**
	GE_CLIP_BOT[7:0]	7:0	2D Clipping Window Bottom Setting.	
58h (6D61h)	**REG6D61**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:3	Reserved.	
	GE_CLIP_BOT[10:8]	2:0	See description of '6D60h'.	
59h (6D64h)	**REG6D64**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	GE_ROT[1:0]	1:0	Coordinate Rotation Degree (Clockwise). # 2'h0: 0º. # 2'h1: 90º. # 2'h2: 180º. # 2'h3: 270º.	
60h (6D81h)	**REG6D81**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	GE_RECT_CV	5	Rectangle Fill Vertical Color Type. # 1'b0: Constant Color Fill. # 1'b1: Gradient Color Fill.	
	GE_RECT_CH	4	Rectangle Fill Horizontal Color Type. # 1'b0: Constant Color Fill. # 1'b1: Gradient Color Fill.	
	GE_LINE_C_TYGE	3	Color Type Setting for Line Drawing. # 1'b0: Constant Color Line Draw. # 1'b1: Gradient Color Line Draw.	
	GE_PRI_Y_DIR	2	For Rectangle Fill and BitBlt:. Primitive Drawing Direction in Y Coordinates for Destination. # 1'b0: Positive Direction: From Top to Bottom. # 1'b1: Negative Direction: From Top to Bottom.	

GE Register (Bank = 36)

Index (Absolute)	Mnemonic	Bit	Description	
	GE_PRI_X_DIR	1	For Rectangle Fill and BitBlt:. Primitive Drawing Direction in X Coordinates for Destination. For Line Drawing: Primitive Drawing Direction in Major Coordinates define in reg_pe_line_major. # 1'b0: Positive Direction: From Left to Right. # 1'b1: Negative Direction: From Right to Left.	
	GE_PRI_S_Y_DIR	0	For Rectangle Fill and BitBlt:. Primitive Drawing Direction in Y Coordinates for Destination. # 1'b0: Positive Direction: From Top to Bottom. # 1'b1: Negative Direction: From Bottom to Top.	
61h (6D84h)	**REG6D84**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_LINE_DELTA[6:0]	7:1	(1) The delta value of minor direction for Line Drawing. (2) The x delta value for BitBlt (s1.12).	
	-	0	Reserved.	
61h (6D85h)	**REG6D85**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_LINE_MAJOR	7	The major direction setting for line drawing. # 1'b0: X is the major direction. # 1'b1: Y is the major direction.	
	GE_LINE_DELTA[13:7]	6:0	See description of '6D84h'.	
62h (6D88h)	**REG6D88**	**7:0**	**Default : 0x3F**	**Access : R/W**
	GE_LPT_RPF[1:0]	7:6	Line Pattern Repeat Factor. # [7:6] 2'h0: Repeat Factor = 1. # [7:6] 2'h1: Repeat Factor = 2. # [7:6] 2'h2: Repeat Factor = 3. # [7:6] 2'h3: Repeat Factor = 4.	
	GE_LPT[5:0]	5:0	Line Pattern. # [5:0]: Line Pattern. LSB will be used first.	
62h (6D89h)	**REG6D89**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	GE_LINE_LAST	1	Line Last Pixel Control. # 1'b0: Do Not Drawing the Last Pixel of Line. # 1'b1: Drawing the Last Pixel of Line.	

GE Register (Bank = 36)

Index (Absolute)	Mnemonic	Bit	Description	
	GE_LPT_RST	0	Line Pattern Reset Control. # A writing by 1'b1 will cause a Line Pattern Reset. After the reset, HW will automatically set this bit back to 1'b0. # 1'b0: Do Not Reset Line Pattern for Line Drawing. # 1'b1: Reset Line Pattern for Line Drawing.	
63h (6D8Ch)	**REG6D8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_LINE_LENGTH[7:0]	7:0	Line Length.	
63h (6D8Dh)	**REG6D8D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_LINE_LENGTH[11:8]	3:0	See description of '6D8Ch'.	
66h (6D98h)	**REG6D98**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_ITC_DIS[7:0]	7:0	Initial distance of the italic font.	
66h (6D99h)	**REG6D99**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_ITC_LINE[7:0]	7:0	Initial line of the italic font.	
67h (6D9Ch)	**REG6D9C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	GE_ITC_DELTA[4:0]	4:0	The delta value of Italic Bitblt (s1.3).	
68h (6DA0h)	**REG6DA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_V0_X[7:0]	7:0	X0, Coordinate X of Primitive Vertex 0 (s11).	
68h (6DA1h)	**REG6DA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_V0_X[11:8]	3:0	See description of '6DA0h'.	
69h (6DA4h)	**REG6DA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_V0_Y[7:0]	7:0	Y0, Coordinate Y of Primitive Vertex 0 (s11).	
69h (6DA5h)	**REG6DA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_V0_Y[11:8]	3:0	See description of '6DA4h'.	
6Ah (6DA8h)	**REG6DA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_V1_X[7:0]	7:0	X1, Coordinate X of Primitive Vertex 1 (s11).	
6Ah (6DA9h)	**REG6DA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_V1_X[11:8]	3:0	See description of '6DA8h'.	
6Bh	**REG6DAC**	**7:0**	**Default : 0x00**	**Access : R/W**

GE Register (Bank = 36)

Index (Absolute)	Mnemonic	Bit	Description	
(6DACh)	GE_PRI_V1_Y[7:0]	7:0	Y1, Coordinate Y of Primitive Vertex 1 (s11).	
6Bh (6DADh)	**REG6DAD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_V1_Y[11:8]	3:0	See description of '6DACh'.	
6Ch (6DB0h)	**REG6DB0**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_V2_X[7:0]	7:0	X2, Coordinate X of Primitive Vertex 2. # Where Vertex 2 is used for the top-left corner pixel of BitBlt Source. (s11).	
6Ch (6DB1h)	**REG6DB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GE_PRI_V2_X[10:8]	2:0	See description of '6DB0h'.	
6Dh (6DB4h)	**REG6DB4**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_V2_Y[7:0]	7:0	Y2, Coordinate Y of Primitive Vertex 2. # Where Vertex 2 is used for the top-left corner pixel of BitBlt Source. (s11).	
6Dh (6DB5h)	**REG6DB5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GE_PRI_V2_Y[10:8]	2:0	See description of '6DB4h'.	
6Eh (6DB8h)	**REG6DB8**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_STBB_S_W[7:0]	7:0	Bitblt Source Width.	
6Eh (6DB9h)	**REG6DB9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_STBB_S_W[11:8]	3:0	See description of '6DB8h'.	
6Fh (6DBCh)	**REG6DBC**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_STBB_S_H[7:0]	7:0	Bitblt Source Height.	
6Fh (6DBDh)	**REG6DBD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_STBB_S_H[11:8]	3:0	See description of '6DBCh'.	
70h	**REG6DC0**	**7:0**	**Default : 0x00**	**Access : R/W**

GE Register (Bank = 36)

Index (Absolute)	Mnemonic	Bit	Description	
(6DC0h)	GE_PRI_B_ST[7:0]	7:0	Bst, Start Value of Primitive B Color. 1BAAFgBg123433 FgBg. 1ABFgBg12355 Bg. FaBaFgBg Bg. Palette 8.	
70h **(6DC1h)**	**REG6DC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_G_ST[7:0]	7:0	Gst, Start Value of Primitive G Color. 1BAAFgBg123433 A. 1ABFgBg12355 Fg. FaBaFgBg Fg.	
71h **(6DC4h)**	**REG6DC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_R_ST[7:0]	7:0	Rst, Start Value of Primitive R Color. 1BAAFgBg123433 BA. 1ABFgBg12355 AB. FaBaFgBg Ba.	
71h **(6DC5h)**	**REG6DC5**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_A_ST[7:0]	7:0	Ast, Start Value of Primitive Alpha Factor. 1BAAFgBg123433 1. 1ABFgBg12355 1. FaBaFgBg Fa.	
72h **(6DC8h)**	**REG6DC8**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_R_DX[7:0]	7:0	Rdx, Primitive Parameter delta R in X direction for Rectangle Fill. # Primitive Parameter delta R for Line Draw (s7.12).	
72h **(6DC9h)**	**REG6DC9**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_R_DX[15:8]	7:0	See description of '6DC8h'.	
73h **(6DCCh)**	**REG6DCC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_R_DX[19:16]	3:0	See description of '6DC8h'.	
74h **(6DD0h)**	**REG6DD0**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_R_DY[7:0]	7:0	Rdy, Primitive Parameter delta R in Y direction for Rectangle Draw (s7.12).	
74h **(6DD1h)**	**REG6DD1**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_R_DY[15:8]	7:0	See description of '6DD0h'.	
75h **(6DD4h)**	**REG6DD4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

GE Register (Bank = 36)

Index (Absolute)	Mnemonic	Bit	Description	
	GE_PRI_R_DY[19:16]	3:0	See description of '6DD0h'.	
76h (6DD8h)	**REG6DD8**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_G_DX[7:0]	7:0	Gdx, Primitive Parameter delta G in X direction for Rectangle Fill. Primitive Parameter delta G for Line Draw (s7.12).	
76h (6DD9h)	**REG6DD9**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_G_DX[15:8]	7:0	See description of '6DD8h'.	
77h (6DDCh)	**REG6DDC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_G_DX[19:16]	3:0	See description of '6DD8h'.	
78h (6DE0h)	**REG6DE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_G_DY[7:0]	7:0	Gdy, Primitive Parameter delta G in Y direction for Rectangle Fill (s7.12).	
78h (6DE1h)	**REG6DE1**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_G_DY[15:8]	7:0	See description of '6DE0h'.	
79h (6DE4h)	**REG6DE4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_G_DY[19:16]	3:0	See description of '6DE0h'.	
7Ah (6DE8h)	**REG6DE8**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_B_DX[7:0]	7:0	Bdx, Primitive Parameter delta B in X direction for Rectangle Fill. Primitive Parameter delta B for Line Draw (s7.12).	
7Ah (6DE9h)	**REG6DE9**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_B_DX[15:8]	7:0	See description of '6DE8h'.	
7Bh (6DECh)	**REG6DEC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GE_PRI_B_DX[19:16]	3:0	See description of '6DE8h'.	
7Ch (6DF0h)	**REG6DF0**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_B_DY[7:0]	7:0	Bdy, Primitive Parameter delta B in Y direction for Rectangle Fill (s7.12).	
7Ch (6DF1h)	**REG6DF1**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_B_DY[15:8]	7:0	See description of '6DF0h'.	
7Dh (6DF4h)	**REG6DF4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

GE Register (Bank = 36)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GE_PRI_B_DY[19:16]	3:0	See description of '6DF0h'.	
7Eh (6DF8h)	**REG6DF8**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_A_DX[7:0]	7:0	Adx, Primitive Parameter delta A in X direction for Rectangle Fill. Primitive Parameter delta A for Line Draw (s4.11).	
7Eh (6DF9h)	**REG6DF9**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_A_DX[15:8]	7:0	See description of '6DF8h'.	
7Fh (6DFCh)	**REG6DFC**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_A_DY[7:0]	7:0	Ady, Primitive Parameter delta A in Y direction for Rectangle Fill (s4.11).	
7Fh (6DFDh)	**REG6DFD**	**7:0**	**Default : 0x00**	**Access : R/W**
	GE_PRI_A_DY[15:8]	7:0	See description of '6DFCh'.	

IRQ Register (Bank = 38)

IRQ Register (Bank = 38)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
40h (7100h)	**REG7100**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_FIQ_MASK[7:0]	7:0	Mask for FIQ, bit [31:0]. 1: Mask. 0: Not mask.	
40h (7101h)	**REG7101**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_FIQ_MASK[15:8]	7:0	See description of '7100h'.	
41h (7104h)	**REG7104**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_FIQ_MASK[23:16]	7:0	See description of '7100h'.	
41h (7105h)	**REG7105**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_FIQ_MASK[31:24]	7:0	See description of '7100h'.	
42h (7108h)	**REG7108**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_FORCE[7:0]	7:0	Force for FIQ, bit [31:0]. 1: Force. 0: Not force.	
42h (7109h)	**REG7109**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_FORCE[15:8]	7:0	See description of '7108h'.	
43h (710Ch)	**REG710C**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_FORCE[23:16]	7:0	See description of '7108h'.	

IRQ Register (Bank = 38)

Index (Absolute)	Mnemonic	Bit	Description	
43h (710Dh)	**REG710D**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_FORCE[31:24]	7:0	See description of '7108h'.	
44h (7110h)	**REG7110**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_CLR7	7	Clear for FIQ, bit7.	
	C_FIQ_CLR6	6	Clear for FIQ, bit6.	
	C_FIQ_CLR5	5	Clear for FIQ, bit5.	
	C_FIQ_CLR4	4	Clear for FIQ, bit4.	
	C_FIQ_CLR3	3	Clear for FIQ, bit3.	
	C_FIQ_CLR2	2	Clear for FIQ, bit2.	
	C_FIQ_CLR1	1	Clear for FIQ, bit1.	
	C_FIQ_CLR0	0	Clear for FIQ, bit0.	
44h (7111h)	**REG7111**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_CLR15	7	Clear for FIQ, bit15.	
	C_FIQ_CLR14	6	Clear for FIQ, bit14.	
	C_FIQ_CLR13	5	Clear for FIQ, bit13.	
	C_FIQ_CLR12	4	Clear for FIQ, bit12.	
	C_FIQ_CLR11	3	Clear for FIQ, bit11.	
	C_FIQ_CLR10	2	Clear for FIQ, bit10.	
	C_FIQ_CLR9	1	Clear for FIQ, bit9.	
	C_FIQ_CLR8	0	Clear for FIQ, bit8.	
45h (7114h)	**REG7114**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_CLR23	7	Clear for FIQ, bit23.	
	C_FIQ_CLR22	6	Clear for FIQ, bit22.	
	C_FIQ_CLR21	5	Clear for FIQ, bit21.	
	C_FIQ_CLR20	4	Clear for FIQ, bit20.	
	C_FIQ_CLR19	3	Clear for FIQ, bit19.	
	C_FIQ_CLR18	2	Clear for FIQ, bit18.	
	C_FIQ_CLR17	1	Clear for FIQ, bit17.	
	C_FIQ_CLR16	0	Clear for FIQ, bit16.	
45h (7115h)	**REG7115**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_CLR31	7	Clear for FIQ, bit31.	
	C_FIQ_CLR30	6	Clear for FIQ, bit30.	
	C_FIQ_CLR29	5	Clear for FIQ, bit29.	

IRQ Register (Bank = 38)

Index (Absolute)	Mnemonic	Bit	Description	
	C_FIQ_CLR28	4	Clear for FIQ, bit28.	
	C_FIQ_CLR27	3	Clear for FIQ, bit27.	
	C_FIQ_CLR26	2	Clear for FIQ, bit26.	
	C_FIQ_CLR25	1	Clear for FIQ, bit25.	
	C_FIQ_CLR24	0	Clear for FIQ, bit24.	
46h (7118h)	**REG7118**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_RAW_STATUS[7:0]	7:0	FIQ Raw Status, bit [31:0]. Interrupt source status for FIQ.	
46h (7119h)	**REG7119**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_RAW_STATUS[15:8]	7:0	See description of '7118h'.	
47h (711Ch)	**REG711C**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_RAW_STATUS[23:16]	7:0	See description of '7118h'.	
47h (711Dh)	**REG711D**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_RAW_STATUS[31:24]	7:0	See description of '7118h'.	
48h (7120h)	**REG7120**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_FINAL_STATUS[7:0]	7:0	FIQ Final Status, bit [31:0]. Final interrupt status for FIQ.	
48h (7121h)	**REG7121**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_FINAL_STATUS[15:8]	7:0	See description of '7120h'.	
49h (7124h)	**REG7124**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_FINAL_STATUS[23:16]	7:0	See description of '7120h'.	
49h (7125h)	**REG7125**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_FINAL_STATUS[31:24]	7:0	See description of '7120h'.	
4Ah (7128h)	**REG7128**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_SEL_HL_TRIGGER[7:0]	7:0	Select H or L trigger, bit [31:0]. Inverse source polarity for FIQ.	
4Ah (7129h)	**REG7129**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_SEL_HL_TRIGGER[15:8]	7:0	See description of '7128h'.	
4Bh (712Ch)	**REG712C**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_SEL_HL_TRIGGER[23:16]	7:0	See description of '7128h'.	
4Bh (712Dh)	**REG712D**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_SEL_HL_TRIGGER[31:24]	7:0	See description of '7128h'.	
4Ch	**REG7130**	**7:0**	**Default : 0xFF**	**Access : R/W**

IRQ Register (Bank = 38)

Index (Absolute)	Mnemonic	Bit	Description	
(7130h)	C_IRQ_MASK[7:0]	7:0	Mask for IRQ, bit [31:0]. 1: Mask. 0: Not mask.	
4Ch (7131h)	**REG7131**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_IRQ_MASK[15:8]	7:0	See description of '7130h'.	
4Dh (7134h)	**REG7134**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_IRQ_MASK[23:16]	7:0	See description of '7130h'.	
4Dh (7135h)	**REG7135**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_IRQ_MASK[31:24]	7:0	See description of '7130h'.	
50h (7140h)	**REG7140**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_FORCE[7:0]	7:0	Force for IRQ, bit [31:0]. 1: Force. 0: Not force.	
50h (7141h)	**REG7141**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_FORCE[15:8]	7:0	See description of '7140h'.	
51h (7144h)	**REG7144**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_FORCE[23:16]	7:0	See description of '7140h'.	
51h (7145h)	**REG7145**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_FORCE[31:24]	7:0	See description of '7140h'.	
54h (7150h)	**REG7150**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_SEL_HL_TRIGGER[7:0]	7:0	Select H or L trigger, bit [31:0]. Inverse source polarity for IRQ.	
54h (7151h)	**REG7151**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_SEL_HL_TRIGGER[15:8]	7:0	See description of '7150h'.	
55h (7154h)	**REG7154**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_SEL_HL_TRIGGER[23:16]	7:0	See description of '7150h'.	
55h (7155h)	**REG7155**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_SEL_HL_TRIGGER[31:24]	7:0	See description of '7150h'.	
58h (7160h)	**REG7160**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS[7:0]	7:0	IRQ Raw Status, bit [63:0]. Interrupt source status for IRQ.	
58h (7161h)	**REG7161**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS[15:8]	7:0	See description of '7160h'.	
59h	**REG7164**	**7:0**	**Default : 0x00**	**Access : RO**

IRQ Register (Bank = 38)

Index (Absolute)	Mnemonic	Bit	Description	
(7164h)	IRQ_RAW_STATUS[23:16]	7:0	See description of '7160h'.	
59h (7165h)	**REG7165**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS[31:24]	7:0	See description of '7160h'.	
5Ah (7168h)	**REG7168**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS[39:32]	7:0	See description of '7160h'.	
5Ah (7169h)	**REG7169**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS[47:40]	7:0	See description of '7160h'.	
5Bh (716Ch)	**REG716C**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS[55:48]	7:0	See description of '7160h'.	
5Bh (716Dh)	**REG716D**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS[63:56]	7:0	See description of '7160h'.	
5Ch (7170h)	**REG7170**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS[7:0]	7:0	IRQ Final Status, bit [63:0]. Final interrupt status for IRQ.	
5Ch (7171h)	**REG7171**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS[15:8]	7:0	See description of '7170h'.	
5Dh (7174h)	**REG7174**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS[23:16]	7:0	See description of '7170h'.	
5Dh (7175h)	**REG7175**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS[31:24]	7:0	See description of '7170h'.	
5Eh (7178h)	**REG7178**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS[39:32]	7:0	See description of '7170h'.	
5Eh (7179h)	**REG7179**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS[47:40]	7:0	See description of '7170h'.	
5Fh (717Ch)	**REG717C**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS[55:48]	7:0	See description of '7170h'.	
5Fh (717Dh)	**REG717D**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS[63:56]	7:0	See description of '7170h'.	
60h (7180h)	**REG7180**	**7:0**	**Default : 0xFF**	**Access : R/W**
	FIQ2IRQOUT[7:0]	7:0	Select FIQ source output to IRQ.	
60h (7181h)	**REG7181**	**7:0**	**Default : 0xFF**	**Access : R/W**
	FIQ2IRQOUT[15:8]	7:0	See description of '7180h'.	
61h	**REG7184**	**7:0**	**Default : 0xFF**	**Access : R/W**

IRQ Register (Bank = 38)

Index (Absolute)	Mnemonic	Bit	Description	
(7184h)	FIQ2IRQOUT[23:16]	7:0	See description of '7180h'.	
61h (7185h)	**REG7185**	**7:0**	**Default : 0xFF**	**Access : R/W**
	FIQ2IRQOUT[31:24]	7:0	See description of '7180h'.	
62h (7188h)	**REG7188**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_IDX[7:0]	7:0	FIQ index for first priority source.	
63h (718Ch)	**REG718C**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_IDX[7:0]	7:0	IRQ index for first priority source.	
64h (7190h)	**REG7190**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPARE0[7:0]	7:0	Spare register.	
64h (7191h)	**REG7191**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPARE1[7:0]	7:0	Spare register.	

SARADC Register (Bank = 3A)

SARADC Register (Bank = 3A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (7400h)	**REG7400**	**7:0**	**Default : 0x01**	**Access : R/W**
	MUXSEL[2:0]	7:5	Positive signal input select.	
	AUTO_SWITCH	4	Channel auto-switch.	
	FREERUN	3	Saradc FREERUN control.	
	ONESHOT	2	Saradc ONESHOT control.	
	PORZ	1	Saradc digital reset, low active. When PORZ=0, 1.2V logic in saradc will be reset.	
	PD	0	Saradc power down. When PD = 1, saradc power down.	
00h (7401h)	**REG7401**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SPARE0[2:0]	7:5	3-bit spare cell.	
	SAMPLE_FLAG	4	Data sample flag.	
	MUXNSEL[2:0]	3:1	Negative signal input select.	
	SAMPLE_RDY	0	Data sample ready.	
01h (7404h)	**REG7404**	**7:0**	**Default : 0xFF**	**Access : R/W**
	CH3_AVG_MODE[1:0]	7:6	Channel 3 data-out select.	
	CH2_AVG_MODE[1:0]	5:4	Channel 2 data-out select.	
	CH1_AVG_MODE[1:0]	3:2	Channel 1 data-out select.	
	CH0_AVG_MODE[1:0]	1:0	Channel 0 data-out select. 2'b00: no average. 2'b01: 2 stages average. 2'b10: 4 stages average. 2'b11: 8 stages average.	
01h (7405h)	**REG7405**	**7:0**	**Default : 0xFF**	**Access : R/W**
	CH7_AVG_MODE[1:0]	7:6	Channel 7 data-out select.	
	CH6_AVG_MODE[1:0]	5:4	Channel 6 data-out select.	
	CH5_AVG_MODE[1:0]	3:2	Channel 5 data-out select.	
	CH4_AVG_MODE[1:0]	1:0	Channel 4 data-out select.	
02h (7408h)	**REG7408**	**7:0**	**Default : 0x05**	**Access : R/W**
	OS0_PRD[7:0]	7:0	Channel 0 one shot pulse width = 4 * OS0_PRD (clk cycle).	
02h (7409h)	**REG7409**	**7:0**	**Default : 0x05**	**Access : R/W**
	OS1_PRD[7:0]	7:0	Channel 1 one shot pulse width.	
03h	**REG740C**	**7:0**	**Default : 0x50**	**Access : R/W**

SARADC Register (Bank = 3A)

Index (Absolute)	Mnemonic	Bit	Description	
(740Ch)	OS2_PRD[7:0]	7:0	Channel 2 one shot pulse width.	
03h (740Dh)	**REG740D**	**7:0**	**Default : 0x05**	**Access : R/W**
	OS3_PRD[7:0]	7:0	Channel 3 one shot pulse width.	
04h (7410h)	**REG7410**	**7:0**	**Default : 0x05**	**Access : R/W**
	OS4_PRD[7:0]	7:0	Channel 4 one shot pulse width.	
04h (7411h)	**REG7411**	**7:0**	**Default : 0x05**	**Access : R/W**
	OS5_PRD[7:0]	7:0	Channel 5 one shot pulse width.	
05h (7414h)	**REG7414**	**7:0**	**Default : 0x50**	**Access : R/W**
	OS6_PRD[7:0]	7:0	Channel 6 one shot pulse width.	
05h (7415h)	**REG7415**	**7:0**	**Default : 0x50**	**Access : R/W**
	OS7_PRD[7:0]	7:0	Channel 7 one shot pulse width.	
06h (7418h)	**REG7418**	**7:0**	**Default : 0x00**	**Access : RO**
	SAR_DOUT_DFT[7:0]	7:0	Saradc raw data out.	
06h (7419h)	**REG7419**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	TEST[3:0]	7:4	Saradc TEST bits.	
	SAR_SAMP_DFT	3	Saradc raw samp.	
	SAR_EOC_DFT	2	Saradc raw eoc.	
	SAR_DOUT_DFT[9:8]	1:0	See description of '7418h'.	
07h (741Ch)	**REG741C**	**7:0**	**Default : 0x00**	**Access : RO**
	CH0_DOUT[7:0]	7:0	Saradc channel 0 data out.	
07h (741Dh)	**REG741D**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SPARE7[15:10]	7:2	6-bit spare cell.	
	CH0_DOUT[9:8]	1:0	See description of '741Ch'.	
08h (7420h)	**REG7420**	**7:0**	**Default : 0x00**	**Access : RO**
	CH1_DOUT[7:0]	7:0	Saradc channel 1 data out.	
08h (7421h)	**REG7421**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SPARE8[15:10]	7:2	6-bit spare cell.	
	CH1_DOUT[9:8]	1:0	See description of '7420h'.	
09h (7424h)	**REG7424**	**7:0**	**Default : 0x00**	**Access : RO**
	CH2_DOUT[7:0]	7:0	Saradc channel 2 data out.	
09h (7425h)	**REG7425**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SPARE9[15:10]	7:2	6-bit spare cell.	
	CH2_DOUT[9:8]	1:0	See description of '7424h'.	

SARADC Register (Bank = 3A)

Index (Absolute)	Mnemonic	Bit	Description	
10h (7440h)	**REG7440**	**7:0**	**Default : 0x00**	**Access : RO**
	CH3_DOUT[7:0]	7:0	Saradc channel 3 data out.	
10h (7441h)	**REG7441**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SPARE10[15:10]	7:2	6-bit spare cell.	
	CH3_DOUT[9:8]	1:0	See description of '7440h'.	
11h (7444h)	**REG7444**	**7:0**	**Default : 0x00**	**Access : RO**
	CH4_DOUT[7:0]	7:0	Saradc channel 4 data out.	
11h (7445h)	**REG7445**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SPARE11[15:10]	7:2	6-bit spare cell.	
	CH4_DOUT[9:8]	1:0	See description of '7444h'.	
12h (7448h)	**REG7448**	**7:0**	**Default : 0x00**	**Access : RO**
	CH5_DOUT[7:0]	7:0	Saradc channel 5 data out.	
12h (7449h)	**REG7449**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SPARE12[15:10]	7:2	6-bit spare cell.	
	CH5_DOUT[9:8]	1:0	See description of '7448h'.	
13h (744Ch)	**REG744C**	**7:0**	**Default : 0x00**	**Access : RO**
	CH6_DOUT[7:0]	7:0	Saradc channel 6 data out.	
13h (744Dh)	**REG744D**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SPARE13[15:10]	7:2	6-bit spare cell.	
	CH6_DOUT[9:8]	1:0	See description of '744Ch'.	
14h (7450h)	**REG7450**	**7:0**	**Default : 0x00**	**Access : RO**
	CH7_DOUT[7:0]	7:0	Saradc channel 7 data out.	
14h (7451h)	**REG7451**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SPARE14[15:10]	7:2	6-bit spare cell.	
	CH7_DOUT[9:8]	1:0	See description of '7450h'.	
15h (7454h)	**REG7454**	**7:0**	**Default : 0xFF**	**Access : R/W**
	CH_SEL[7:0]	7:0	Select enable channels when auto-switch.	
15h (7455h)	**REG7455**	**7:0**	**Default : 0x00**	**Access : RO**
	SPARE15[6:0]	7:1	7-bit spare cell.	
	FLAG_AUXC1	0	PAD_AUXC1 flag. 1: PAD_AUXC1 voltage is too high. 0: Normal.	
16h	**REG7458**	**7:0**	**Default : 0x0F**	**Access : RO, R/W**

SARADC Register (Bank = 3A)

Index (Absolute)	Mnemonic	Bit	Description
(7458h)	STATE_OBV[3:0]	7:4	Dtop FSM observe.
	AUXI_CTRL[1:0]	3:2	AUX current control. 2'b00: 20uA. 2'b01: 40uA. 2'b10: 80uA. 2'b11: 160uA.
	AUXI_SEL	1	AUX current output pad select. 1'b1: PAD_AUXC1. 1'b0: PAD_AUXC0.
	PD_AUXI	0	Power down AUX current output. 1: Power down. 0: Output AUX current.
16h (7459h)	**REG7459**	**7:0**	**Default : 0x00** **Access : RO, R/W**
	SPARE16[3:0]	7:4	4-bit spare cell.
	STATE_OBV[7:4]	3:0	See description of '7458h'.

UART0 Register (Bank = 3B)

UART0 Register (Bank = 3B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (7600h)	**REG7600**	**7:0**	**Default : 0x00**	**Access : R/W**
	THR_RBR_DLL[7:0]	7:0	1. When "reg_lcr_dl_access"=0. Write: Transmitter Holding Register. Write transmit FIFO; Note that Writing data to a full FIFO results in the write data being lost. Read: Receiver Buffer. Read receive FIFO; Note that any incoming data are lost whenFIFO is full and an overrun error occurs. 2. When "reg_lcr_dl_access" = 1. Divisor Latch LSB.	
02h (7608h)	**REG7608**	**7:0**	**Default : 0x00**	**Access : R/W**
	IER_DLH[7:0]	7:0	1. When "reg_lcr_dl_access" = 0. Interrupt Enable Registers (IER); 1: enabled. Bit [0]: Received Data Available Interrupt and Character Timeout Interrupt. Bit [1]: Transmitter Holding Register Empty Interrupt. Bit [2]: Receiver Line Status Interrupt. Bit [3]: Modem Status interrupt. Bit [7]: Programmable THRE Interrupt. 2. When "reg_lcr_dl_access" = 1. Divisor Latch MSB. Boud rate = (serial clock freq.) / (16 * divisor).	
04h (7610h)	**REG7610**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCR_IIR[7:0]	7:0	1. Write. FIFO Control Register (FCR). Bit [0]: FIFO enable. Bit [1]: write "1" to clear RX FIFO. Bit [2]: write "1" to clear TX FIFO. Bit [5:4]: Transmit FIFO Empty trigger level. "00" - FIFO empty; "01" - 2 characters in the FIFO; "10" - FIFO 1/4 full; "11" - FIFO 1/2 full;	

UART0 Register (Bank = 3B)

Index (Absolute)	Mnemonic	Bit	Description
			Bit [7:6]: Receiver FIFO Interrupt trigger level. "00" - 1 character in the FIFO; "01" - FIFO 1/4 full; "10" - FIFO 1/2 full; "11" - FIFO 2 less than full. 2. Read. Interrupt Identification Registers (IIR). Bit [0]: 1: no interrupt is pending. Bit [3:1]: interrupt identify. "110" - character timeout. "011" - Receiver Line Status. "010" - Receiver Data Available. "001" - Transmitter Holding Register empty. "000" - Modem Status.
06h (7618h)	**REG7618**	**7:0**	**Default : 0x03** **Access : R/W**
	LCR_DL_ACCESS	7	Divisor Latch Access; 1: The divisor latches can be accessed.
	-	6:5	Reserved.
	LCR_EVEN_PARITY_SEL	4	1: Select even parity.
	LCR_PARITY_EN	3	1: Generate parity bit on serial out.
	LCR_STOP_BITS	2	Specify the number of stop bits. "0" - 1 stop bit; "1" - 1.5 stop bits when 5-bit character length selected and 2 bits otherwise.
	LCR_CHAR_BITS[1:0]	1:0	Select number of bits in each character. "00" - 5 bits; "01" - 6 bits; "10" - 7 bits; "11" - 8 bits.
08h (7620h)	**REG7620**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:6	Reserved.
	MCR_AFCE	5	Auto Flow Control Enable; 1: enable.
	MCR_LOOPBACK	4	1: Loopback mode. SOUT -> SIN. RTS-> CTS.
	-	3:2	Reserved.
	MCR_RTS	1	Request To Send (RTS) signal control. "0" - RTS is "1"; "1" - RTS is "0".
	-	0	Reserved.

UART0 Register (Bank = 3B)

Index (Absolute)	Mnemonic	Bit	Description	
0Ah (7628h)	**REG7628**	**7:0**	**Default : 0x00**	**Access : RO**
	LSR_ERROR	7	Receiver FIFO Error bit.	
	LSR_TX_EMPTY	6	1: Transmitter (tx FIFO and shift registers) Empty indicator. Clear after writing data into tx FIFO.	
	LSR_TXFIFO_EMPTY	5	1: Transmit FIFO is empty. Clear after writing data into tx FIFO; Gen a Transmitter Holding Register Empty interrupt.	
	-	4	Reserved.	
	LSR_FE	3	1: Framing Error indicator. Clear when reading; Gen a Receiver Line Status interrupt.	
	LSR_PE	2	1: Parity Error indicator. Clear when reading; Gen a Receiver Line Status interrupt.	
	LSR_OE	1	1: RX Overrun Error indicator. Clear when reading; Gen a Receiver Line Status interrupt.	
	LSR_DR	0	1: Received Data Ready indicator.	
0Ch (7630h)	**REG7630**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	MSR_CTS_COMP	4	Complement of "CTS" or equal to "RTS" in loopback.	
	-	3:1	Reserved.	
	MSR_DCTS	0	Delta Clear To Send (DCTS) indicator. "1" - the "CTS" line has changed its state. Clear when reading.	
0Eh (7638h)	**REG7638**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	USR_BUSY	0	UART busy.	

UART1 Register (Bank = 3B)

UART1 Register (Bank = 3B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
20h (7680h)	**REG7680**	**7:0**	**Default : 0x00**	**Access : R/W**
	THR_RBR_DLL[7:0]	7:0	1. When "reg_lcr_dl_access" = 0. Write: Transmitter Holding Register. Write transmit FIFO; Note that Writing data to a full FIFO results in the write data being lost. Read: Receiver Buffer. Read receive FIFO; Note that any incoming data are lost whenFIFO is full and an overrun error occurs. 2. When "reg_lcr_dl_access" = 1. Divisor Latch LSB.	
22h (7688h)	**REG7688**	**7:0**	**Default : 0x00**	**Access : R/W**
	IER_DLH[7:0]	7:0	1. When "reg_lcr_dl_access" = 0. Interrupt Enable Registers (IER); 1: enabled. Bit [0]: Received Data Available Interrupt and Character Timeout Interrupt. Bit [1]: Transmitter Holding Register Empty Interrupt. Bit [2]: Receiver Line Status Interrupt. Bit [3]: Modem Status interrupt. Bit [7]: Programmable THRE Interrupt. 2. When "reg_lcr_dl_access" = 1. Divisor Latch MSB. Boud rate = (serial clock freq.) / (16 * divisor).	
24h (7690h)	**REG7690**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCR_IIR[7:0]	7:0	1. Write. FIFO Control Register (FCR). Bit [0]: FIFO enable. Bit [1]: write "1" to clear RX FIFO. Bit [2]: write "1" to clear TX FIFO. Bit [5:4]: Transmit FIFO Empty trigger level. "00" - FIFO empty; "01" - 2 characters in the FIFO; "10" - FIFO 1/4 full; "11" - FIFO 1/2 full;	

UART1 Register (Bank = 3B)

Index (Absolute)	Mnemonic	Bit	Description	
			Bit [7:6]: Receiver FIFO Interrupt trigger level. "00" - 1 character in the FIFO; "01" - FIFO 1/4 full; "10" - FIFO 1/2 full; "11" - FIFO 2 less than full. 2. Read. Interrupt Identification Registers (IIR). Bit [0]: 1: no interrupt is pending. Bit [3:1]: interrupt identify. "110" - character timeout. "011" - Receiver Line Status. "010" - Receiver Data Available. "001" - Transmitter Holding Register empty. "000" - Modem Status.	
26h (7698h)	**REG7698**	**7:0**	**Default : 0x03**	**Access : R/W**
	LCR_DL_ACCESS	7	Divisor Latch Access; 1: The divisor latches can be accessed.	
	-	6:5	Reserved.	
	LCR_EVEN_PARITY_SEL	4	1: Select even parity.	
	LCR_PARITY_EN	3	1: Generate parity bit on serial out.	
	LCR_STOP_BITS	2	Specify the number of stop bits. "0" - 1 stop bit; "1" - 1.5 stop bits when 5-bit character length selected and 2 bits otherwise.	
	LCR_CHAR_BITS[1:0]	1:0	Select number of bits in each character. "00" - 5 bits; "01" - 6 bits; "10" - 7 bits; "11" - 8 bits.	
28h (76A0h)	**REG76A0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MCR_AFCE	5	Auto Flow Control Enable; 1: enable.	
	MCR_LOOPBACK	4	1: Loopback mode. SOUT -> SIN. RTS-> CTS.	
	-	3:2	Reserved.	
	MCR_RTS	1	Request To Send (RTS) signal control. "0" - RTS is "1"; "1" - RTS is "0".	
	-	0	Reserved.	

UART1 Register (Bank = 3B)

Index (Absolute)	Mnemonic	Bit	Description	
2Ah (76A8h)	**REG76A8**	**7:0**	**Default : 0x00**	**Access : RO**
	LSR_ERROR	7	Receiver FIFO Error bit.	
	LSR_TX_EMPTY	6	1: Transmitter (tx FIFO and shift registers) Empty indicator. Clear after writing data into tx FIFO.	
	LSR_TXFIFO_EMPTY	5	1: Transmit FIFO is empty. Clear after writing data into tx FIFO. Gen a Transmitter Holding Register Empty interrupt.	
	-	4	Reserved.	
	LSR_FE	3	1: Framing Error indicator. Clear when reading; Gen a Receiver Line Status interrupt.	
	LSR_PE	2	1: Parity Error indicator. Clear when reading; Gen a Receiver Line Status interrupt.	
	LSR_OE	1	1: RX Overrun Error indicator. Clear when reading; Gen a Receiver Line Status interrupt.	
	LSR_DR	0	1: Received Data Ready indicator.	
2Ch (76B0h)	**REG76B0**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	MSR_CTS_COMP	4	Complement of "CTS" or equal to "RTS" in loopback.	
	-	3:1	Reserved.	
	MSR_DCTS	0	Delta Clear To Send (DCTS) indicator. "1" - the "CTS" line has changed its state. Clear when reading.	
2Eh (76B8h)	**REG76B8**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	USR_BUSY	0	UART busy.	
30 (76C0h~ 76C8h)		**7:0**	**Default : 0x00**	**Access : -**
		7:1	Reserved.	

UART2 Register (Bank = 3B)

UART2 Register (Bank = 3B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
40h (7700h)	**REG7700**	**7:0**	**Default : 0x00**	**Access : R/W**
	THR_RBR_DLL[7:0]	7:0	1. When "reg_lcr_dl_access" = 0. Write: Transmitter Holding Register. Write transmit FIFO; Note that Writing data to a full FIFO results in the write data being lost. Read: Receiver Buffer. Read receive FIFO; Note that any incoming data are lost when FIFO is full and an overrun error occurs. 2. When "reg_lcr_dl_access" = 1. Divisor Latch LSB.	
42h (7708h)	**REG7708**	**7:0**	**Default : 0x00**	**Access : R/W**
	IER_DLH[7:0]	7:0	1. When "reg_lcr_dl_access" = 0. Interrupt Enable Registers (IER); 1: enabled. Bit [0]: Received Data Available Interrupt and Character Timeout Interrupt. Bit [1]: Transmitter Holding Register Empty Interrupt. Bit [2]: Receiver Line Status Interrupt. Bit [3]: Modem Status interrupt. Bit [7]: Programmable THRE Interrupt. 2. When "reg_lcr_dl_access" = 1. Divisor Latch MSB. Boud rate = (serial clock freq.) / (16 * divisor).	
44h	**REG7710**	**7:0**	**Default : 0x00**	**Access : R/W**

UART2 Register (Bank = 3B)

Index (Absolute)	Mnemonic	Bit	Description
(7710h)	FCR_IIR[7:0]	7:0	1. Write. FIFO Control Register (FCR). Bit [0]: FIFO enable. Bit [1]: write "1" to clear RX FIFO. Bit [2]: write "1" to clear TX FIFO. Bit [5:4]: Transmit FIFO Empty trigger level. "00" - FIFO empty; "01" - 2 characters in the FIFO; "10" - FIFO 1/4 full; "11" - FIFO 1/2 full; Bit [7:6]: Receiver FIFO Interrupt trigger level. "00" - 1 character in the FIFO; "01" - FIFO 1/4 full; "10" - FIFO 1/2 full; "11" - FIFO 2 less than full. 2. Read. Interrupt Identification Registers (IIR). Bit [0]: 1: no interrupt is pending. Bit [3:1]: interrupt identify. "110" - character timeout. "011" - Receiver Line Status. "010" - Receiver Data Available. "001" - Transmitter Holding Register empty. "000" - Modem Status.
46h (7718h)	**REG7718**	**7:0**	**Default : 0x03** **Access : R/W**
	LCR_DL_ACCESS	7	Divisor Latch Access; 1: The divisor latches can be accessed.
	-	6:5	Reserved.
	LCR_EVEN_PARITY_SEL	4	1: Select even parity.
	LCR_PARITY_EN	3	1: Generate parity bit on serial out.
	LCR_STOP_BITS	2	Specify the number of stop bits. "0" - 1 stop bit; "1" - 1.5 stop bits when 5-bit character length selected and 2 bits otherwise.
	LCR_CHAR_BITS[1:0]	1:0	Select number of bits in each character. "00" - 5 bits; "01" - 6 bits; "10" - 7 bits; "11" - 8 bits.

UART2 Register (Bank = 3B)

Index (Absolute)	Mnemonic	Bit	Description	
48h (7720h)	**REG7720**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MCR_AFCE	5	Auto Flow Control Enable; 1: enable.	
	MCR_LOOPBACK	4	1: Loopback mode. SOUT -> SIN. RTS-> CTS.	
	-	3:2	Reserved.	
	MCR_RTS	1	Request To Send (RTS) signal control. "0" - RTS is "1"; "1" - RTS is "0".	
	-	0	Reserved.	
4Ah (7728h)	**REG7728**	**7:0**	**Default : 0x00**	**Access : RO**
	LSR_ERROR	7	Receiver FIFO Error bit.	
	LSR_TX_EMPTY	6	1: Transmitter (tx FIFO and shift registers) Empty indicator. Clear after writing data into tx FIFO.	
	LSR_TXFIFO_EMPTY	5	1: Transmit FIFO is empty. Clear after writing data into tx FIFO. Gen a Transmitter Holding Register Empty interrupt.	
	-	4	Reserved.	
	LSR_FE	3	1: Framing Error indicator. Clear when reading. Gen a Receiver Line Status interrupt.	
	LSR_PE	2	1: Parity Error indicator. Clear when reading. Gen a Receiver Line Status interrupt.	
	LSR_OE	1	1: RX Overrun Error indicator. Clear when reading. Gen a Receiver Line Status interrupt.	
	LSR_DR	0	1: Received Data Ready indicator.	
4Ch (7730h)	**REG7730**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	MSR_CTS_COMP	4	Complement of "CTS" or equal to "RTS" in loopback.	
	-	3:1	Reserved.	
	MSR_DCTS	0	Delta Clear To Send (DCTS) indicator. "1" - the "CTS" line has changed its state. Clear when reading.	

UART2 Register (Bank = 3B)

Index (Absolute)	Mnemonic	Bit	Description	
4Eh (7738h)	**REG7738**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	USR_BUSY	0	UART busy.	
50h (7740h)	**REG7740**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
52h (7748h)	**REG7784**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
54h (7750h)	**REG7750**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	SW_RSTZ	0	Software reset UART; 0: enable.	

TIMER1 Register (Bank = 3B)

TIMER1 Register (Bank = 3B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
60h (7780h)	**REG7780**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	TIMER_TRIG	1	Set: Enable timer counting one time (from 0 to max, then stop). Clear: By reset itself OR set reg_timer_en.	
	TIMER_EN	0	Set: Enable timer counting rolled (from 0 to max, then rolled). Clear: By reset itself OR set reg_timer_trig.	
60h (7781h)	**REG7781**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	TIMER_INT_EN	0	Set: Enable interrupt. Clear: By reset itself.	
61h (7784h)	**REG7784**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	TIMER_HIT	0	Assert: When counter enabled and matches reg_timer_max. Deassert: By write 1 OR set reg_timer_en, reg_timer_once, reg_timer_max.	
62h (7788h)	**REG7788**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TIMER_MAX[7:0]	7:0	Timer maximum value.	
62h (7789h)	**REG7789**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TIMER_MAX[15:8]	7:0	See description of '7788h'.	
63h (778Ch)	**REG778C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TIMER_MAX[23:16]	7:0	See description of '7788h'.	
63h (778Dh)	**REG778D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TIMER_MAX[31:24]	7:0	See description of '7788h'.	
64h (7790h)	**REG7790**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CAP[7:0]	7:0	Timer current value. Note: With non-32-bit-data system, please read from LSB.	
64h (7791h)	**REG7791**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CAP[15:8]	7:0	See description of '7790h'.	
65h (7794h)	**REG7794**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CAP[23:16]	7:0	See description of '7790h'.	

TIMER1 Register (Bank = 3B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
65h (7795h)	**REG7795**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CAP[31:24]	7:0	See description of '7790h'.	

TIMER2 Register (Bank = 3B)

TIMER2 Register (Bank = 3B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
70h (77C0h)	**REG77C0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	TIMER_TRIG	1	Set: Enable timer counting one time (from 0 to max, then stop). Clear: By reset itself OR set reg_timer_en.	
	TIMER_EN	0	Set: Enable timer counting rolled (from 0 to max, then rolled). Clear: By reset itself OR set reg_timer_trig.	
70h (77C1h)	**REG77C1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	TIMER_INT_EN	0	Set: Enable interrupt. Clear: By reset itself.	
71h (77C4h)	**REG77C4**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	TIMER_HIT	0	Assert: When counter enabled and matches reg_timer_max. Deassert: By write 1 OR set reg_timer_en, reg_timer_once, reg_timer_max.	
72h (77C8h)	**REG77C8**	**7:0**	**Default : 0Xff**	**Access : R/W**
	TIMER_MAX[7:0]	7:0	Timer maximum value.	
72h (77C9h)	**REG77C9**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TIMER_MAX[15:8]	7:0	See description of '77C8h'.	
73h (77CCh)	**REG77CC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TIMER_MAX[23:16]	7:0	See description of '77C8h'.	
73h (77CDh)	**REG77CD**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TIMER_MAX[31:24]	7:0	See description of '77C8h'.	
74h (77D0h)	**REG77D0**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CAP[7:0]	7:0	Timer current value. Note: With non-32-bit-data system, please read from LSB.	
74h (77D1h)	**REG77D1**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CAP[15:8]	7:0	See description of '77D0h'.	
75h (77D4h)	**REG77D4**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CAP[23:16]	7:0	See description of '77D0h'.	
75h (77D5h)	**REG77D5**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CAP[31:24]	7:0	See description of '77D0h'.	

PIU_MISC Register (Bank = 3C)

PIU_MISC Register (Bank = 3C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Dh (7834h)	**REG7834**	**7:0**	**Default : 0x00**	**Access : R/W**
	CRC_DUM_0D[7:0]	7:0	Bit[8] : xd2miu software reset. 1: Reset. 0: Not reset. Bit[10] :miu_size. 1: 512MB. 0: 128MB.	
0Dh (7835h)	**REG7835**	**7:0**	**Default : 0x00**	**Access : R/W**
	CRC_DUM_0D[15:8]	7:0	See description of '7834h'.	
7Dh (79F4h)	**REG79F4**	**7:0**	**Default : 0x00**	**Access : RO**
	TEST_RO1[7:0]	7:0		
7Dh (79F5h)	**REG79F5**	**7:0**	**Default : 0x00**	**Access : RO**
	TEST_RO1[15:8]	7:0	See description of '79F4h'.	
7Eh (79F8h)	**REG79F8**	**7:0**	**Default : 0x00**	**Access : RO**
	TEST_RO[7:0]	7:0		
7Eh (79F9h)	**REG79F9**	**7:0**	**Default : 0x00**	**Access : RO**
	TEST_RO[15:8]	7:0	See description of '79F8h'.	
7Fh (79FCh)	**REG79FC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	TEST_SEL[2:0]	2:0		

UART2_DMA Register (Bank = 3D)

UART2_DMA Register (Bank = 3D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (7A00h)	**REG7A00**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_SW_RST	7	RX Engine software reset. 0: De-assert. 1: Assert.	
	TX_SW_RST	6	TX Engine software reset. 0: De-assert. 1: Assert.	
	RX_ENDINA	5	Software select MIU read data, endian define. 0: MIU_Rdata[63:0] = {B7, B6, B5, B4, B3, B2, B1, B0}. 1: MIU_Rdata[63:0] = {B4, B5, B6, B7, B0, B1, B2, B3}.	
	TX_ENDINA	4	Software select MIU read data, endian define. 0: MIU_Rdata[63:0] = {B7, B6, B5, B4, B3, B2, B1, B0}. 1: MIU_Rdata[63:0] = {B4, B5, B6, B7, B0, B1, B2, B3}.	
	RX_URDMA_EN	3	URDMA RX Hardware Enable. 0: Disable. 1: Enable.	
	TX_URDMA_EN	2	URDMA TX Hardware Enable. 0: Disable. 1: Enable.	
	URDMA_MODE	1	URDMA Mode selects, when mode enable, URDMA hardware will replace MCU to access UART, otherwise MCU still control UART directly. 0: Disable. 1: Enable.	
	SW_RST	0	URDMA software reset. 0: De-assert. 1: Assert.	
00h (7A01h)	**REG7A01**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:6	Reserved.	
	RX_BUSY	5	RX controller in BUSY state.	
	TX_BUSY	4	TX controller in BUSY state.	
	RX_OP_MODE	3	RX controller operation mode. 0: Default. 1: Stop RX DMA activity when threshold interrupt occurs, until update RX_BUF_BASE.	

UART2_DMA Register (Bank = 3D)

Index (Absolute)	Mnemonic	Bit	Description	
	RESERVE [2:0]	2:0	Reserve.	
01h (7A04h)	**REG7A04**	**7:0**	**Default : 0x40**	**Access : R/W**
	INTR_THRESHOLD[7:0]	7:0	Interrupt threshold, to configure interrupt MCU period. Setting how much. Data received from UART, and alert MCU, byte unit.	
01h (7A05h)	**REG7A05**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	INTR_THRESHOLD[11:8]	3:0	See description of '7A04h'.	
02h (7A08h)	**REG7A08**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_BASE_H[7:0]	7:0	Configure TX buffer base address [31:16] in DRAM, 8byte unit.	
02h (7A09h)	**REG7A09**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_BASE_H[15:8]	7:0	See description of '7A08h'.	
03h (7A0Ch)	**REG7A0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_BASE_L[7:0]	7:0	Configure TX buffer base address [15:0] in DRAM, 8byte unit.	
03h (7A0Dh)	**REG7A0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_BASE_L[15:8]	7:0	See description of '7A0Ch'.	
04h (7A10h)	**REG7A10**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_SIZE[7:0]	7:0	Configure TX buffer size in DRAM, 8byte unit. Ex: BUF_SIZE = 0x400; access region between 0x000~0x3FF.	
04h (7A11h)	**REG7A11**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	TX_BUF_SIZE[12:8]	4:0	See description of '7A10h'.	
05h (7A14h)	**REG7A14**	**7:0**	**Default : 0x00**	**Access : RO**
	TX_BUF_RPTR[7:0]	7:0	Read TX buffer read pointer from URDMA, byte unit.	
05h (7A15h)	**REG7A15**	**7:0**	**Default : 0x00**	**Access : RO**
	TX_BUF_RPTR[15:8]	7:0	See description of '7A14h'.	
06h (7A18h)	**REG7A18**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_WPTR[7:0]	7:0	Update TX buffer write pointer to URDMA, byte unit.	
06h (7A19h)	**REG7A19**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_BUF_WPTR[15:8]	7:0	See description of '7A18h'.	
07h	**REG7A1C**	**7:0**	**Default : 0x0A**	**Access : R/W**

UART2_DMA Register (Bank = 3D)

Index (Absolute)	Mnemonic	Bit	Description	
(7A1Ch)	-	7:4	Reserved.	
	TX_TIMEOUT[3:0]	3:0	Configure TX time out value, to clean TX buffer data and send to UART. 2^(TX_TIMEOUT) Cycle unit.	
08h (7A20h)	**REG7A20**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_BUF_BASE_H[7:0]	7:0	Configure RX buffer base address [31:16] in DRAM, 8byte unit.	
08h (7A21h)	**REG7A21**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_BUF_BASE_H[15:8]	7:0	See description of '7A20h'.	
09h (7A24h)	**REG7A24**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_BUF_BASE_L[7:0]	7:0	Configure RX buffer base address [15:0] in DRAM, 8byte unit.	
09h (7A25h)	**REG7A25**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_BUF_BASE_L[15:8]	7:0	See description of '7A24h'.	
0Ah (7A28h)	**REG7A28**	**7:0**	**Default : 0x00**	**Access : R/W**
	RX_BUF_SIZE[7:0]	7:0	Configure RX buffer size in DRAM, 8byte unit. Ex: BUF_SIZE = 0x400; access region between 0x000~0x3FF.	
0Ah (7A29h)	**REG7A29**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	RX_BUF_SIZE[12:8]	4:0	See description of '7A28h'.	
0Bh (7A2Ch)	**REG7A2C**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_BUF_WPTR[7:0]	7:0	Read RX buffer write pointer from URDMA, byte unit.	
0Bh (7A2Dh)	**REG7A2D**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_BUF_WPTR[15:8]	7:0	See description of '7A2Ch'.	
0Ch (7A30h)	**REG7A30**	**7:0**	**Default : 0x0A**	**Access : R/W**
	-	7:4	Reserved.	
	RX_TIMEOUT[3:0]	3:0	Configure RX time out value, to clean UART RX FIFO and write to DRAM. 2^(RX_TIMEOUT) Cycle unit.	
0Dh (7A34h)	**REG7A34**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	RX_MCU_INTR	7	Identify rx controller to MCU interrupt event, this bit is logical OR of RX_INTR1~2 flag, and clear by RX_INTR_CLR.	
	RESERVE_A	6	Reserve.	

UART2_DMA Register (Bank = 3D)

Index (Absolute)	Mnemonic	Bit	Description	
	RX_INTR2	5	Identify Rx interrupt is cause by interrupt threshold function.	
	RX_INTR1	4	Identify Rx interrupt is cause by timeout function.	
	RESERVE	3	RESERVE.	
	RX_INTR2_EN	2	Rx interrupt threshold function enable.	
	RX_INTR1_EN	1	Rx timeout interrupt function enable.	
	RX_INTR_CLR	0	MCU clear rx control interrupt signal. Once write and auto clear.	
0Dh (7A35h)	**REG7A35**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	TX_MCU_INTR	7	Identify tx controller to MCU interrupt event.	
	RESERVE_B[4:0]	6:2	Reserve.	
	TX_INTR_EN	1	TX controller to MCU interrupt enable.	
	TX_INTR_CLR	0	MCU clear tx control interrupt signal. Once write and auto clear.	
0Eh (7A38h)	**REG7A38**	**7:0**	**Default : 0x00**	**Access : RO**
	RESERVE[7:0]	7:0	Reserve.	
0Eh (7A39h)	**REG7A39**	**7:0**	**Default : 0x00**	**Access : RO**
	RESERVE[15:8]	7:0	Reserve.	
0Fh (7A3Ch)	**REG7A3C**	**7:0**	**Default : 0x00**	**Access : RO**
	RESERVE[7:0]	7:0	Reserve.	
0Fh (7A3Dh)	**REG7A3D**	**7:0**	**Default : 0x00**	**Access : RO**
	RESERVE[15:8]	7:0	Reserve.	
10h (7A40h)	**REG7A40**	**7:0**	**Default : 0x01**	**Access : RO, R/W**
	RESERVE[4:0]	7:3	Reserve.	
	PREFCH_CLK_GATE1	2	Gated clock MINF post-write module. 0: Clock enable. 1: Clock gated.	
	PREFCH_CLK_GATE	1	Gated clock MINF pre-fetch module. 0: Clock enable. 1: Clock gated.	
	MINF_SW_RSTZ	0	MINF pre-fetch / post-write module SW reset. 0: SW reset. 1: Normal.	
10h	**REG7A41**	**7:0**	**Default : 0x00**	**Access : RO**

UART2_DMA Register (Bank = 3D)

Index (Absolute)	Mnemonic	Bit	Description	
(7A41h)	POSTWR_BUSY	7	Identify MINF post write in busy state.	
	RESERVE [11:5]	6:0	Reserve.	
11h (7A44h)	**REG7A44**	**7:0**	**Default : 0x46**	**Access : R/W**
	PREFCH_PATCH	7	SW patch control bit.	
	PREFCH_BLEN[1:0]	6:5	Define MINF DRAM access burst length. 0: Burst 16. 1: Burst 8. 2: Burst 4. 3: N/A.	
	PREFCH_PRI_SEL	4	SW control DRAM access priority signals select. 0: Depend on HW priority signal. 1: Depend on POSTWR_PRI.	
	PREFCH_PRI	3	Define DRAM access priority.	
	PREFCH_RASTRD	2	MINF pre-fetch fast read enable.	
	PREFCH_BYPASS	1	MINF bypass. 0: DRAM access through MINF module. 1: DRAM access bypass MINF module.	
	PREFCH_CLR	0	SW clear MINF pre-fetch buffer. 0: Normal. 1: Clear.	
11h (7A45h)	**REG7A45**	**7:0**	**Default : 0x46**	**Access : R/W**
	POSTWR_FLUSH1_PATCH	7	SW flush path.	
	POSTWR_BLEN[1:0]	6:5	Define MINF DRAM access burst length. 0: Burst 16. 1: Burst 8. 2: Burst 4. 3: N/A.	
	POSEWR_PRI_SEL	4	SW control DRAM access priority signals select. 0: Depend on HW priority signal. 1: Depend on POSTWR_PRI.	
	POSTWR_PRI	3	Define DRAM access priority.	
	POSTWR_FLUSH_SW	2	SW flush path.	
	POSTWR_BYPASS	1	MINF bypass. 0: DRAM access through MINF module. 1: DRAM access bypass MINF module.	

UART2_DMA Register (Bank = 3D)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	POSTWR_FLUSH	0	SW flush MINF post write buffer. 0: Normal. 1: Flush.

PMU Register (Bank = 3F)

PMU Register (Bank = 3F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (7E00h)	**REG7E00**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	LDOVWIFI_PG	6	LDO power good.	
	LDOVLCM_PG	5	LDO power good.	
	LDOVMEM_PG	4	LDO power good.	
	-	3	Reserved.	
	LDOVPER3_PG	2	LDO power good.	
	LDOVPER2_PG	1	LDO power good.	
	LDOVPER1_PG	0	LDO power good.	
00h (7E01h)	**REG7E01**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	LDO_ERR_INT	6	Ldo vmem vlcm vio vper1/2/3 has an error.	
	-	5:0	Reserved.	
01h (7E04h)	**REG7E04**	**7:0**	**Default : 0x11**	**Access : R/W**
	LDOVMEM_D_TIME[1:0]	7:6	Suspend mode turn-off delay time. 00: 0us. 01: 250us. 10: 500us. 11: 1ms.	
	LDOVMEM_S_LQ	5	Enable ldo_vmem LQ mode in suspend mode.	
	LDOVMEM_S_EN	4	Enable ldo_vmem in suspend mode, default = 1.	
	-	3:2	Reserved.	
	LDOVMEM_A_LQ	1	Enable ldo_vmem LQ mode in active mode.	
	LDOVMEM_A_EN	0	Enable ldo_vmem in active mode, default = 1.	
01h (7E05h)	**REG7E05**	**7:0**	**Default : 0x21**	**Access : R/W**
	LDOVLCM_D_TIME[1:0]	7:6	Suspend mode turn-off delay time. 00: 0us. 01: 250us. 10: 500us. 11: 1ms.	
	LDOVLCM_S_LQ	5	Enable ldo_vlcm LQ mode in suspend mode.	
	LDOVLCM_S_EN	4	Enable ldo_vlcm in suspend mode, default = 0.	

PMU Register (Bank = 3F)

Index (Absolute)	Mnemonic	Bit	Description	
	LDOVLCM_VSET[1:0]	3:2	Select output voltage level, // default from efuse[23:22],. Can be over write by set reg_level_ov_en=1. [00]: 3.2V (default). [01]: 2.9V. [10]: 2.8V. [11]: 1.8V.	
	LDOVLCM_A_LQ	1	Enable ldo_vlcm LQ mode in active mode.	
	LDOVLCM_A_EN	0	Enable ldo_vlcm in active mode, default = 1.	
02h (7E08h)	**REG7E08**	**7:0**	**Default : 0x20**	**Access : R/W**
	LDOVWIFI_D_TIME[1:0]	7:6	Suspend mode turn-off delay time. 00: 0us. 01: 250us. 10: 500us. 11: 1ms.	
	LDOVWIFI_S_LQ	5	Enable ldo_vwifi LQ mode in suspend mode.	
	LDOVWIFI_S_EN	4	Enable ldo_vwifi in suspend mode, default = 0.	
	LDOVWIFI_VSET[1:0]	3:2	Select output voltage level, (user ldo_150m_hv). [00]: 3.2V (default). [01]: 2.9V. [10]: 1.8V. [11]: 1.2V.	
	LDOVWIFI_A_LQ	1	Enable ldo_vwifi LQ mode in active mode.	
	LDOVWIFI_A_EN	0	Enable ldo_vwifi in active mode, default = 0.	
03h (7E0Ch)	**REG7E0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUSPD_PASSWD[7:0]	7:0	Set the password to make the master FSM into the suspend mode.	
03h (7E0Dh)	**REG7E0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUSPD_PASSWD[15:8]	7:0	See description of '7E0Ch'.	
04h (7E10h)	**REG7E10**	**7:0**	**Default : 0x00**	**Access : RO**
	GPIO_G_IN[7:0]	7:0	The PAD_Cs of GPIO.	
04h (7E11h)	**REG7E11**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	GPIO_G_IN[12:8]	4:0	See description of '7E10h'.	
05h (7E14h)	**REG7E14**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

PMU Register (Bank = 3F)

Index (Absolute)	Mnemonic	Bit	Description	
	LDOVWIFI_ERR_EN	6	Enable LDO power good error interrupt.	
	LDOVLCM_ERR_EN	5	Enable LDO power good error interrupt.	
	LDOVMEM_ERR_EN	4	Enable LDO power good error interrupt.	
	-	3	Reserved.	
	LDOVPER3_ERR_EN	2	Enable LDO power good error interrupt.	
	LDOVPER2_ERR_EN	1	Enable LDO power good error interrupt.	
	LDOVPER1_ERR_EN	0	Enable LDO power good error interrupt.	
06h (7E18h)	**REG7E18**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	NOBAT_INT	7	On battery detection interrupt.	
	BATDET	6	Battery detection flag.	
	TEST_BATDET[1:0]	5:4	Battery detection test.	
	EN_BATDET	3	Enable battery detection. 0: Disable 1: enable.	
	BATDET_DEBOUNCE[2:0]	2:0	Battery detection debounce time. 000: 0.1us 100: 5us. 001: 0.6us 101: 10us. 010: 1.2us 110: 20us. 011: 2.4us 111: 40us.	
07h (7E1Ch)	**REG7E1C**	**7:0**	**Default : 0x60**	**Access : R/W**
	-	7	Reserved.	
	BK2_REFGEN_S_EN	6	Enable buck2 refgen in suspend mode.	
	BK2_REFGEN_A_EN	5	Enable buck2 refgen in active mode.	
	-	4:0	Reserved.	
08h (7E20h)	**REG7E20**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	REF_OTP	7	Refgen OTP flag.	
	EN_VERFOTP_TST	6	VREF of OTP test enable.	
	-	5:4	Reserved.	
	OTP_VTH[1:0]	3:2	Reference gen OTP VTH selection. 00: 428mV, 150degC. 01: 448mV, 140degC. 10: 468mV, 130degC. 11: 408mV, 160degC.	
	EN_OTP	1	Reference gen OTP enable control. 0: OFF 1:ON.	

PMU Register (Bank = 3F)

Index (Absolute)	Mnemonic	Bit	Description	
	VREF_TST	0	VREF test enable. 0: Disable (default). 1: Enable.	
08h (7E21h)	**REG7E21**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	TEST_I[4:0]	5:1	Register to mux test current to AUX.	
	TEMP_MEASURE	0	Enable the test bench for OTP.	
0Ah (7E28h)	**REG7E28**	**7:0**	**Default : 0x20**	**Access : RO, R/W**
	AUTOTRIM_BIT[1:0]	7:6	Auto trimming bits result. Initial value: 6'b100000.	
	EFUSETRIM_BIT[5:0]	5:0	Bandgap trimming bits. Big3 read efuse values from asura and load at this register.	
0Ah (7E29h)	**REG7E29**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	REFTRIM_OUT	6	Bandgap trimming out bit.	
	EN_REFTRIM	5	Bandgap trimming enable.	
	TRIMBIT_SEL	4	Trimming bit selection. 0: Reg_autotrim_bit. 1: Reg_efusetrim_bit.	
	AUTOTRIM_BIT[5:2]	3:0	See description of '7E28h'.	
0Bh (7E2Ch)	**REG7E2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWRHLD_PASSWD[7:0]	7:0	Power hold password register: cpu need to set this password when the first power on. 8'h5A: active to off. 8'hA5: power hold to active.	
0Bh (7E2Dh)	**REG7E2D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	PMU_SUSPEND_FLAG	1	Pmu suspend flag.	
	PMU_ACTIVE_FLAG	0	Pmu active flag.	
0Ch (7E30h)	**REG7E30**	**7:0**	**Default : 0x00**	**Access : R/W**
	WAIT_TIME[7:0]	7:0	Set wait time for exit sleep mode.	
0Ch (7E31h)	**REG7E31**	**7:0**	**Default : 0x00**	**Access : R/W**
	WAIT_TIME[15:8]	7:0	See description of '7E30h'.	
0Dh	**REG7E34**	**7:0**	**Default : 0x00**	**Access : RO**

PMU Register (Bank = 3F)

Index (Absolute)	Mnemonic	Bit	Description	
(7E34h)	WAKEUP_SRC_OUT_VAL[7:0]	7:0	Pmu wakeup source output value. [15]: USB_CID_OUT. [14]: MS_INS_OUT. [13]: SD_CDZ_OUT. [12:2]:GPIO_OUT. [1]: KEY0_OUT. [0]: TP_OUT.	
0Dh (7E35h)	**REG7E35**	**7:0**	**Default : 0x00**	**Access : RO**
	WAKEUP_SRC_OUT_VAL[15:8]	7:0	See description of '7E34h'.	
0Eh (7E38h)	**REG7E38**	**7:0**	**Default : 0x00**	**Access : RO**
	PMU_STATE[7:0]	7:0	Pmu fsm state. [0]: DDR3 or not. [4]: Charger short or not. [5]: Buck1 once bad or not.	
0Eh (7E39h)	**REG7E39**	**7:0**	**Default : 0x00**	**Access : RO**
	PMU_STATE[15:8]	7:0	See description of '7E38h'.	
0Fh (7E3Ch)	**REG7E3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	DDR_CTRL_VAL	6	DDR I/O control under self-refresh mode. 0: Non-gating DDR I/O. 1: Gating DDR I/O.	
	DDR_CTRL_SEL	5	DDR I/O control under self-refresh mode. 0: PM atop control. 1: SW register control.	
	SLFRSH_CTRL	4	DDR I/O control. 0: Normal path. 1: Self-refresh path.	
	DBBUS_SEL[3:0]	3:0	Debug bus selection.	
0Fh (7E3Dh)	**REG7E3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CLSDINMUX[5:0]	5:0	ClassD mux.	
10h (7E40h)	**REG7E40**	**7:0**	**Default : 0x00**	**Access : R/W**
	RIU_CKSUM_PROT_OFF[7:0]	7:0	Key to off riu_cksum_prot (h51685168).	
10h (7E41h)	**REG7E41**	**7:0**	**Default : 0x00**	**Access : R/W**
	RIU_CKSUM_PROT_OFF[15:8]	7:0	See description of '7E40h'.	
11h	**REG7E44**	**7:0**	**Default : 0x00**	**Access : R/W**

PMU Register (Bank = 3F)

Index (Absolute)	Mnemonic	Bit	Description	
(7E44h)	RIU_CKSUM_PROT_OFF[23:16]	7:0	See description of '7E40h'.	
11h (7E45h)	**REG7E45**	**7:0**	**Default : 0x00**	**Access : R/W**
	RIU_CKSUM_PROT_OFF[31:24]	7:0	See description of '7E40h'.	
13h (7E4Ch)	**REG7E4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VBST_PWM	7	Boost PWM control by host when VBST_PWM_en=0.	
	VBST_PWM_EN	6	Boost internal PWM enable. 0: Disable 1: enable.	
	VBST_PWM_PERIOD	5	Boost PWM Ferequence select. QOFF: (0:200Hz 1:100Hz). DIM: (0:200KHz 1:100KHz).	
	VBST_PWM_RATIO[3:0]	4:1	Boost PWM Duty Control. 0000: OFF. 0001: 6.7%. 0010: 13.4%,.....,1111: 100%.	
	BST_EN	0	Boost enable. 1: ON. 0: OFF.	
13h (7E4Dh)	**REG7E4D**	**7:0**	**Default : 0x9D**	**Access : R/W**
	BST_FB_SEL	7	EA output clamping. 1: Enable (default). 0: Disable.	
	BSTLVL[1:0]	6:5	Boost output voltage selection for 5V application with INT diver. 00: 5V. 01: 5.2V. 10: 4.8V. 11: 4.5V.	
	BST_VCL_SEL	4	Clamp voltage for slope compensation. 0: 0.4V (peak current limit ~770mA). 1: 0.8V (peak current limit=2A).	
	BST_COMP[2:0]	3:1	Boost slope compensation (000:0.1V/us, 001:0.2V/us, 010:0.3V/us, 011:0.4V/us, 100:0.5V/us, 101:0.6V/us,. 110: 0.7V/us, 111:0.8V/us).	
	VBST_PWM_INV	0	Inverse PWM signal.	
14h	**REG7E50**	**7:0**	**Default : 0x10**	**Access : R/W**

PMU Register (Bank = 3F)

Index (Absolute)	Mnemonic	Bit	Description
(7E50h)	BST_SEL_DIM_REF[2:0]	7:5	Error amp reference voltage selection:. 00000: 1V 00001:0.98V 00010:0.96V 00011:0.94V. 00100: 0.92V 00101:0.90V 00110:0.88V 00111:0.86V. 01000: 0.84V 01001:0.82V 01010:0.80V 01011:0.78V. 01100: 0.76V 01101:0.72V 01110:0.68V 01111:0.64V. 10000: 0.60V 10001:0.56V 10010:0.52V 10011:0.48V. 10100: 0.44V 10101:0.40V 10110:0.36V 10111:0.32V. 11000: 0.28V 11001:0.24V 11010:0.20V 11011:0.16V. 11100: 0.12V 11101:0.08V 11110:0.04V 11111:0.00V.
	BST_OVP_EN	4	Over voltage protection control. 0: OFF 1:ON.
	BSTCP[3:0]	3:0	Boost internal compensation. [3:2], 00:100K, 01:60K, 10:40K, 00:20K. [1:0]: EA output clamping level. [1:0]=2'b00: 0.7+VGS. [1:0]=2'b01: 0.8+VGS. [1:0]=2'b10: 0.9+VGS. [1:0]=2'b11: 1.0+VGS.
14h (7E51h)	**REG7E51**	**7:0**	**Default : 0x00** **Access : R/W**
	BST_CLK_SEL	7	Boost clock select. 0: Buck1 clk from FRO. 1: Buck1 clk from MCLK.
	DIS_SLOPECOMP	6	Disable slope compare.
	QOFF_USE_PWM	5	Boost PWM use by QOFF. 0: To CLK_DIM. 1: To QOFF.
	-	4	Reserved.
	BST_SEL_VDIM[1:0]	3:2	Analog dimming control source selection. 11: No path to PAD, pull high to error amp. 01: Not allowed. 10: Internal PWM signal. 11: External PWM signal.
	BST_SEL_DIM_REF[4:3]	1:0	See description of '7E50h'.
18h (7E60h)	**REG7E60**	**7:0**	**Default : 0x00** **Access : R/W**
	SW_SPARE0[7:0]	7:0	Pmu spare register (for SW).
18h (7E61h)	**REG7E61**	**7:0**	**Default : 0x00** **Access : R/W**
	SW_SPARE0[15:8]	7:0	See description of '7E60h'.

PMU Register (Bank = 3F)

Index (Absolute)	Mnemonic	Bit	Description	
19h (7E64h)	**REG7E64**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_SPARE1[7:0]	7:0	Pmu spare register (for SW).	
19h (7E65h)	**REG7E65**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_SPARE1[15:8]	7:0	See description of '7E64h'.	
1Ah (7E68h)	**REG7E68**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_SPARE2[7:0]	7:0	Pmu spare register (for SW).	
1Ah (7E69h)	**REG7E69**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_SPARE2[15:8]	7:0	See description of '7E68h'.	
1Bh (7E6Ch)	**REG7E6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_SPARE3[7:0]	7:0	Pmu spare register (for SW).	
1Bh (7E6Dh)	**REG7E6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_SPARE3[15:8]	7:0	See description of '7E6Ch'.	
1Ch (7E70h)	**REG7E70**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	WKUP_TIMER_SEL[1:0]	2:1	Wakeup delay time. 00: 26 ms. 01: 20 ms. 10: 6 ms. 11: 500 us.	
	VBK2_LVL_OV	0	Buck2 voltage level control source. 0: From hardware strapping. 1: From reg_vbk2_lvl.	
1Dh (7E74h)	**REG7E74**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PMU_PAD_CTRL[7:0]	7:0	[0]: Reg_pm_ms_ins_pe. [1]: Reg_pm_ms_ins_ps. [2]: Reg_pm_sd_cdz_pe. [3]: Reg_pm_sd_cdz_ps. [4]: Reg_gpio_g00_pe. [5]: Reg_gpio_g00_ps. [6]: Reg_gpio_g01_pe. [7]: Reg_gpio_g01_ps. [8]: Reg_gpio_g02_pe. [9]: Reg_gpio_g02_ps. [10]: Reg_gpio_g03_pe. [11]: Reg_gpio_g03_ps. [12:15] : reserved.	

PMU Register (Bank = 3F)

Index (Absolute)	Mnemonic	Bit	Description	
1Dh (7E75h)	**REG7E75**	**7:0**	**Default : 0xFF**	**Access : R/W**
	-	7:4	Reserved.	
	PMU_PAD_CTRL[11:8]	3:0	See description of '7E74h'.	
27h (7E9Ch)	**REG7E9C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	CLK32K_FLAG	4	32k flag.	
	-	3:0	Reserved.	
34h (7ED0h)	**REG7ED0**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	BK2RAMP_CTRL[1:0]	7:6	Buck2 ramp control.	
	MEM_RAMP_TARGET[4:0]	5:1	MEM LDO ramping target (when DRM=1). 00000: -100 mV. 00001: -150 mV. 00010: -200 mV. 00011: -250 mV. 00100: -300 mV. 00101: -350 mV. 00110: -400 mV. 00111: -450 mV. 01000: -500 mV. 01001: -550 mV. 01010: -600 mV. Others: -100 mV.	
	MEM_RAMP_STEP	0	MEM LDO ramping step. 0: 50mV 1: 100mV.	
34h (7ED1h)	**REG7ED1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	BK2RAMP_CTRL[4:2]	2:0	See description of '7ED0h'.	
42h (7F08h)	**REG7F08**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:2	Reserved.	
	VL_S_EN	1	VL enable in suspend mode.	
	VL_A_EN	0	VL enable in active mode. VL need enable before buck enable.	
44h (7F10h)	**REG7F10**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	FRO_S_EN	5	FRO enable at suspend mode.	

PMU Register (Bank = 3F)

Index (Absolute)	Mnemonic	Bit	Description	
	FRO_A_EN	4	FRO enable at active mode.	
	FRO_CLK_ADJ[3:0]	3:0	Fro clock adjust. //default from efuse[15:12]. Can be over write by set reg_level_ov_en=1 ,.	
45h (7F14h)	**REG7F14**	**7:0**	**Default : 0x20**	**Access : R/W**
	LDOVPER1_D_TIME[1:0]	7:6	Standby mode turn-off delay time. 00: 0us. 01: 250us. 10: 500us. 11: 1ms.	
	LDOVPER1_S_LQ	5	Enable ldo_vper1 Low-Quiescent mode in suspend mode.	
	LDOVPER1_S_EN	4	Enable ldo_vper1 in suspend mode.	
	LDOVPER1_VSET[1:0]	3:2	Select output voltage level, (user ldo_150m_hv). 00: 2.9V. 01: 1.2V. 10: 2.8V. 11: 3.2V.	
	LDOVPER1_A_LQ	1	Enable ldo_vper1 Low-Quiescent mode in acitve mode.	
	LDOVPER1_A_EN	0	Enable ldo_vper1 in active mode.	
45h (7F15h)	**REG7F15**	**7:0**	**Default : 0x20**	**Access : R/W**
	LDOVPER2_D_TIME[1:0]	7:6	Standby mode turn-off delay time. 00: 0us. 01: 250us. 10: 500us. 11: 1ms.	
	LDOVPER2_S_LQ	5	Enable ldo_vper2 Low-Quiescent mode in suspend mode.	
	LDOVPER2_S_EN	4	Enable ldo_vper2 in standby mode.	
	LDOVPER2_VSET[1:0]	3:2	Select output voltage level, (user ldo_150m_hv). 00: 2.9V. 01: 1.8V. 10: 2.8V. 11: 3.2V.	
	LDOVPER2_A_LQ	1	Enalbe ldo_vper2 Low-Quiescent mode in acitve mode.	
	LDOVPER2_A_EN	0	Enable ldo_vper2 in active mode.	
46h	**REG7F18**	**7:0**	**Default : 0x21**	**Access : R/W**

PMU Register (Bank = 3F)

Index (Absolute)	Mnemonic	Bit	Description	
(7F18h)	LDOVPER3_D_TIME[1:0]	7:6	Standby mode turn-off delay time. 00: 0us. 01: 250us. 10: 500us. 11: 1ms.	
	LDOVPER3_S_LQ	5	Enable ldo_vper3 Low-Quiescent mode in suspend mode.	
	LDOVPER3_S_EN	4	Enable ldo_vper3 in suspend mode.	
	LDOVPER3_VSET[1:0]	3:2	Select output voltage level, (user ldo_150m_lv). // default from efuse[23:22],. Can be over write by set reg_level_ov_en=1 ,. 00: 2.9V. 01: 1.8V. 10: 2.8V. 11: 3.2V.	
	LDOVPER3_A_LQ	1	Enalbe ldo_vper3 Low-Quiescent mode in acitve mode.	
	LDOVPER3_A_EN	0	Enable ldo_vper3 in active mode.	
47h (7F1Ch)	**REG7F1C**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	BUCK2_PTEST	7	Buck2 PMOS RON test mode.	
	BUCK2_TEST[1:0]	6:5	Buck2 test mode.	
	BK1_OCP_FLAG	4	BUCK1 short circuit flag, read only.	
	BUCK1_CLK_OK	3	BUCK1 clock OK flag.	
	BUCK1_PTEST	2	Buck1 PMOS RON test mode.	
	BUCK1_TEST[1:0]	1:0	Buck1 test mode.	
47h (7F1Dh)	**REG7F1D**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	REF_VBK1OK	7	BUCK1 reference is OK.	
	-	6	Reserved.	
	SEL_STDLDO2_REF	5	Select STDLDO2 reference voltage. 0: VSTD = 1.7V. 1: VSTD = 1.8V.	
	PG_VBK2	4	Buck2 power good.	
	PG_VBK1	3	Buck1 power good.	
	VREFSTD2_TEST	2	Test mode select, output VREFSTD2.	
	BK2_OCP_FLAG	1	BUCK2 short circuit flag, read only.	
	BUCK2_CLK_OK	0	BUCK2 clock OK flag.	
48h	**REG7F20**	**7:0**	**Default : 0x21**	**Access : R/W**

PMU Register (Bank = 3F)

Index (Absolute)	Mnemonic	Bit	Description	
(7F20h)	BUCK1_SC[1:0]	7:6	Buck1 Slop Compensation select. 000: 0.2v/us 001: 0.3v/us 010: 0.4v/us 011: 0.5v/us. 100: 0.6v/us 101: 0.7v/us 110: 0.8v/us 111: 0.9v/us.	
	BUCK1_FPWM	5	Buck1 operation mode control.	
	BUCK1_CLK_SEL	4	Buck1 clock select. 0: Buck1 clk from FRO. 1: Buck1 clk from MCLK.	
	BUCK1_SS_OFF	3	Buck1 soft_start off control //ECO U01 change to 0.	
	-	2	Reserved.	
	BUCK1_S_EN	1	Enable buck1 in suspend mode.	
	BUCK1_A_EN	0	Enable buck1 in active mode.	
48h (7F21h)	**REG7F21**	**7:0**	**Default : 0x18**	**Access : R/W**
	VBK1_LVL[2:0]	7:5	Buck1 voltage level control. 000: 1.20v 001: 1.25v 010: 1.30v 011: 1.35v. 100: X 101: 1.05v 110: 1.10v 111: 1.15v.	
	BUCK1_OCP_SEL[1:0]	4:3	Buck1 OCP current select (over current protect level). 00: 600mA 01:700mA 10:800mA 11:900mA.	
	BUCK1_INT_COMP[1:0]	2:1	Buck1 internal compensation select. 00: Ceq=200pF Req=40kohm. 01: Ceq=400pF Req=40kohm. 00: Ceq=200pF Req=60kohm. 11: OFF Cboost.	
	BUCK1_SC[2]	0	See description of '7F20h'.	
49h (7F24h)	**REG7F24**	**7:0**	**Default : 0x08**	**Access : R/W**
	PM_RAMP_STEP	7	PM LDO ramping step. 0: 50mV 1: 100mV.	
	-	6:4	Reserved.	
	PMLDO_S_LQ	3	Enable ldo_pm Low-Quiescent mode in suspend mode.	
	PMLDO_A_LQ	2	Enable ldo_pm Low-Quiescent mode in active mode.	
	-	1:0	Reserved.	
49h (7F25h)	**REG7F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	BUCK_TD_CTRL[1:0]	7:6	Buck dead time control. 00: 10 ns 01/10: 7 ns 11: 3ns.	
	VREFSTD1_TEST	5	Test mode select, output VREFSTD1.	

PMU Register (Bank = 3F)

Index (Absolute)	Mnemonic	Bit	Description	
	PM_RAMP_TARGET[4:0]	4:0	PM LDO ramping target (when DRM=1). 00000: -100 mV. 00001: -150 mV. 00010: -200 mV. 00011: -250 mV. 00100: -300 mV. 00101: -350 mV. 00110: -400 mV. 00111: -450 mV. 01000: -500 mV. 01001: -550 mV. 01010: -600 mV. Others: -100 mV.	
4Ah (7F28h)	**REG7F28**	**7:0**	**Default : 0x61**	**Access : R/W**
	BUCK2_SC[1:0]	7:6	Buck2 Slop Compensation select. 000: 0.2v/us 001: 0.3v/us 010: 0.4v/us 011: 0.5v/us. 100: 0.6v/us 101: 0.7v/us 110: 0.8v/us 111: 0.9v/us.	
	BUCK2_FPWM	5	Buck2 operation mode control.	
	BUCK2_CLK_SEL	4	Buck2 clock select. 0: Buck2 clk from FRO. 1: Buck2 clk from MCLK.	
	-	3	Reserved.	
	BUCK2_SS_OFF	2	Buck2 soft_start off control //ECO U01 change to 0.	
	BUCK2_S_EN	1	Enable buck2 in suspend mode.	
	BUCK2_A_EN	0	Enable buck2 in active mode.	
4Ah (7F29h)	**REG7F29**	**7:0**	**Default : 0x18**	**Access : R/W**
	VBK2_LVL[2:0]	7:5	Buck2 voltage level control. 000: 1.8V. 001: 1.5V. 010: 1.85V. 011: 1.55V. 100: 1.9V. 101: 1.6V. 110: 1.75V. 111: 1.45V.	
	BUCK2_OCP_SEL[1:0]	4:3	Buck2 OCP current select (over current protect level). 00: 600mA 01:700mA 10:800mA 11:900mA.	

PMU Register (Bank = 3F)

Index (Absolute)	Mnemonic	Bit	Description	
	BUCK2_INT_COMP[1:0]	2:1	Buck2 internal compensation select. 00: Ceq=200pF Req=40kohm. 01: Ceq=400pF Req=40kohm. 00: Ceq=200pF Req=60kohm. 11: OFF Cboost.	
	BUCK2_SC[2]	0	See description of '7F28h'.	
5Ch (7F70h)	**REG7F70**	**7:0**	**Default : 0x00**	**Access : RO**
	PMU_TESTBUS[7:0]	7:0	Pmu testbus : selection by reg_dbbus_sel.	
5Ch (7F71h)	**REG7F71**	**7:0**	**Default : 0x00**	**Access : RO**
	PMU_TESTBUS[15:8]	7:0	See description of '7F70h'.	
5Dh (7F74h)	**REG7F74**	**7:0**	**Default : 0x00**	**Access : RO**
	PMU_TESTBUS[23:16]	7:0	See description of '7F70h'.	
5Fh (7F7Ch)	**REG7F7C**	**7:0**	**Default : 0x00**	**Access : RO**
	RESERVED_STATUS[7:0]	7:0	Read only reserved status [15:0] = 16'b0.	
5Fh (7F7Dh)	**REG7F7D**	**7:0**	**Default : 0x00**	**Access : RO**
	RESERVED_STATUS[15:8]	7:0	See description of '7F7Ch'.	
60h (7F80h)	**REG7F80**	**7:0**	**Default : 0x01**	**Access : R/W**
	CHRG_FB_SEL	7	Charger feedback voltage selection 0: from VSYS; 1:fromVBAT.	
	ENVBAT_MEAS	6	Enable measuring VBAT.	
	EN_PRECHARGE	5	Enable pre-charger block.	
	-	4:2	Reserved.	
	CLED_PWM	1	PWM is controlled by CPU when CLED_PWM_en =0.	
	EN_CLED	0	Enable Charger LED Driver.	
60h (7F81h)	**REG7F81**	**7:0**	**Default : 0x00**	**Access : R/W**
	CVTARGET[1:0]	7:6	CV level selection. 00: 4.2V. 01: 4.3V. 10: 4.1V. 11: 4.0V.	

PMU Register (Bank = 3F)

Index (Absolute)	Mnemonic	Bit	Description	
	CCTARGET[2:0]	5:3	Charging current selection. 000: 500mA. 001: 750mA. 010: 900mA. 011: 1000mA. 100: 100mA. 101: 200mA. 110: 300mA. 111: 400mA.	
	CHRGOFF	2	Disable Charger function; 0: enable 1: disable.	
	CCTARGET_SEL	1	Cctarget selection. 0: Cctarget will be force 500mA when PMTEST=1; cctarget = reg_cctarget when PMTEST=0. 1: Cctarget from reg_cctarget.	
	CV_SEL	0	CV level selection; 0: CV level = 3.67V; 1: CV level = 4.2V.	
61h (7F84h)	**REG7F84**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VBAT_LVL2	7	VBAT voltage level flag. (VBAT>3.1V).	
	VBAT_LVL1	6	VBAT voltage level flag. (VBAT>2.6V).	
	ADA_EXIST	5	Adapter plug-in flag. 1. High: Plug-in. 2. Low: No plug-in.	
	VBATOK	4	Battery ok flag from PM_logic.	
	CS_GAIN	3	Current source gain adjustment.	
	OFST_TST	2	Offset voltage test mode.	
	PD_AUTO	1	Power down auto-zero CS amplifier. 0--> on, 1--> off.	
	CHARGE_CTRL_PULSE	0	Enable pulse for reg_chrgoff, reg_cctarget.	
61h (7F85h)	**REG7F85**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	SW_ON	6	Pull low gate voltage of external PMOS. 0: Gate voltage pull high. 1: Gate voltage pull low.	
	PD_HW_SWON	5	Disable hardwire switch control.	
	VBAT_V3P2_OK	4	Vbattery 3.2 v ok flag.	

PMU Register (Bank = 3F)

Index (Absolute)	Mnemonic	Bit	Description	
	VBAT_V3P0_OK	3	Vbattery 3.0 v ok flag.	
	VBAT_V2P8_OK	2	Vbattery 2.8 v ok flag.	
	CHRG_PGIN	1	Charger plug-in interrupt (RTC domain). High: Plug-in. Low plug-out.	
	CHRG_OVER_V	0	Adapter voltage over voltage flag. (Vadapter>6V).	
62h (7F88h)	**REG7F88**	**7:0**	**Default : 0x00**	**Access : R/W**
	ABBRESET_PASSWD[7:0]	7:0	PAD password for enable PAD_ABBRESET. All zero is enable (from pad). Not all zero; PAD_ABBRESET will be disable (ABBRESET = 0).	
63h (7F8Ch)	**REG7F8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	PHONE_OFF_PASSWD[7:0]	7:0	Phone off pass word; with reg_phone_off and reg_phone_off_lockb. All one is enable. Not all one is disable.	
63h (7F8Dh)	**REG7F8D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PHONE_OFF_LOCKB	1	Enable reg_PHONE_OFF funtion. 0: Disable reg_PHONE_OFF. 1: Enable reg_PHONE_OFF.	
	PHONE_OFF	0	Enable turn off phone.	
64h (7F90h)	**REG7F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	LEVEL_OV_EN	7	All level control override enable (0: disable; 1: enable).	
	-	6:5	Reserved.	
	BAT_NO_OK_TURNOFF	4	When vbat <2.8v bat is not ok. 0: Battery < 2.8v will not turn off phone. 1: Battery < 2.8v turn off phone.	
	BAT_OK_TIME_SEL	3	Select vbat ok debounce clock. 0: Use 2ms debounce. 1: Use 16ms debounce.	
	-	2:1	Reserved.	
	SUSPD_EN	0	Enable master suspend function.	
64h (7F91h)	**REG7F91**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7	Reserved.	

PMU Register (Bank = 3F)

Index (Absolute)	Mnemonic	Bit	Description	
	PMU_DIG_RSTZ	6	Pmu soft ware reset for irq. Ldo soft start, pwm. 0: Reset. 1: Release.	
	-	5:2	Reserved.	
	STD_TIME_STEP[1:0]	1:0	Standby mode entry/exit time step. 00: 125 us (default). 01: 250 us. 10: 500 us. 11: (reserved).	
65h (7F94h)	**REG7F94**	**7:0**	**Default : 0x00**	**Access : RO**
	PMTEST	7	PAD PM_TEST flag to pmu_fsm.	
	PIN_PWRHLD	6	PAD PWRHLD flag to pmu_fsm.	
	PMU_OFF	5	PMU_OFF flag.	
	PIN_STDBYN_M	4	Master standby_n flag.	
	CHGDET_DEBOUNCE	3	Charger plug in flag.	
	BAT_ON_DEBOUNCE	2	Battery on flag.	
	ONOFF_APPEAR	1	ONOFF_APPEAR from rtc_fsm to pmu_fsm.	
	PMU_FSM_EN	0	PMU_FSM_EN from rtc_fsm to pmu_fsm.	
65h (7F95h)	**REG7F95**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	BK1RAMP_CTRL[4:0]	5:1	Buck ramp control.	
	REF_BKLDOOK	0	Refgen and buck ldo ok flag.	
66h (7F98h)	**REG7F98**	**7:0**	**Default : 0x00**	**Access : RO**
	PMU_FSM_STATUS[7:0]	7:0	Pmu_fsm state[23:8]. [17:0] : pmu_state. [31:18]: reserved.	
66h (7F99h)	**REG7F99**	**7:0**	**Default : 0x00**	**Access : RO**
	PMU_FSM_STATUS[15:8]	7:0	See description of '7F98h'.	
67h (7F9Ch)	**REG7F9C**	**7:0**	**Default : 0x00**	**Access : RO**
	PMU_FSM_STATUS[23:16]	7:0	See description of '7F98h'.	
67h (7F9Dh)	**REG7F9D**	**7:0**	**Default : 0x00**	**Access : RO**
	PMU_FSM_STATUS[31:24]	7:0	See description of '7F98h'.	
68h	**REG7FA0**	**7:0**	**Default : 0x00**	**Access : RO**

PMU Register (Bank = 3F)

Index (Absolute)	Mnemonic	Bit	Description	
(7FA0h)	SUSPEND_STATUS[7:0]	7:0	M suspend fsm and status. [8:0]: m_state. [15:9]: reseverd.	
68h (7FA1h)	**REG7FA1**	**7:0**	**Default : 0x00**	**Access : RO**
	SUSPEND_STATUS[15:8]	7:0	See description of '7FA0h'.	
69h (7FA4h)	**REG7FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	KEYOFF_TIME_OUT[7:0]	7:0	Time out value for ON/OFF button shut-down.	
69h (7FA5h)	**REG7FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	KEYOFF_TIMER_CLEAR	4	Clear timer of ON/OFF button.	
	KEYOFF_TIMER_EN	3	Enable press ON/OFF button for force shut-down.	
	KEYOFF_TIME_OUT[10:8]	2:0	See description of '7FA4h'.	
6Ah (7FA8h)	**REG7FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	EN_TM_OUTBUF	5	Output buffer enable.	
	SEL_TMUX[4:0]	4:0	Tmmux selection.	
6Bh (7FACh)	**REG7FAC**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLASSD_TST[7:0]	7:0	ClassD test register.	
6Bh (7FADh)	**REG7FAD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CLASSD_CLK_SEL	6	ClassD clock select. 0: Buck1 clk from FRO. 1: Buck1 clk from MCLK.	
	CLASSD_ISEL[5:0]	5:0	Select the bias current:. ISEL[1:0]: PGA OP. ISEL[3:2]: Modulator OP. ISEL[5:4]: Trigen OP. 00: 20uA. 01: 10uA. 10: 40uA. 11: 30uA.	
6Ch	**REG7FB0**	**7:0**	**Default : 0x00**	**Access : R/W**

PMU Register (Bank = 3F)

Index (Absolute)	Mnemonic	Bit	Description
(7FB0h)	CLASSD_OCP_SEL	7	(CLASSD_MOD_18_2). Enable ClassD OCP modification circuit. 0: Off. 1: Enable.
	CLASSD_DIS_OCP	6	(CLASSD_MOD_DRIVER_18_0). ClassD Over current protection disable. 0: Enable OCP. 1: Disable OCP.
	CLASSD_DRV_SLEW	5	(CLASSD_MOD_DRIVER_18_1). Output driver slew rate control (No connect).
	DIS_VCM_MOD	4	(CLASSD_MOD_18_1). Disable classD modulator VCM modification resistor. 0: On. 1: Disable.
	CLASSD_CLK_DIV2	3	(CLASSD_TRI_18_1). ClassD CLK DIV 2X. 0: CLK/4 (2.4MHz, triangle wave: 1.2MHz). 1: CLK/8 (1.2MHz, triangle wave: 0.6MHz).
	CLASSD_BIAS_SEL[1:0]	2:1	(CLASSD_TRI_18_0 CLASSD_MOD_DRIVER_18_2). ClassD bias current ratio selection. 00: 1X. 01: OFF. 10: 1.5X. 11: 0.5X.
	CLASSD_EN	0	ClassD enable. 0: ClassD off. 1: ClassD on.
6Ch (7FB1h)	**REG7FB1**	**7:0**	**Default : 0x01** **Access : RO, R/W**
	-	7	Reserved.
	PD_CLASSD	6	
	OCP_CLASSD	5	
	PGA_MUTE	4	
	CLASSD_MOD_GAIN_SEL	3	ClassD gain selection. 0: 2X. 1: 4X.

PMU Register (Bank = 3F)

Index (Absolute)	Mnemonic	Bit	Description	
	CLASSD_BYP_MOD	2	(CLASSD_TRI_18_2). Bypass ClassD modulator (No connect). 0: Normal operation. 1: Bypass modulator.	
	RSET_OCP_STAT	1	Clear OCP flag. 0: No action. 1: Clear OCP flag, OCP_CLASSD_=0.	
	CLASSD_MUTE	0	ClassD mute control. 0: Normal operation. 1: Mute.	
6Dh (7FB4h)	**REG7FB4**	**7:0**	**Default : 0x00**	**Access : R/W**
	PD_CD	7	Reserved.	
	EN_LINE_BYP	6	Enable lineout signal bypass to PADs.	
	EN_MX_LINE	5	Enable lineout driver signal input.	
	LINE_MUTE	4	Enable mute control of lineout amplifier.	
	LINE_DRGN[2:0]	3:1	Gain setting for lineout driver gain. 000: 0dB, gain=1. 001: -4.4dB, gain=0.6. 010: 1.6dB, gain=1.2. 011: 3dB, gain= 1.4. 100: 6dB, gain=2. 101: 9dB, gain=2.8. 110: 10dB, gain=3.4. 111: 12dB, gain= 4.	
	EN_DRVER_TOT	0	Reserved.	
6Dh (7FB5h)	**REG7FB5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	EN_LINE_DIS	3	Lineout discharge path enable.	
	EN_DRVER[2:0]	2:0	Enable control. EN_DRVER[0]: lineout amplifier to Class-D. EN_DRVER[1]: RCV class-AB amplifier. EN_DRVER[2]: R-string for VCM (1.4V).	
70h (7FC0h)	**REG7FC0**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK[7:0]	7:0	Mask interrupt.	
70h (7FC1h)	**REG7FC1**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK[15:8]	7:0	See description of '7FC0h'.	

PMU Register (Bank = 3F)

Index (Absolute)	Mnemonic	Bit	Description	
71h (7FC4h)	**REG7FC4**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK[23:16]	7:0	See description of '7FC0h'.	
71h (7FC5h)	**REG7FC5**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK[31:24]	7:0	See description of '7FC0h'.	
72h (7FC8h)	**REG7FC8**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_FORCE[7:0]	7:0	Force interrupt to be 1.	
72h (7FC9h)	**REG7FC9**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_FORCE[15:8]	7:0	See description of '7FC8h'.	
73h (7FCCh)	**REG7FCC**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_FORCE[23:16]	7:0	See description of '7FC8h'.	
73h (7FCDh)	**REG7FCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_FORCE[31:24]	7:0	See description of '7FC8h'.	
74h (7FD0h)	**REG7FD0**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_CLR[7:0]	7:0	Clear interrupt.	
74h (7FD1h)	**REG7FD1**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_CLR[15:8]	7:0	See description of '7FD0h'.	
75h (7FD4h)	**REG7FD4**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_CLR[23:16]	7:0	See description of '7FD0h'.	
75h (7FD5h)	**REG7FD5**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_CLR[31:24]	7:0	See description of '7FD0h'.	
76h	**REG7FD8**	**7:0**	**Default : 0x00**	**Access : RO**

PMU Register (Bank = 3F)

Index (Absolute)	Mnemonic	Bit	Description	
(7FD8h)	IRQ_RAW_STATUS[7:0]	7:0	IRQ raw status. [31]: Reserved. [30]: Checksum protect. [29]: USB insertion. [28]: MS insertion. [27]: SD card insertion. [26:16] : GPIO interrupt. [15]: SAR key detection. [14]: Touch panel detection. [13]: RTC alarm. [12]: ONOFF_PULSE; ONOFF KEY push. [11]: KEYOFF_PULSE; ONOFF KEY release. [10]: Adaptor_unplug_irq; charger plug-out. [9]: Adaptor_plug_irq; charger plug-in. [8]: Bat_low_irq; battery <3.0V. [7]: No_bat_int; no battery. [6]: Irq_ocp_classd; CLASS-D over current protect. [5]: Irq_pga_mute; AUDIO receiver PGA mute. [4]: LDO_ERR_IRQ; LDO ERROR. [3]: Otp_debounce; refgen over temperature protect. [2]: Over_voltage_irq; charger over voltage. [1]: Buck2ocp_debounce; buck2 over current protect. [0]: Buck1ocp_debounce; buck1 over current protect.	
76h (7FD9h)	**REG7FD9**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS[15:8]	7:0	See description of '7FD8h'.	
77h (7FDCh)	**REG7FDC**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS[23:16]	7:0	See description of '7FD8h'.	
77h (7FDDh)	**REG7FDD**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS[31:24]	7:0	See description of '7FD8h'.	
78h (7FE0h)	**REG7FE0**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS[7:0]	7:0	IRQ final status.	
78h (7FE1h)	**REG7FE1**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS[15:8]	7:0	See description of '7FE0h'.	
79h (7FE4h)	**REG7FE4**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS[23:16]	7:0	See description of '7FE0h'.	
79h (7FE5h)	**REG7FE5**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS[31:24]	7:0	See description of '7FE0h'.	

PMU Register (Bank = 3F)

Index (Absolute)	Mnemonic	Bit	Description	
7Ah (7FE8h)	**REG7FE8**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_POLARITY[7:0]	7:0	Irq source polarity.	
7Ah (7FE9h)	**REG7FE9**	**7:0**	**Default : 0xC0**	**Access : R/W**
	IRQ_POLARITY[15:8]	7:0	See description of '7FE8h'.	
7Bh (7FECh)	**REG7FEC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_POLARITY[23:16]	7:0	See description of '7FE8h'.	
7Bh (7FEDh)	**REG7FED**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_POLARITY[31:24]	7:0	See description of '7FE8h'.	
7Ch (7FF0h)	**REG7FF0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDIO_MODE[0]	7	Refer to pad mux table.	
	SD3_MODE[1:0]	6:5	Refer to pad mux table.	
	-	4	Reserved.	
	NF_MODE[2:0]	3:1	Refer to pad mux table.	
	-	0	Reserved.	
7Ch (7FF1h)	**REG7FF1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	IDPULLUP	2	Enable USBCID pull-up.	
	USBPHY_MODE	1	IDDIG signal generation source. 0: Reg_idpullup (from pmu domain). 1. Usb_idpullup (from core domain).	
	SDIO_MODE[1]	0	See description of '7FF0h'.	
7Dh (7FF4h)	**REG7FF4**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIO_G_OUT[7:0]	7:0	The PAD_Is of GPIO.	
7Dh (7FF5h)	**REG7FF5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	GPIO_G_OUT[12:8]	4:0	See description of '7FF4h'.	
7Eh (7FF8h)	**REG7FF8**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GPIO_G_OEN[7:0]	7:0	The PAD_OENs of GPIO.	
7Eh (7FF9h)	**REG7FF9**	**7:0**	**Default : 0x1F**	**Access : R/W**
	-	7:5	Reserved.	
	GPIO_G_OEN[12:8]	4:0	See description of '7FF8h'.	

REGISTER TABLE REVISION HISTORY

Date	Bank	Register
01/03/11		• Created first version.