

20V(D-S) Dual N-Channel Enhancement Mode Power MOS FET

General Features

- $V_{DS} = 20V, I_D = 7A$
 $R_{DS(ON)} < 27m\Omega @ V_{GS}=2.5V$
 $R_{DS(ON)} < 21m\Omega @ V_{GS}=4.5V$
 ESD Rating: 2000V HBM
- High power and current handing capability
- Lead free product is acquired
- Surface mount package
- ESD protected



Lead Free

Application

- PWM application
- Load switch

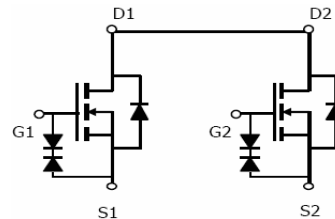


Marking and pin assignment

PIN Configuration



TSSOP-8 top view



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MSC0207GE	MSC0207GE	TSSOP-8	Ø330mm	12mm	3000 units

Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 12	V
Drain Current-Continuous	I_D	7	A
Drain Current-Pulsed ^(Note 1)	I_{DM}	30	A
Maximum Power Dissipation	P_D	1.5	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	83.3	$^\circ C/W$
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Electrical Characteristics (T_A=25 °C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	20	21.5	23	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =20V, V _{GS} =0V	-	-	1	μA
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±10V, V _{DS} =0V	-	-	±10	μA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	0.5	0.65	0.9	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =4.5V, I _D =6.5A	-	15	21	mΩ
		V _{GS} =2.5V, I _D =5.5A	-	20	27	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =7A	-	20	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{ISS}	V _{DS} =10V, V _{GS} =0V, F=1.0MHz	-	1150	-	PF
Output Capacitance	C _{OSS}		-	185	-	PF
Reverse Transfer Capacitance	C _{RSS}		-	145	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =10V, R _L =1.35Ω V _{GS} =5V, R _{GEN} =3Ω	-	6		nS
Turn-on Rise Time	t _r		-	13		nS
Turn-Off Delay Time	t _{d(off)}		-	52		nS
Turn-Off Fall Time	t _f		-	16		nS
Total Gate Charge	Q _g	V _{DS} =10V, I _D =7A, V _{GS} =4.5V	-	15		nC
Gate-Source Charge	Q _{gs}		-	0.8	-	nC
Gate-Drain Charge	Q _{gd}		-	3.2	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =1A	-	-	1.2	V
Diode Forward Current (Note 2)	I _S		-	-	7	A

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

Typical Electrical and Thermal Characteristics

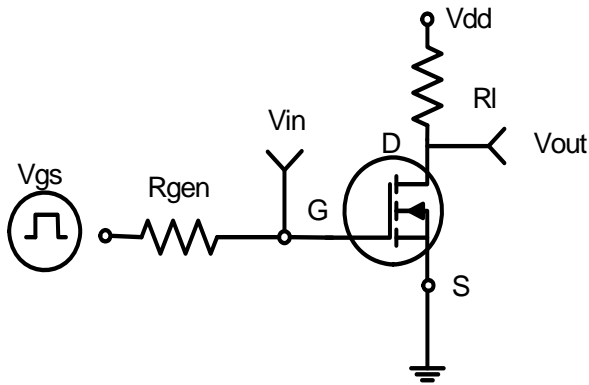


Figure 1: Switching Test Circuit

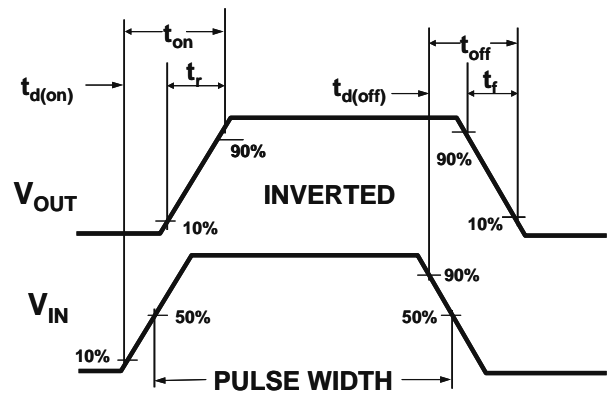


Figure 2: Switching Waveforms

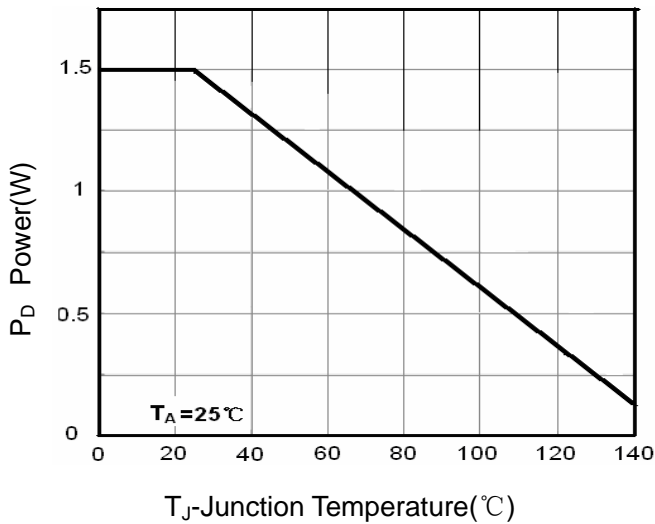


Figure 3 Power Dissipation

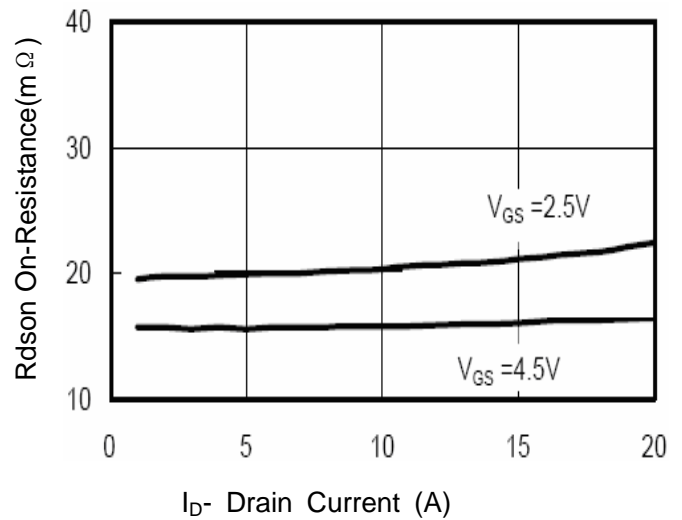


Figure 6 Drain-Source On-Resistance

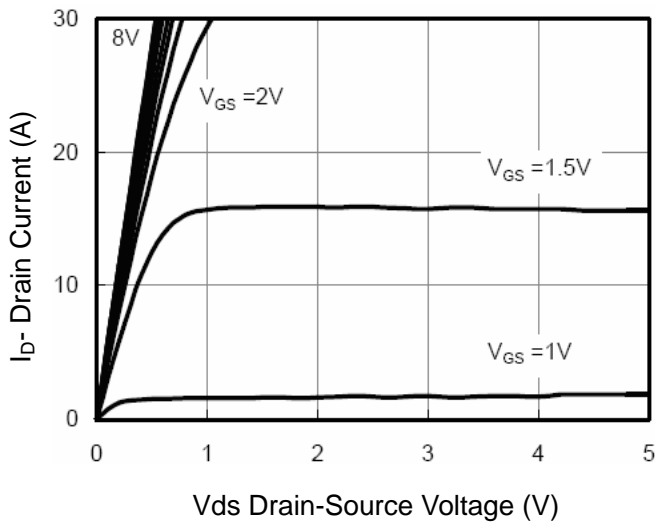


Figure 5 Output Characteristics

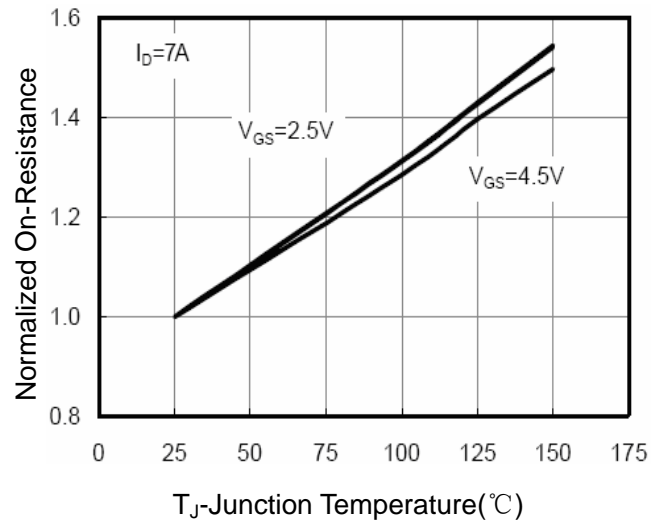
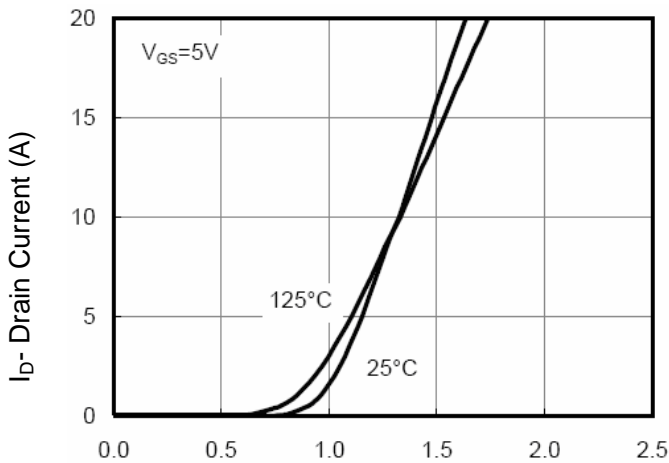
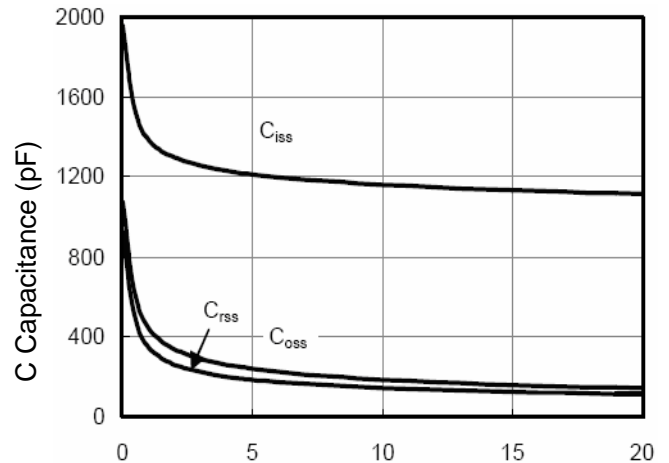


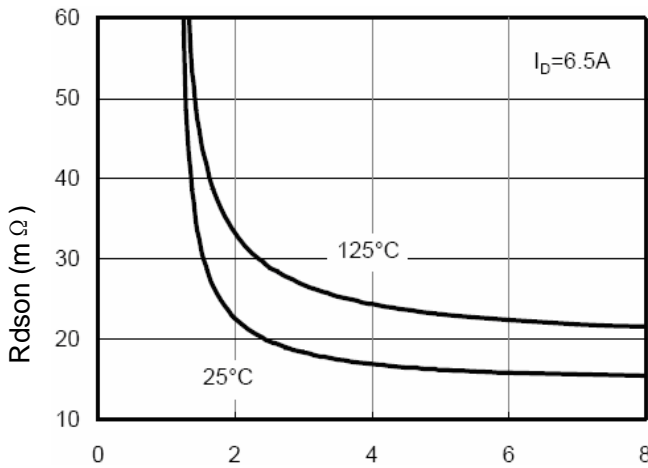
Figure 8 Drain-Source On-Resistance



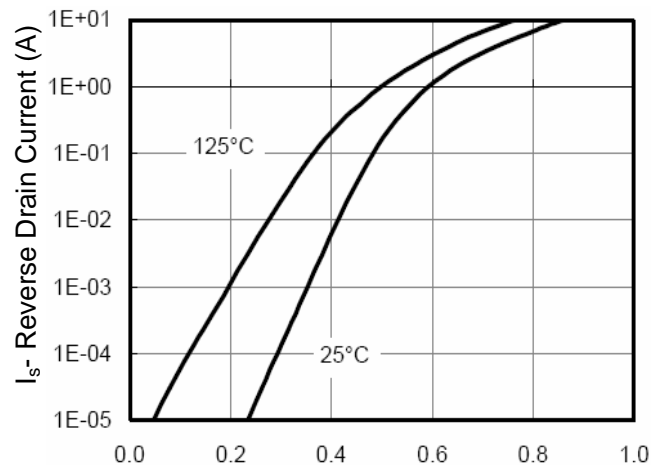
Vgs Gate-Source Voltage (V)
Figure 7 Transfer Characteristics



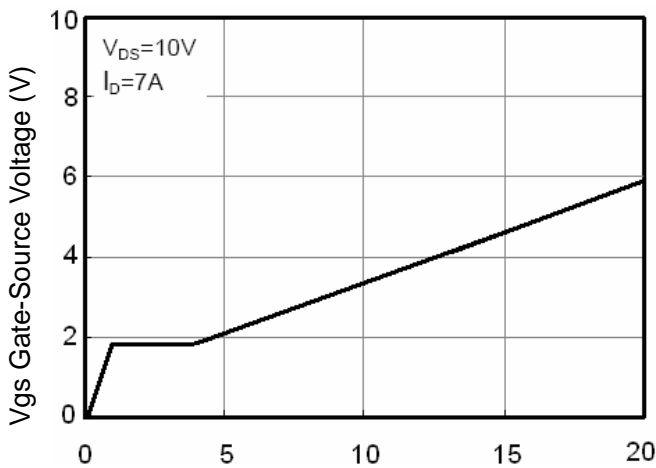
Vds Drain-Source Voltage (V)
Figure 8 Capacitance vs Vds



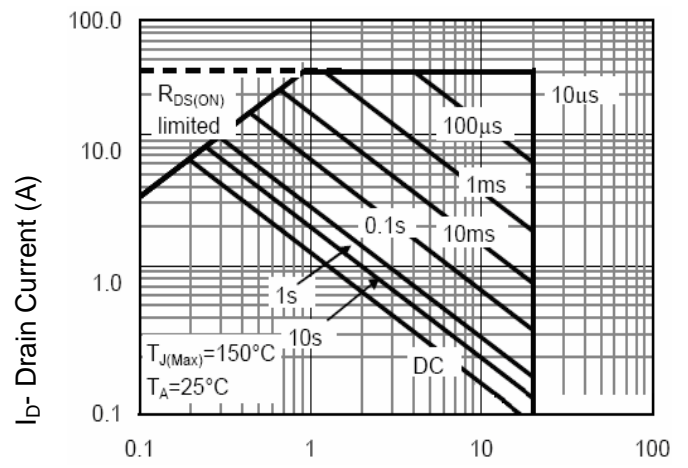
Vgs Gate-Source Voltage (V)
Figure 9 Rdson vs Vgs



Vds Drain-Source Voltage (V)
Figure 10 Capacitance vs Vds



Qg Gate Charge (nC)
Figure 11 Gate Charge



Vds Drain-Source Voltage (V)
Figure 13 Safe Operation Area

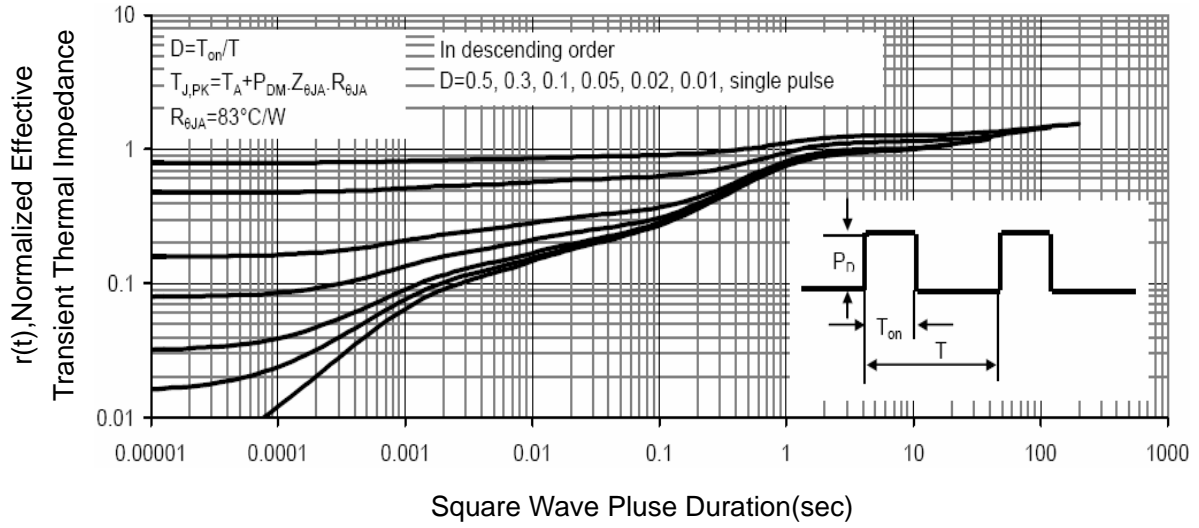
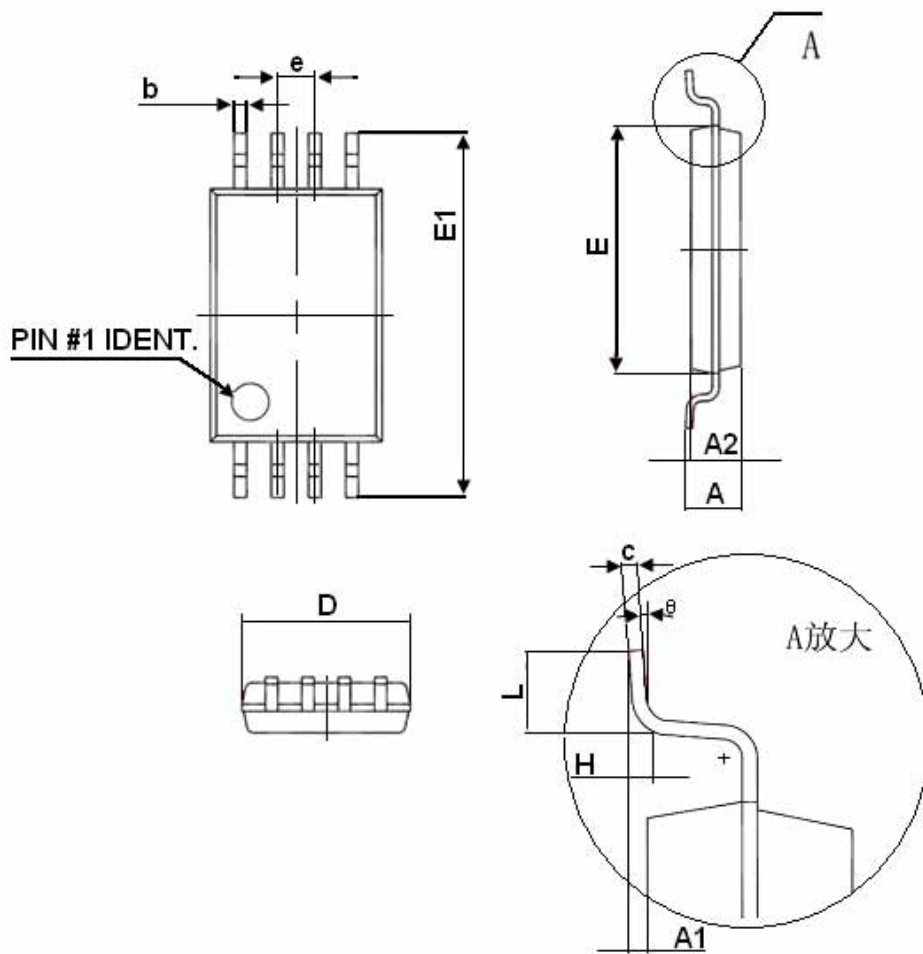


Figure 14 Normalized Maximum Transient Thermal Impedance

TSSOP-8 Package Information



Symbol	Dimensions In Millimeters	
	Min	Max
D	2.900	3.100
E	4.300	4.500
b	0.190	0.300
c	0.090	0.200
E1	6.250	6.550
A		1.100
A2	0.800	1.000
A1	0.020	0.150
e	0.65(BSC)	
L	0.500	0.700
H	0.25(TYP)	
θ	1°	7°