OKI Semiconductor

This version: Sep. 2000
Previous version: Nov. 1997

www.DataSheet4U.com

MSC1200-01/1200V-01

30-Bit Duplex Controller/Driver with Digital/Analog Dimming and Keyscan Functions

GENERAL DESCRIPTION

The MSC1200-01/1200V-01 is a Bi-CMOS display driver for 1/2-duty vacuum fluorescent display tube. This device consists of a 64-bit shift register, latches, an analog dimming circuit, a digital dimming circuit, a keyscan circuit, and drivers.

The interface with a microcomputer can be done only with four signal lines (CS, DATA I/O, CLOCK, and INT). Also, the DATA I/O and CLOCK signal lines can be shared with other peripherals by using the chip select function.

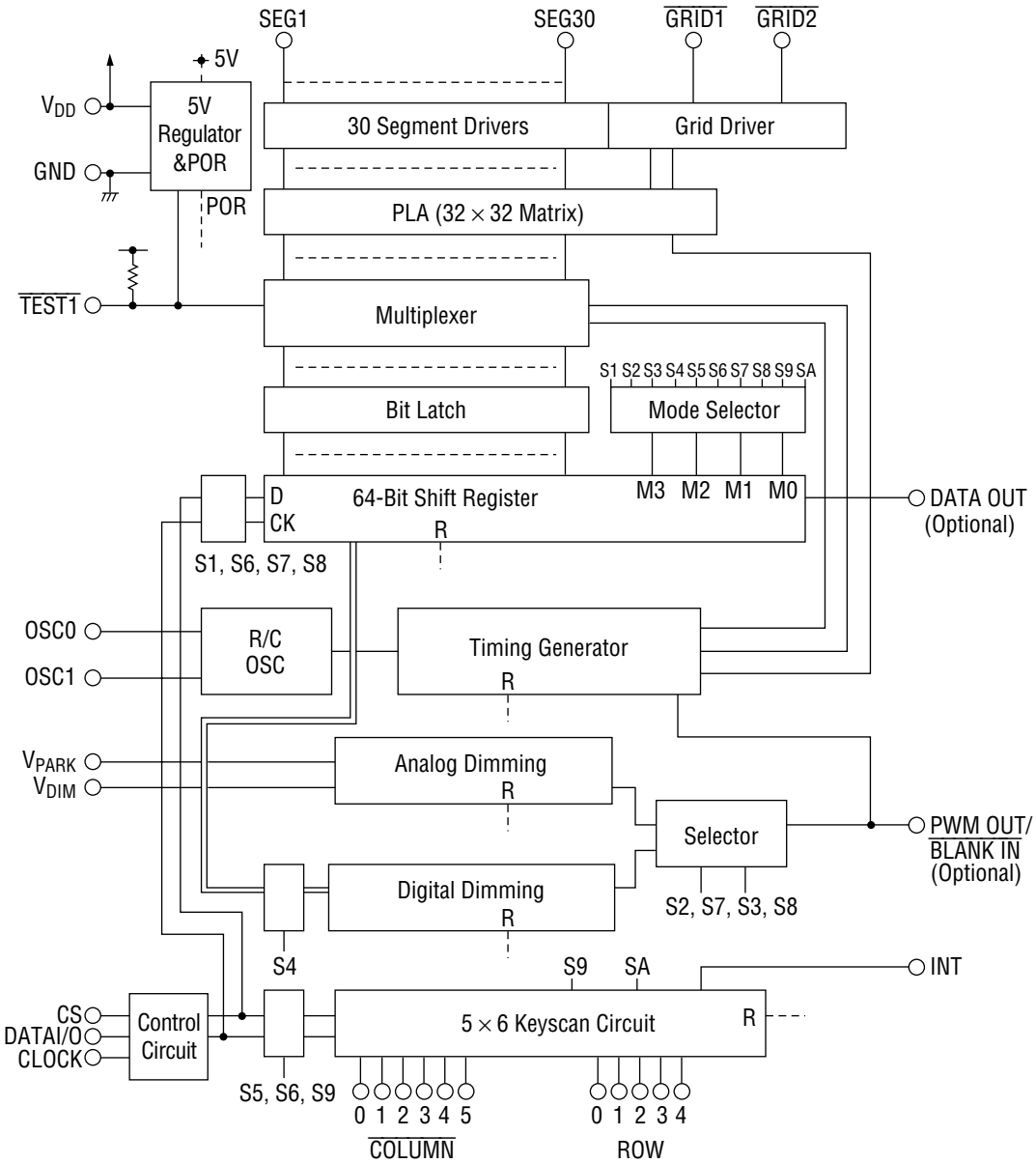
FEATURES

- Power supply voltage : 8V to 18V (built-in 5V regulator for logic)
- Operating temperature range : –40°C to +85°C
- 30-segment driver outputs (I_{OH} = –6mA at V_{OH} = V_{DD} – 0.8V)
- Built-in analog dimming circuit (PWM: 12.5% Max at 6-bit resolution)
- Built-in digital dimming circuit (11-bit resolution)
- Built-in 5 x 6 keyscan circuit
- Built-in RC oscillation circuit (external R and C)
- Built-in power-on-reset circuit.
- The product name differs depending on the bonding option pin selected:
  PWM OUT/$\overline{\text{BLANK IN}}$: MSC1200-01
  DATA OUT : MSC1200V-01
- Package :
  56-pin plastic QFP (QFP56–P–910-0.65–2K) (Product name: MSC1200-01GS-2K/MSC1200V-01GS-2K)

www.DataSheet4U.com

www.DataSheet4U.com

BLOCK DIAGRAM

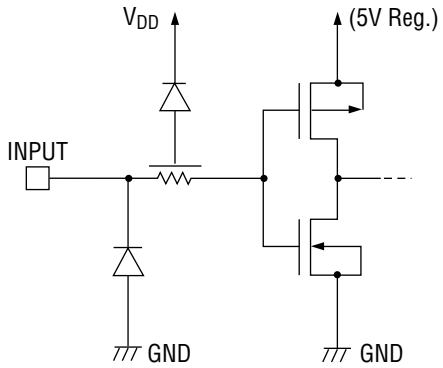


www.DataSheet4U.com

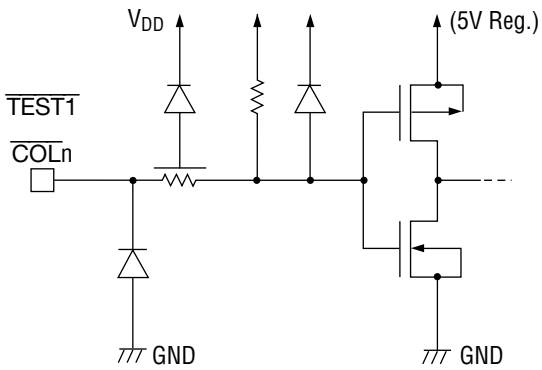
www.DataSheet4U.com

INPUT AND OUTPUT CONFIGURATION

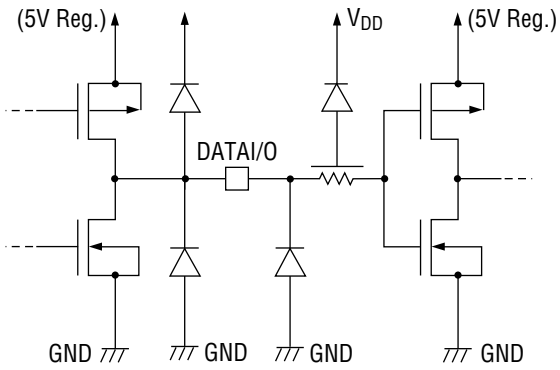
• Schematic Diagrams of Logic Portion Input Circuit



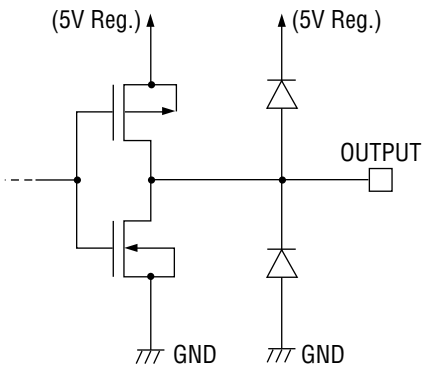
• Schematic Diagrams of Logic Portion Input Circuit 2



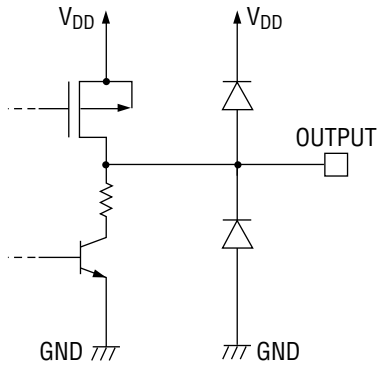
• Schematic Diagrams of Logic Portion Input/Output Circuit



• Schematic Diagrams of Logic Portion Output Circuit



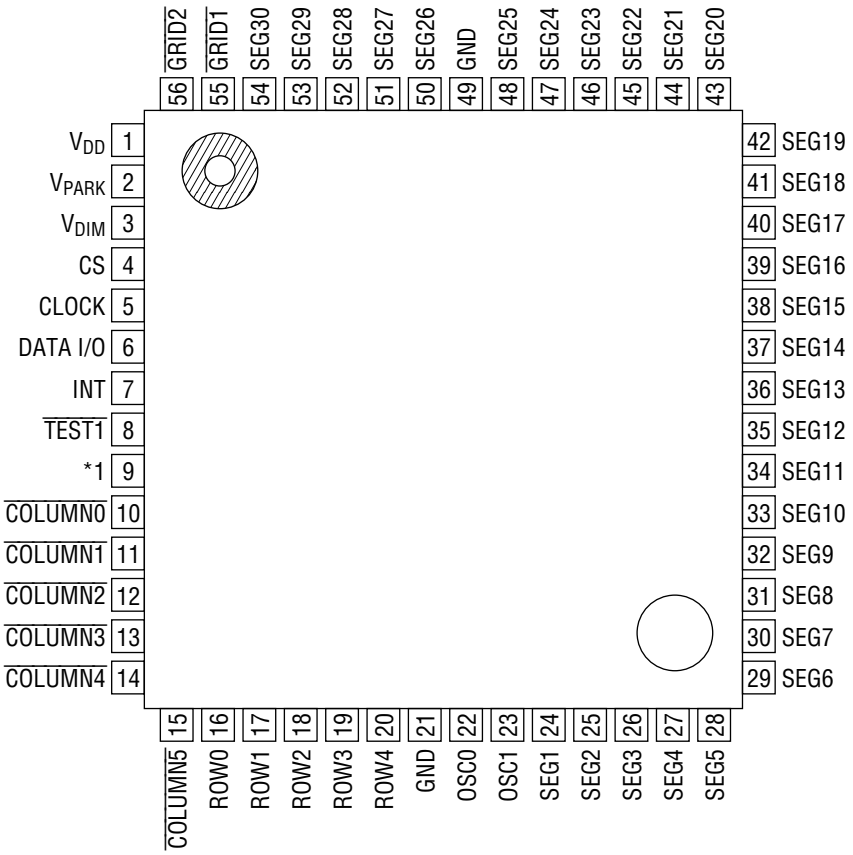
• Schematic Diagrams of Driver Output Circuit



www.DataSheet4U.com

www.DataSheet4U.com

PIN CONFIGURATION (TOP VIEW)



56-Pin Plastic QFP

*1 Bonding option pin (DATA OUT or PWM OUT/$\overline{\text{BLANK IN}}$)

www.DataSheet4U.com

www.DataSheet4U.com

PIN DESCRIPTIONS

Pin	Symbol	Type	Description
1	V_{DD}	—	Power Supply
2	V_{PARK}	I	Day/night switching pin. When the high level is input, the IC enters the night mode and the value determined by the analog or digital dimming circuit is used as the output duty. When the low level is input, the IC enters the day mode and the output duty is about 100%.
3	V_{DIM}	I	Analog voltage input for determining the analog dimming value. When the analog dimming circuit is used, the output duty is determined by the analog voltage to be input to this pin. When only the digital dimming circuit is used, pull down this pin to GND.
4	CS	I	Chip select input. Only when the high level is input to this pin, interfacing with a microcomputer is available through "CLOCK" and "DATA I/O" pins. Therefore, 2 signal lines of "CLOCK" and "DATA I/O" can be shared with other peripherals.
5	CLOCK	I	Serial clock input. Data is input-output through "DATA I/O" pin at the rising edge of the serial clock.
6	DATA I/O	I/O	Serial data input-output. This pin enters output mode only when the keyscan mode is selected. It enters input mode when other mode is selected.
7	INT	O	Interrupt signal output to microcomputer. When any key is pressed or released, key scanning is started. After the completion of the one cycle, this pin goes to the high level and keeps the high level until keyscan stop mode is selected.
8	$\overline{\text{TEST1}}$	I	Test signal input. As this pin has a built-in pull-up resistor, it must be left open or pulled up in the normal operation mode. When the low level is input to this pin, SEG1-30 go to the high level, and $\overline{\text{GRID1}}$ and $\overline{\text{GRID2}}$ go to the low level. (All segments go on.)
9	DATA OUT (Option)	O	Serial data output. Selecting this pin specifies the MSC1200V-01. The data from DATA I/O is shifted out on the rising edge of the shift clock with a delay of 64 bits in the shift register. This pin can be used for connecting the IC with a LED driver in series.
9	PWM OUT/ $\overline{\text{BLANK IN}}$ (Option)	I/O	When the V_{PARK} pin is at the high level, the pulse with the duty ratio determined by the analog or digital dimming circuit is output through this pin. When this pin is at the low level, the pulse with the duty ratio determined by external circuit is input to this pin. This pin has an internal active pull-up resistor, which becomes active only when the V_{PARK} pin is at the low level. When the V_{PARK} pin is at the low level, this pin receives blanking signal from external circuits, so that output duty cycle can be controlled. Selecting this pin specifies the MSC1200-01.

www.DataSheet4U.com

www.DataSheet4U.com

Pin	Symbol	Type	Description
10-15	$\overline{\text{COLUMN}}$ $\overline{\text{0-5}}$	I	Return inputs from key matrix switch. A pull-up resistor is internally connected to each of these pins so that they are at the high level except when the low level is input by depression of a key. These pins are "L" active.
16-20	ROW0-4	O	Key switch scanning outputs. Normally the low level is output through these pins. When any key is depressed or released, keyscanning is started and is continued until keyscan stop mode is selected. When the keyscan stop mode is selected and then keyscanning is stopped, all outputs of ROW0-4 go back to the low level.
21, 49	GND	—	Ground
22, 23	OSC0 OSC1	I/O	Connecting pins for RC oscillation circuit. Connect a resistor between OSC1 and OSC0, and a capacitor between OSC0 and ground.
24-48, 50-54	SEG1-30	O	Segment signal output. Signals for driving VF display tube are output through these pins.
55, 56	$\overline{\text{GRID1,2}}$	O	Grid signal output. Signals for driving VF display tube are output through these pins. Signals inverted with respect to grid signals are output. Normally, these pins are connected to the external grid driver (PNP transistor etc.) inputs.

www.DataSheet4U.com

www.DataSheet4U.com

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	—	–0.3 to +20	V
Input Voltage (1)	V_{IN1}	All inputs except V_{PARK}	–0.3 to +6	V
Input Voltage (2)	V_{IN2}	V_{PARK}	–0.3 to V_{DD} +0.3	V
Storage Temperature	T_{STG}	—	–65 to +150	°C
Power Dissipation	P_D	Ta = 85°C	400	mW

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	—	8	—	18	V
High Level Input Voltage (1)	V_{IH1}	All inputs except V_{PARK} & OSC0	3.8	—	5.5	V
High Level Input Voltage (2)	V_{IH2}	V_{PARK}	3.8	—	V_{DD}	V
High Level Input Voltage (3)	V_{IH3}	OSC0	4.5	—	5.5	V
Low Level Input Voltage (1)	V_{IL1}	All inputs except OSC0	0	—	0.8	V
Low Level Input Voltage (2)	V_{IL2}	OSC0	0	—	0.5	V
Clock Frequency	f_C	—	—	—	250	kHz
OSC Frequency	f_{OSC}	R = 4.7kΩ, C=10pF	—	3.3	—	MHz
Frame Frequency	f_{FR}	f_{OSC}=3MHz	—	201	—	Hz
Operating Temperature	T_{op}	—	–40	—	+85	°C

www.DataSheet4U.com

www.DataSheet4U.com

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Ta = –40 to +85°C, V_{DD} = 8 to 18V)

Parameter	Symbol	Condition	Min.	Max.	Unit
High Level Input Voltage (1) *1	V_{IH1}	—	3.8	5.5	V
High Level Input Voltage (2) *9	V_{IH2}	—	3.8	V_{DD}	V
High Level Input Voltage (3) *2	V_{IH3}	—	4.5	5.5	V
Low Level Input Voltage (1) *10	V_{IL1}	—	0	0.8	V
Low Level Input Voltage (2) *2	V_{IL2}	—	0	0.5	V
High Level Input Current (1) *3	I_{IH1}	V_{IH1} = 5.0V	–5	5	µA
High Level Input Current (2) *4	I_{IH2}	V_{IH2} = 5.0V	–30	30	µA
High Level Input Current (3) *5	I_{IH3}	V_{IH3} = 5.0V	–80	80	µA
Low Level Input Current (1) *3	I_{IL1}	V_{IL1} = 0V	–5	–5	µA
Low Level Input Current (2) *4	I_{IL2}	V_{IL2} = 0V	–160	–15	µA
Low Level Input Current (3) *5	I_{IL3}	V_{IL3} = 0V	–0.6	0.1	mA
Input Leakage Current *6	I_{IL}	V_I = 0 to 5.5V	–10	10	µA
High Level Output Voltage (1) *7	V_{OH1}	V_{DD} = 9.5V, I_{OH1} = –6mA	V_{DD} –0.8	—	V
High Level Output Voltage (2) *8	V_{OH2-1}	V_{DD} = 9.5V, I_{OH2} = –200µA	4	6	V
	V_{OH2-2}	V_{DD} = 9.5V, Output Open	4.5	6	V
Low Level Output Voltage (1) *7	V_{OL1-1}	V_{DD} = 9.5V, I_{OL1-1} = 500µA	—	2	V
	V_{OL1-2}	V_{DD} = 9.5V, I_{OL1-2} = 200µA	—	1	V
	V_{OL1-3}	V_{DD} = 9.5V, I_{OL1-3} = 2µA	—	0.3	V
Low Level Output Voltage (2) *8	V_{OL2}	V_{DD} = 9.5V, I_{OL2} = 200µA	—	0.8	V
Power Supply Current	I_{DD}	f_{OSC} = 3.3MHz, No load	—	20	mA

*1 Applicable to all input pins (except V_{PARK} and OSC0 pins)
*2 Applicable to OSC0 pin
*3 Applicable to CLOCK, DATA I/O, CS, and V_{PARK} pins
*4 Applicable to $\overline{\text{COLUMN0}}$ to $\overline{\text{COLUMN5}}$ and PWM OUT/$\overline{\text{BLANK IN}}$ pins
*5 Applicable to $\overline{\text{TEST1}}$ pin
*6 Applicable to V_{DIM} pin
*7 Applicable to SEG1 to SEG30, $\overline{\text{GRID1}}$, and $\overline{\text{GRID2}}$ pins
*8 Applicable to ROW0 to ROW4, DATA I/O, PWMOUT/$\overline{\text{BLANK IN}}$, DATAOUT, and INT pins.
*9 Applicable to V_{PARK} pin
*10 Applicable to all input pins (except OSC0)

www.DataSheet4U.com

www.DataSheet4U.com

AC Characteristics

(Ta = –40 to +85°C, V_{DD} = 8 to 18V)

Parameter	Symbol	Condition	Min.	Max.	Unit
Oscillation Frequency	f_{OSC}	R = 4.7kΩ±1%, C = 10pF±5%	2	4.66	MHz
Input Frequency to OSC0 from Outside	f_{OSCI}	External input only	2.4	3.7	MHz
Frame Frequency	f_{FR}	—	122	284	Hz
PWM OUT Frequency	f_{PWM}	—	244	568	Hz
Clock Frequency	f_C	—	—	250	kHz
Clock Pulse Width	t_{CW}	—	1.3	—	µs
Data Setup Time	t_{DS}	—	1	—	µs
Data Hold Time	t_{DH}	—	200	—	ns
CS Pulse Width	t_{CSW}	—	68	—	µs
CS Off Time	t_{CSL}	—	30	—	µs
CS Setup Time CS – Clock Time	t_{CSH}	—	2	—	µs
CS Hold Time Clock – CS Time	t_{CSH}	—	2	—	µs
Data Output Delay Clock – Data output Time	t_{PD}	—	—	1	µs
SEG & $\overline{GRID}$ Output Delay from CS	t_{ODS}	Cl = 100pF	—	8	µs
Slew Rate (All Drivers)	t_R	Cl = 100pF, t = 20% to 80% or 80% to 20% of V_{DD}	—	5	µs
CS Time at Power-on	t_{PCS}	—	300	—	µs
Hold Time at Power-off	t_{POF}	When mounted on the unit V_{DD}=0.0V	5	—	ms
Rise Time at Power-on	t_{PRZ}	When mounted on the unit	—	100	µs

www.DataSheet4U.com

www.DataSheet4U.com

Dimming Characteristics

• DC characteristics

(Ta = –40 to +85°C, V_{DD} = 8 to 18V)

Parameter	Condition	Min.	Typ.	Max.	Unit
D/A Output Voltage Error	—	—	—	±3	%
Reference Voltage Accuracy	Note 1	—	—	±6	%

Note: 1. Reference voltage is 6.6V typical.

Keyscan Characteristics

(Ta = –40 to +85°C, V_{DD} = 8 to 18V)

Parameter	Condition	Min.	Typ.	Max.	Unit
Keyscan Cycle Time	f_{OSC}=3.3 MHz	275	390	640	µs
Keyscan Pulse Width	f_{OSC}=3.3 MHz	55	78	128	µs

www.DataSheet4U.com

www.DataSheet4U.com

TIMING DIAGRAM

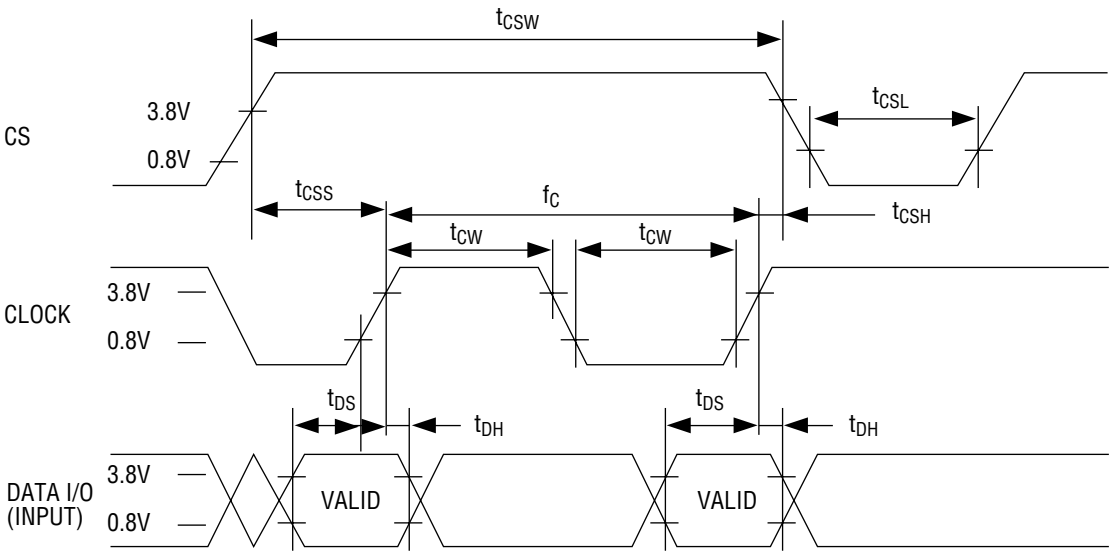


Figure 1 Data Input Timing

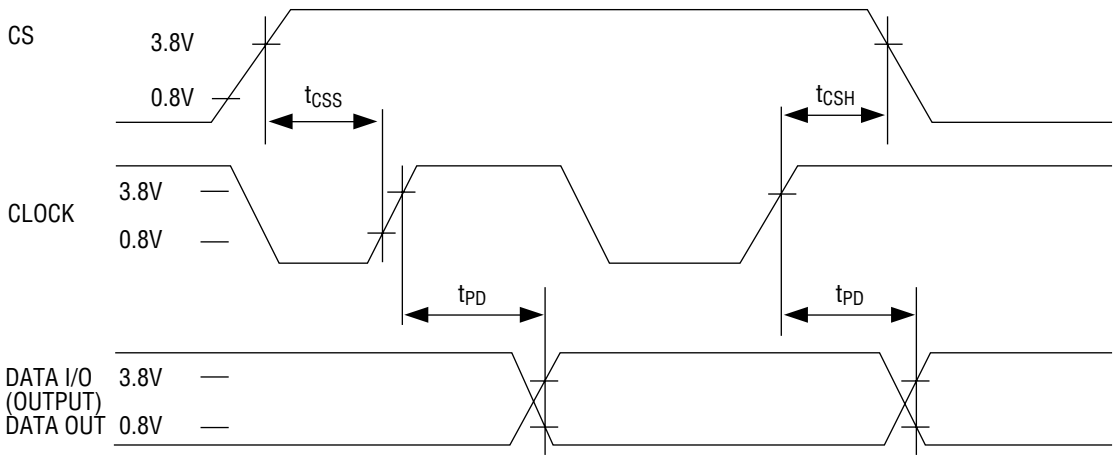


Figure 2 Data Output Timing

www.DataSheet4U.com

www.DataSheet4U.com

TIMING DIAGRAM (Continued)

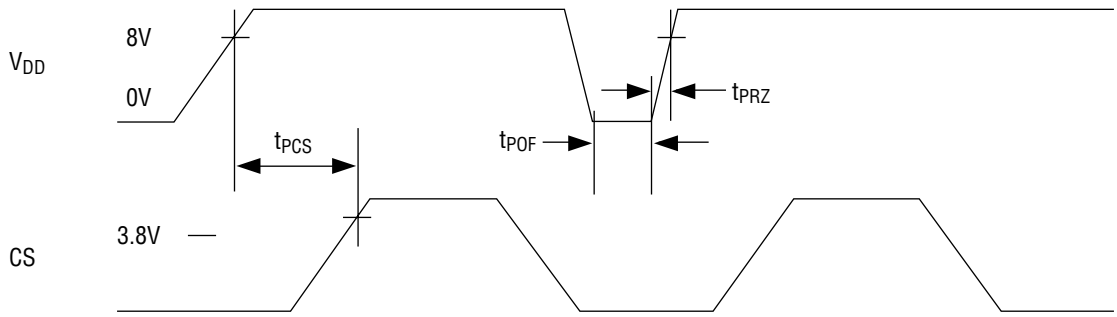


Figure 3 Power-On Timing

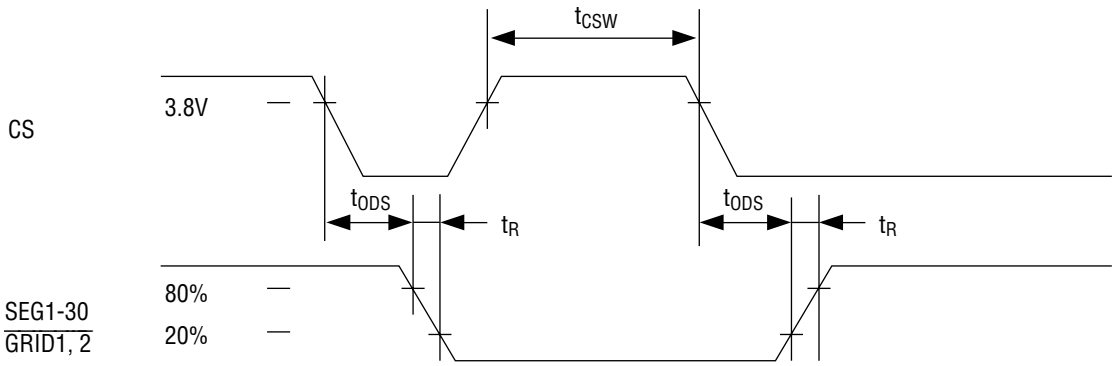


Figure 4 SEG & $\overline{GRID}$ Output Timing

www.DataSheet4U.com

www.DataSheet4U.com

FUNCTIONAL DESCRIPTION

Power-on Reset

The IC is initialized by the built-in power-on reset circuit at power-on. The status of the internal circuit after initialization is as follows;

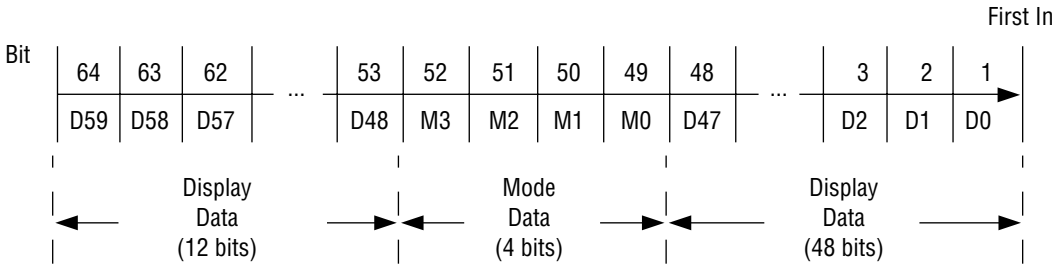
1) Shift registers and latches are reset.
2) Analog dimming is selected.
3) Digital dimming data register is reset.
4) Display data input mode is selected.

Data Input

Data input is valid only when the high level is applied to the "CS" pin. Input data is input into the shift register through "DATA I/O" pin at the rising edge of CLOCK. The data is automatically loaded to latches at the falling edge of "CS" signal.

[Data Format]

1) Display Data Input Mode
   Input data : 64 bits
   VF display data : 60 bits
   Mode select data : 4 bits



2) Correspondence between segment outputs and shift register bits

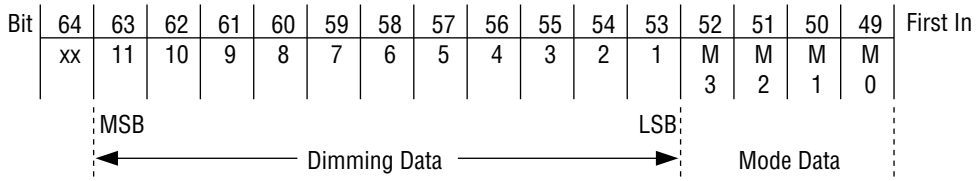
	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	SEGn
Bit	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	GRID1
	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	GRID2

www.DataSheet4U.com

www.DataSheet4U.com

3) Digital Dimming Data Input Mode

Input data : 16 bits
Digital dimming data : 11 bits
Mode select data : 4 bits



(MSB)											(LSB)	DUTY CYCLE
X	0	0	0	0	0	0	0	0	0	0	0	0/2048
X	0	0	0	0	0	0	0	0	0	0	1	1/2048
X	1	1	1	1	1	1	1	0	0	0	0	2032/2048
X	1	1	1	1	1	1	1	1	1	1	1	2032/2048

www.DataSheet4U.com

www.DataSheet4U.com

4) Function Mode

Mode	M3	M2	M1	M0	Function
S1	0	0	0	0	Display Data Input
S2	0	0	1	1	Analog Dimming Select
S3	0	1	0	1	Digital Dimming Select
S4	0	0	0	1	Digital Dimming Data Input & Digital Dimming Select
S5	0	1	1	1	Keyscan Data Output
S6	0	1	1	0	Display Data Input & Keyscan Data Output
S7	0	0	1	0	Display Data Input & Analog Dimming Select
S8	0	1	0	0	Display Data Input & Digital Dimming Select
S9	1	0	0	0	Keyscan Data Output & Keyscan Stop
SA	1	0	0	1	Keyscan S_{TOP}

Note: Other combinations are used for test modes.

5) Analog Dimming Mode

Analog dimming is automatically selected when the V_{PARK} pin is set to the high level after power-on. Therefore, when digital dimming is used, mode setting is required before the V_{PARK} pin is set to the high level.
The output duty ratio for analog dimming is 12.5% maximum. The correspondence between threshold voltage and output duty ratio is shown in V_{DIN} Threshold Dimming Voltage VS. PWM Duty Cycle.

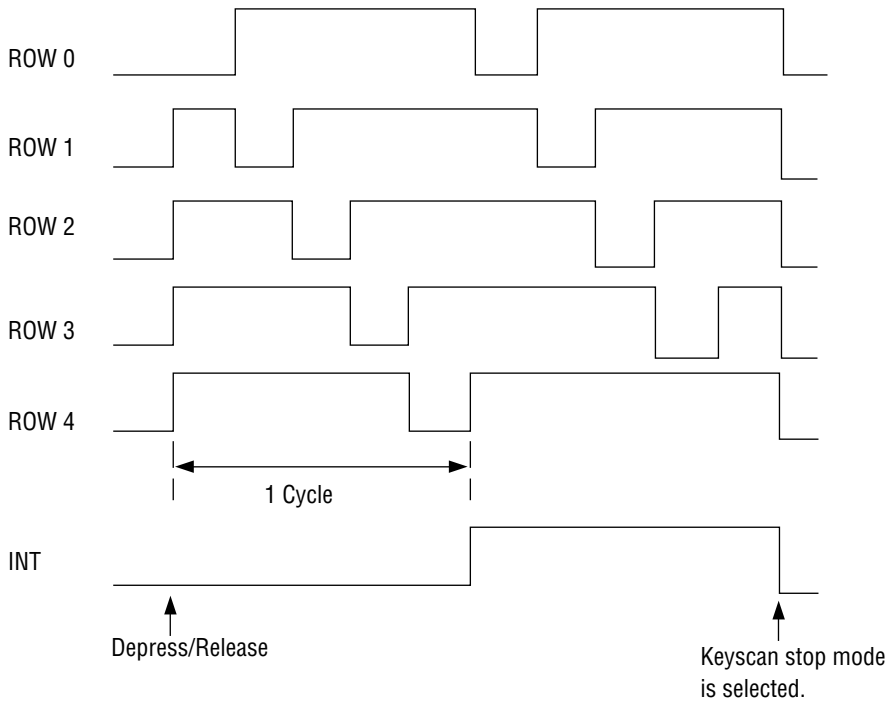
www.DataSheet4U.com

www.DataSheet4U.com

Keyscan

Keyscanning is started only when depression or release of any key is detected in order to minimize noise caused by scanning signal. Then, keyscanning is continued until the keyscan stop mode signal is sent from a microcomputer. The INT pin goes to the high level at the completion of 1-cycle scanning after the keyscan start, so the (high level) signal sent from the INT pin can be used as an interrupt signal.

[Keyscan Timing]



Note: Keyscanning cannot be stopped by selecting the keyscan stop mode only once if:
- keyscanning is started after depression or release of any key is detected, and then
- a key is depressed or released again before the keyscan stop mode is selected.

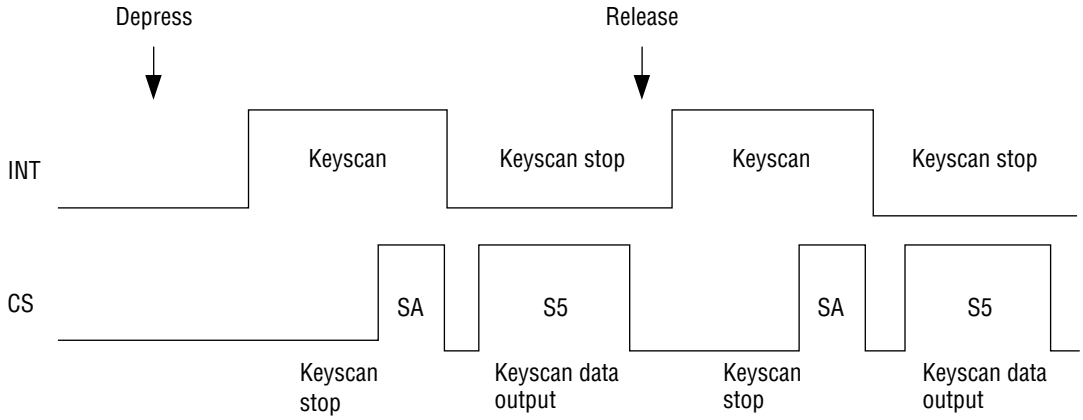
To stop keyscanning, it is required to select the keyscan stop mode once again.

www.DataSheet4U.com

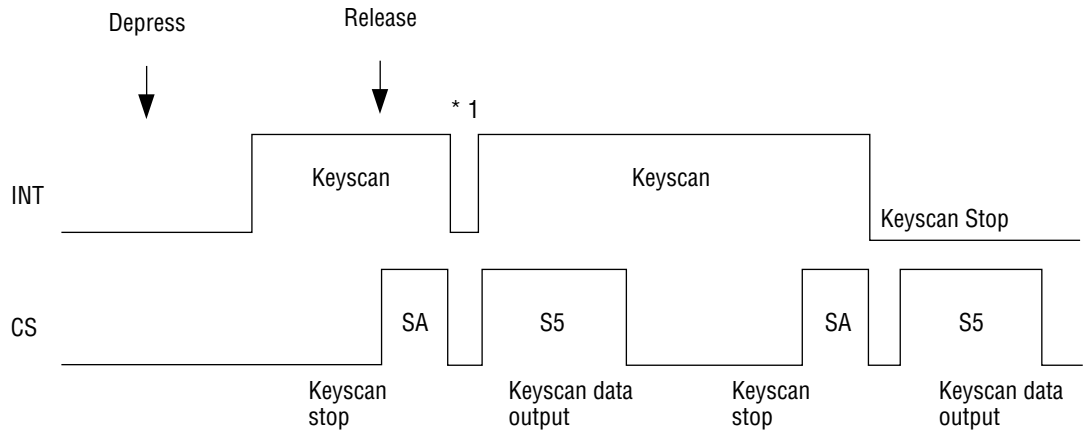
www.DataSheet4U.com

[Example]

A) When Key Input Status is Changed



B) When Key Input Status is Changed before Keyscan Stop Mode Select



*1: Keyscanning resumes after short period of keyscan stop.

www.DataSheet4U.com

www.DataSheet4U.com

Keyscan Data Output

When keyscan data output mode is selected, "DATA I/O" pin is changed to an output mode. Then, 30 bits of keyscan data come out from "DATA I/O" pin synchronizing with the rising edge of the clock. After the completion of 30 bits data output, the IC returns to the display data input mode synchronizing with the falling edge of CS.

[Data Format]

1) Keyscan Data Stop Mode

Since the DATA I/O pin goes to the output mode after the keyscan stop mode signal is received, be sure to output the keyscan data.
Input data : 16 bits
Mode select data : 4 bits

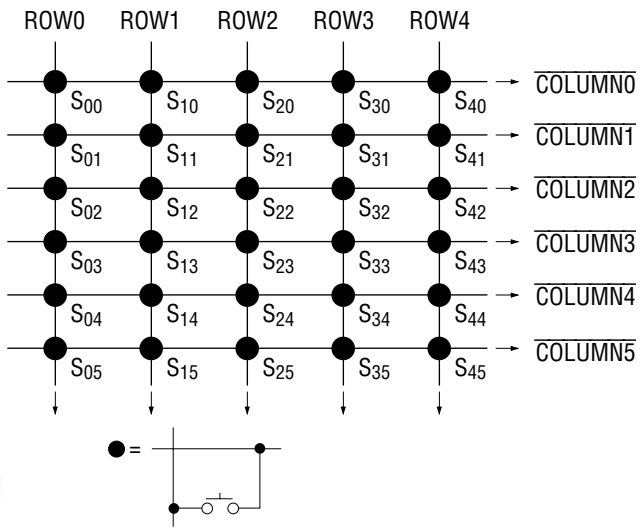
Bit	64	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	First In
	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	M 3	M 2	M 1	M 0	
													Mode Data				

2) Keyscan Data Output Mode
Input data : 30 bits
Output data : 30 bits

CLOCK	30	29	28	·····	9	8	7	6	5	4	3	2	1	First Out
	S 45	S 44	S 43	·····	S 12	S 11	S 10	S 05	S 04	S 03	S 02	S 01	S 00	Keyscan Data

S x x
↑ ↑
ROW $\overline{\text{COLUMN}}$

3) Key switch matrix for $\overline{\text{COLUMN}}$ input and ROW output



www.DataSheet4U.com

www.DataSheet4U.com

GRID/SEG Driver Operation and Digital/Analog Dimming Operation

Figure 5 shows the output timing of the GRID and SEG driver when the V_{PARK} is the "H" level.

Figure 6 shows the output timing of the GRID and SEG drivers for the digital diming mode operation.

Figure 7 shows the output timing of the GRID and SEG drivers for the analog dimming mode operation.

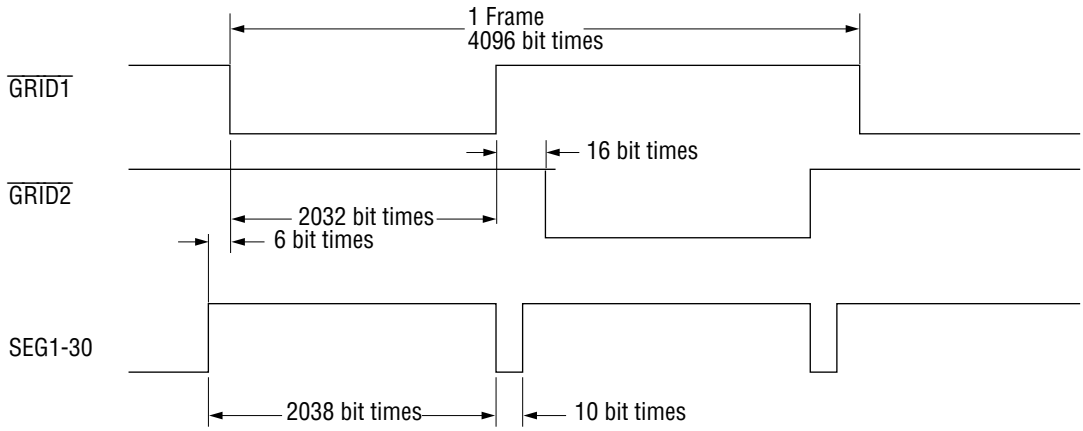


Figure 5 GRID and SEG Output Timing (V_{PARK}="H")

Note: 1 bit time = T_{OSC} $(4/f_{OSC})$ = 1.2µs (typ.)

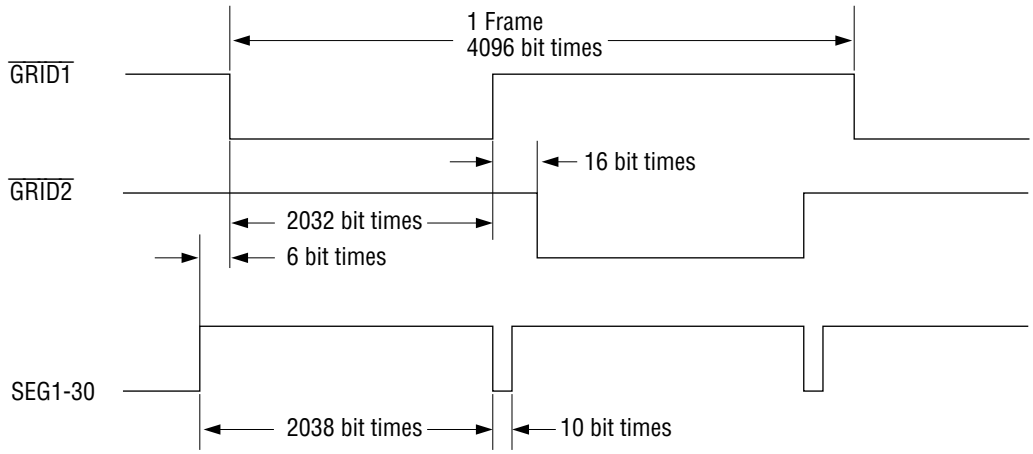


Figure 6 GRID and SEG Output Timing (Digital Dimming Mode)

Notes: 1. Shown above is the timing in the digital dimming mode with the duty cycle of 2032/2048 at V_{PARK} = "L".
2. The length of time that the grids and the segments are turned on is specified with respect to 11 bits of the ditigal dimming data.
3. 1 bit time = T_{OSC} $(4/f_{OSC})$ = 1.2µs (typ.)

www.DataSheet4U.com

www.DataSheet4U.com

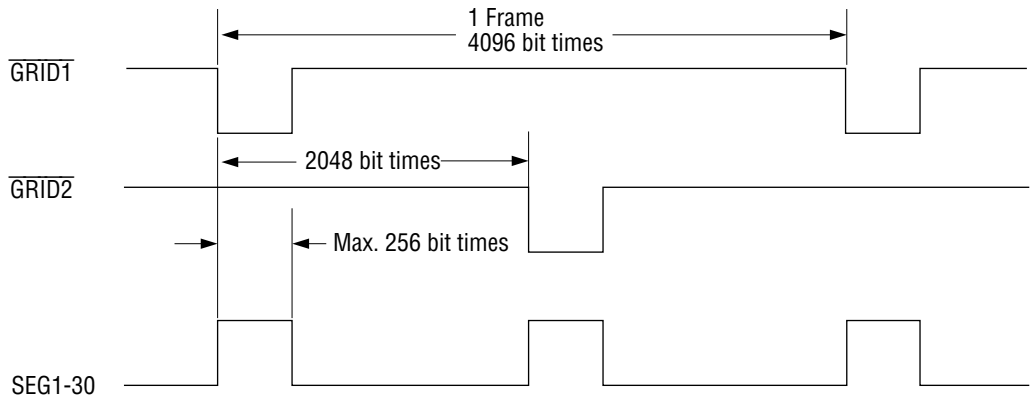


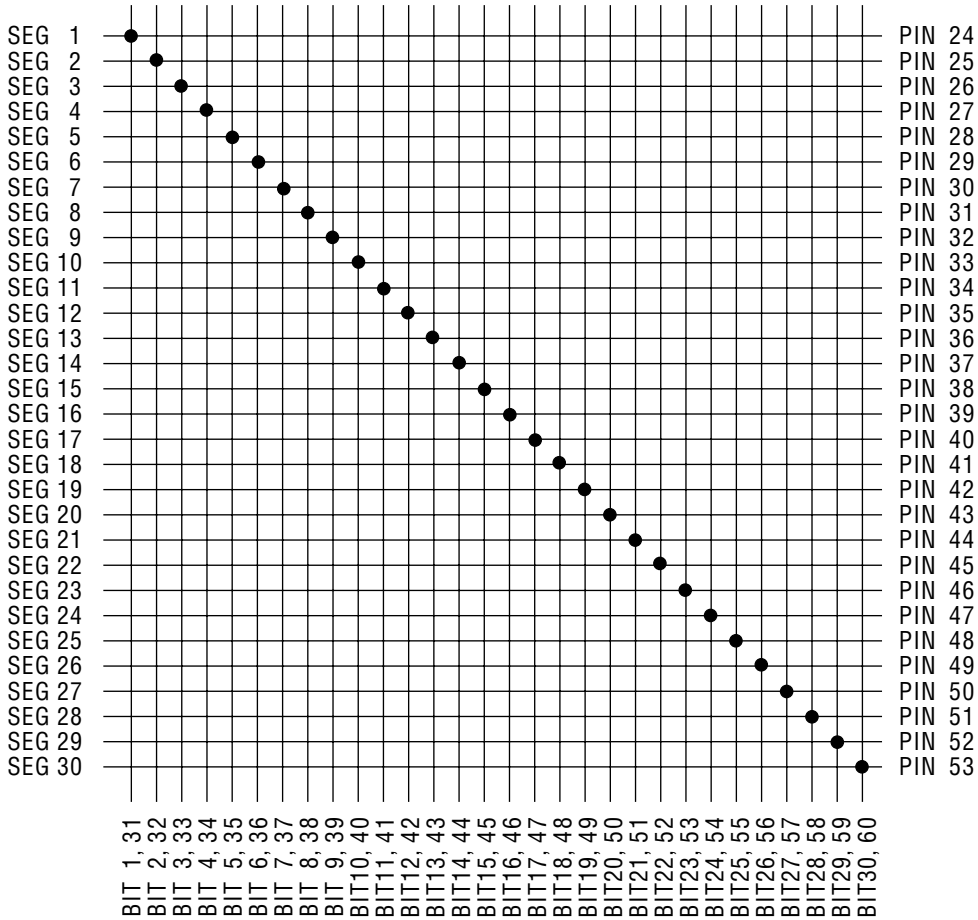
Figure 7 GRID and SEG Output Timing (Analog Dimming Mode)

Notes: 1. Shown above is the timing for the GRID and SEG Drivers in the analog dimming mode at V_{PARK} = "L".
2. 1 bit time = T_{OSC} $(4/f_{OSC})$ = 1.2µs (typ.)

www.DataSheet4U.com

www.DataSheet4U.com

PLA Code Table



PIN NAME	OUTPUT	PIN NAME	OUTPUT	PIN NAME	OUTPUT
SEG1	BIT 1, 31	SEG11	BIT 11, 41	SEG21	BIT 21, 51
SEG2	BIT 2, 32	SEG12	BIT 12, 42	SEG22	BIT 22, 52
SEG3	BIT 3, 33	SEG13	BIT 13, 43	SEG23	BIT 23, 53
SEG4	BIT 4, 34	SEG14	BIT 14, 44	SEG24	BIT 24, 54
SEG5	BIT 5, 35	SEG15	BIT 15, 45	SEG25	BIT 25, 55
SEG6	BIT 6, 36	SEG16	BIT 16, 46	SEG26	BIT 26, 56
SEG7	BIT 7, 37	SEG17	BIT 17, 47	SEG27	BIT 27, 57
SEG8	BIT 8, 38	SEG18	BIT 18, 48	SEG28	BIT 28, 58
SEG9	BIT 9, 39	SEG19	BIT 19, 49	SEG29	BIT 29, 59
SEG10	BIT 10, 40	SEG20	BIT 20, 50	SEG30	BIT 30, 60

www.DataSheet4U.com

www.DataSheet4U.com

V_{DIM} Threshold Dimming Voltage VS. PWM Duty Cycle

V_{DD}=12.8V

Pulse Step Number	PWM Duty Cycle		Threshold Voltage	Pulse Step Number	PWM Duty Cycle		Threshold Voltage
	Pulse Count	%	Vref		Pulse Count	%	3.000
52	256/2048	12.5	4.200	26	56/2048	2.73	2.950
51	240/2048	11.7	4.130	25	52/2048	2.54	2.900
50	224/2048	10.9	4.070	24	48/2048	2.34	2.850
49	208/2048	10.2	4.000	23	46/2048	2.25	2.820
48	192/2048	9.38	3.930	22	44/2048	2.15	2.800
47	184/2048	8.98	3.890	21	42/2048	2.05	2.770
46	176/2048	8.59	3.850	20	40/2048	1.95	2.740
45	168/2048	8.20	3.810	19	38/2048	1.86	2.710
44	160/2048	7.81	3.770	18	36/2048	1.76	2.680
43	152/2048	7.42	3.725	17	34/2048	1.66	2.650
42	144/2048	7.03	3.680	16	32/2048	1.56	2.615
41	136/2048	6.64	3.625	15	30/2048	1.46	2.580
40	128/2048	6.25	3.580	14	28/2048	1.37	2.540
39	120/2048	5.86	3.525	13	26/2048	1.27	2.500
38	112/2048	5.47	3.460	12	24/2048	1.17	2.470
37	104/2048	5.08	3.400	11	23/2048	1.12	2.450
36	96/2048	4.69	3.340	10	22/2048	1.07	2.430
35	92/2048	4.49	3.305	9	21/2048	1.03	2.410
34	88/2048	4.30	3.270	8	20/2048	0.98	2.390
33	84/2048	4.10	3.240	7	19/2048	0.93	2.370
32	80/2048	3.91	3.200	6	18/2048	0.88	2.340
31	76/2048	3.71	3.160	5	17/2048	0.83	2.320
30	72/2048	3.52	3.120	4	16/2048	0.78	2.295
29	68/2048	3.32	3.080	3	15/2048	0.73	2.270
28	64/2048	3.13	3.040	2	14/2048	0.68	2.245
27	60/2048	2.93	2.93	1	13/2048	0.63	0.000
				0			

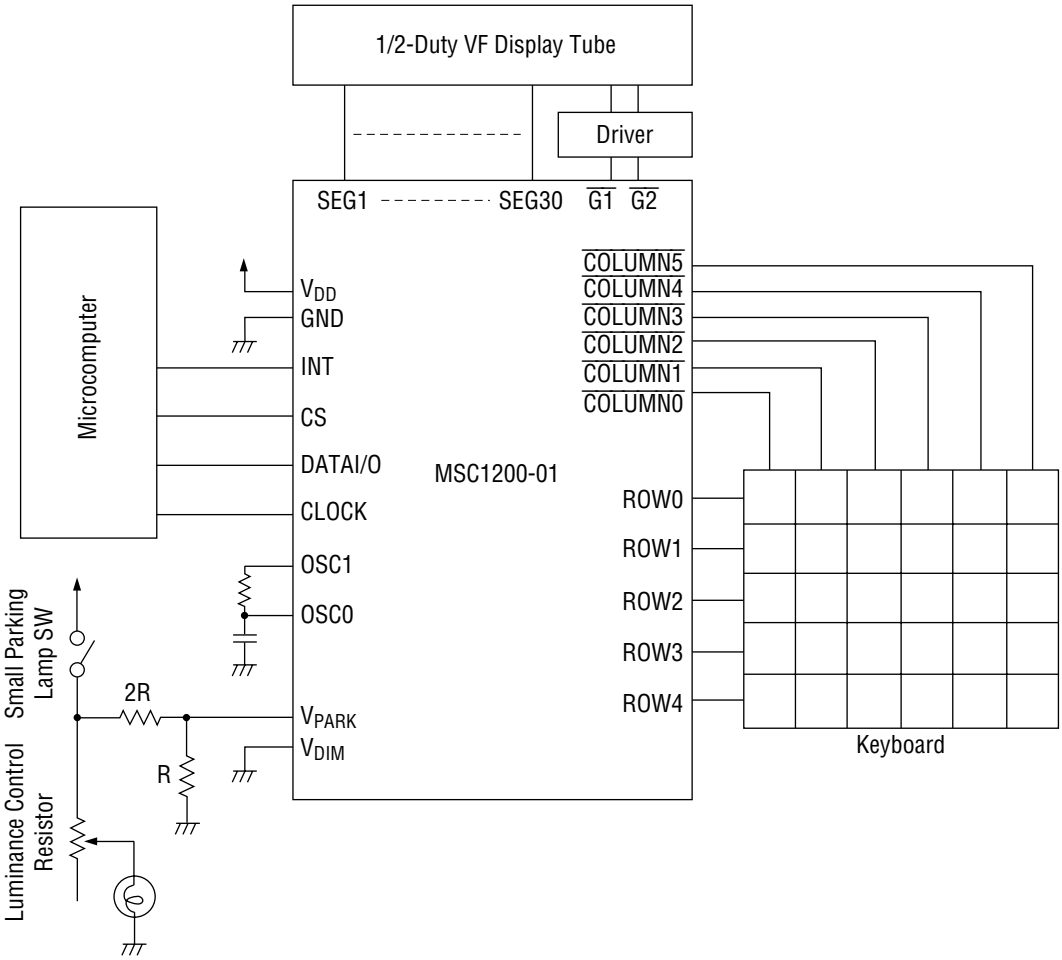
Note: A threshold voltage more than 5V cannot be set.

www.DataSheet4U.com

www.DataSheet4U.com

APPLICATION CIRCUITS

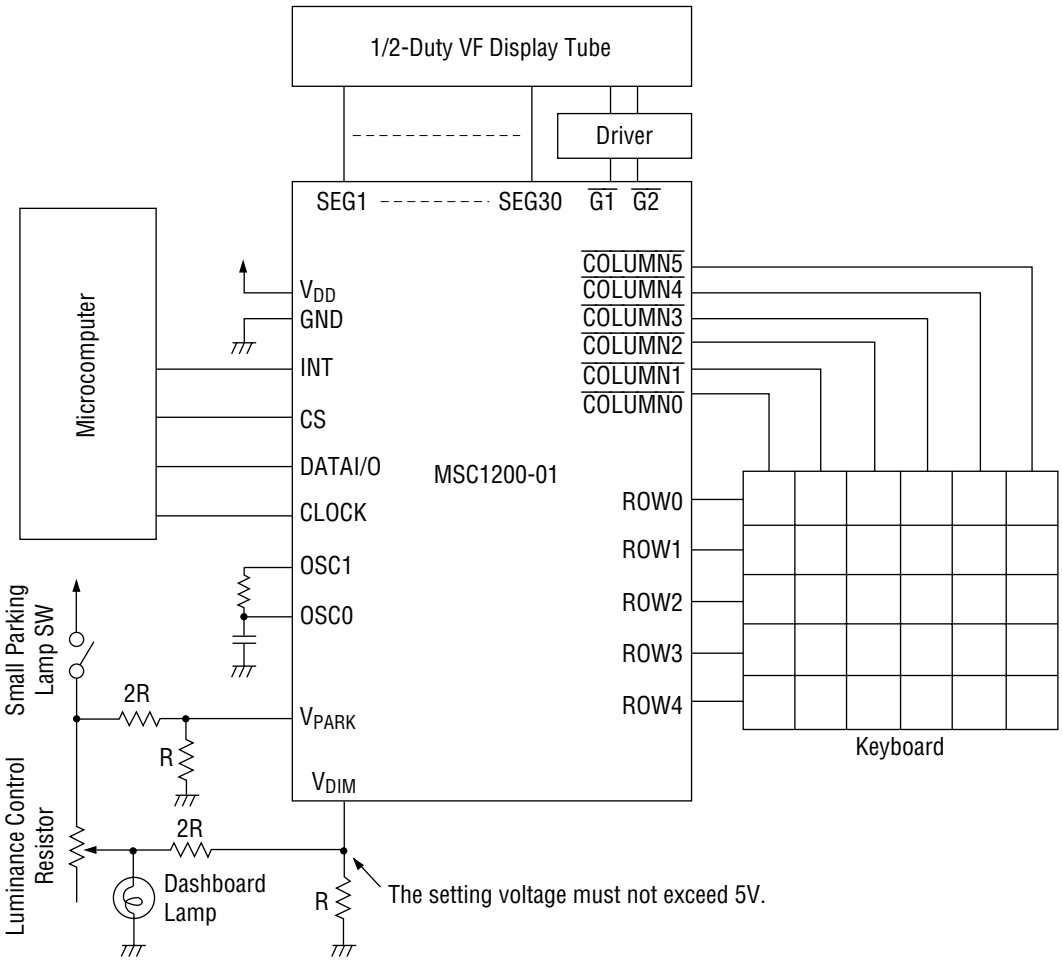
(A) Digital Dimming



www.DataSheet4U.com

www.DataSheet4U.com

(B) Analog Dimming



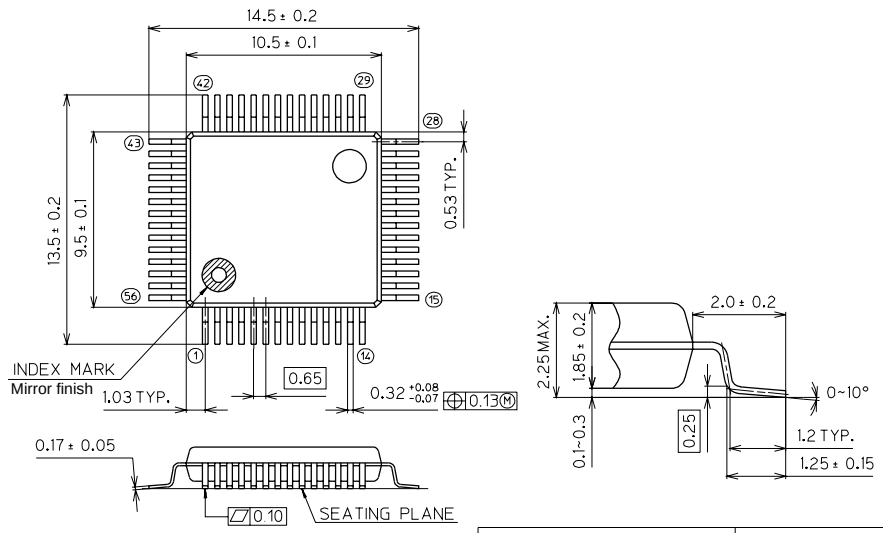
www.DataSheet4U.com

www.DataSheet4U.com

PACKAGE DIMENSIONS

(Unit : mm)

QFP56-P-910-0.65-2K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5 mm)
Package weight (g)	0.43 TYP.
Rev. No./Last Revised	4/Vov. 28, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

www.DataSheet4U.com

www.DataSheet4U.com

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

5. Neither indemnity against nor license of a third party's industrial and intellectual property right, etc. is granted by us in connection with the use of the product and/or the information and drawings contained herein. No responsibility is assumed by us for any infringement of a third party's right which may result from the use thereof.

6. The products listed in this document are intended for use in general electronics equipment for commercial applications (e.g., office automation, communication equipment, measurement equipment, consumer electronics, etc.). These products are not authorized for use in any system or application that requires special or enhanced quality and reliability characteristics nor in any system or application where the failure of such system or application may result in the loss or damage of property, or death or injury to humans. Such applications include, but are not limited to, traffic and automotive equipment, safety devices, aerospace equipment, nuclear power control, medical equipment, and life-support systems.

7. Certain products in this document may need government approval before they can be exported to particular countries. The purchaser assumes the responsibility of determining the legality of export of these products and will take appropriate and necessary steps at their own expense for these.

8. No part of the contents contained herein may be reprinted or reproduced without our prior permission.

9. MS-DOS is a registered trademark of Microsoft Corporation.

Copyright 2000 Oki Electric Industry Co., Ltd.

Printed in Japan

www.DataSheet4U.com