

MSC1201-xx

60-Bit VFD Tube Driver with Digital Dimming and PWM Conversion Function

GENERAL DESCRIPTION

The MSC1201-xx is a 1/2 duty vacuum fluorescent display tube driver implemented in Bi-CMOS technology. This LSI consists of 64-bit shift registers, 64 latches, PWM conversion circuit, a digital dimming circuit, 30-segment driver and 2-grid driver. As the MSC1201-xx has both a digital dimming circuit and a PWM conversion circuit which converts PWM signal for lamp dimming control to PWM signal for VFD tube dimming control, the dimming control can be realized without any external circuit.

The interface with a MCU can be done only with 3 wires (CS, DATA and CLOCK signals). Also, DATA and CLOCK signal lines can be shared with other peripherals because of chip select function by CS signal.

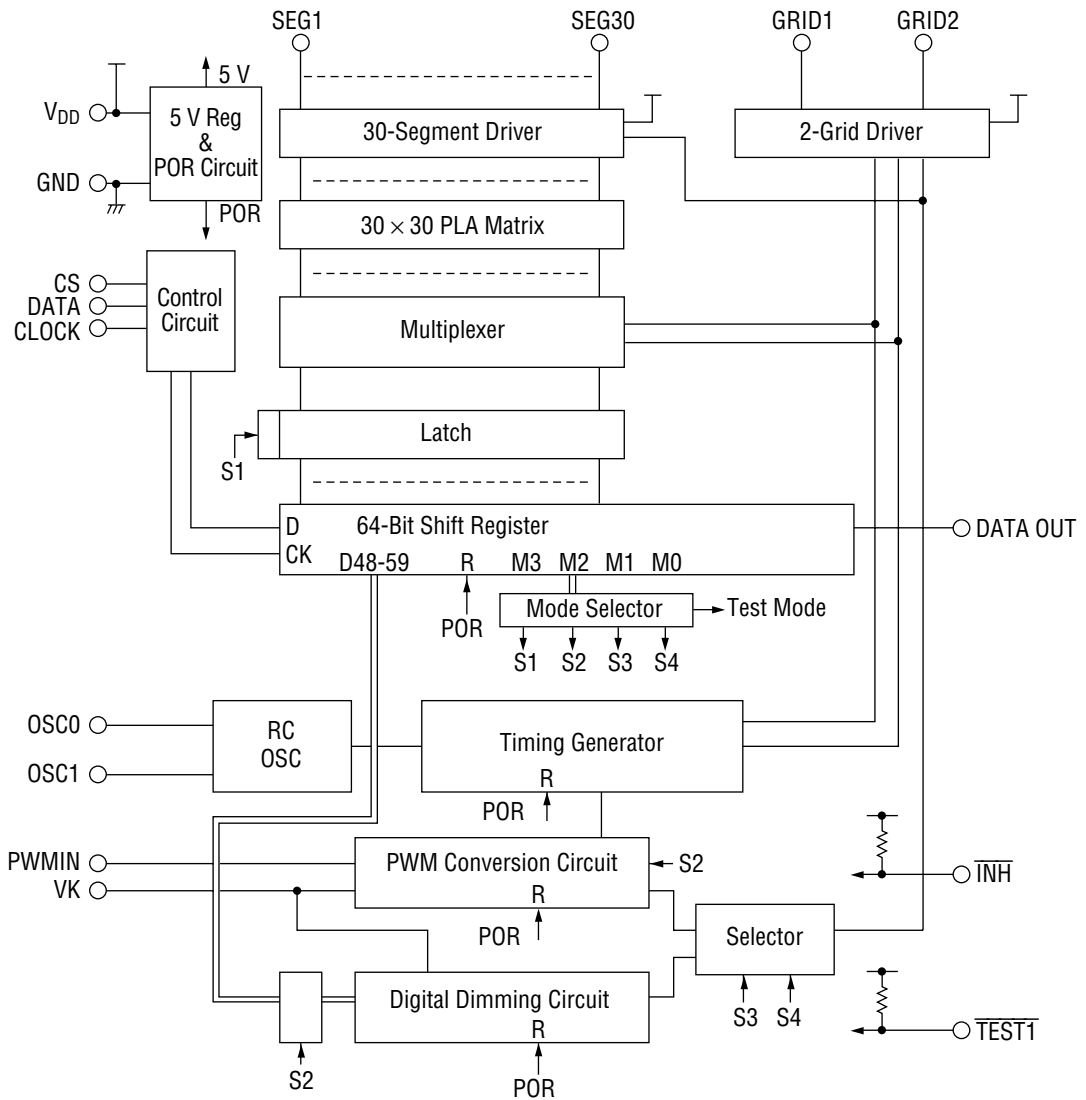
For the general purpose code, the code number is -01. (Product name: MSC1201-01GS-2K)

For a custom code, the code number will be ordered at any time.

FEATURES

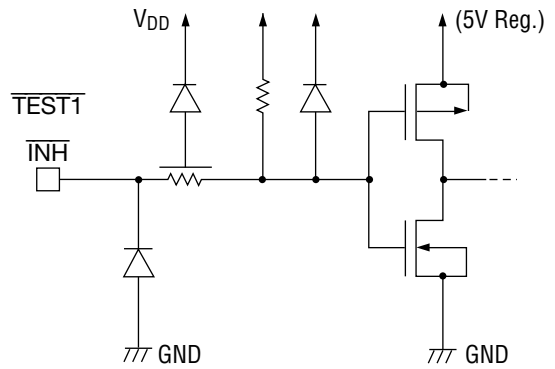
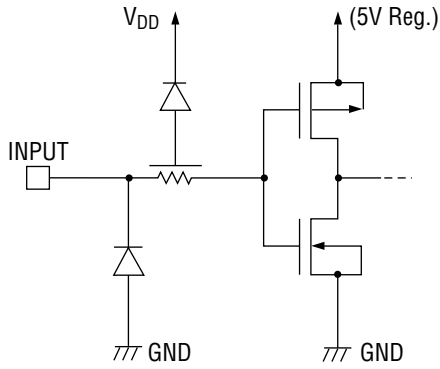
- Single supply voltage : $V_{DD} = 8\text{ V to }18\text{ V}$ (built-in 5 V logic regulator)
- Operating temperature range : $T_a = -40^\circ\text{C to }+85^\circ\text{C}$
- 30-segment driver outputs ($I_{OH} = -6\text{ mA at }V_{OH} = V_{DD} - 0.8\text{ V}$)
- 2-grid pre-driver outputs ($I_{OH} = -30\text{ mA at }V_{OH} = V_{DD} - 0.8\text{ V}$)
- Built-in digital dimming circuit (11-bit resolution)
- Built-in oscillation circuit (external R and C, $f_{OSC} = 2.0\text{ MHz}$)
- Built-in Power-On-Reset circuit.
- Lamp PWM signal → Built-in PWM conversion circuit for vacuum fluorescent display tube.
- Built-in RC Oscillation (external R and C)
- Correspondence between shift register and output segment is settable optionally using built in mask programmable 30×30 PLA.
- Package :
44-pin plastic QFP (QFP44-P-910-0.80-2K) (Product name: MSC1201-xxGS-2K)
xx indicates the code number

BLOCK DIAGRAM

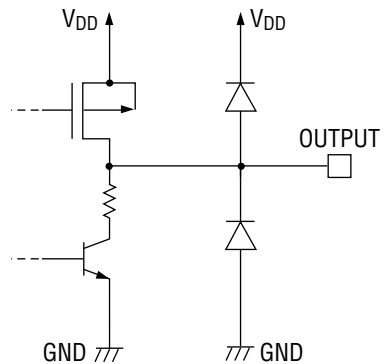
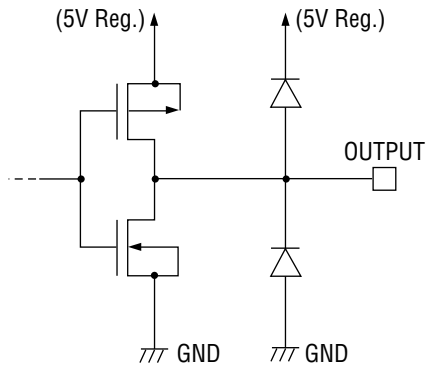


INPUT AND OUTPUT CONFIGURATION

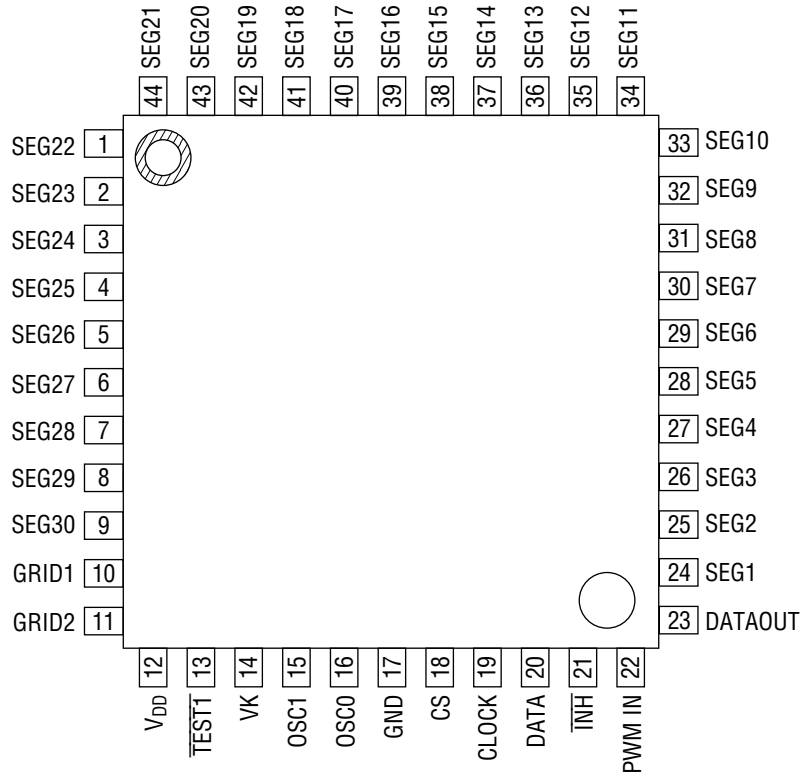
- Schematic Diagrams of Logic Portion Input Circuit 1
- Schematic Diagrams of Logic Portion Input Circuit 1



- Schematic Diagrams of Logic Portion Output Circuit
- Schematic Diagrams of Driver Output Circuit



PIN CONFIGURATION (TOP VIEW)



44-Pin Plastic Package

PIN DESCRIPTIONS

| Pin | Symbol | I/O | Description |
|--------------|---------------------------|-----|---|
| 1-9 24-44 | SEG1-30 | 0 | Segment output pin for VFD |
| 10, 11 | GRID1, 2 | 0 | Grid 1 and Grid 2 output pins for VFD |
| 16 | OSC0 | I | RC oscillation pins. Connect a resistor between OSC1 and OSC0 pin and a capacitor between OSC0 and GND pin. |
| 15 | OSC1 | 0 | |
| 18 | CS | I | Chip select input. Only when the high level is input to this pin, interfacing with a MCU is available through "CLOCK" and "DATA" pins. Therefore, 2-signal lines of "CLOCK" and "DATA" can be shared with other peripherals. |
| 20 | DATA | I | Input which receives display data and digital dimming data from a MCU. Data is shifted in at the rising edge of the shift clock. |
| 19 | CLOCK | I | Serial clock input. Data that is input through "DATA" pin is input and output by synchronization with the rising edge of the serial clock. |
| 23 | DATA OUT | 0 | Serial data output. Data is shifted out at the rising edge of the serial clock with the delay of 64-bit time. This pin is used for cascading this LSI with other drivers such as a LED driver. |
| 22 | PWMIN | I | PWM signal input. |
| 14 | VK | I | Dimming select input. When the high level is input, daylight-mode output duty cycle is about 100% for each grid time for PWM conversion and digital dimming mode. When the low level is input, the dark-mode output duty cycle is determined by the duty cycle of the PWM signal input to PWM IN and the digital dimming output duty cycle is determined by digital dimming data. |
| 21 | $\overline{\text{INH}}$ | I | Blank Display input with a built-in pull-up resistor. When set to "L", all the drivers output "L". When display duty is not controlled by this signal, leave this pin open. |
| 13 | $\overline{\text{TEST1}}$ | I | Test signal input pin. As this pin is used for shipping test of the LSI, leave open in the normal operation mode. |
| 12 | V _{DD} | — | Power Supply |
| 17 | GND | — | Ground |

ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Condition | Rating | Unit |
|---------------------------|------------------|-----------------------|-------------|------|
| Supply Voltage | V _{DD} | — | -0.3 to +20 | V |
| Input Voltage | V _{IN} | All inputs | -0.3 to +6 | V |
| Storage Temperature Range | T _{STG} | — | -65 to +150 | °C |
| Power Dissipation | P _D | T _a = 85°C | 0.4 | W |

RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|------------------------------|------------------|----------------------------|------|------|-----------------|------|
| Supply Voltage | V _{DD} | — | 8 | — | 18 | V |
| High Level Input Voltage (1) | V _{IH1} | All inputs except OSC0, VK | 3.8 | — | 5.5 | V |
| High Level Input Voltage (2) | V _{IH2} | VK | 3.8 | — | V _{DD} | V |
| High Level Input Voltage (3) | V _{IH3} | OSC0 | 4.5 | — | 5.5 | V |
| Low Level Input Voltage (1) | V _{IL1} | All inputs except OSC0 | 0 | — | 0.8 | V |
| Low Level Input Voltage (2) | V _{IL2} | OSC0 | 0 | — | 0.5 | V |
| Clock Frequency | f _C | — | — | — | 250 | kHz |
| OSC Frequency | f _{OSC} | R = 4.7kΩ, C=22pF | — | 2 | — | MHz |
| Frame Frequency | F _{FR} | f _{OSC} = 2 MHz | — | 224 | — | Hz |
| Operating Temperature Range | T _{op} | — | -40 | — | 85 | °C |

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Ta = -40 to +85°C, VDD = 8 to 18 V)

| Parameter | Symbol | Condition | Min. | Max. | Unit |
|---------------------------------------|--------------------|---|----------------------|-----------------|------|
| Hight Level Input Voltage (1) *1 | V _{IH1} | — | 3.8 | 5.5 | V |
| Hight Level Input Voltage (2) *9 | V _{IH2} | — | 3.8 | V _{DD} | V |
| Hight Level Input Voltage (3) *2 | V _{IH3} | — | 4.5 | 5.5 | V |
| Low Level Input Voltage (1) *10 | V _{IL1} | — | 0 | 0.8 | V |
| Low Level Input Voltage (2) *2 | V _{IL2} | — | 0 | 0.5 | V |
| Hight Level Input Current (1) *3 | I _{IH1} | V _{IH1} = 5.0 V | -5 | 5 | μA |
| Hight Level Input Current (2) *4 | I _{IH2} | V _{IH2} = 5.0 V | -80 | 80 | μA |
| Hight Level Input Current (3) *5 | I _{IH3} | V _{IH3} = 5.0 V | -60 | 60 | μA |
| Low Level Input Current (1) *3 | I _{IL1} | V _{IL1} = 0.0 V | -5 | 5 | μA |
| Low Level Input Current (2) *4 | I _{IL2} | V _{IL2} = 0.0 V | -0.6 | -0.1 | mA |
| Low Level Input Current (3) *5 | I _{IL3} | V _{IL3} = 0.0 V | -320 | -30 | μA |
| High Level Output Voltage (1) *6 | V _{OH1} | V _{DD} = 9.5 V I _{OH1} = -6 mA | V _{DD} -0.8 | — | V |
| High Level Output Voltage (2) *7 | V _{OH2} | V _{DD} = 9.5 V I _{OH2} = -30 mA | V _{DD} -0.8 | — | V |
| High Level Output Voltage (3) *8 | V _{OH3-1} | V _{DD} = 9.5 V I _{OH3-1} = -200 μA | 4 | 6 | V |
| | V _{OH3-2} | V _{DD} = 9.5 V Output Open | 4.5 | 6 | V |
| Low Level Output Voltage (1) *6 *7 | V _{OL1-1} | V _{DD} = 9.5 V I _{OL1-1} = 500 μA | — | 2 | V |
| | V _{OL1-2} | V _{DD} = 9.5 V I _{OL1-2} = 200 μA | — | 1 | V |
| | V _{OL1-3} | V _{DD} = 9.5 V I _{OL1-3} = 2 μA | — | 0.3 | V |
| Low Level Output Voltage (2) *8 | V _{OL2} | V _{DD} = 9.5 V I _{OL2} = 200 μA | — | 0.8 | V |
| Power Supply Current | I _{DD} | f _{osc} = 2 MHz, No load | — | 20 | mA |

- Notes: *1 Applicable to all input pins (except VK, OSC0 pin)
 *2 Applicable to OSC0 pin
 *3 Applicable to CLOCK, DATA, CS, VK, and PWMIN pin
 *4 Applicable to $\overline{\text{TEST1}}$
 *5 Applicable to $\overline{\text{INH}}$ pin
 *6 Applicable to pins SEG1 to SEG30
 *7 Applicable to GRID1 and GRID2
 *8 Applicable to DATA OUT pin
 *9 Applicable to VK pin
 *10 Applicable to all input pins (except OSC0 pin)

AC Characteristics

(Ta = -40 to +85°C, VDD = 8 to 18 V)

| Parameter | Symbol | Condition | Min. | Max. | Unit |
|--|-------------------|---|------|------|------|
| Oscillation Frequency | f _{OSC} | R = 4.7kΩ, C = 22pF | 1.2 | 2.8 | MHz |
| OSCO Input Frequency | f _{OSCI} | External input only | 1.5 | 2.5 | MHz |
| Clock Frequency | f _C | — | — | 250 | kHz |
| Clock Pulse Width | t _{CW} | — | 1.3 | — | μs |
| Data Set-up Time | t _{DS} | — | 1 | — | μs |
| Data Hold Time | t _{DH} | — | 200 | — | ns |
| CS Pulse Width | t _{CSW} | — | 68 | — | μs |
| CS Off Time | t _{CSL} | — | 30 | — | μs |
| CS Set-up Time CS-Clock Time | t _{CSS} | — | 2 | — | μs |
| CS Hold Time Clock-CS Time | t _{CSH} | — | 2 | — | μs |
| Data Output Delay Clock-Data out Time | t _{PD} | — | — | 1 | μs |
| SEG & GRID Output Delay from CS | t _{ODS} | C _L = 100pF | — | 8 | μs |
| Slew Rate (All Drivers) | t _R | C _L = 100pF, t = 20% to 80% or 80% to 20% | — | 5 | μs |
| Power-on CS Time | t _{PCS} | — | 300 | — | μs |
| Power-off Hold Time | t _{POF} | When the Unit mounted V _{DD} = 0 V | 5 | — | ms |
| Power-on Rise Time | t _{PRZ} | When the Unit mounted | — | 100 | μs |
| Frame Frequency | F _{FR} | — | 146 | 342 | Hz |

PWM Conversion Characteristics

(Ta = -40 to +85°C, VDD = 8 to 18 V)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|-------------------------|------------------|-----------|------|------|------|------|
| PWM Input Frequency | f _{PWM} | — | 176 | 256 | 336 | Hz |
| Input Threshold Voltage | V _R | — | 0.8 | 2.5 | 3.8 | V |
| PWM Input Duty Cycle | d _U | — | 20 | — | 100 | % |

TIMING DIAGRAM

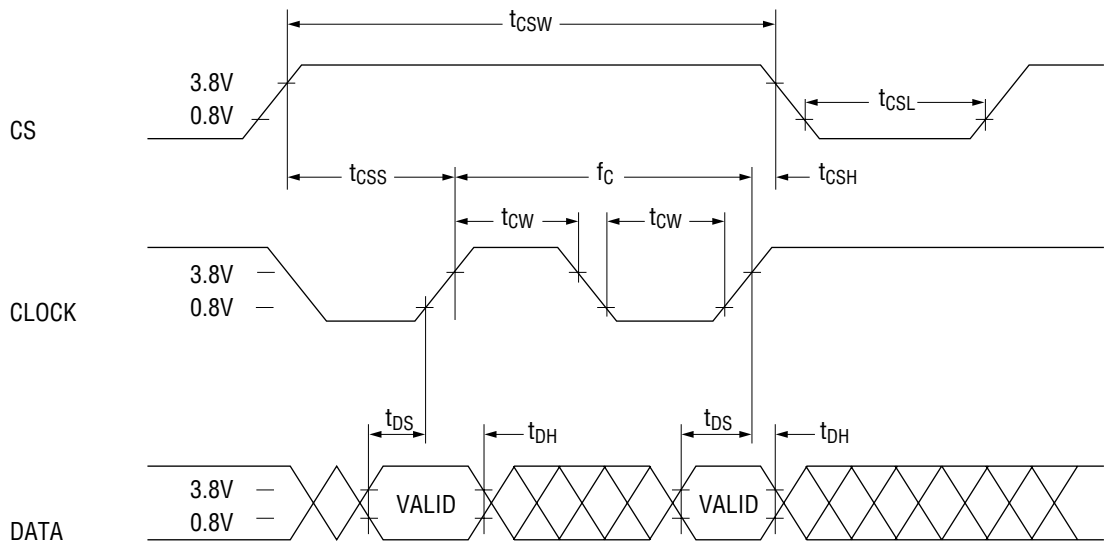


Fig. 1 Data Input Timing

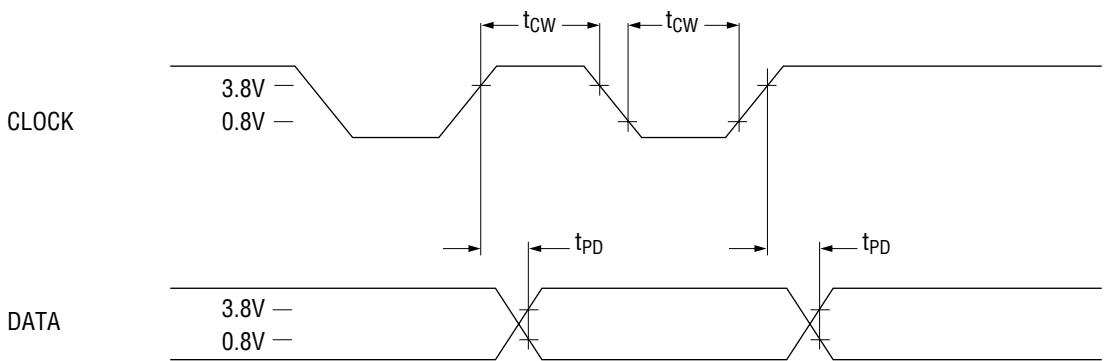


Fig. 2 Data Output Timing

TIMING DIAGRAM (Continued)

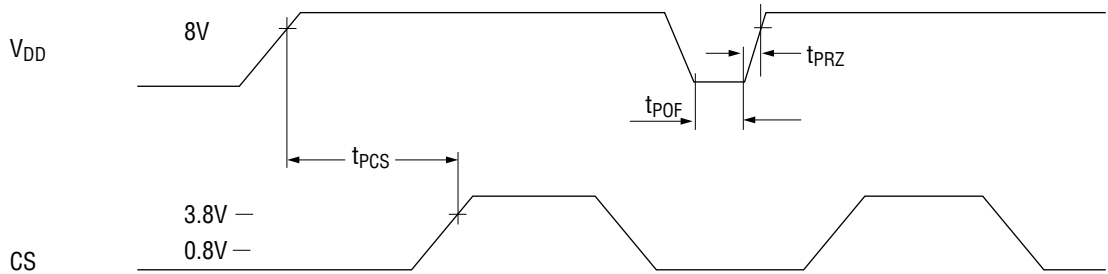


Fig. 3 Power-On Timing

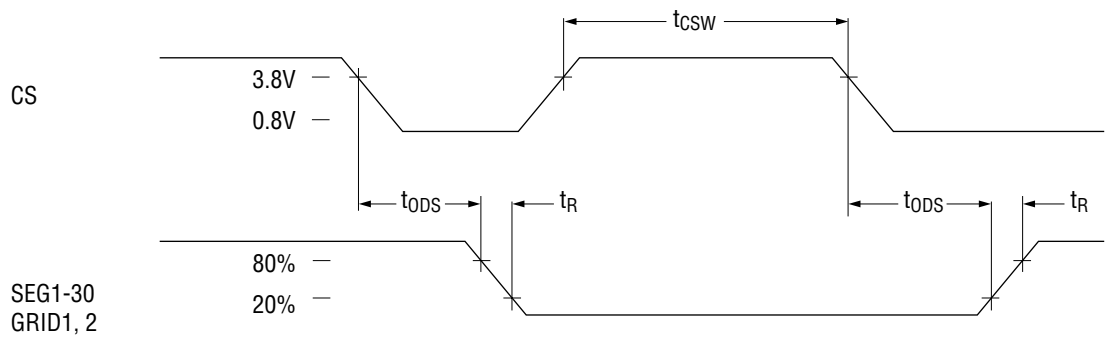


Fig. 4 SEG & GRID Driver Output Timing

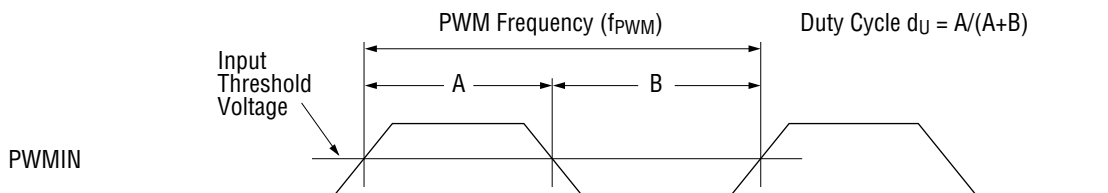


Fig. 5 PWM Input Waveform

FUNCTIONAL DESCRIPTION

Power-On-Reset

The status of the internal circuit after power-on reset is as follows;

- 1) Shift registers and latches are reset.
- 2) PWM conversion mode is selected.

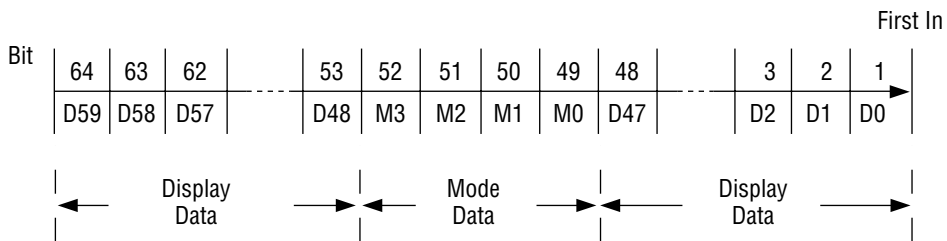
DATA Input

Data input is available only when the high level is applied to the "CS" pin. Input data is shifted into shift registers through "Data" pin at the rising edge of the shift clock. The data is automatically loaded to latches at the falling edge of "CS" signal. When M0 = "0", input data should include display data (total of 64 bits data should be input.) and when M0 = "1", input data should exclude display data (Total of 16-bit data should be input.)

[Data Format]

1) Display Data Input Mode

- Input Data : 64 bits
- VF Display Data : 60 bits
- Mode Select Data : 4 bits



2) Segment outputs/Shift Registers Bit Correspondence Table

The content of the table depends on a PLA code.

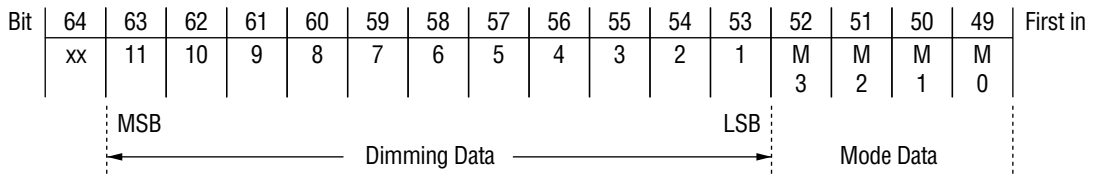
This table is modeled on the general purpose code of -01.

Segment output positions can be changed dependent on the PLA code, but the segment-bit correspondence cannot be changed.

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|
| | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | SEGn |
| Bit | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | GRID1 |
| | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 | 31 | GRID2 |

3) Digital Dimming Data Input Mode

Input Data : 16 bits
 Digital Dimming Data : 11 bits
 Mode Select Data : 4 bits



| (MSB) | INPUT DATA | | | | | | | | | | | (LSB) | DUTY CYCLE | |
|-------|------------|---|---|---|---|---|---|---|---|---|---|-------|------------|--------|
| X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0/2048 |
| X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1/2048 |
| | | | | | | | | | | | | | | |
| X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 2032/2048 | |
| | | | | | | | | | | | | | | |
| X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 2032/2048 | |

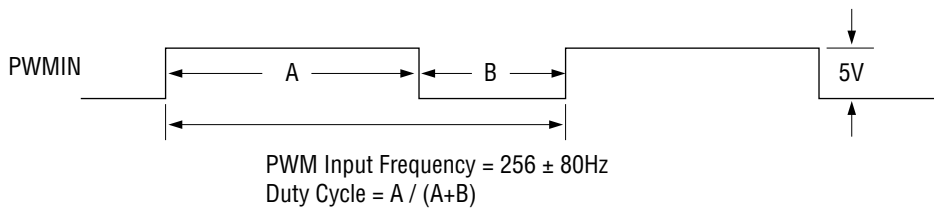
4) Function Mode

| Mode | M3 | M2 | M1 | M0 | Function |
|------|----|----|----|----|---|
| S1 | 0 | 0 | 0 | 0 | Display Data Input |
| S2 | 0 | 0 | 0 | 1 | Digital Dimming Data Input |
| S3 | 0 | 0 | 1 | 0 | PWM Conversion Select & Display Data Input |
| S4 | 0 | 0 | 1 | 1 | PWM Conversion Select |
| S5 | 0 | 1 | 0 | 0 | Digital Dimming Select & Display Data Input |
| S6 | 0 | 1 | 0 | 1 | Digital Dimming Select |

PWM Conversion

In the PWM conversion mode, "lamp PWM", which is used for dimming control of back-light for instrument clusters or other displays, is used to generate the PWM signal for VFD tube dimming control. The lamp PWM input to "PWM IN" pin is converted to PWM signal for VFD tube with a built-in PWM conversion look-up table (User-Programmable Mask ROM).

The duty cycle of the lamp PWM is defined as follows:



Note: The duty cycle of the lamp PWM signal is measured with a reference point of 2.5 V typ. As the reference point of 2.5 V is the threshold voltage of "PWM IN" pin, it deviates to some value between 0.8 V and 3.8 V due to process parameter deviation. Therefore, the PWM conversion error increases as the rise/fall time of the lamp PWM increases.

GRID/SEG Driver Operation and Digital/Analog Dimming Operation

Figure 6 shows an output timing of the GRID and SEG Driver when the VK is "H" level. Output timings of the GRID and SEG drivers are shown in figure 7 for the digital dimming mode operation in figure 8 for the PWM conversion mode operation.

(1) GRID and SEG drivers output timings when VK = "H"

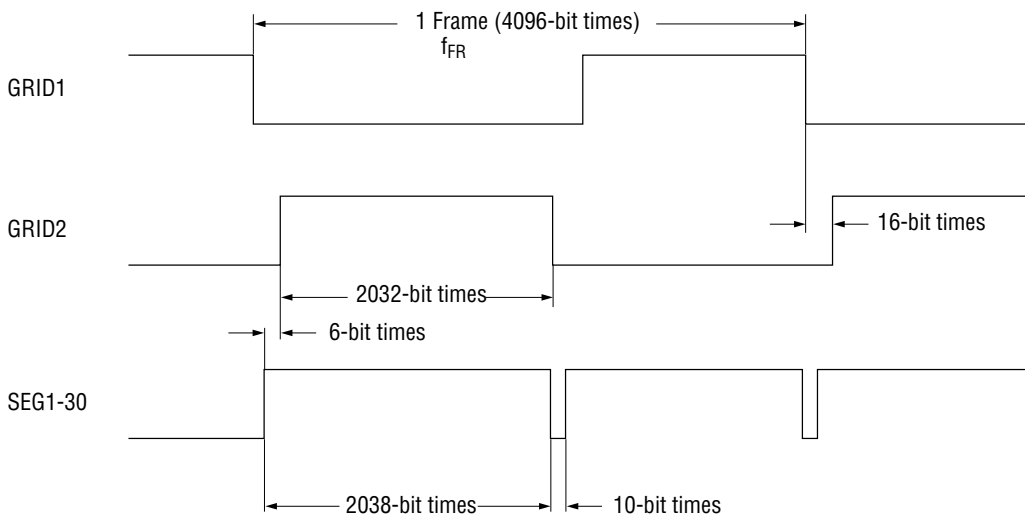


Fig. 6 GRID and SEG Output Timing (VK = "H")

Note: One bit time = $2/f_{OSC} = 1 \mu s$ typ.

(2) GRID and SEG driver output timing when VK = "L" and in Digital Dimming Mode.

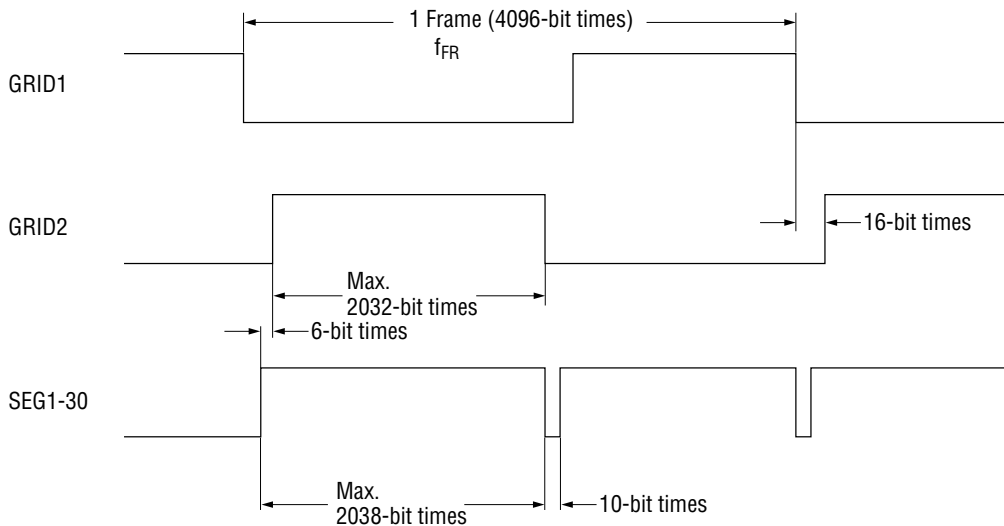


Fig. 7 GRID and SEG Output Timing (digital dimming mode)

- Notes:
- The above indicates the timing for the digital dimming mode with the duty cycle of 2032/2048 at $V_{PARK} = "L"$ level.
 - The On-times for GRID and SEG are specified with the 11 bits of the digital dimming data.
 - One bit time = $2/f_{OSC} = 1 \mu s$ typ.

(3) GRID and SEG driver output timings when VK = "L" and in PWM Conversion Mode

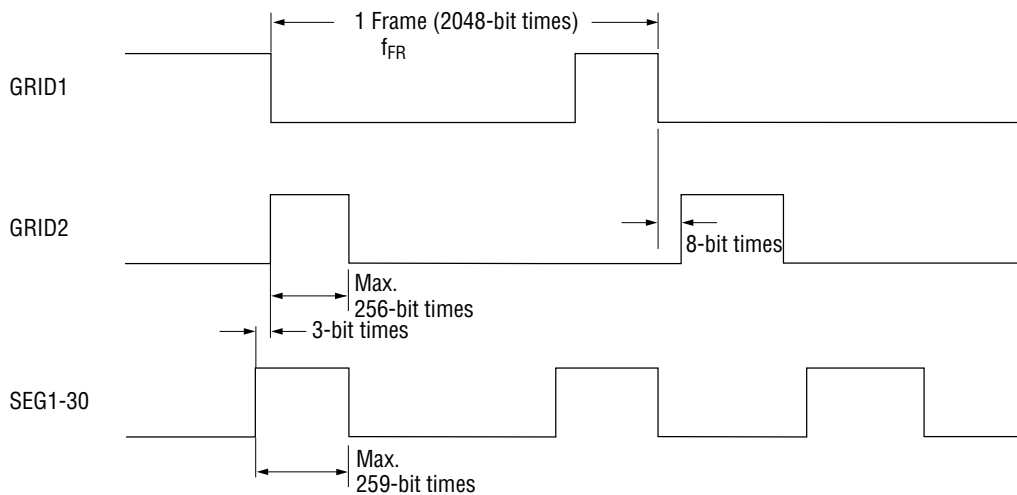


Fig. 8 GRID and SEG Driver Output Timing (PWM conversion mode)

- Notes:
- The above indicates the GRID and SEG Drivers Timing when the PWM conversion mode at VK = "L" level is selected.
 - One bit time = $4/f_{OSC} = 2 \mu s$ typ.

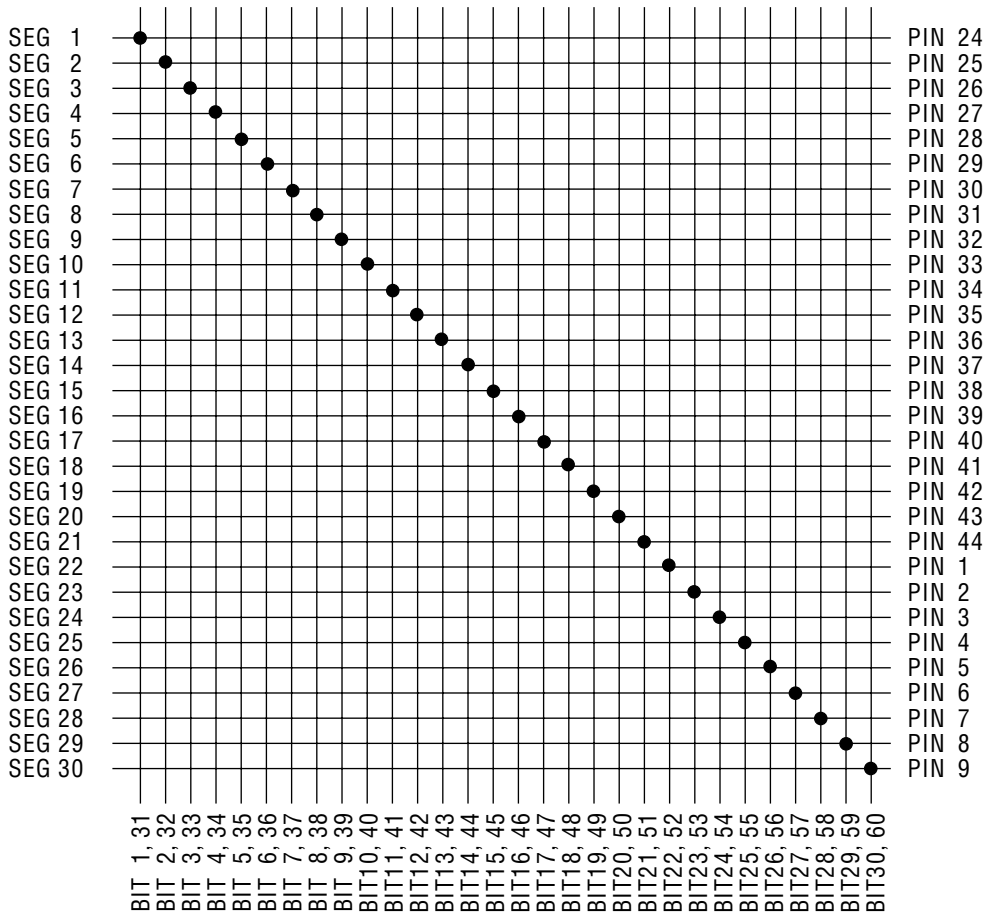
PWM Conversion Table

MSC1201-01

| STEP No. | LAMP PWM DUTY CYCLE | VF PWM DUTY CYCLE | STEP No. | LAMP PWM DUTY CYCLE | VF PWM DUTY CYCLE |
|----------|---------------------|-------------------|----------|---------------------|-------------------|
| 0 | 100.00% | 12.50% | 33 | 58.75% | 6.05% |
| 1 | 98.75% | 12.30% | 34 | 57.50% | 5.86% |
| 2 | 97.50% | 12.11% | 35 | 56.25% | 5.66% |
| 3 | 96.25% | 11.91% | 36 | 55.00% | 5.47% |
| 4 | 95.00% | 11.72% | 37 | 53.75% | 5.27% |
| 5 | 93.75% | 11.52% | 38 | 52.50% | 5.08% |
| 6 | 92.50% | 11.33% | 39 | 51.25% | 4.88% |
| 7 | 91.25% | 11.13% | 40 | 50.00% | 4.69% |
| 8 | 90.00% | 10.94% | 41 | 48.75% | 4.49% |
| 9 | 88.75% | 10.74% | 42 | 47.50% | 4.30% |
| 10 | 87.50% | 10.55% | 43 | 46.25% | 4.10% |
| 11 | 86.25% | 10.35% | 44 | 45.00% | 3.91% |
| 12 | 85.00% | 10.16% | 45 | 43.75% | 3.71% |
| 13 | 83.75% | 9.96% | 46 | 42.50% | 3.52% |
| 14 | 82.50% | 9.77% | 47 | 41.25% | 3.32% |
| 15 | 81.25% | 9.57% | 48 | 40.00% | 3.13% |
| 16 | 80.00% | 9.38% | 49 | 38.75% | 2.93% |
| 17 | 78.75% | 9.18% | 50 | 37.50% | 2.73% |
| 18 | 77.50% | 8.98% | 51 | 36.25% | 2.54% |
| 19 | 76.25% | 8.79% | 52 | 35.00% | 2.34% |
| 20 | 75.00% | 8.59% | 53 | 33.75% | 2.15% |
| 21 | 73.75% | 8.40% | 54 | 32.50% | 1.95% |
| 22 | 72.50% | 8.20% | 55 | 31.25% | 1.76% |
| 23 | 71.25% | 8.01% | 56 | 30.00% | 1.56% |
| 24 | 70.00% | 7.81% | 57 | 28.75% | 1.37% |
| 25 | 68.75% | 7.62% | 58 | 27.50% | 1.17% |
| 26 | 67.50% | 7.42% | 59 | 26.25% | 0.98% |
| 27 | 66.25% | 7.23% | 60 | 25.00% | 0.78% |
| 28 | 65.00% | 7.03% | 61 | 23.75% | 0.59% |
| 29 | 63.75% | 6.84% | 62 | 22.50% | 0.39% |
| 30 | 62.50% | 6.64% | 63 | 21.25% | 0.20% |
| 31 | 61.25% | 6.45% | 64 | 20.00% | 0.10% |
| 32 | 60.00% | 6.25% | | | |

PLA Code Table

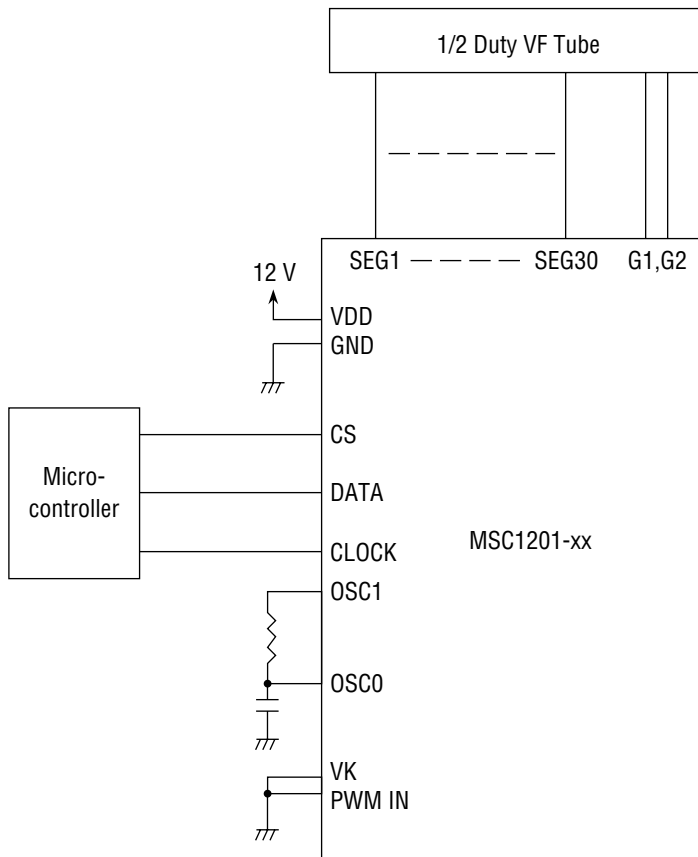
MSC1201-01



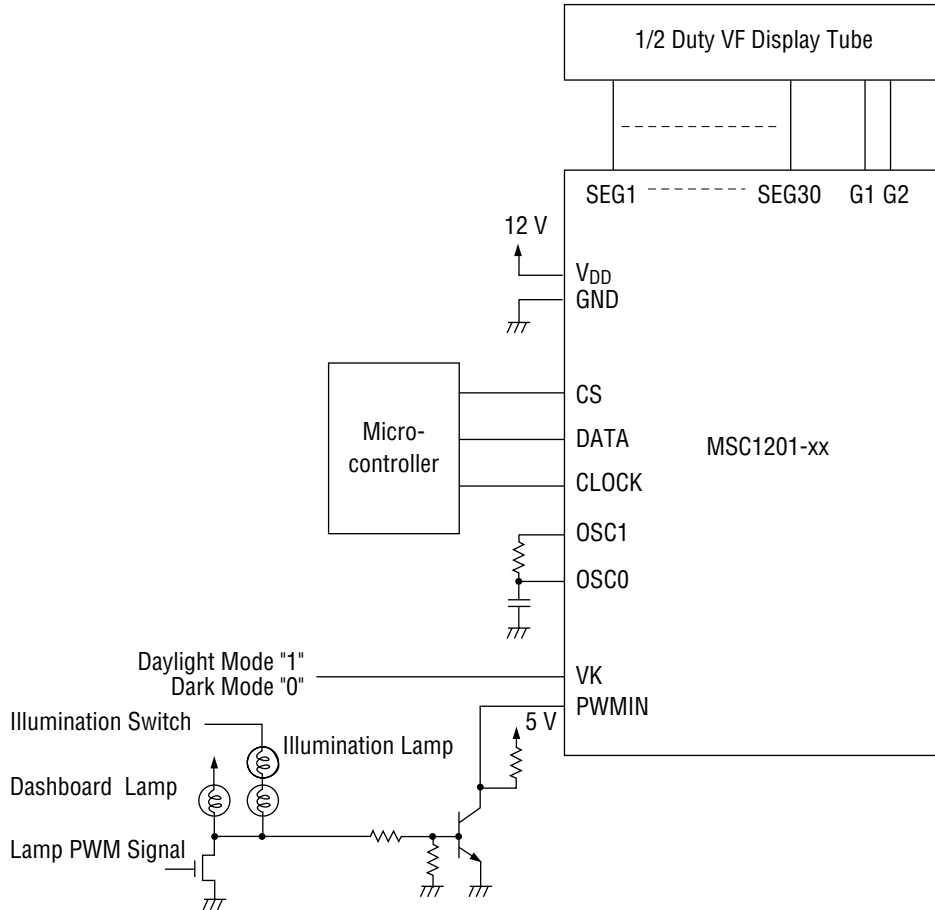
| Pin Name | Output | Pin Name | Output |
|-----------------|---------------|-----------------|---------------|
| SEG1 | BIT 1,31 | SEG16 | BIT 16,46 |
| SEG2 | BIT 2,32 | SEG17 | BIT 17,47 |
| SEG3 | BIT 3,33 | SEG18 | BIT 18,48 |
| SEG4 | BIT 4,34 | SEG19 | BIT 19,49 |
| SEG5 | BIT 5,35 | SEG20 | BIT 20,50 |
| SEG6 | BIT 6,36 | SEG21 | BIT 21,51 |
| SEG7 | BIT 7,37 | SEG22 | BIT 22,52 |
| SEG8 | BIT 8,38 | SEG23 | BIT 23,53 |
| SEG9 | BIT 9,39 | SEG24 | BIT 24,54 |
| SEG10 | BIT 10,40 | SEG25 | BIT 25,55 |
| SEG11 | BIT 11,41 | SEG26 | BIT 26,56 |
| SEG12 | BIT 12,42 | SEG27 | BIT 27,57 |
| SEG13 | BIT 13,43 | SEG28 | BIT 28,58 |
| SEG14 | BIT 14,44 | SEG29 | BIT 29,59 |
| SEG15 | BIT 15,45 | SEG30 | BIT 30,60 |

APPLICATION CIRCUITS

(1) Digital Dimming Mode

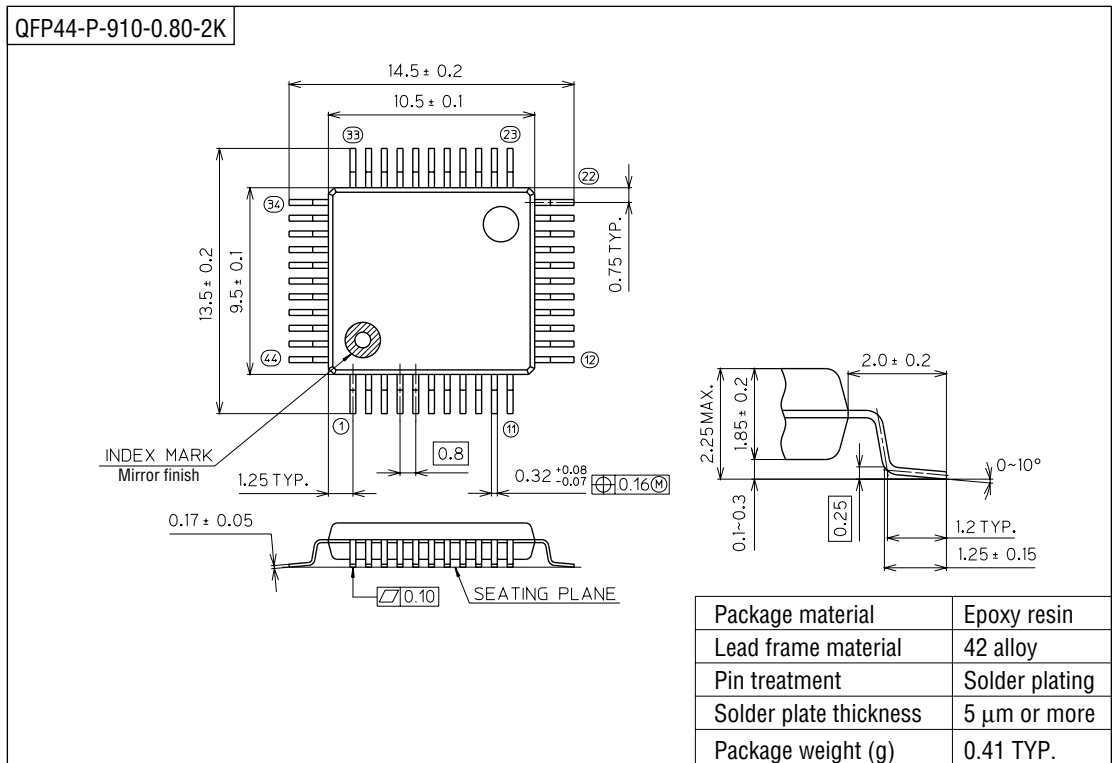


(2) PWM Conversion Mode



PACKAGE DIMENSIONS

(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).