

MSC2313258A-xxBS2/DS2

1,048,576-Word × 32-Bit DRAM MODULE : FAST PAGE MODE TYPE WITH EDO

DESCRIPTION

The Oki MSC2313258A-xxBS2/DS2 is a fully decoded 1,048,576-word × 32-bit CMOS dynamic random access memory composed of two 16-Mb (1M × 16) DRAMs in SOJ. The mounting of two DRAMs together with decoupling capacitors on a 72-pin glass epoxy SIMM Package supports any application where high density and large capacity of storage memory are required.

FEATURES

- 1,048,576-word × 32-bit organization
- 72-pin SIMM
 - MSC2313258A-xxBS2 : Gold tab
 - MSC2313258A-xxDS2 : Solder tab
- Single 5 V supply ±10% tolerance
- Input : TTL compatible
- Output : TTL compatible, 3-state, nonlatch
- Refresh : 1024 cycles/16 ms
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ hidden refresh, $\overline{\text{RAS}}$ -only refresh capability
- Fast Page Mode with EDO capability

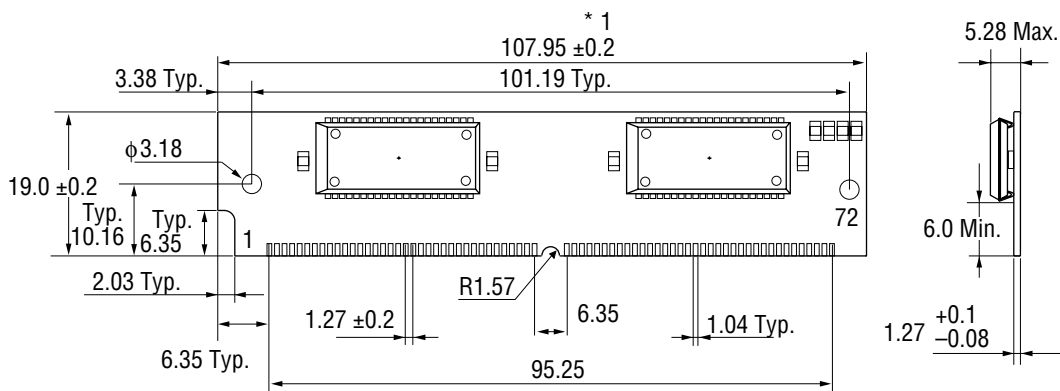
PRODUCT FAMILY

Family	Access Time (Max.)			Cycle Time (Min.)	Power Dissipation	
	t _{RAC}	t _{AA}	t _{CAC}		Operating (Max.)	Standby (Max.)
MSC2313258A-60BS2/DS2	60 ns	30 ns	15 ns	110 ns	2420 mW	11 mW
MSC2313258A-70BS2/DS2	70 ns	35 ns	20 ns	130 ns	2200 mW	

PIN CONFIGURATION

MSC2313258A-xxBS2/DS2

(Unit : mm)



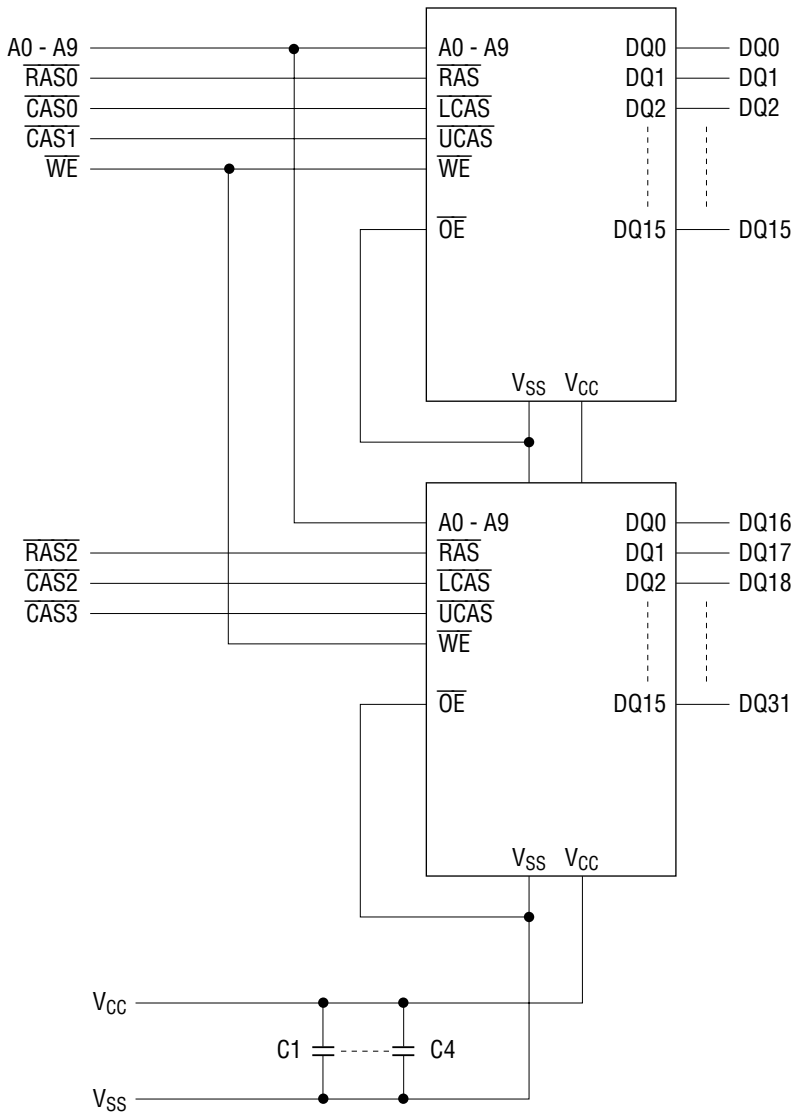
*1 The common size difference of the board width 12.5 mm of its height is specified as ± 0.2 . The value above 12.5 mm is specified as ± 0.5 .

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V _{SS}	16	A4	31	A8	46	NC	61	DQ13
2	DQ0	17	A5	32	A9	47	\overline{WE}	62	DQ30
3	DQ16	18	A6	33	NC	48	NC	63	DQ14
4	DQ1	19	NC	34	$\overline{RAS2}$	49	DQ8	64	DQ31
5	DQ17	20	DQ4	35	NC	50	DQ24	65	DQ15
6	DQ2	21	DQ20	36	NC	51	DQ9	66	NC
7	DQ18	22	DQ5	37	NC	52	DQ25	67	PD1
8	DQ3	23	DQ21	38	NC	53	DQ10	68	PD2
9	DQ19	24	DQ6	39	V _{SS}	54	DQ26	69	PD3
10	V _{CC}	25	DQ22	40	$\overline{CAS0}$	55	DQ11	70	PD4
11	NC	26	DQ7	41	$\overline{CAS2}$	56	DQ27	71	NC
12	A0	27	DQ23	42	$\overline{CAS3}$	57	DQ12	72	V _{SS}
13	A1	28	A7	43	$\overline{CAS1}$	58	DQ28		
14	A2	29	NC	44	$\overline{RAS0}$	59	V _{CC}		
15	A3	30	V _{CC}	45	NC	60	DQ29		

Presence Detect Pins

Pin No.	Pin Name	MSC2313258A -60BS2/DS2	MSC2313258A -70BS2/DS2
67	PD1	V _{SS}	V _{SS}
68	PD2	V _{SS}	V _{SS}
69	PD3	NC	V _{SS}
70	PD4	NC	NC

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 to 7.0	V
Voltage V_{CC} Supply Relative to V_{SS}	V_{CC}	-1.0 to 7.0	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D	2.6	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	-40 to 125	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

($T_a = 0^\circ\text{C}$ to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

Capacitance

($T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A9)	C_{IN1}	—	16	pF
Input Capacitance (\overline{WE})	C_{IN2}	—	20	pF
Input Capacitance ($\overline{RAS0}, \overline{RAS2}$)	C_{IN3}	—	13	pF
Input Capacitance ($\overline{CAS0} - \overline{CAS3}$)	C_{IN4}	—	13	pF
I/O Capacitance (DQ0 - DQ31)	C_{DQ}	—	13	pF

Note : Capacitance measured with Boonton Meter.

DC Characteristics

($V_{CC} = 5\text{ V} \pm 10\%$, $T_a = 0^\circ\text{C}$ to 70°C)

Parameter	Symbol	Condition	MSC2313258A -60BS2/DS2		MSC2313258A -70BS2/DS2		Unit	Note
			Min.	Max.	Min.	Max.		
Input Leakage Current	I_{LI}	$0\text{ V} \leq V_I \leq 6.5\text{ V}$; All other pins not under test = 0 V	-20	20	-20	20	μA	
Output Leakage Current	I_{LO}	D_{OUT} disable $0\text{ V} \leq V_O \leq 5.5\text{ V}$	-10	10	-10	10	μA	
Output High Voltage	V_{OH}	$I_{OH} = -5.0\text{ mA}$	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	$I_{OL} = 4.2\text{ mA}$	0	0.4	0	0.4	V	
Average Power Supply Current (Operating)	I_{CC1}	\overline{RAS} , \overline{CAS} cycling, $t_{RC} = \text{Min.}$	—	440	—	400	mA	1, 2
Power Supply Current (Standby)	I_{CC2}	\overline{RAS} , $\overline{CAS} = V_{IH}$	—	4	—	4	mA	1
		\overline{RAS} , \overline{CAS} $\geq V_{CC} - 0.2\text{ V}$	—	2	—	2	mA	1
Average Power Supply Current (RAS-only Refresh)	I_{CC3}	\overline{RAS} cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = \text{Min.}$	—	440	—	400	mA	1, 2
Average Power Supply Current (CAS before RAS Refresh)	I_{CC6}	\overline{RAS} cycling, \overline{CAS} before \overline{RAS} , $t_{RC} = \text{Min.}$	—	440	—	400	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{RAS} = V_{IL}$, \overline{CAS} cycling, $t_{HPC} = \text{Min.}$	—	440	—	400	mA	1, 3

- Notes:
- I_{CC} Max. is specified as I_{CC} for output open condition.
 - Address can be changed once or less while $\overline{RAS} = V_{IL}$.
 - Address can be changed once or less while $\overline{CAS} = V_{IH}$.

AC Characteristics (1/2)

(V_{CC} = 5 V ±10%, T_a = 0°C to 70°C) Note 1,2,3

Parameter	Symbol	MSC2313258A -60BS2/DS2		MSC2313258A -70BS2/DS2		Unit	Note
		Min.	Max.	Min.	Max.		
		Random Read or Write Cycle Time	t _{RC}	110	—		
Fast Page Mode Cycle Time	t _{HPC}	25	—	30	—	ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}	—	60	—	70	ns	4, 5, 6
Access Time from $\overline{\text{CAS}}$	t _{CAC}	—	15	—	20	ns	4, 5
Access Time from Column Address	t _{AA}	—	30	—	35	ns	4, 6
Access Time from $\overline{\text{CAS}}$ Precharge	t _{CPA}	—	35	—	40	ns	4
Output Low Impedance Time from $\overline{\text{CAS}}$	t _{CLZ}	0	—	0	—	ns	4
Output Hold Time from $\overline{\text{CAS}}$ Low	t _{DOH}	5	—	5	—	ns	
$\overline{\text{CAS}}$ to Data Output Buffer Turn-off Delay Time	t _{CEZ}	0	15	0	15	ns	7, 8
$\overline{\text{RAS}}$ to Data Output Buffer Turn-off Delay Time	t _{REZ}	0	15	0	15	ns	7, 8
$\overline{\text{WE}}$ to Data Output Buffer Turn-off Delay Time	t _{WEZ}	0	15	0	15	ns	7
Transition Time	t _T	3	50	3	50	ns	3
Refresh Period	t _{REF}	—	16	—	16	ms	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	40	—	50	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	60	10k	70	10k	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RASP}	60	100k	70	100k	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	15	—	20	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t _{CP}	10	—	10	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	10	10k	10	10k	ns	
$\overline{\text{RAS}}$ Low to $\overline{\text{CAS}}$ High Delay Time	t _{CSH}	40	—	45	—	ns	
$\overline{\text{CAS}}$ High to $\overline{\text{RAS}}$ Low Delay Time	t _{CRP}	5	—	5	—	ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	35	—	40	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	20	45	20	50	ns	5
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	30	15	35	ns	6
$\overline{\text{RAS}}$ to Second $\overline{\text{CAS}}$ Delay Time	t _{RSCD}	60	—	70	—	ns	
Row Address Set-up Time	t _{ASR}	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	10	—	10	—	ns	
Column Address Set-up Time	t _{ASC}	0	—	0	—	ns	
Column Address Hold Time	t _{CAH}	10	—	15	—	ns	
Column Address Hold Time from $\overline{\text{RAS}}$	t _{AR}	45	—	50	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t _{RAL}	30	—	35	—	ns	

AC Characteristics (2/2)

(V_{CC} = 5 V ±10%, T_a = 0°C to 70°C) Note 1,2,3

Parameter	Symbol	MSC2313258A -60BS2/DS2		MSC2313258A -70BS2/DS2		Unit	Note
		Min.	Max.	Min.	Max.		
Read Command Set-up Time	t _{RCS}	0	—	0	—	ns	
Read Command Hold Time	t _{RCH}	0	—	0	—	ns	9
Read Command Hold Time referenced to $\overline{\text{RAS}}$	t _{RRH}	0	—	0	—	ns	9
Write Command Set-up Time	t _{WCS}	0	—	0	—	ns	
Write Command Hold Time	t _{WCH}	10	—	15	—	ns	
Write Command Hold Time from $\overline{\text{RAS}}$	t _{WCR}	45	—	50	—	ns	
Write Command Pulse Width	t _{WP}	10	—	15	—	ns	
Write Command Pulse Width (Output Disable)	t _{WPE}	5	—	10	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t _{RWL}	15	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t _{CWL}	15	—	20	—	ns	
Data-in Set-up Time	t _{DS}	0	—	0	—	ns	
Data-in Hold Time	t _{DH}	15	—	15	—	ns	
Data-in Hold Time from $\overline{\text{RAS}}$	t _{DHR}	45	—	50	—	ns	
$\overline{\text{CAS}}$ Active Delay Time from $\overline{\text{RAS}}$ Precharge	t _{RPC}	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{CSR}	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{CHR}	10	—	15	—	ns	

- Notes:
1. A start-up delay of 200 μ s is required after power-up, followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh) before proper device operation is achieved.
 2. The AC characteristics assume $t_T = 5$ ns.
 3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL} .
 4. This parameter is measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, access time is controlled by t_{CAC} .
 6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, access time is controlled by t_{AA} .
 7. t_{CEZ} (Max.), t_{REZ} (Max.) and t_{WEZ} (Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
 8. t_{CEZ} and t_{REZ} must be satisfied for open circuit condition.
 9. t_{RCH} or t_{RRH} must be satisfied for a read cycle.

See ADDENDUM H for AC Timing Waveforms