OKI Semiconductor

MSC23136C/CL-xxBS10/DS10

1,048,576-Word × 36-Bit DRAM MODULE : FAST PAGE MODE TYPE

DESCRIPTION

The OKI MSC23136C/CL-xxBS10/DS10 is a fully decoded 1,048,576-word × 36-bit CMOS Dynamic Random Access Memory Module composed of eight 4-Mb DRAMs (1M × 4) in SOJ packages and two 2-Mb DRAMs (1M × 2) in SOJ packages mounted with ten decoupling capacitors on a 72-pin glass epoxy single-inline package. This module is generally used for memory expansion in parity applications such as workstations. The low-power version (CL) offers reduced power consumption for mobile computing applications like laptops and palmtops.

FEATURES

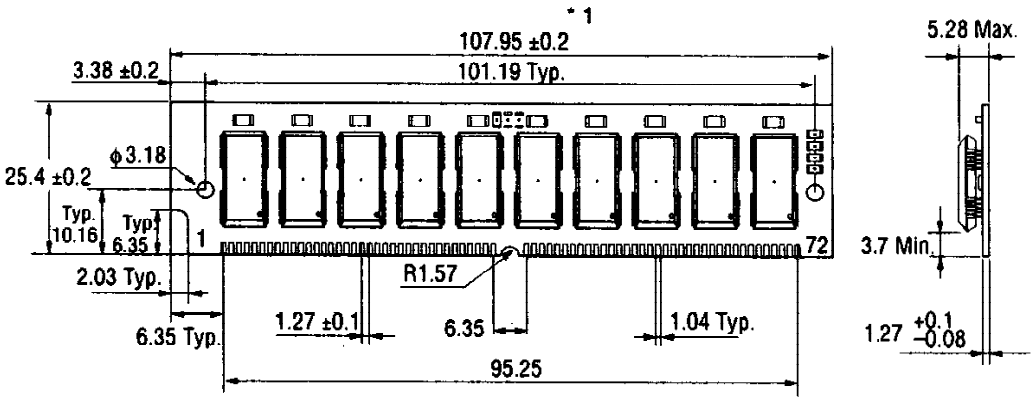
- 1-Meg × 36-bit organization
- 72-Pin Socket Insertable Module
  MSC23136C/CL-xxBS10 : Gold tab
  MSC23136C/CL-xxDS10: Solder tab
- Single 5 V supply ±10% tolerance
- Access times : 60, 70, 80 ns
- Input : TTL compatible
- Output : TTL compatible, 3-state
- Refresh : 1024 cycles/16 ms (128 ms : L-version)
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{CAS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$-only refresh capability
- Multi-bit test mode capability
- Fast Page Mode capability

PRODUCT FAMILY

Family	Access Time (Max.)			Cycle Time (Min.)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}		Operating (Max.)	Standby (Max.)
MSC23136C/CL-60BS10/DS10	60 ns	30 ns	15 ns	110 ns	5280 mW	55 mW/ 9.9 mW (L-version)
MSC23136C/CL-70BS10/DS10	70 ns	35 ns	20 ns	130 ns	4730 mW	
MSC23136C/CL-80BS10/DS10	80 ns	40 ns	20 ns	150 ns	4180 mW	

PIN CONFIGURATION

MSC23136C/CL-xxBS10/DS10



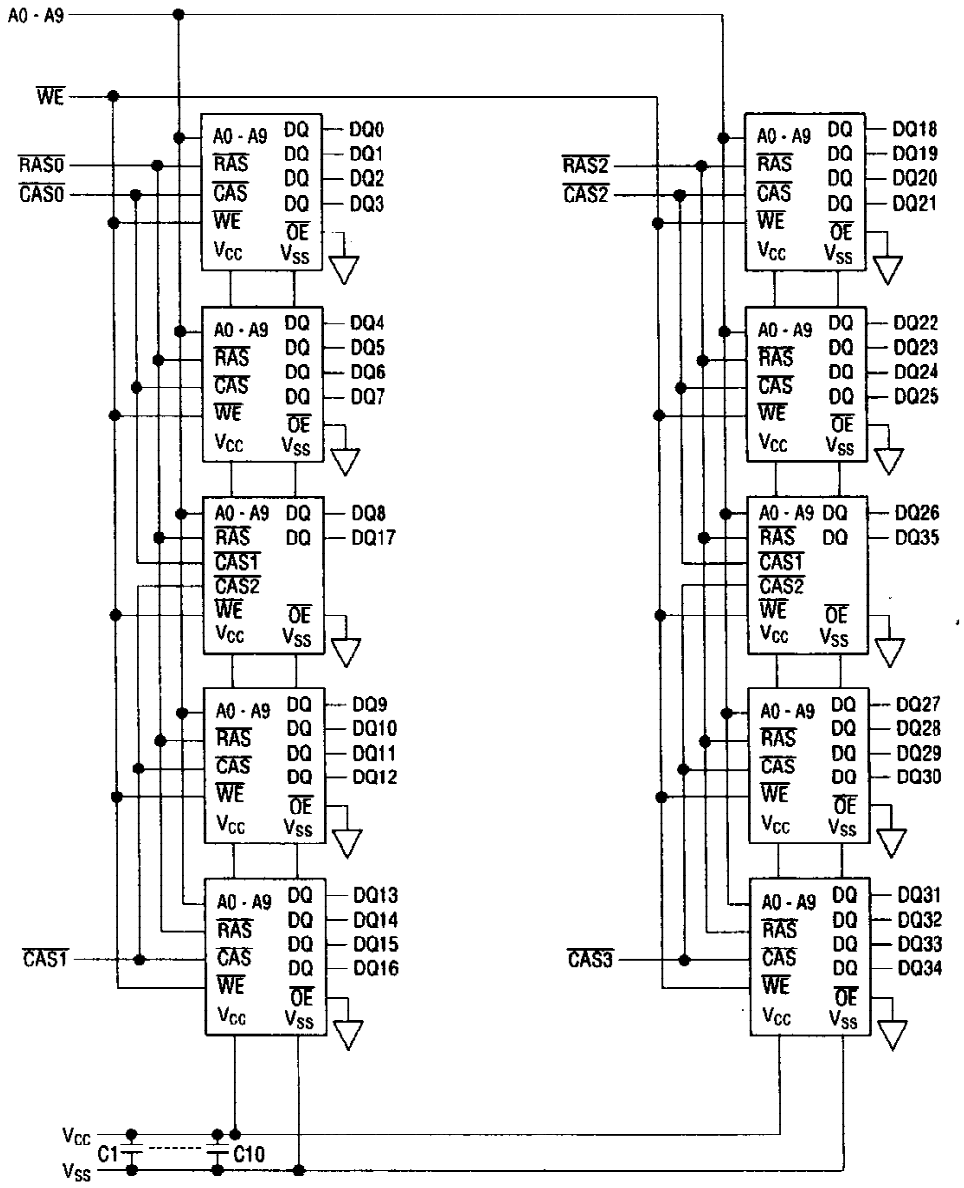
*1 The common size difference of the board width 12.5 mm of its height is specified as ±0.2. The value above 12.5 mm is specified as ±0.5.

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	16	A4	31	A8	46	NC	61	DQ14
2	DQ0	17	A5	32	A9	47	$\overline{WE}$	62	DQ33
3	DQ18	18	A6	33	NC	48	NC	63	DQ15
4	DQ1	19	NC	34	$\overline{RAS2}$	49	DQ9	64	DQ34
5	DQ19	20	DQ4	35	DQ26	50	DQ27	65	DQ16
6	DQ2	21	DQ22	36	DQ8	51	DQ10	66	NC
7	DQ20	22	DQ5	37	DQ17	52	DQ28	67	PD1
8	DQ3	23	DQ23	38	DQ35	53	DQ11	68	PD2
9	DQ21	24	DQ6	39	V_{SS}	54	DQ29	69	PD3
10	V_{CC}	25	DQ24	40	$\overline{CAS0}$	55	DQ12	70	PD4
11	NC	26	DQ7	41	$\overline{CAS2}$	56	DQ30	71	NC
12	A0	27	DQ25	42	$\overline{CAS3}$	57	DQ13	72	V_{SS}
13	A1	28	A7	43	$\overline{CAS1}$	58	DQ31		
14	A2	29	NC	44	$\overline{RAS0}$	59	V_{CC}		
15	A3	30	V_{CC}	45	NC	60	DQ32		

Presence Detect Pins

Pin No.	Pin Name	MSC23136C/CL -60BS10/DS10	MSC23136C/CL -70BS10/DS10	MSC23136C/CL -80BS10/DS10
67	PD1	V_{SS}	V_{SS}	V_{SS}
68	PD2	V_{SS}	V_{SS}	V_{SS}
69	PD3	NC	V_{SS}	NC
70	PD4	NC	NC	V_{SS}

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1.0 to 7.0	V
Voltage V_{CC} Supply Relative to V_{SS}	V_{CC}	−1.0 to 7.0	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D	10	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	−40 to 125	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

(Ta = 0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

CapacitanceCapacitance

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A9)	C_{IN1}	—	70	pF
Input Capacitance ($\overline{WE}$)	C_{IN2}	—	80	pF
Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{IN3}	—	43	pF
Input Capacitance ($\overline{CAS0}$ - $\overline{CAS3}$)	C_{IN4}	—	24	pF
I/O Capacitance (DQ0 - DQ35)	C_{DQ}	—	13	pF

Note : Capacitance measured with Boonton Meter.

DC Characteristics

(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C)

Parameter	Symbol	Condition	MSC23136C/CL -60BS10/DS10		MSC23136C/CL -70BS10/DS10		MSC23136C/CL -80BS10/DS10		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Input Leakage Current	I_{LI}	0 V ≤ V_I ≤ 6.5 V; All other pins not under test = 0 V	−100	100	−100	100	−100	100	µA	
Output Leakage Current	I_{LO}	D_{OUT} disable 0 V ≤ V_O ≤ 5.5 V	−10	10	−10	10	−10	10	µA	
Output High Voltage	V_{OH}	I_{OH} = −5.0 mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL} = 4.2 mA	0	0.4	0	0.4	0	0.4	V	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = Min.	—	960	—	860	—	760	mA	1, 2
Power Supply Current (Standby)	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	—	20	—	20	—	20	mA	1
		$\overline{RAS}$, $\overline{CAS}$	—	10	—	10	—	10	mA	1
		≥ V_{CC} −0.2 V	—	1.8	—	1.8	—	1.8	mA	1, 5
Average Power Supply Current ($\overline{RAS}$-only Refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = Min.	—	960	—	860	—	760	mA	1, 2
Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$, t_{RC} = Min.	—	960	—	860	—	760	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = Min.	—	760	—	670	—	580	mA	1, 3
Average Power Supply Current (Battery Backup)	I_{CC10}	t_{RC} = 125 µs, $\overline{CAS}$ before $\overline{RAS}$ cycling	—	3	—	3	—	3	mA	1, 2 4, 5

Notes: 1. Specified values are obtained with the output open.
2. Address can be changed once or less while $\overline{RAS}$=V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$=V_{IH}.
4. V_{CC} - 0.2 V ≤ V_{IH} ≤ 6.5 V, -1.0 V ≤ V_{IL} ≤ 0.2 V.
5. L-version.

AC Characteristics (1/2)

(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C) Note 1,2,3,9,10

Parameter	Symbol	MSC23136C/CL -60BS10/DS10		MSC23136C/CL -70BS10/DS10		MSC23136C/CL -80BS10/DS10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	110	—	130	—	150	—	ns	
Fast Page Mode Cycle Time	t_{PC}	40	—	45	—	50	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	ns	4, 5, 6
Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	20	—	20	ns	4, 5
Access Time from Column Address	t_{AA}	—	30	—	35	—	40	ns	4, 6
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	35	—	40	—	45	ns	4
Output Low Impedance Time from $\overline{CAS}$	t_{CLZ}	0	—	0	—	0	—	ns	4
Output Buffer Turn-off Delay Time	t_{OFF}	0	15	0	20	0	20	ns	7
Transition Time	t_T	3	50	3	50	3	50	ns	3
Refresh Period	t_{REF}	—	16	—	16	—	16	ms	
Refresh Period (L-version)	t_{REF}	—	128	—	128	—	128	ms	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	60	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15	—	20	—	20	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10K	20	10K	20	10K	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	20	60	ns	5
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	15	40	ns	6
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	10	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	15	—	ns	
Column Address Hold Time from $\overline{RAS}$	t_{AR}	50	—	55	—	60	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	ns	

AC Characteristics (2/2)

(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C) Note 1,2,3,9,10

Parameter	Symbol	MSC23136C/CL -60BS10/DS10		MSC23136C/CL -70BS10/DS10		MSC23136C/CL -80BS10/DS10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns	8
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	8
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	
Write Command Hold Time	t_{WCH}	10	—	10	—	10	—	ns	
Write Command Hold Time from $\overline{RAS}$	t_{WCR}	45	—	50	—	60	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	10	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15	—	20	—	20	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15	—	20	—	20	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	
Data-in Hold Time	t_{DH}	15	—	15	—	15	—	ns	
Data-in Hold Time from $\overline{RAS}$	t_{DHR}	50	—	55	—	60	—	ns	
$\overline{CAS}$ Active Delay Time from $\overline{RAS}$ Precharge	t_{RPC}	5	—	5	—	5	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time (Refresh Counter Test)	t_{CPT}	30	—	35	—	40	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{WRP}	10	—	10	—	10	—	ns	
$\overline{WE}$ Hold Time from $\overline{RAS}$ ($\overline{CAS}$ before $\overline{RAS}$)	t_{WRH}	10	—	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Set-up Time (Test Mode)	t_{WTS}	10	—	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Hold Time (Test Mode)	t_{WTH}	10	—	10	—	10	—	ns	

Notes:

1. A start-up delay of 200 μs is required after power-up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh) before proper device operation is achieved.
   When using the internal refresh counter, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ initialization cycles is required.
2. AC mesurement assume t_T = 5 ns.
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, access time is controlled by t_{CAC}.
6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, access time is controlled by t_{AA}.
7. t_{OFF} (Max.) defines the time at which the output achieves an open circuit condition and is not referenced to output voltage levels.
8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. The test mode is initiated by performing a $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. This mode is latched and remains in effect until the exit cycle is generated.
   In a test mode CA0 is not used and each DQ pin now accesses 2 bit locations. In a read cycle, if the 2 data bits are equal, the DQ pin will indicate a high level. If the 2 data bits are not equal, the DQ pin will indicate a low level.
   The test mode is cleared and the memory device returned to its normal operating state by performing a $\overline{RAS}$-only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
10. In a test mode read cycle, the access time parameters are delayed by 5 ns. The test mode parameters are obtained by adding 5 ns to the normal read cycle values.

See ADDENDUM E for AC Timing Waveforms