

MSC2320B-xxYS9/DS9

262,144-Word by 36-Bit DRAM Module: Fast Page Mode

DESCRIPTION

The OKI MSC2320B-xxYS9/DS9 is a fully decoded 262,144-word x 36-bit CMOS Dynamic Random Access Memory Module . It is composed of eight 1-Mb DRAMs in SOJ (MSM514256B) packages, and four 256Kb DRAMs in PLCC (MSM51C256A) packages mounted with twelve 0.2 μ F decoupling capacitors on a 72-pin glass epoxy single-inline package. This module is generally used for memory expansion in parity applications such as workstations.

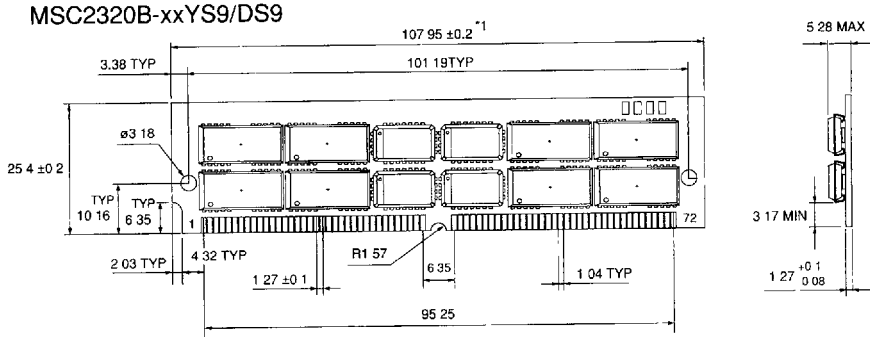
FEATURES

- 256K x 36-bit organization
- 72-pin socket insertable module
 - MSC2320B-xxYS9: Gold tab
 - MSC2320B-xxDS9: Solder tab
- Single +5 V supply $\pm 10\%$ tolerance
- Access times: 70, 80, 100 ns
- Input: TTL compatible
- Output: TTL compatible, three-state
- Refresh: 512 cycles/8 ms
- CAS-before-RAS refresh, CAS-before-RAS hidden refresh, RAS-only refresh capability

Family Organization

Part Number	Access Time (Max)			Cycle Time (Min)	Power Dissipation (Max)	
	t_{RAC}	t_{AA}	t_{CAC}		Operating	Standby
MSC2320B-70YS9/DS9	70 ns	35 ns	20 ns	140 ns	4950 mW	88 mW (MOS level)
MSC2320B-80YS9/DS9	80 ns	40 ns	20 ns	160 ns	4290 mW	
MSC2320B-10YS9/DS9	100 ns	50 ns	25 ns	190 ns	3630 mW	

PIN CONFIGURATION



*1 The common size difference of the board width 12.5 mm of its height is specified as ±0.2. The value above 12.5 mm is specified as ±0.5.

Pin Configuration

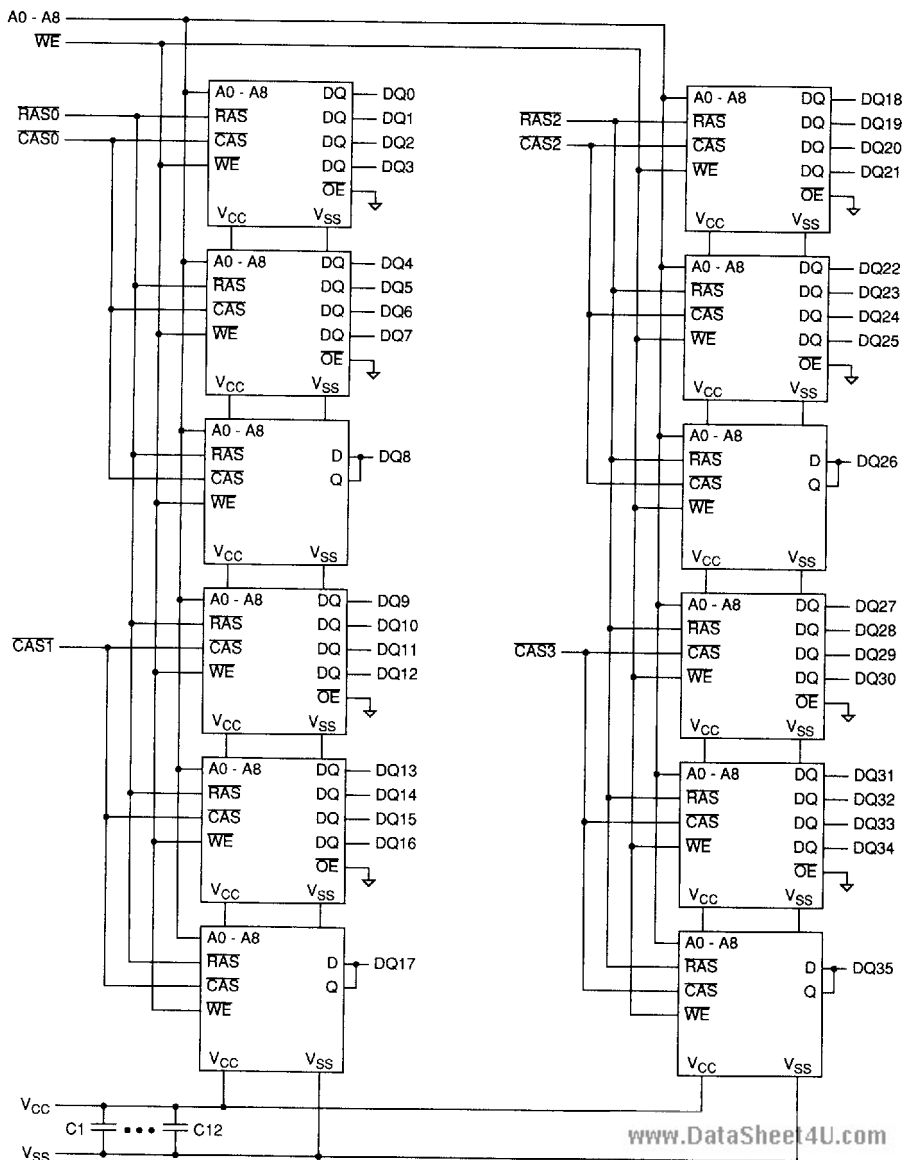
Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
1	V _{SS}	16	A4	31	A8	46	N.C.	61	DQ14
2	DQ0	17	A5	32	N.C.	47	WE	62	DQ33
3	DQ18	18	A6	33	N.C.	48	N.C.	63	DQ15
4	DQ1	19	N.C.	34	RAS2	49	DQ9	64	DQ34
5	DQ19	20	DQ4	35	DQ26	50	DQ27	65	DQ16
6	DQ2	21	DQ22	36	DQ8	51	DQ10	66	N.C.
7	DQ20	22	DQ5	37	DQ17	52	DQ28	67	PD0
8	DQ3	23	DQ23	38	DQ35	53	DQ11	68	PD1
9	DQ21	24	DQ6	39	V _{SS}	54	DQ29	69	PD2
10	V _{CC}	25	DQ24	40	CAS0	55	DQ12	70	PD3
11	N.C.	26	DQ7	41	CAS2	56	DQ30	71	N.C.
12	A0	27	DQ25	42	CAS3	57	DQ13	72	V _{SS}
13	A1	28	A7	43	CAS1	58	DQ31		
14	A2	29	N.C.	44	RAS0	59	V _{CC}		
15	A3	30	V _{CC}	45	N.C.	60	DQ32		

Presence Detect Pins

Pin Number	Pin Name	70 ns	80 ns	100 ns
67	PD0	V _{SS}	V _{SS}	V _{SS}
68	PD1	N.C.	N.C.	N.C.
69	PD2	V _{SS}	N.C.	V _{SS}
70	PD3	N.C.	V _{SS}	V _{SS}

BLOCK DIAGRAM

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ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings ^[1]

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-1 0 ~ +7 0	V
Voltage V _{CC} supply relative to V _{SS}	V _{CC}	-1 0 ~ +7.0	V
Short circuit output current	I _{OS}	50	mA
Power dissipation	P _D	12	W
Operating temperature	T _{OPR}	0 ~ +70	°C
Storage temperature	T _{STG}	-40 ~ +125	°C

- 1 Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions (T_a = 0 ~ +70°C)

Parameter	Symbol	Rated Value			Unit
		Min	Typ	Max	
Power supply voltage	V _{CC}	4.5	5.0	5.5	V
	V _{SS}	0	0	0	V
Input high voltage	V _{IH}	2.4	-	6.5	V
Input low voltage	V _{IL}	-1.0	-	0.8	V

Capacitance (T_a = 25°C, f = 1 MHz) ^[1]

Parameter	Symbol	Typ	Max	Unit
Input capacitance (A0 ~ A8)	C _{IN1}	-	102	pF
Input capacitance (WE)	C _{IN2}	-	104	pF
Input capacitance (RAS0, RAS2)	C _{IN3}	-	62	pF
Input capacitance (CAS0 ~ CAS3)	C _{IN4}	-	41	pF
I/O capacitance (DQ0~DQ7, DQ9~DQ16, DQ18~DQ25, DQ27~DQ34)	C _{DQ1}	-	17	pF
I/O capacitance (DQ8, DQ17, DQ26, DQ35)	C _{DQ2}	-	23	pF

- 1 Capacitance measured with Boonton Meter

DC Characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $T_a = 0^\circ\text{C} \sim +70^\circ\text{C}$)

Parameter	Symbol	Condition	70 ns		80 ns		100 ns		Unit	Note
			Min	Max	Min	Max	Min	Max		
Input leakage current	I_{LI}	$0\text{ V} \leq V_I \leq 6.5\text{ V}$, All other pins not under test = 0 V	-120	120	-120	120	-120	120	μA	
Output leakage current	I_{LO}	D_{OUT} disable $0\text{ V} \leq V_O \leq 5.5\text{ V}$	-10	10	-10	10	-10	10	μA	
Output high voltage	V_{OH}	$I_{OH} = -5.0\text{ mA}$	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	$I_{OL} = 4.2\text{ mA}$	0	0.4	0	0.4	0	0.4	V	
Average power supply current (Operating)	I_{CC1}	RAS, CAS cycling, $t_{RC} = \text{min}$	-	900	-	780	-	660	mA	[1] [2]
Power supply current (Standby)	I_{CC2}	RAS = V_{IH} , CAS = V_{IH} $D_{OUT} = \text{Hi-Z}$	TTL	-	28	-	28	-	28	mA
			MOS	-	16	-	16	-	16	mA
Average power supply current (RAS-only refresh)	I_{CC3}	RAS cycling, CAS = V_{IH} , $t_{RC} = \text{min}$	-	900	-	780	-	660	mA	[1] [2]
Average power supply current (CAS-before-RAS refresh)	I_{CC6}	RAS cycling, CAS-before-RAS, $t_{RC} = \text{min}$	-	900	-	780	-	660	mA	[1]
Average power supply current (Fast Page Mode)	I_{CC7}	RAS = V_{IL} , CAS cycling, $t_{PC} = \text{min}$	-	780	-	660	-	580	mA	[1] [3]

1 I_{CC} depends on output loading and cycle rates. Specified values are obtained with the output open

2 Address can be changed once or less while RAS = V_{IL}

3 Address can be changed once or less while CAS = V_{IH} .

AC Characteristics ($V_{CC} = 5 V \pm 10\%$, $T_a = 0^\circ C \sim +70^\circ C$) [1] [2] [3]

Parameter	Symbol	70 ns		80 ns		100 ns		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	140	-	160	-	190	-	ns	
Fast Page Mode cycle time	t_{PC}	45	-	50	-	55	-	ns	
Access time from RAS	t_{RAC}	-	70	-	80	-	100	ns	[4] [5] [6]
Access time for CAS	t_{CAC}	-	20	-	20	-	25	ns	[4] [5]
Access time from column address	t_{AA}	-	35	-	40	-	50	ns	[4] [6]
Access time from CAS precharge	t_{CPA}	-	40	-	45	-	50	ns	[4]
Output low impedance time from CAS	t_{CLZ}	0	-	0	-	0	-	ns	
Output buffer turn-off delay time	t_{OFF}	0	20	0	20	0	20	ns	[7]
Transition time	t_T	3	50	3	50	3	50	ns	[3]
Refresh period	t_{REF}	-	8	-	8	-	8	ms	
RAS precharge time	t_{RP}	60	-	70	-	80	-	ns	
RAS pulse width	t_{RAS}	70	10K	80	10K	100	10K	ns	
RAS pulse width (Fast Page Mode)	t_{RASP}	70	100K	80	100K	100	100K	ns	
RAS hold time	t_{RSH}	20	-	20	-	25	-	ns	
CAS precharge time (Fast Page Mode)	t_{CP}	10	-	10	-	10	-	ns	
CAS pulse width	t_{CAS}	20	10K	20	10K	25	10K	ns	
CAS hold time	t_{CSH}	70	-	80	-	100	-	ns	
CAS to RAS precharge time	t_{CRP}	10	-	10	-	10	-	ns	
RAS to CAS delay time	t_{RCD}	20	50	20	60	25	75	ns	[5]
RAS to column address delay time	t_{RAD}	15	35	17	40	20	50	ns	[6]
Row address set-up time	t_{ASR}	0	-	0	-	0	-	ns	
Row address hold time	t_{RAH}	10	-	12	-	15	-	ns	
Column address set-up time	t_{ASC}	0	-	0	-	0	-	ns	
Column address hold time	t_{CAH}	15	-	15	-	20	-	ns	
Column address hold time from RAS	t_{AR}	55	-	60	-	75	-	ns	
Column address to RAS lead time	t_{RAL}	35	-	40	-	50	-	ns	
Read command set-up time	t_{RCS}	0	-	0	-	0	-	ns	
Read command hold time	t_{RCH}	0	-	0	-	0	-	ns	[8]
Read command hold time reference to RAS	t_{RRH}	10	-	10	-	10	-	ns	[8]
Write command set-up time	t_{WCS}	0	-	0	-	0	-	ns	
Write command hold time	t_{WCH}	15	-	15	-	20	-	ns	
Write command hold time from RAS	t_{WCR}	55	-	60	-	75	-	ns	
Write command pulse width	t_{WP}	15	-	15	-	20	-	ns	
Write command to RAS lead time	t_{RWL}	20	-	20	-	25	-	ns	
Write command to CAS lead time	t_{CWL}	20	-	20	-	25	-	ns	
Data-in set-up time	t_{DS}	0	-	0	-	0	-	ns	
Data-in hold time	t_{DH}	15	-	15	-	20	-	ns	

AC Characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $T_a = 0^\circ\text{C} \sim +70^\circ\text{C}$) ^{[1] [2] [3]} (Continued)

Parameter	Symbol	70 ns		80 ns		100 ns		Unit	Note
		Min	Max	Min	Max	Min	Max		
Data-in hold time from RAS	t_{DHR}	55	-	60	-	75	-	ns	
CAS active delay from RAS precharge	t_{RPC}	10	-	10	-	10	-	ns	
RAS to CAS set-up time (CAS-before-RAS)	t_{CSR}	10	-	10	-	10	-	ns	
RAS to CAS hold time (CAS-before-RAS)	t_{CHR}	30	-	30	-	30	-	ns	
CAS precharge time (Refresh counter test)	t_{CPT}	40	-	40	-	50	-	ns	

- 1 A start-up delay of 100 μs is required after power-up followed by a minimum of eight initialization cycles (RAS-only refresh or CAS-before-RAS refresh) before proper device operation is achieved. When using the internal refresh counter, a minimum of eight CAS-before-RAS initialization cycles is required
- 2 AC measurements assume $t_T = 5\text{ ns}$
- 3 V_{IH} (min) and V_{IL} (max) are reference levels for measuring input timing signals. Transition times are measured between V_{IH} and V_{IL}
- 4 Measured with a load circuit equivalent to 2 TTL + 100 pF
- 5 Operation within the $t_{RCD}(\text{max})$ limit ensures that $t_{RAC}(\text{max})$ can be met. $t_{RCD}(\text{max})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, access time is controlled by t_{CAC}
- 6 Operation within the $t_{RAD}(\text{max})$ limit ensures that $t_{RAC}(\text{max})$ can be met. $t_{RAD}(\text{max})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, access time is controlled by t_{AA}
- 7 t_{OFF} defines the time at which the output achieves an open circuit condition and is not referenced to output voltage levels
- 8 t_{RCH} or t_{RRH} must be satisfied for a read cycle

See ADDENDUM A for AC Timing Waveforms