

MSC23409C/CL-xxDS9**4,194,304-Word × 9-Bit DRAM MODULE : FAST PAGE MODE TYPE****DESCRIPTION**

The OKI MSC23409C/CL-xxDS9 is a fully decoded 4,194,304-word × 9-bit CMOS Dynamic Random Access Memory Module composed of nine 4-Mb DRAMs (4M × 1) in SOJ packages mounted with nine decoupling capacitors on a 30-pin glass epoxy single-inline package. This module is generally used for memory expansion in parity applications such as workstations. The low-power version (CL) offers reduced power consumption for mobile computing applications like laptops and palmtops.

FEATURES

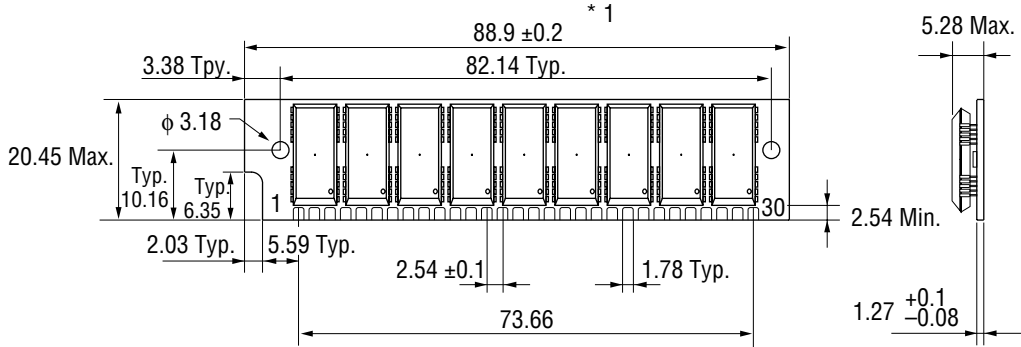
- 4-Meg × 9-bit organization
- 30-Pin Socket Insertable Module
MSC23409C/CL-xxDS9 : Solder tab
- Single 5 V supply ±10% tolerance
- Access times : 60, 70, 80 ns
- Input : TTL compatible
- Output : TTL compatible, 3-state
- Refresh : 1024 cycles/16 ms (128 ms : L-version)
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ hidden refresh, $\overline{\text{RAS}}$ -only refresh capability
- Multi-bit test mode capability
- Fast Page Mode capability

PRODUCT FAMILY

Family	Access Time (Max.)			Cycle Time (Min.)	Power Dissipation	
	t _{RAC}	t _{AA}	t _{CAC}		Operating (Max.)	Standby (Max.)
MSC23409C/CL-60DS9	60 ns	30 ns	15 ns	110 ns	4950 mW	49.5 mW/ 9.9 mW (L-version)
MSC23409C/CL-70DS9	70 ns	35 ns	20 ns	130 ns	4455 mW	
MSC23409C/CL-80DS9	80 ns	40 ns	20 ns	150 ns	3960 mW	

PIN CONFIGURATION

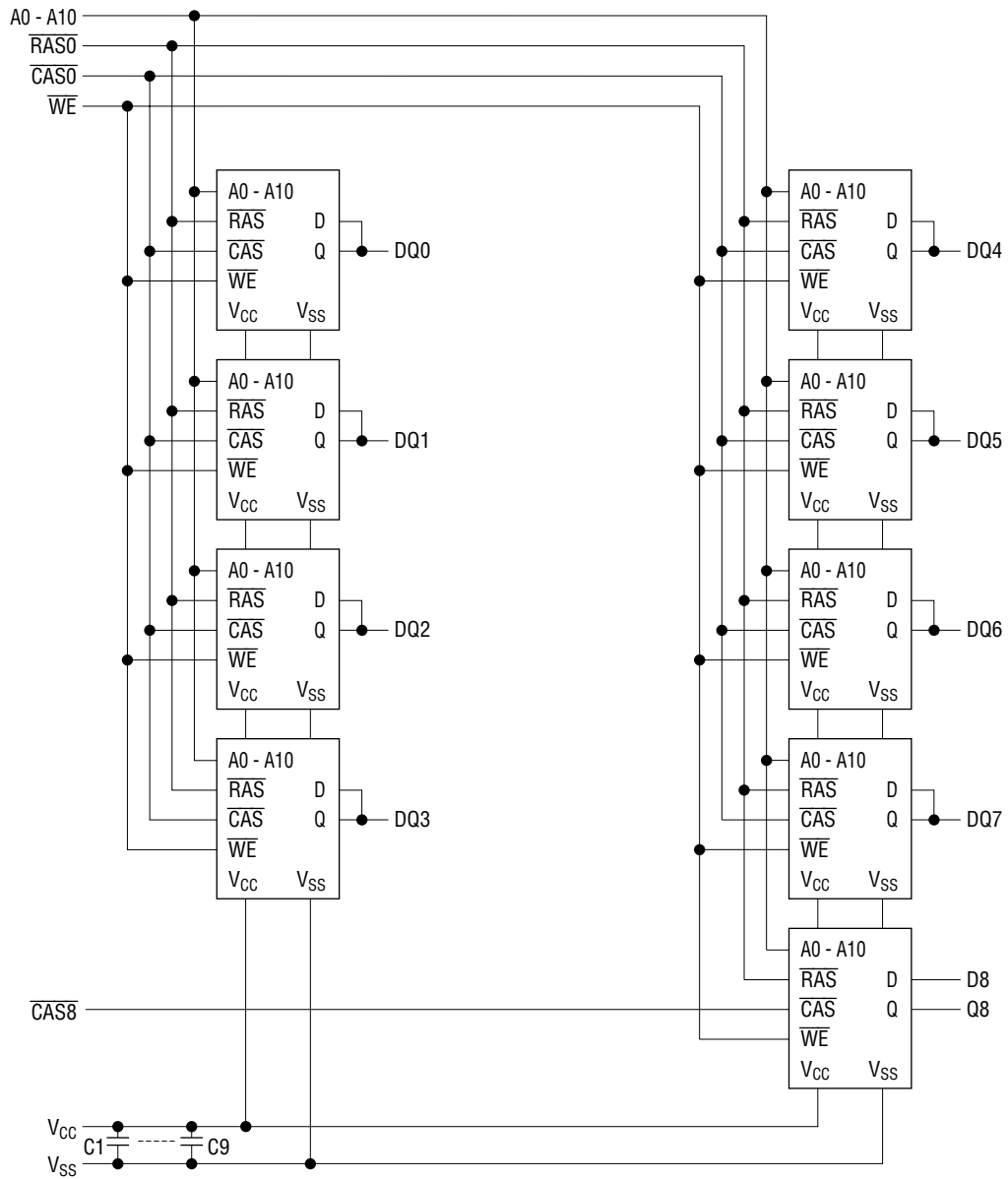
MSC23409C/CL-xxDS9



*1 The common size difference of the board width 12.5 mm of its height is specified as ± 0.2 . The value above 12.5 mm is specified as ± 0.5 .

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V _{CC}	11	A4	21	\overline{WE}
2	\overline{CAS}	12	A5	22	V _{SS}
3	DQ0	13	DQ3	23	DQ6
4	A0	14	A6	24	NC
5	A1	15	A7	25	DQ7
6	DQ1	16	DQ4	26	Q8
7	A2	17	A8	27	\overline{RAS}
8	A3	18	A9	28	$\overline{CAS8}$
9	V _{SS}	19	A10	29	D8
10	DQ2	20	DQ5	30	V _{CC}

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS**Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V _{SS}	V _{IN} , V _{OUT}	-1.0 to 7.0	V
Voltage V _{CC} Supply Relative to V _{SS}	V _{CC}	-1.0 to 7.0	V
Short Circuit Output Current	I _{OS}	50	mA
Power Dissipation	P _D	9	W
Operating Temperature	T _{opr}	0 to 70	°C
Storage Temperature	T _{stg}	-40 to 125	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

(Ta = 0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V _{CC}	4.5	5.0	5.5	V
	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	6.5	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

Capacitance

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A10)	C _{IN1}	—	64	pF
Input Capacitance (RAS, CAS, WE)	C _{IN2}	—	73	pF
I/O Capacitance (DQ0 - DQ7)	C _{DQ}	—	19	pF
Input Capacitance (CAS8)	C _{IN3}	—	13	pF
Input Capacitance (D8)	C _{IN4}	—	12	pF
Output Capacitance (Q8)	C _{OUT}	—	13	pF

Note : Capacitance measured with Boonton Meter.

DC Characteristics

($V_{CC} = 5\text{ V} \pm 10\%$, $T_a = 0^\circ\text{C}$ to 70°C)

Parameter	Symbol	Condition	MSC23409C/CL		MSC23409C/CL		MSC23409C/CL		Unit	Note
			-60DS9		-70DS9		-80DS9			
			Min.	Max.	Min.	Max.	Min.	Max.		
Input Leakage Current	I_{LI}	$0\text{ V} \leq V_I \leq 6.5\text{ V}$; All other pins not under test = 0 V	-90	90	-90	90	-90	90	μA	
Output Leakage Current	I_{LO}	DOUT disable $0\text{ V} \leq V_O \leq 5.5\text{ V}$	-10	10	-10	10	-10	10	μA	
Output High Voltage	V_{OH}	$I_{OH} = -5.0\text{ mA}$	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	$I_{OL} = 4.2\text{ mA}$	0	0.4	0	0.4	0	0.4	V	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling, $t_{RC} = \text{Min.}$	—	900	—	810	—	720	mA	1, 2
Power Supply Current (Standby)	I_{CC2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}} = V_{IH}$	—	18	—	18	—	18	mA	1
		$\overline{\text{RAS}}$, $\overline{\text{CAS}}$	—	9	—	9	—	9	mA	1
		$\geq V_{CC} - 0.2\text{ V}$	—	1.8	—	1.8	—	1.8	mA	1, 5
Average Power Supply Current ($\overline{\text{RAS}}$ -only Refresh)	I_{CC3}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} = V_{IH}$, $t_{RC} = \text{Min.}$	—	900	—	810	—	720	mA	1, 2
Average Power Supply Current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	I_{CC6}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$, $t_{RC} = \text{Min.}$	—	900	—	810	—	720	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{\text{RAS}} = V_{IL}$, $\overline{\text{CAS}}$ cycling, $t_{PC} = \text{Min.}$	—	720	—	630	—	540	mA	1, 3
Average Power Supply Current (Battery Backup)	I_{CC10}	$t_{RC} = 125\ \mu\text{s}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycling	—	2.7	—	2.7	—	2.7	mA	1, 2 4, 5

- Notes:
- Specified values are obtained with the output open.
 - Address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$.
 - Address can be changed once or less while $\overline{\text{CAS}} = V_{IH}$.
 - $V_{CC} - 0.2\text{ V} \leq V_{IH} \leq 6.5\text{ V}$, $-1.0\text{ V} \leq V_{IL} \leq 0.2\text{ V}$.
 - L-version.

AC Characteristics (1/2)

(V_{CC} = 5 V ±10%, T_a = 0°C to 70°C) Note 1,2,3,9,10

Parameter	Symbol	MSC23409C/CL		MSC23409C/CL		MSC23409C/CL		Unit	Note
		-60DS9		-70DS9		-80DS9			
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t _{RC}	110	—	130	—	150	—	ns	
Fast Page Mode Cycle Time	t _{PC}	40	—	45	—	50	—	ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}	—	60	—	70	—	80	ns	4, 5, 6
Access Time from $\overline{\text{CAS}}$	t _{CAC}	—	15	—	20	—	20	ns	4, 5
Access Time from Column Address	t _{AA}	—	30	—	35	—	40	ns	4, 6
Access Time from $\overline{\text{CAS}}$ Precharge	t _{CPA}	—	35	—	40	—	45	ns	4
Output Low Impedance Time from $\overline{\text{CAS}}$	t _{CLZ}	0	—	0	—	0	—	ns	4
Output Buffer Turn-off Delay Time	t _{OFF}	0	15	0	20	0	20	ns	7
Transition Time	t _T	3	50	3	50	3	50	ns	3
Refresh Period	t _{REF}	—	16	—	16	—	16	ms	
Refresh Period (L-version)	t _{REF}	—	128	—	128	—	128	ms	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	40	—	50	—	60	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	60	10K	70	10K	80	10K	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	15	—	20	—	20	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t _{CP}	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	15	10K	20	10K	20	10K	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	60	—	70	—	80	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	20	45	20	50	20	60	ns	5
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	30	15	35	15	40	ns	6
Row Address Set-up Time	t _{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	10	—	10	—	10	—	ns	
Column Address Set-up Time	t _{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t _{CAH}	15	—	15	—	15	—	ns	
Column Address Hold Time from $\overline{\text{RAS}}$	t _{AR}	50	—	55	—	60	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t _{RAL}	30	—	35	—	40	—	ns	

AC Characteristics (2/2)

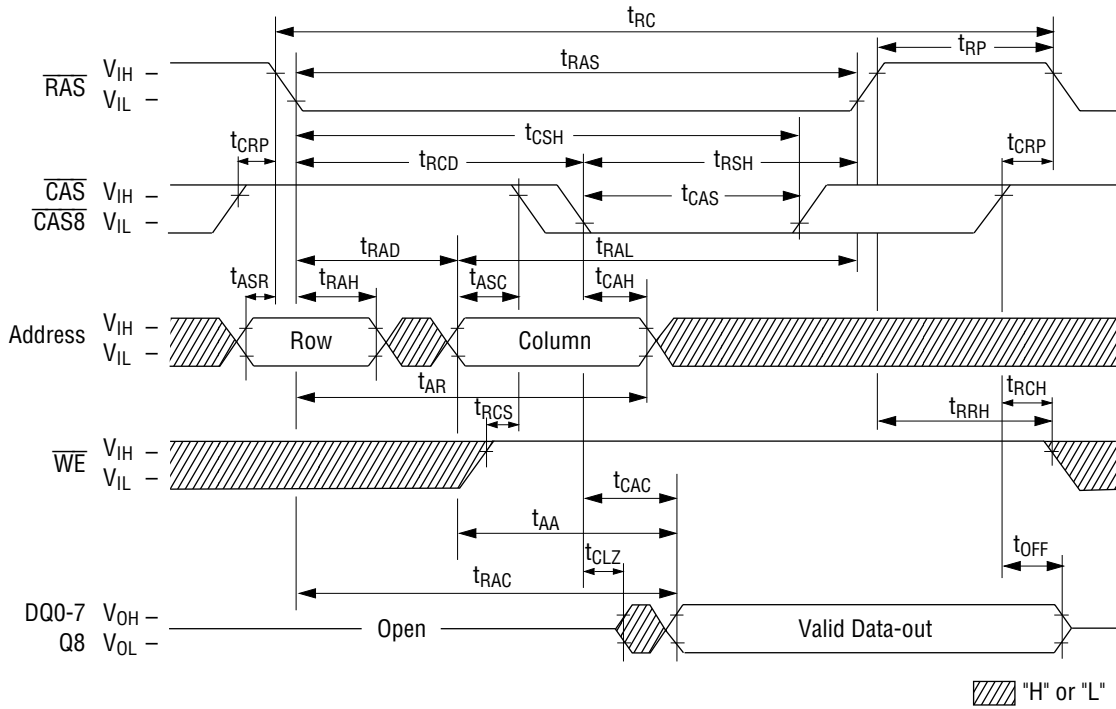
($V_{CC} = 5\text{ V} \pm 10\%$, $T_a = 0^\circ\text{C}$ to 70°C) Note 1,2,3,9,10

Parameter	Symbol	MSC23409C/CL		MSC23409C/CL		MSC23409C/CL		Unit	Note
		-60DS9		-70DS9		-80DS9			
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns	8
Read Command Hold Time referenced to \overline{RAS}	t_{RRH}	0	—	0	—	0	—	ns	8
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	
Write Command Hold Time	t_{WCH}	10	—	10	—	10	—	ns	
Write Command Hold Time from \overline{RAS}	t_{WCR}	45	—	50	—	60	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	10	—	ns	
Write Command to \overline{RAS} Lead Time	t_{RWL}	15	—	20	—	20	—	ns	
Write Command to \overline{CAS} Lead Time	t_{CWL}	15	—	20	—	20	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	
Data-in Hold Time	t_{DH}	15	—	15	—	15	—	ns	
Data-in Hold Time from \overline{RAS}	t_{DHR}	50	—	55	—	60	—	ns	
\overline{CAS} Active Delay Time from \overline{RAS} Precharge	t_{RPC}	5	—	5	—	5	—	ns	
\overline{RAS} to \overline{CAS} Set-up Time (\overline{CAS} before \overline{RAS})	t_{CSR}	5	—	5	—	5	—	ns	
\overline{RAS} to \overline{CAS} Hold Time (\overline{CAS} before \overline{RAS})	t_{CHR}	10	—	10	—	10	—	ns	
\overline{CAS} Precharge Time (Refresh Counter Test)	t_{CPT}	30	—	35	—	40	—	ns	
\overline{WE} to \overline{RAS} Precharge Time (\overline{CAS} before \overline{RAS})	t_{WRP}	10	—	10	—	10	—	ns	
\overline{WE} Hold Time from \overline{RAS} (\overline{CAS} before \overline{RAS})	t_{WRH}	10	—	10	—	10	—	ns	
\overline{RAS} to \overline{WE} Set-up Time (Test Mode)	t_{WTS}	10	—	10	—	10	—	ns	
\overline{RAS} to \overline{WE} Hold Time (Test Mode)	t_{WTH}	10	—	10	—	10	—	ns	

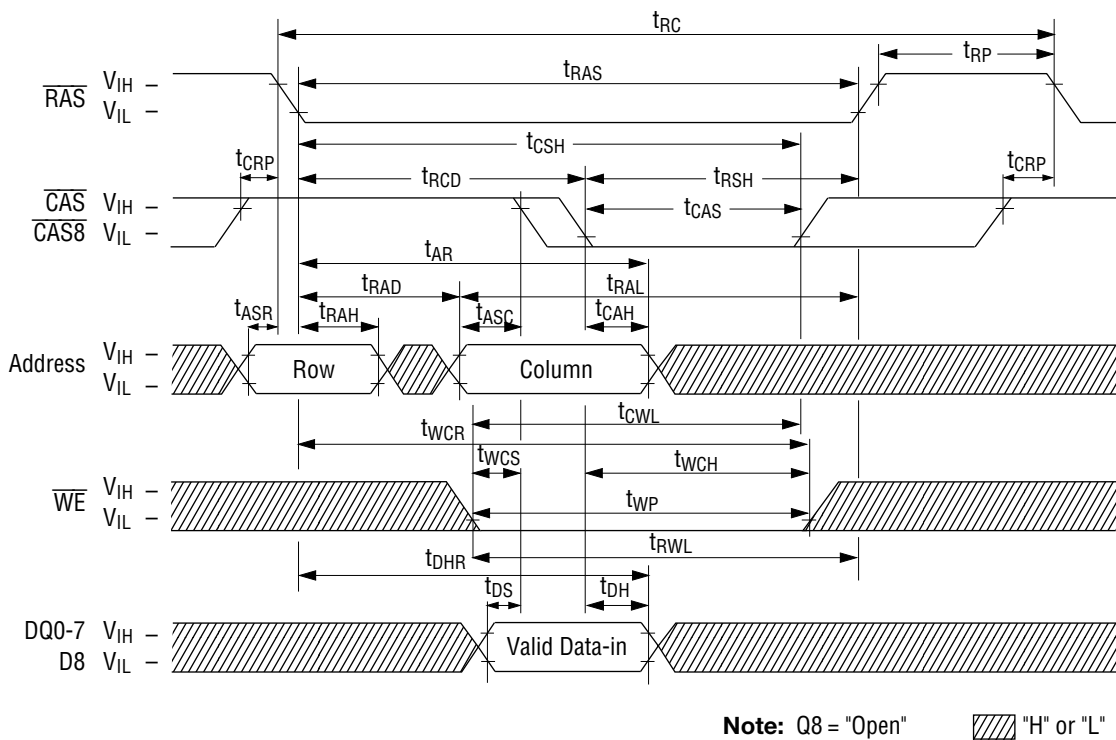
- Notes:
1. A start-up delay of 200 μ s is required after power-up followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh) before proper device operation is achieved.
When using the internal refresh counter, a minimum of eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ initialization cycles is required.
 2. AC measurement assume $t_T = 5$ ns.
 3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times are measured between V_{IH} and V_{IL} .
 4. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, access time is controlled by t_{CAC} .
 6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, access time is controlled by t_{AA} .
 7. t_{OFF} (Max.) defines the time at which the output achieves an open circuit condition and is not referenced to output voltage levels.
 8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 9. The test mode is initiated by performing a $\overline{\text{WE}}$ and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. This mode is latched and remains in effect until the exit cycle is generated.
The test mode specified in this data sheet is an 8-bit parallel test function. RA10, CA10 and CA0 are not used. In a read cycle, if all internal bits are equal, the data output pin will indicate a high level. If any internal bits are not equal, then data output pin will indicate a low level.
The test mode is cleared and the memory device returned to its normal operational state by performing a $\overline{\text{RAS}}$ -only refresh cycle or a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.
 10. In a test mode read cycle, the access time parameters are delayed by 5 ns. The test mode parameters are obtained by adding 5 ns to the normal read cycle values.

TIMING WAVEFORM

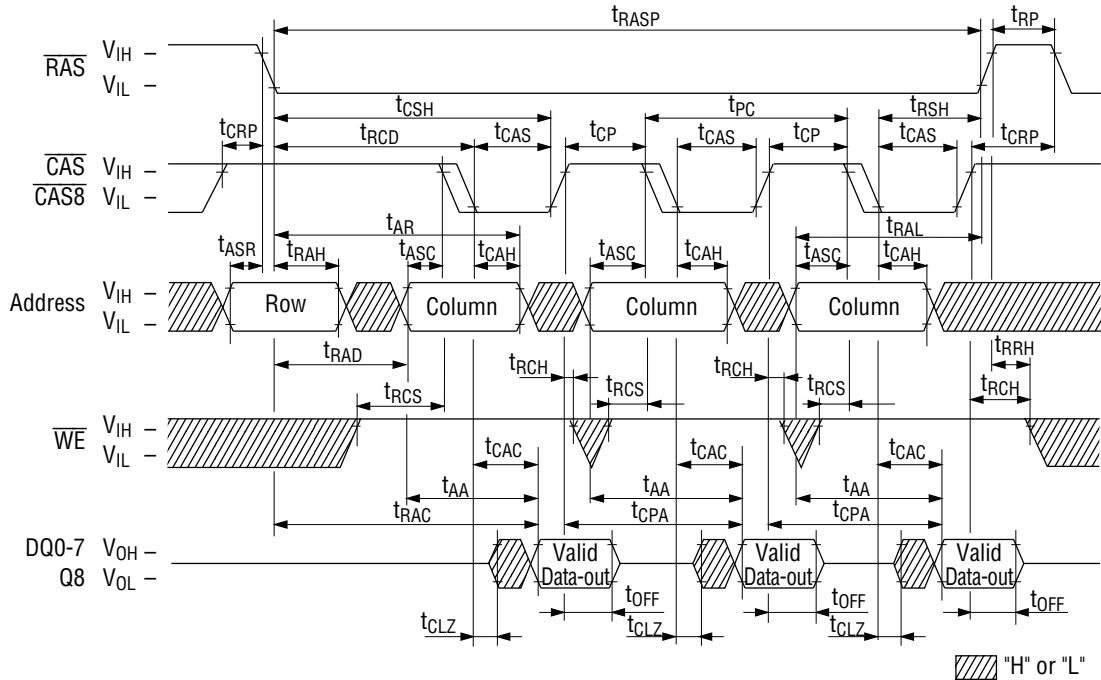
Read Cycle



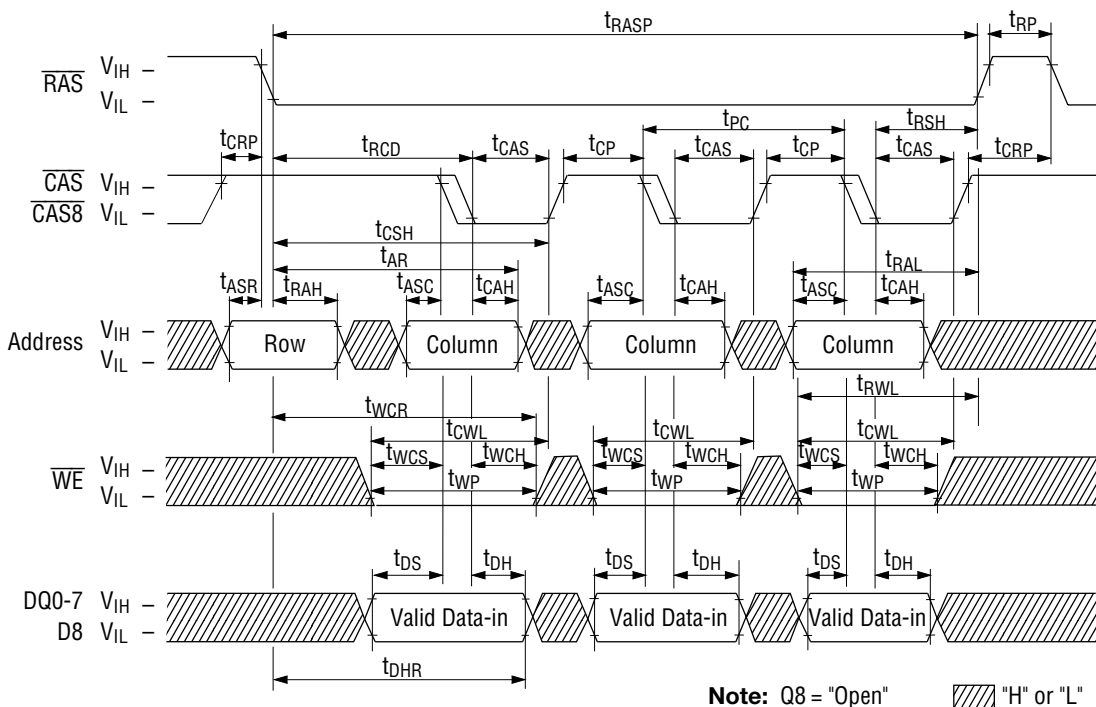
Write Cycle (Early Write)



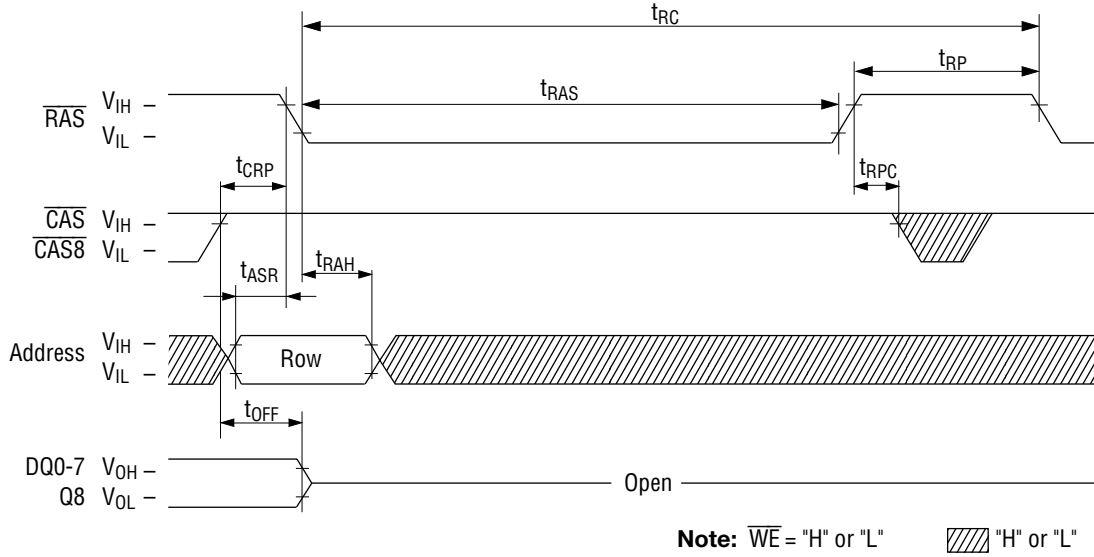
Fast Page Mode Read Cycle



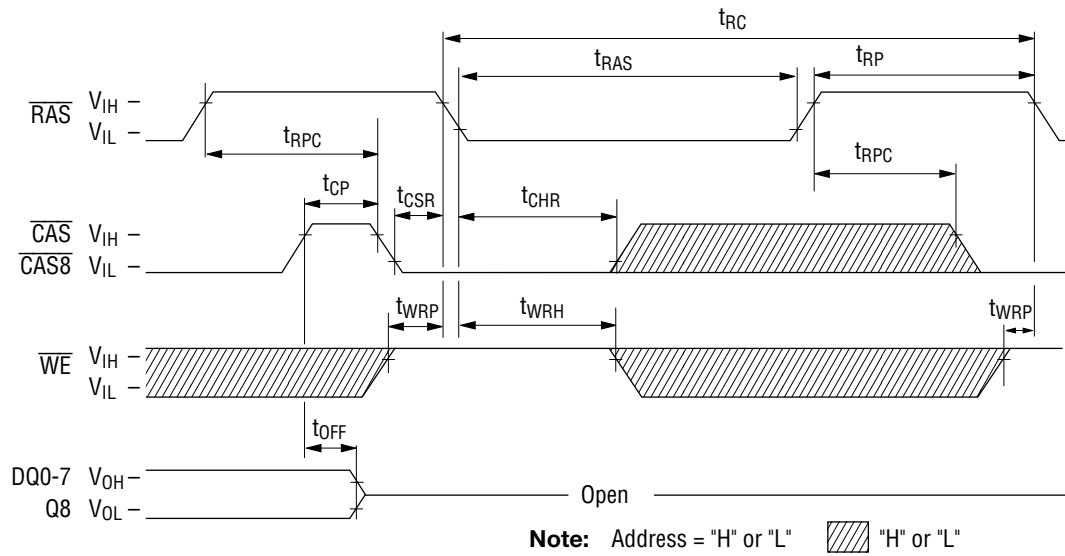
Fast Page Mode Write Cycle (Early Write)



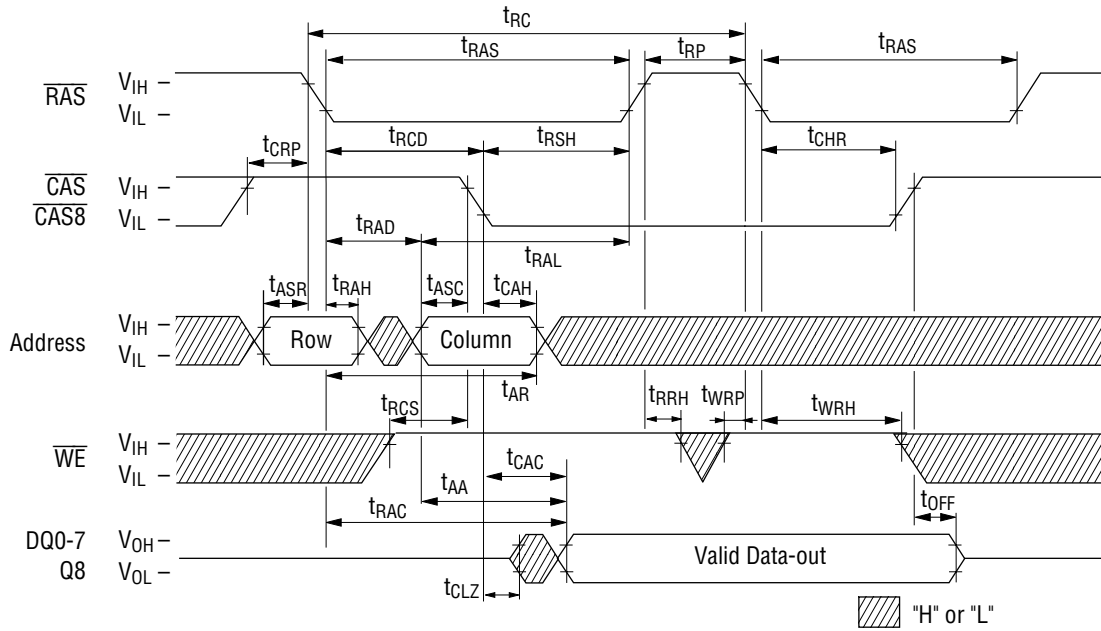
RAS-Only Refresh Cycle



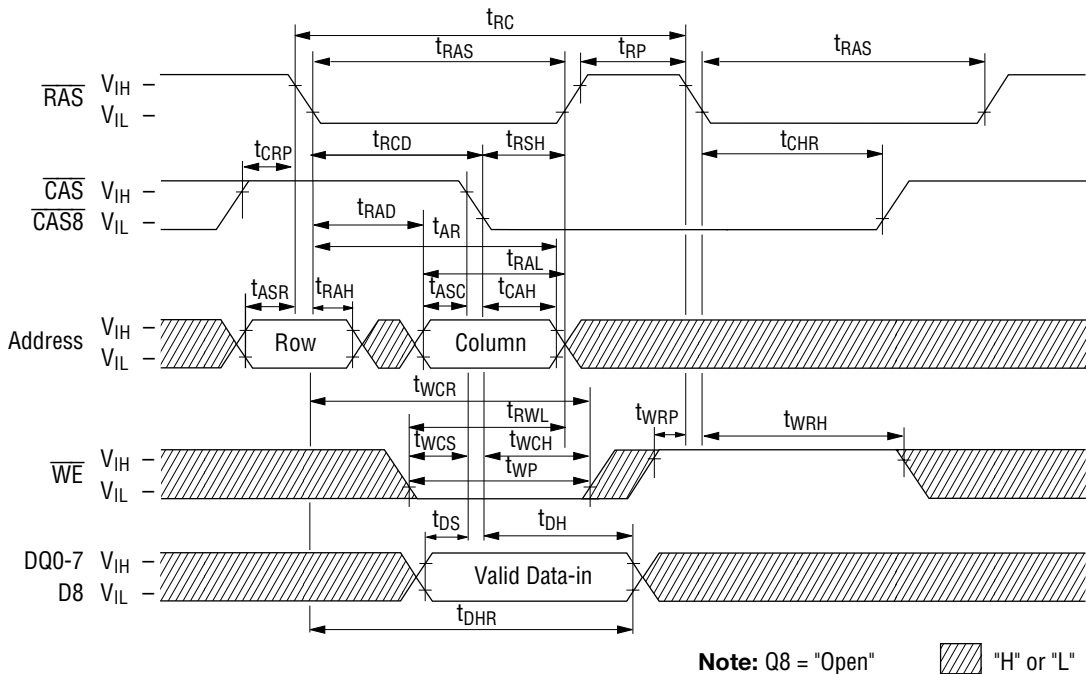
CAS before RAS Refresh Cycle



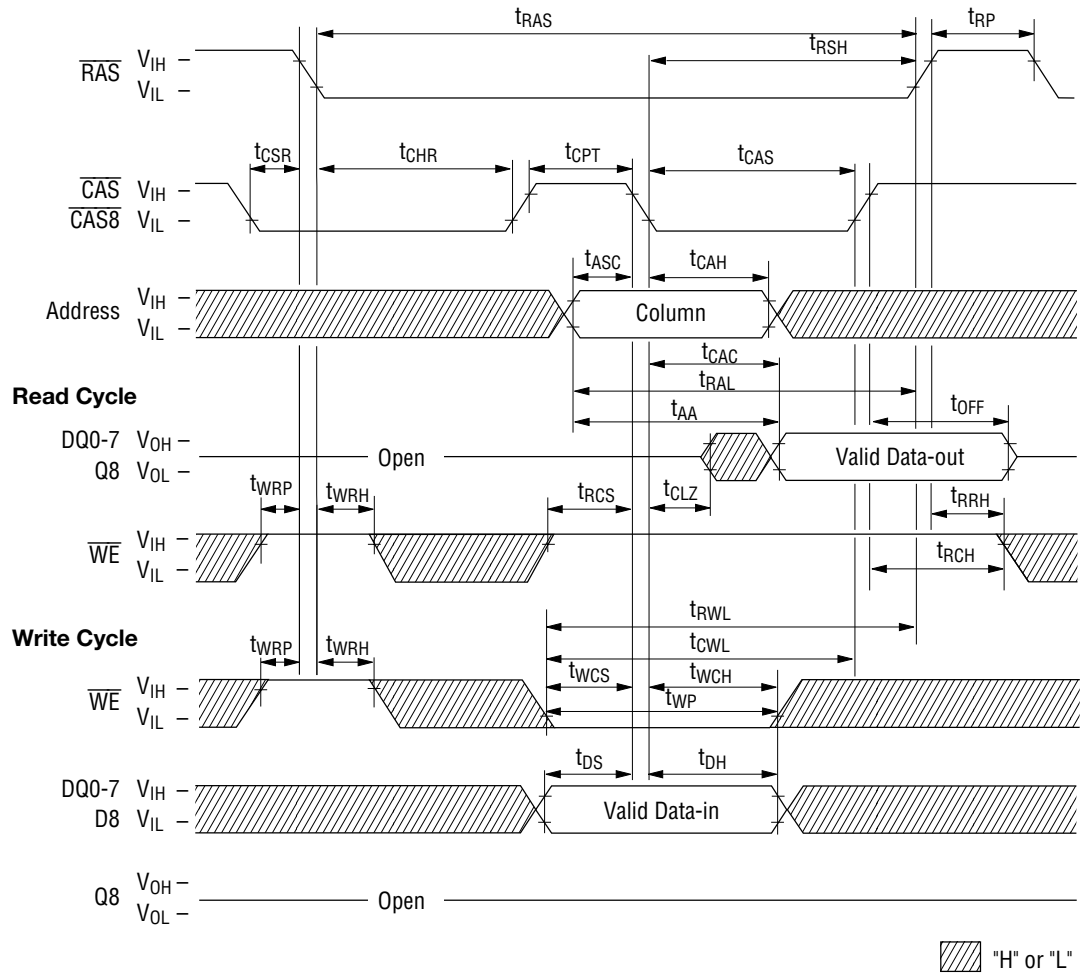
Hidden Refresh Read Cycle



Hidden Refresh Write Cycle



CAS before RAS Refresh Counter Test Cycle



WE • CAS before RAS Refresh Cycle

