OKI Semiconductor

This version: Nov. 1997
Previous version: Mar. 1996



# MSC5301B-02

## LCD COMMON/SEGMENT DRIVER WITH RAM

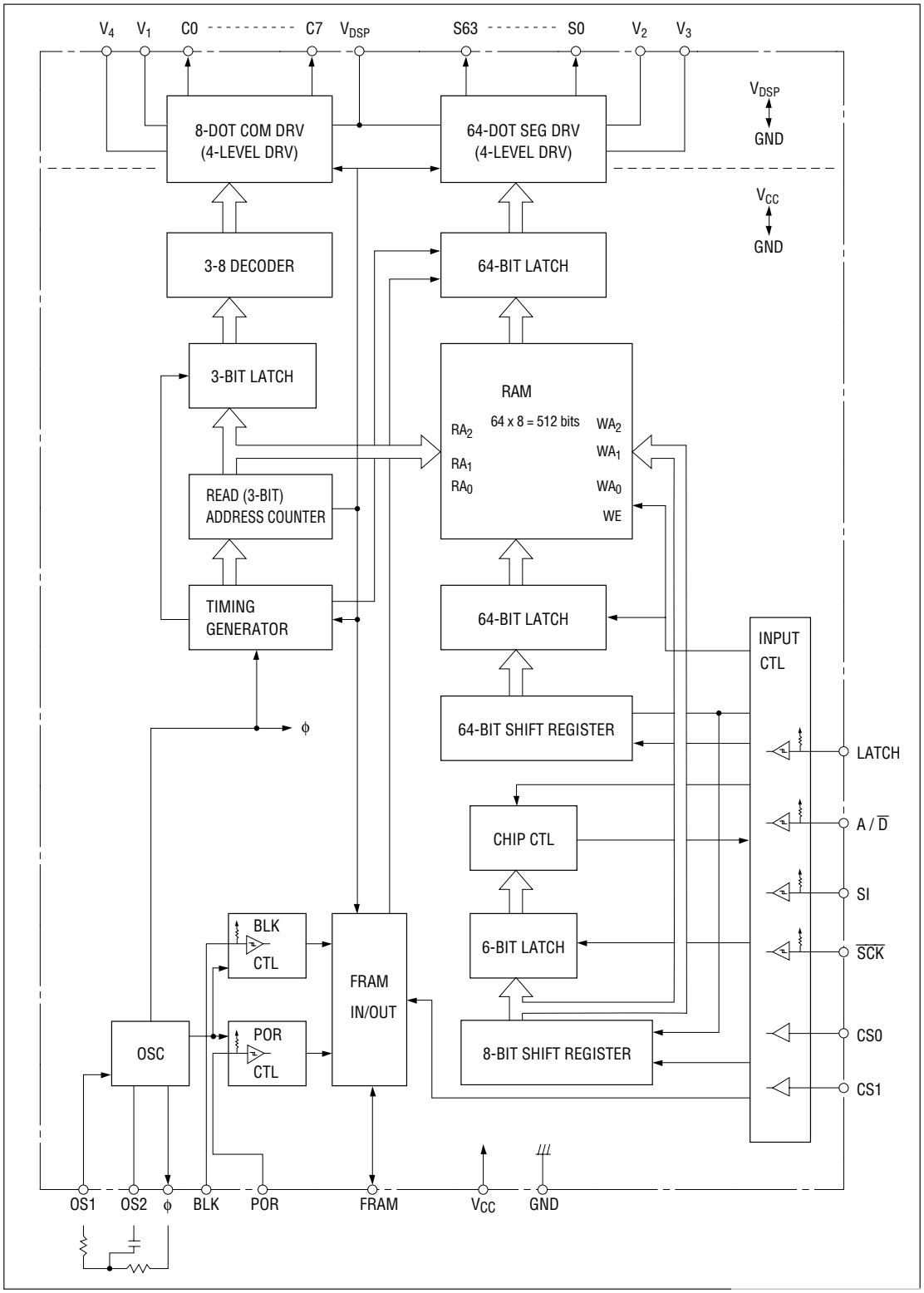
## GENERAL DESCRIPTION

The MSC5301B-02 is an LCD driver LSI with a built-in RAM. The device's bit mapping method offers greater flexibility in which each bit of the display RAM controls each section on the LCD panel. It can form a graphic display system of 64 x 8 dots in one chip. In addition, the display can be expanded by using the additional LSIs.

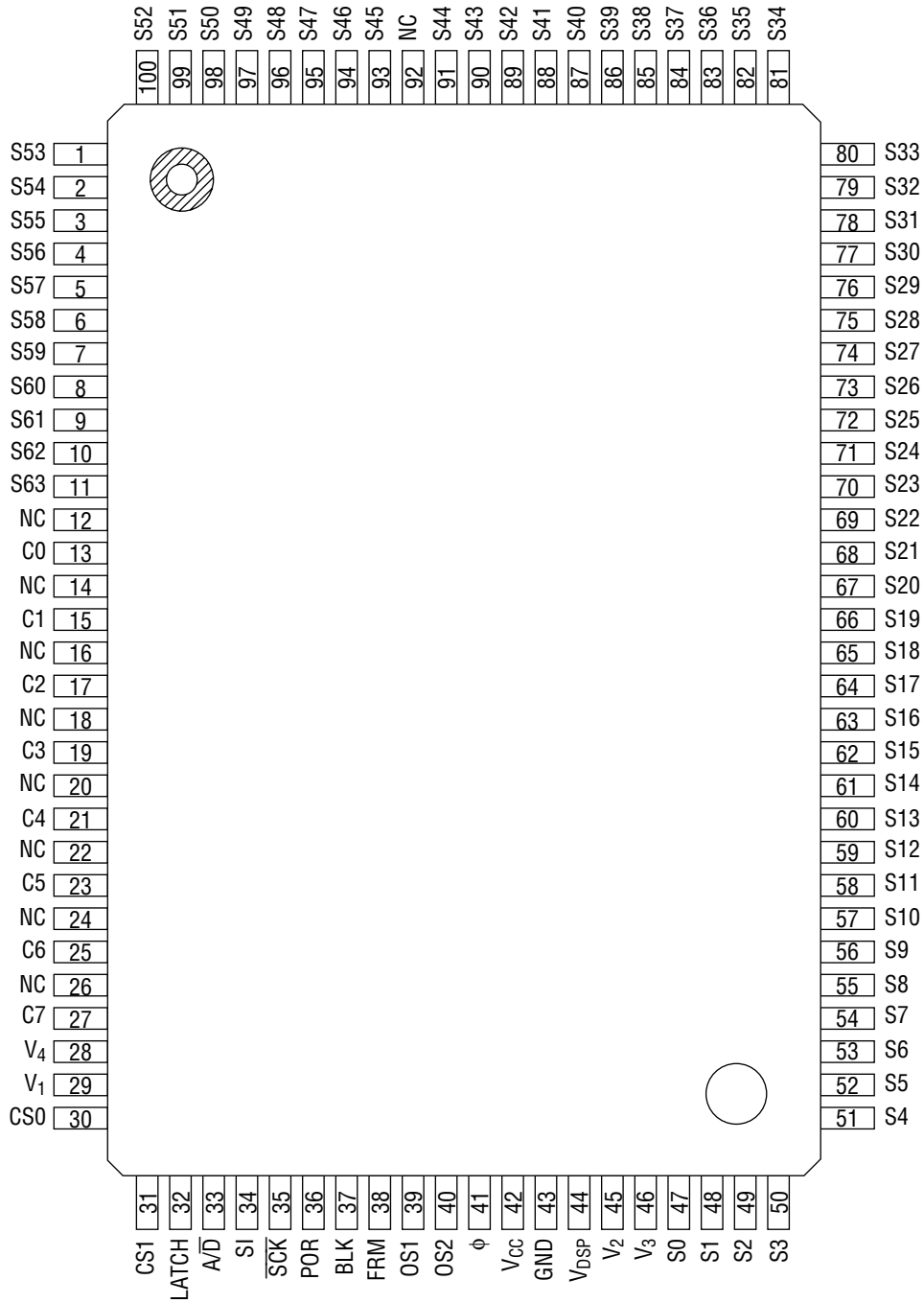
## FEATURES

- LCD driving voltage range : 6 to 16V
- Operating power supply voltage range : 5V ±10%
- Display duty : 1/8 (1/4 bias)
- Common output : 8 outputs
- Segment output : 64 outputs
- RAM capacity : 8 x 64 = 512 bits
- Serial transfer clock frequency ($f_{SCK}$) : 500 kHz Max.
- Multichip configuration available
- Blanking available
- Built-in RC oscillation circuit
- Package:
  100-pin plastic QFP (QFP100-P-1420-0.65-BK) (Product name: MSC5310B-02GS-BK)

## BLOCK DIAGRAM



## PIN CONFIGURATION (TOP VIEW)




NC: No connection

**100-Pin Plastic QFP**

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | Ta = 25°C | –0.3 to +6.5 | V |
| Power Supply Voltage | $V_{DSP}$ | Ta = 25°C | –0.3 to +18.0 *1 | V |
| Input Voltage | $V_{IN}$ | Ta = 25°C | $-0.3V \le V_{IN} \le V_{CC}+0.3$ | V |
| Input Voltage | $V_{INDP}$ | Ta = 25°C | $-0.3 \le V_{INDP} \le V_{DSP}+0.3$ | V |
| Power Dissipation | $P_D$ | Ta = 85°C | 275 | mW |
| Storage Temperature | $T_{STG}$ | — | –55 to +125 | °C |

*1 $V_{DSP}>V_1>V_2\ge V_3>V_4>GND$

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Condition | Range | Unit |
|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | GND = 0V | 4.5 to 5.5 | V |
| Power Supply Voltage | $V_{DSP}$ | GND = 0V | 6.0 to 16.0 *1 | V |
| Operating Temperature | $T_{op}$ | — | –40 to +85 | °C |
| Shift Frequency | $f_{SCK}$ | — | 25 to 500 | kHz |
| Oscillation Frequency | $f_\phi$ | — | 1.92 to 8.0 | kHz |
| Frame Frequency | $f_{FR}$ | — | 60 to 250 | Hz |

*1 $V_{DSP}>V_1>V_2\ge V_3>V_4>GND$

## ELECTRICAL CHARACTERISTICS

### DC Characteristics

($V_{CC}$ = 5V, Ta = –40 to +85°C)

| Parameter | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| "H" Input Voltage | $V_{IH}$ | | *1 | 3.5 | — | $V_{CC}$ | V |
| "L" Input Voltage | $V_{IL}$ | | *1 | 0 | — | 1.5 | V |
| Hysteresis Voltage 1 | $V_{HS1}$ | | *2 | 0.3 | 0.8 | 1.4 | V |
| Hysteresis Voltage 2 | $V_{HS2}$ | | *9 | 0.2 | 0.4 | 0.8 | V |
| Pull-up Resistance | $R_{PU}$ | $V_I$ = 0V | *2 | 10 | 35 | 60 | kΩ |
| Pull-up Voltage | $V_{PH}$ | $\|I_{IN}\| < 1\mu A$ | *2 | 4.9 | — | — | V |
| "H" Input Current | $I_{IH}$ | $V_{CC}$ = 5.5V, $V_{IH}$ = 5.5V | *3 | — | — | ±10 | μA |
| "L" Input Current | $I_{IL}$ | $V_{CC}$ = 5.5V, $V_{IL}$ = 0V | *3 | — | — | ±10 | μA |
| "H" Output Voltage | $V_{OH}$ | $I_O$ = –0.4mA | *4 | 4.6 | — | — | V |
| "L" Output Voltage | $V_{OL}$ | $I_O$ = 1.6mA | *4 | — | — | 0.4 | V |
| Common Driver | $V_{DP}$ | $V_{DSP}$ = 10V | I = –10μA | $V_{DSP}$–0.4 | — | — | V |
| Output Voltage | $V_1$ | *5 | I = ±10μA | $V_1$–0.4 | — | $V_1$+0.4 | V |
| | $V_4$ | | I = ±10μA | $V_4$–0.4 | — | $V_4$+0.4 | V |
| | $V_{SS}$ | | I = +10μA | — | — | 0.4 | V |
| Segment Driver | $V_{DP}$ | $V_{DSP}$ = 10V | I = –10μA | $V_{DSP}$–0.4 | — | — | V |
| Output Voltage | $V_2$ | *6 | I = ±10μA | $V_2$–0.4 | — | $V_2$+0.4 | V |
| | $V_3$ | | I = ±10μA | $V_3$–0.4 | — | $V_3$+0.4 | V |
| | $V_{SS}$ | | I = +10μA | — | — | 0.4 | V |
| Supply Current 1 | $I_{CC}$ | $V_{CC}$ = 5.0V | *7 | — | — | 6.0 | mA |
| Supply Current 2 | $I_{DSP}$ | $V_{CC}$ = 5.0V | *8 | — | — | 0.5 | mA |

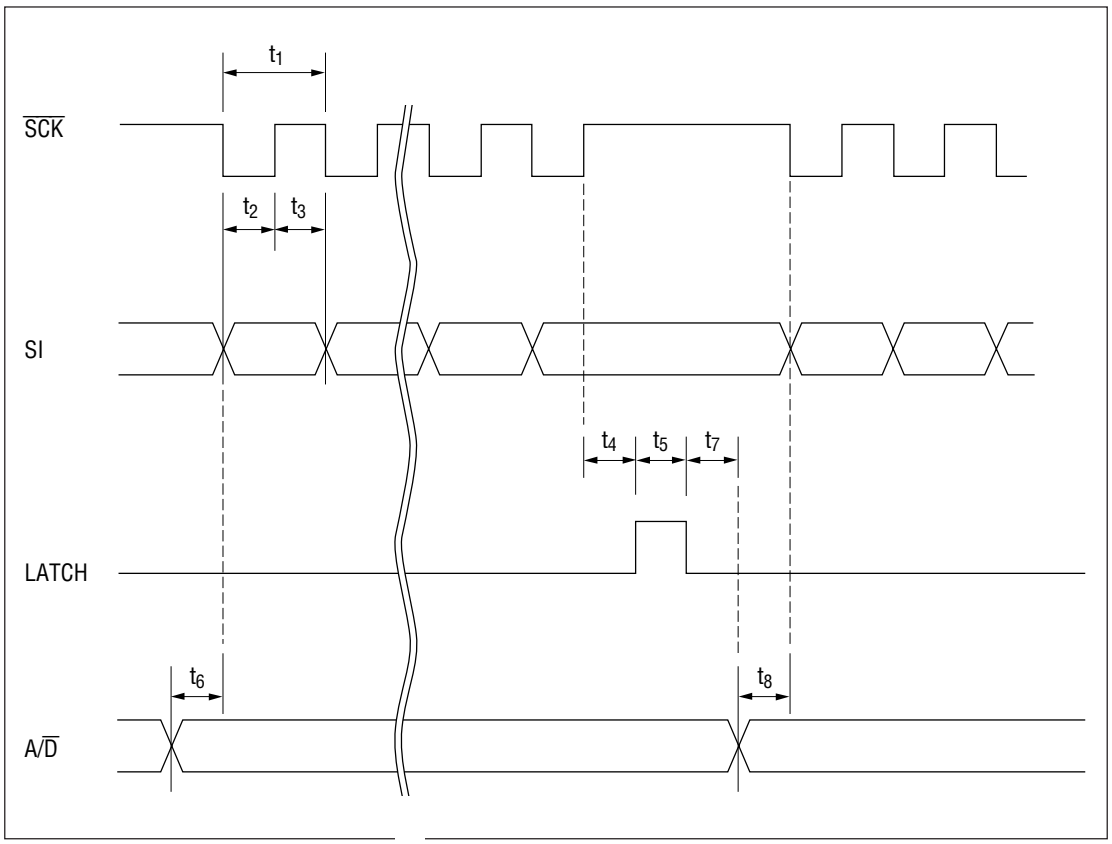
*1 Applicable to all input pins
*2 Applicable to LATCH, A/$\overline{D}$, SI, $\overline{SCK}$, BLK and POR pins
*3 Applicable to CS0, CS1, OS1 and FRAM pins
*4 Applicable to FRAM and ϕ pins
*5 Applicable to C0 - C7 pins
*6 Applicable to S0 - S63 pins
*7 fϕ = 3.2 kHz, $f_{SCK}$ = 200 kHz, no load, display pattern = checkers
$V_{DSP}$ = 16V, Current flows into $V_{CC}$ pin.
*8 fϕ = 3.2 kHz, $f_{SCK}$ = 200 kHz, no load, display pattern = checkers
$V_{DSP}$ = 16V, Current flows into $V_{DSP}$ pin.
*9 Applicable to OS1 pin

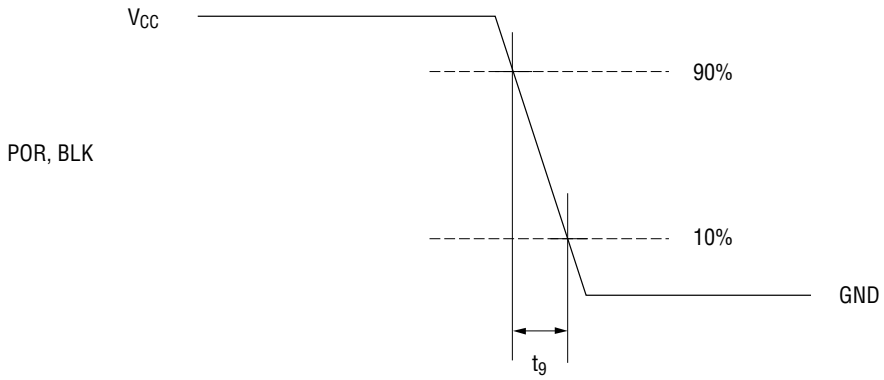
## AC Characteristics

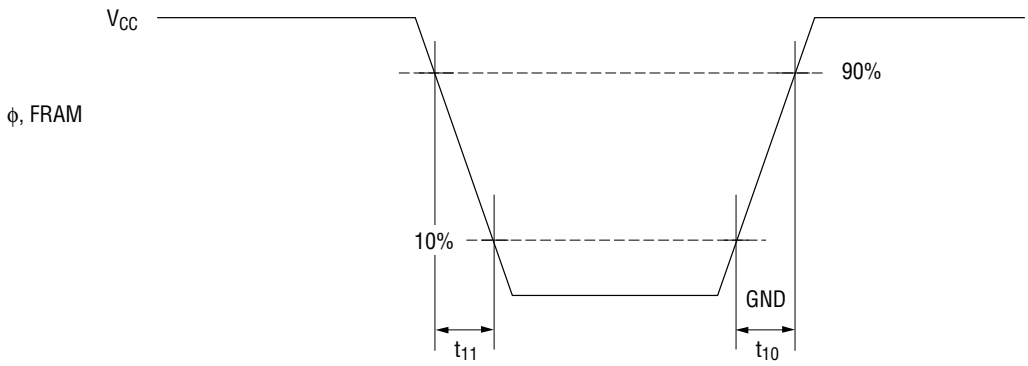
($V_{CC}$ = 5V, Ta = –40 to +85°C)

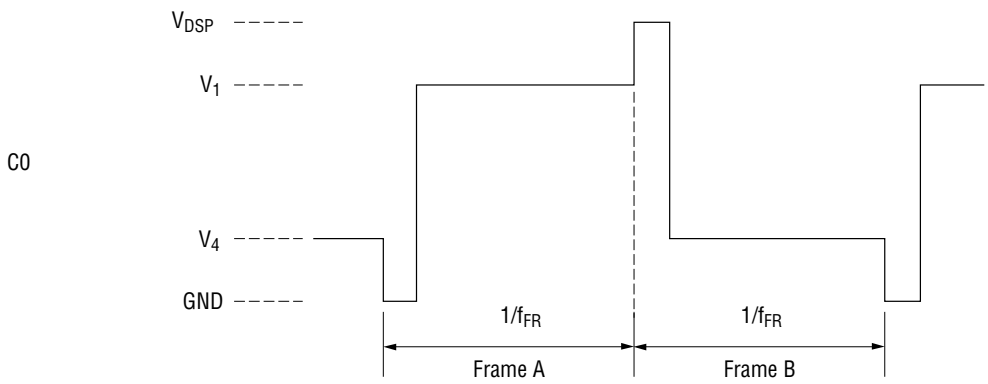
| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| SCK Clock Period | $t_1$ | — | 2 | — | — | µs |
| SI Data Setup Time | $t_2$ | — | 1 | — | — | µs |
| SI Data Hold Time | $t_3$ | — | 1 | — | — | µs |
| SCK-LATCH Time | $t_4$ | — | 1 | — | — | µs |
| LATCH Pulse Width | $t_5$ | — | 15 | — | — | µs |
| A/$\overline{D}$ Setup Time | $t_6$ | — | 1 | — | — | µs |
| A/$\overline{D}$ Hold Time | $t_7$ | — | 1 | — | — | µs |
| A/$\overline{D}$-SCK Time | $t_8$ | — | 1 | — | — | µs |
| POR, BLK Fall Time | $t_9$ | — | — | — | 20 | µs |
| ϕ, FRAM Rise Time | $t_{10}$ | $C_L$ = 50 pF | — | — | 0.3 | µs |
| ϕ, FRAM Fall Time | $t_{11}$ | $C_L$ = 50 pF | — | — | 0.3 | µs |
| Frame Frequency | $f_{FR}$ | *1 | 85 | 100 | 115 | Hz |

*1 The dispersion for external resistors and capacitors is not included.
$R_S$ = 1kΩ, $R_T$ = 15kΩ, $C_T$ = 0.01µF, $V_{CC}$ = 4.5V to 5.5V





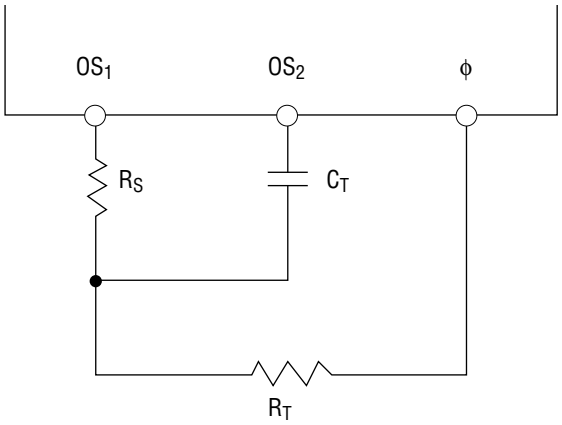



## FUNCTIONAL DESCRIPTION

### Pin Functional Description

- **OS1 (Pin 39), OS2 (Pin 40), ϕ (Pin 41)**

  These are pins for the RC oscillation circuit. Connect external resistors and a capacitor as shown below. When inputting the external clock pulse, input it to OS1 pin. OS2 and ϕ pins should be left open.




The relation of frame frequency $f_{FR}$ and internal clock frequency fϕ is shown by the following equation.
(RC oscillation frequency = internal clock frequency)

$$f\phi = 4 \times 8 \times f_{FR}$$

In addition, the relation of frame frequency $f_{FR}$ and frame synchronizing signal frequency $f_{FRAM}$ is shown by the following equation.

$$f_{FRAM} = f_{FR}/2$$

- **CS0 (Pin 30), CS1 (Pin 31)**

  Chip select input pins. Master and slave modes are determined by CS0 and CS1 as shown in the table below. A maximum of 4 devices can be connected in this manner. Use the master mode when using a single chip.

| CS0 | CS1 | Operation mode |
|---|---|---|
| L | L | Master mode |
| H | L | Slave mode |
| L | H | Slave mode |
| H | H | Slave mode |

H : $V_{CC}$ level
L : GND level

- **FRAM (Pin 38)**
  This is an input and output pin for the frame synchronizing signal to be used for master/slave configuration. It becomes an output pin in master mode and an input pin in slave mode.

- **SI (Pin 34)**
  This is a serial data input pin of address data (8 bits) and segment data (64 bits). A pull-up resistor (10 kΩ - 60 kΩ) and the Schmitt circuit are contained. The serial data is shifted at the rising edge of $\overline{SCK}$.

- **$\overline{SCK}$ (Pin 35)**
  This is a shift clock input pin of address data (8 bits) and segment data (64 bits). The serial data is shifted at the rising edge of $\overline{SCK}$ pulse. A pull-up resistor (10 kΩ - 60 kΩ) and the Schmitt circuit are contained.

- **LATCH (Pin 32)**
  This is a latch pulse input pin of address data (8 bits) and segment data (64 bits). The latch data comes through at "H" level of LATCH and the data just before "H" level is latched at "L" level. A pull-up resistor (10 kΩ - 60 kΩ) and the Schmitt circuit are contained.

- **A/$\overline{D}$ (Pin 33)**
  This is a data select signal input pin of address data (8 bits) and segment data (64 bits). "H" level is set in the case of address 8-bit input and "L" level is set in the case of segment data 64-bit input. A pull-up resistor (10 kΩ - 60 kΩ) and the Schmitt circuit are contained.

- **$V_{DSP}$ (Pin 44), $V_1$ (Pin 29), $V_2$ (Pin 45), $V_3$ (Pin 46), $V_4$ (Pin 28), $V_{CC}$ (Pin 42), GND (Pin 43)**
  These are power supply pins for this LSI and bias power supply pins for LCD driving. $V_{CC}$, which is a power supply pin, is from 4.5V to 5.5V; GND, which is a ground pin, is 0V; $V_{DSP}$, which is an LCD driving power supply pin, is usually used in the range between 6V and 16V. $V_1$, $V_2$, $V_3$ and $V_4$ are bias power supply pins for LCD driving and are usually used by supplying bias voltage from an external source.

- **BLK (Pin 37)**
  This is an input pin to control the LCD panel display.
  When a "H" level is input (or when this pin is open), the segment output pins S0 - S63 come to the levels $V_2$ - $V_3$ and the LCD panel is turned off. In addition, during this period, the data read from a display RAM is stopped but writing into the display RAM of address and segment data inputted from the SI pin is available.
  When this pin is changed from "H" level to "L", the frame synchronizing signal FRAM is output within the 2 cycles of an internal clock fϕ, and it is synchronized at multi-chip. Then, the display RAM address is set to "000". After 1/8 frame cycle from FRAM signal generation, the output is applied from the "001" data of the display RAM address to the segment driver. Because the display RAM contents are undefined at the time the power is turned on, keep this pin to "H" level (or leave open) until writing data to the RAM is completed. A pull-up resistor (10kΩ - 60kΩ) and the Schmitt circuit are contained.

- **POR (Pin 36)**
  This is a power-on-reset input pin. When a "H" level is input (or when this pin is open), the common and segment outputs come to the static light-out state in no relation to the BLK pin and the segment output pins S0 - S63 become $V_3$ level and the common output pins C0 - C8 become $V_4$ level.
  When this pin is changed from "H" level to "L", the frame synchronizing signal FRAM is output within the 2 cycles of an interval clock fϕ, and it is synchronized when multiple devices are connected and is moreover dynamic-operated from the frame Ⓑ. Then, the display RAM address is set to "000". After 1/8 frame cycle from FRAM signal generation, the "001" data of the display RAM address is output to the segment driver. However, because the BLK pin is usually at "H" level when the power-on-reset is released, reading data from the display RAM is stopped and light-out segment data is forcibly transferred to the segment output. A pull-up resistor (10kΩ - 60kΩ) and the Schmitt circuit are contained.

- **C0 (Pin 13) - C7 (Pin 27)**
  These are 8-output pins of the common driver which are used for LCD panel driving. The outputs of 4 levels are obtained ($V_{DSP}$ and GND are select levels, and $V_1$ and $V_4$ are nonselect levels).

- **S0 (Pin 47) - S63 (Pin 11)**
  These are 64-output pins of segment driver which are used for LCD panel driving. The outputs of 4 levels are obtained ($V_{DSP}$ and GND are select levels, which correspond to "1" of the display RAM data, and $V_2$ and $V_3$ are nonselect levels, which correspond to "0" of the display RAM data).

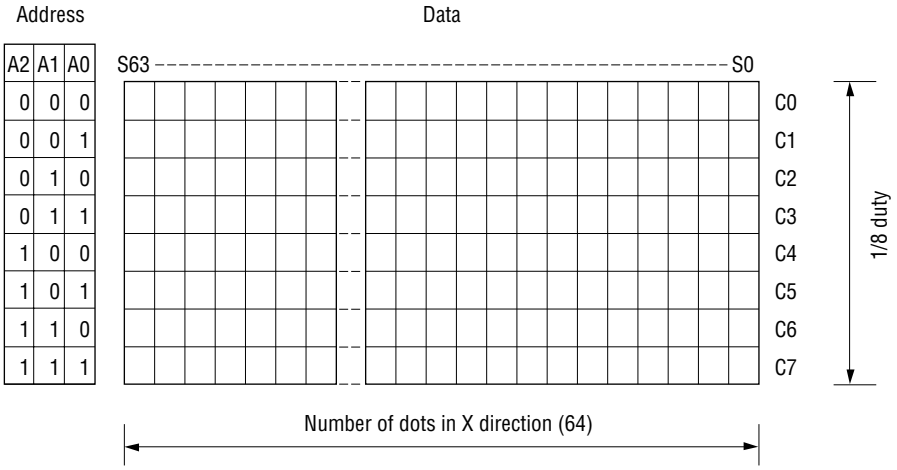
## NOTES ON USE

Note the following when turning power on and off:
The LCD drivers of this IC require a high voltage. For this reason, if a high voltage is applied to the LCD drivers with the logic power supply floating, excess current flows. This may damage the IC. Be sure to carry out the following power-on and power-off sequences:

When turning power on:
First $V_{CC}$ ON, next $V_{DSP}$, $V_4$, $V_3$, $V_2$, $V_1$ ON. Or both ON at the same time.
When turning power off:
First $V_{DSP}$, $V_4$, $V_3$, $V_2$, $V_1$ OFF, next $V_{CC}$ OFF. Or both OFF at the same time.

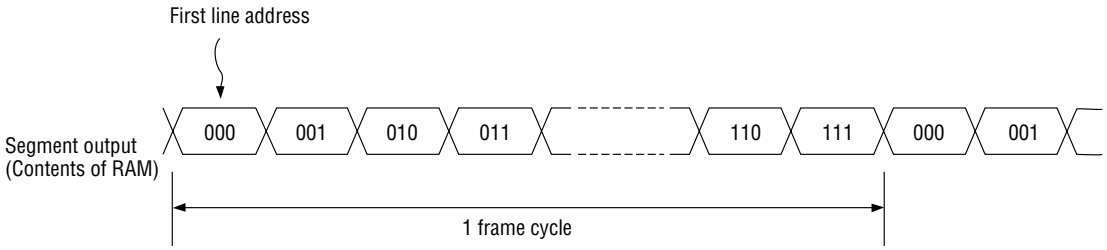
### Relation Between LCD Screen Size and Display RAM

This LCD driver has a built-in RAM for the display of 8 × 64 = 512 bits and the address corresponds to the duty of the LCD.
The data corresponds to the number of dots in the X direction. The relation between the LCD screen size and the display RAM is shown below.




### Relation Between Frame Cycle and Display RAM Data

The output of the display RAM data corresponds to the segment output. The relation between the frame cycle and the display RAM data is as follows:



### Multiple Configuration

This LCD driver can form multiple configuration.
It is possible to form a maximum of 4 devices (a panel of up to 256 × 8 dots in size can be formed) by using chip select signals CS0 and CS1. The devices in multiple configuration must be synchronized with one another. In this configuration, one device in the master mode, where the original oscillation signal ϕ and the synchronous signal FRAM are output, and the other devices in the slave mode, where the original oscillation signal ϕ and the synchronous signal FRAM are input, are used in combination.
Refer to items CS0 and CS1 of the pin description on the mode setting method.
The original oscillation signal output pin ϕ of the master mode devices is connected to the OS1 pin of the slave mode device and the synchronizing signal pin FRAM is also connected to the FRAM pin of the slave mode device.
Connect SI, $\overline{SCK}$, LATCH, A/$\overline{D}$, POR and BLK of the master mode devices to SI, $\overline{SCK}$, LATCH, A/$\overline{D}$, POR and BLK of each of the slave mode devices and connect them to CPU for control.
In addition, connect the devices so that $V_{DSP}$, $V_1$, $V_2$, $V_3$, $V_4$ and GND are shared between the devices, and connect them to each voltage level divided by resistors.

### Address Data Configuration

(MSB) (LSB)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Dummy data 2 | | Upper address | | Lower address | | | Dummy data 1 |
| DM2 | DM1 | CS1 | CS0 | A2 | A1 | A0 | DM0 |
| 2 bits | | 2 bits | | 3 bits | | | 1 bit |

The lower address, which is the address of the display RAM, corresponds to the common sides C0 - C7 of LCD panel. Dummy data 1 must be always set to "H".
The upper address corresponds to the logical state of chip select pins CS0 and CS1 and lower address is set to the chip only with which corresponded.
For the chip to output the common signal (ϕ, FRAM), set both of the upper address 2 bits to "L".
The 2 bits of dummy data can be set to either "L" or "H".

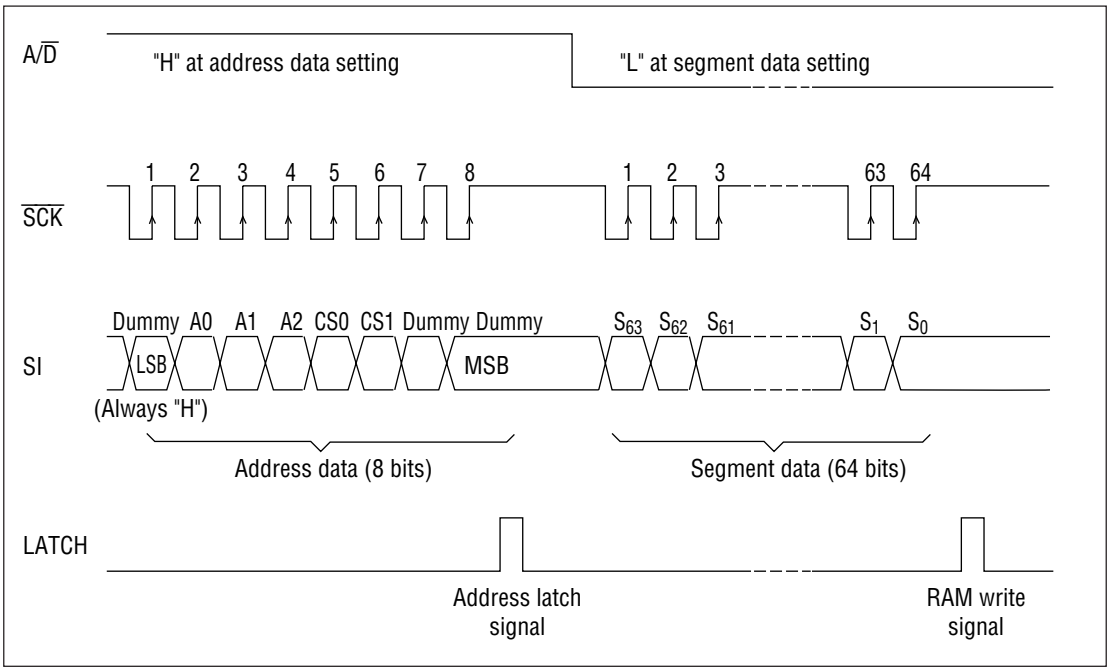
### Serial Signal to be Input From CPU

The following signals are input from an external CPU to this LCD driver:
- Serial transfer clock → $\overline{SCK}$
- Serial transfer data → SI
- Serial transfer latch → LATCH
- Serial data select → A/$\overline{D}$

The operations are shown in the following table.

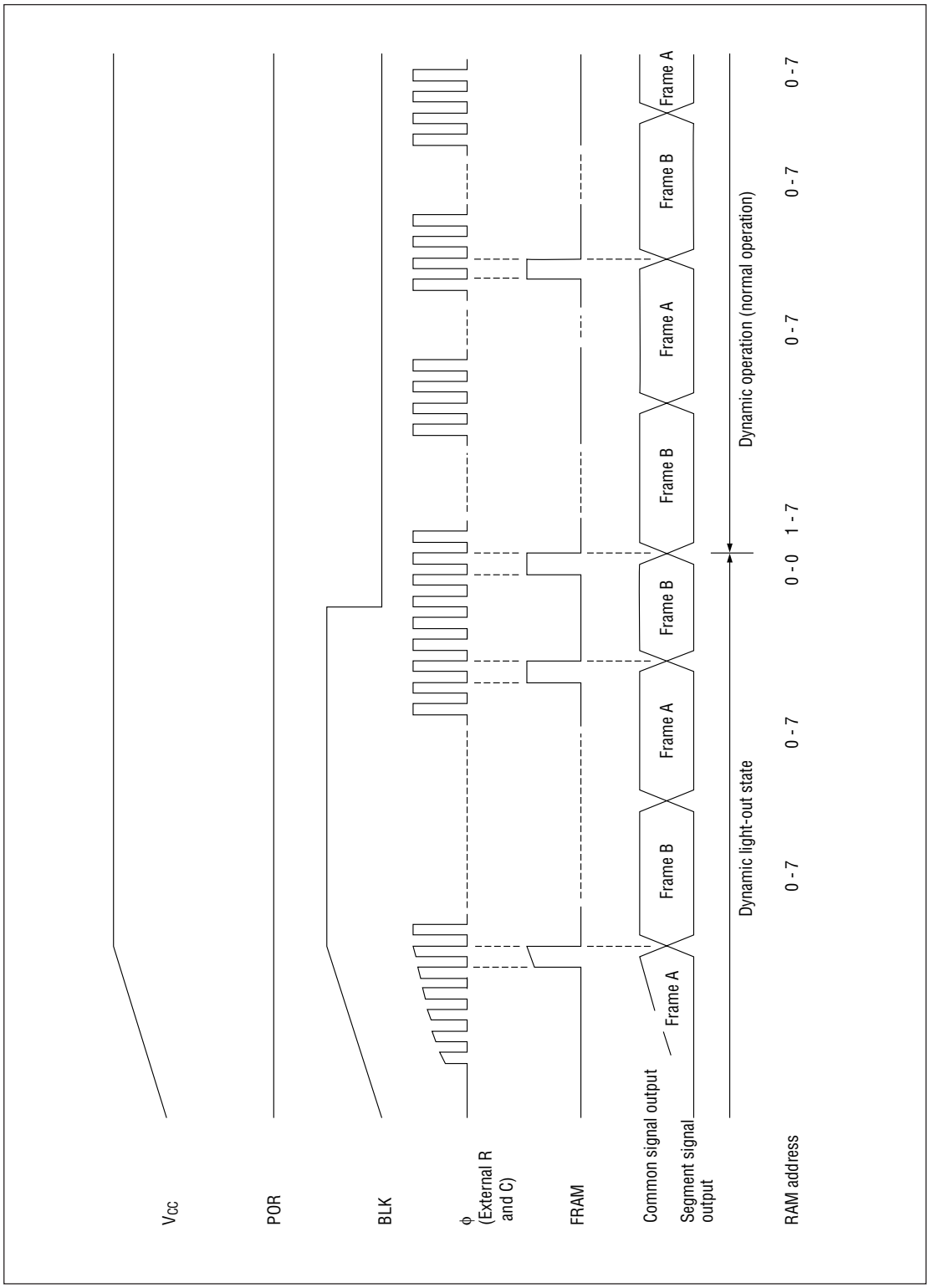
| Mode | A/$\overline{D}$ | $\overline{SCK}$ | LATCH | SI |
|---|---|---|---|---|
| Address data input mode | H | Shifts at the rising edge | 8-bit address data is latched at falling edge (level type) | 8-bit address data<br>Serial input from LSB side |
| Segment data input mode | L | Shifts at the rising edge | 64-bit segment data is latched at falling edge (level type) | 64-bit segment data<br>The first segment data shifted into the shift register corresponds to S63.<br>"1" : Light-on data, "0" : Light-out data |

### Timing for Serial Signal Transferred From CPU




Notes:
1. Be sure to set the address before writing the segment data to RAM. Then, write the segment data to RAM.
2. While the POR pin is "H" (upon power-on reset), neither address data nor segment data can be entered.

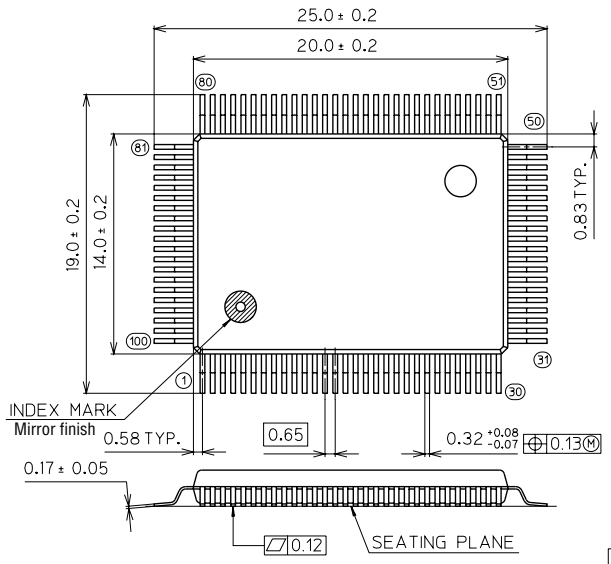
## Operation upon Power ON (When Single Device Used)

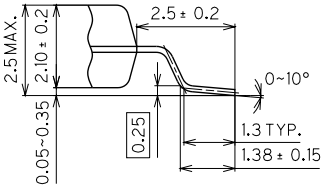


## PACKAGE DIMENSIONS

(Unit : mm)

QFP100-P-1420-0.65-BK




| | |
|---|---|
| Package material | Epoxy resin |
| Lead frame material | 42 alloy |
| Pin treatment | Solder plating |
| Solder plate thickness | 5 μm or more |
| Package weight (g) | 1.29 TYP. |

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).