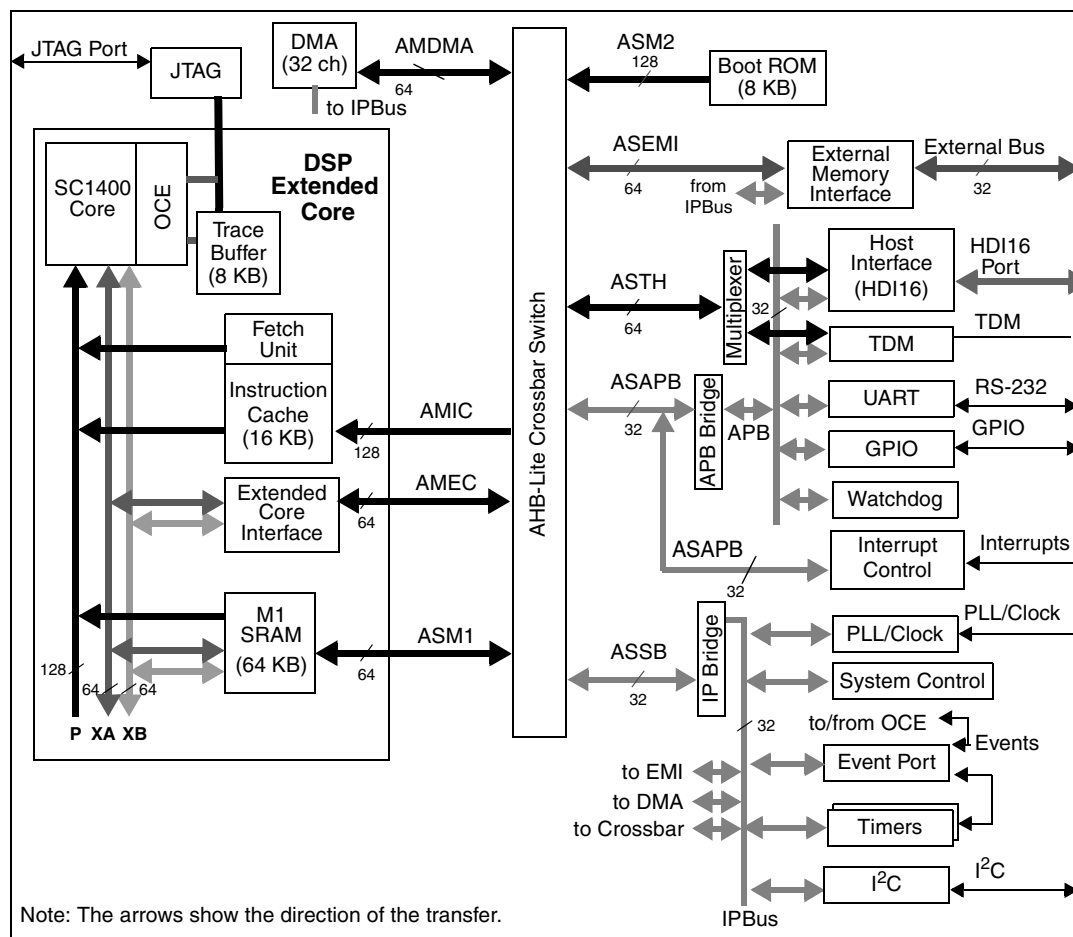# MSC7110

Low-Cost 16-Bit DSP with DDR Controller

The MSC7110 device targets high-bandwidth highly computational DSP applications and is optimized for Enterprise class packet telephony applications, providing a competitive price per channel for voice over packet systems.

Figure 1. MSC7110 Block Diagram

The MSC7110 device is a highly integrated DSP processor that contains the StarCore™ SC1400 core, 64 KB of SRAM memory, a 16 KB ICache, an 8 KB boot ROM, a 128-channel time-division multiplexing (TDM) interface with hardware support for μ/A-law decoding/encoding, a UART, a 32-channel DMA controller, a 16-bit host interface (HDI16) to support an external host processor, a programmable interrupt controller (PIC), an I^2C interface, two 16-bit quad cascadable timers, GPIO signals, and an on-chip emulator (OCE) and event port for enhanced debug capability. The SC1400 core has four ALUs and performs at 1000 DSP million multiply accumulates per second (MMACS) with an internal 266 MHz clock at 1.2 V.

freescale™
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Features

Table 1 lists the features of the Freescale MSC7110 device.

Table 1. MSC7110 Features

Feature	Description
StarCore™ SC1400 Core	• Up to 1000 MMACS using an internal 266 MHz clock at 1.2 V. A multiply-accumulate operation includes a multiply-add instruction with the associated data move and pointer update. • 4 data ALUs. • 16 data registers, 40 bits each. • 27 address registers, 32 bits each. • Hardware support for fractional and integer data types. • Very rich 16-bit wide orthogonal instruction set. • Up to six instructions executed in a single clock cycle. • Variable-length execution set (VLES) that can be optimized for code density and performance. • JTAG port designed to comply with **IEEE**® Std 1149.1™. • On-chip emulator (OCE) module with real-time debugging capabilities.
Extended Core	The high performance extended core delivers up to 1000 MMACS using 4 ALUs running up to 266 MHz, including: • SC1400 core processor. • 64 KB multi-port SRAM (M1) accessed by the SC1400 core with no wait states. • 16 KB, 16-way instruction cache (ICache). • Programmable instruction fetch unit. • Write buffer (4-entry). • Extended core interface module.
Internal Memory	The large internal memory space totals 88 KB: • 64 KB of M1 memory. • 16 KB ICache. • 8 KB boot ROM accessible from the SC1400 core.

External Memory Interface	• DDR memory controller.
	• Glueless interface to 133 MHz DDR-RAM (synchronous and half of internal clock).
	• 14-bit external address bus supporting up to 1 GB.
	• 16- or 32-bit external data bus.
	• Memory controller supports:
	  • Byte enables for 32-bit external data bus.
	  • Data pipeline to reduce data set-up time for synchronous devices.

Crossbar Switch	AHB-Lite crossbar switch, allowing up to four parallel data transfers between four master ports and six slave ports, where each port connects to an AHB-Lite bus.

DMA Controller	Multi-channel DMA controller:
	• Up to 32 time-multiplexed channels.
	• Priority-based time-multiplexing between channels using 32 internal priority levels
	• Priorities can be fixed or round-robin.
	• A flexible channel configuration:
	  • All channels support all features.
	  • All channels connect to the slave ports on the crossbar.

External Interfaces	External interfaces and control modules managed on the advanced peripheral bus (APB) including: • Time-division multiplexing (TDM) module supporting up to 128 channels. • Two 16-bit quad timers. • RS-232 interface/universal asynchronous receiver/transmitter (UART). • I^2C interface. • Up to 37 general-purpose input/output (GPIO) signals. • Interrupt controller to handle external interrupt functions (input and output).

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Table 1. MSC7110 Features (Continued)

Feature	Description
Host Interface (HDI16)	Enhanced 16-bit wide interface provides a glueless connection to industry-standard microcontrollers, microprocessors, and DSPs.
TDM Module	TDM module with the following features: • Totally independent receive and transmit, each having one data line, one clock line, and one frame sync line. • Frame sync line and/or clock line can be shared between receive and transmit. • Glueless interface to E1/T1 frames and MVIP, SCAS, and H.110 buses. • Hardware A-law/μ-law conversion • Up to 50 Mbps (50 MHz bit clock). • Maximum rate is 1/4 the core frequency. • Up to 128 channels. • Each channel can be programmed to be active or inactive. • 8- or 16-bit word widths. • The TDM Sync Signal (TDMxTFS/TDMxRFS) can be configured as either input or output. • The TDM clock signal (TDMxTCK/TDMxRCK) can be configured as either input or output. • Frame sync and data signals can be programmed to be sampled either on the rising edge or on the falling edge of the clock. • Frame sync can be programmed as active low or active high. • Selectable delay (0–3 bits) between the Frame Sync signal and the beginning of the frame. • MSB or LSB first support.
Timers	Two 16-bit quad timers, each with the following features: • Cyclic or one-shot. • Input clock polarity control. • Interrupt request when counting reaches a programmed threshold. • Pulse or level interrupts. • Dynamically updated programmed threshold. • Read counter any time. • Maximum rate is 1/4 the core frequency.
UART	• Two signals for transmit data and receive data. • No clock, asynchronous mode. • Full-duplex operation. • Standard mark/space non-return-to-zero (NRZ) format. • 13-bit baud rate selection. • Programmable 8-bit or 9-bit data format. • Separately enabled transmitter and receiver. • Programmable transmitter output polarity. • Two receiver wake-up methods: • Idle line wake-up. • Address mark wake-up. • Separate receiver and transmitter interrupt requests. • Eight flags, the first five can generate interrupt request: • Transmitter empty. • Transmission complete. • Receiver full. • Idle receiver input. • Receiver overrun. • Noise error. • Framing error. • Parity error. • Receiver framing error detection. • Hardware parity checking. • 1/16 bit-time noise detection. • Maximum bit rate 5.0 Mbps. • Single-wire and loop operations.

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Table 1. MSC7110 Features (Continued)

Feature	Description
I²C Port	• 2-wire serial interface through GPIO. • Filtered inputs for noise suppression. • Compatibility with I²C bus standard up to 100 kbps for standard mode and up to 400 kbps for Fast mode. • Bidirectional Data Transfer Protocol. • Multiple-master operation that also allows any number of devices implementing the I²C-master software module to access the memory simultaneously at boot or any time. • Compatible with the I²C-serial EEPROM access protocol, allowing memory access of up to one MB.
General-Purpose I/O (GPIO) Port	Bidirectional signal lines that either serve the peripherals or act as programmable I/O ports. Each port can be programmed separately to serve up to two dedicated peripherals.
Programmable Interrupt Controller (PIC)	Consolidates maskable interrupt and non-maskable interrupt sources.
System Control	• Reset controller. • Clock controller module. • Hardware bus monitors for the MSC7110 buses. • Software watchdog timer function. • fieldBIST™ hardware health diagnostics that can be invoked at power-up or off-line via software. • Event port.
Internal PLL	Generates up to 266 MHz clock for the SC1400 core and up to 133 MHz for the crossbar switch, DMA channels, M2 memory, and other peripherals.
Clock Synthesis Module	• Programmable low-power Stop and Wait modes. • Generation of all device clocks. • Halt and restart capability for on-chip peripherals.
Reduced Power Dissipation	• Separate power supply for internal logic and I/O. • Typical case power consumption of 300–400 mW • Low-power standby modes. • Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent).
fieldBIST™ Hardware Diagnostics	Detects and provides visibility into unlikely field failures for systems with high availability. The unique fieldBIST ensures that the device: • Has structural integrity. • Operates at the rated speed. • Is free from reliability defects. Diagnostics can report partial or complete device inoperability. fieldBIST resolution can pinpoint the following uniquely: • 6 memory blocks, including ROM • 3 logic levels (top, extended core, and peripherals) • 1 PLL Simple JTAG interface allows easy integration to system firmware.
Packaging	400 ball MAP-BGA. • 17 × 17 mm. • 0.8 mm pitch. • Pb-free or Pb-bearing spheres.

Table 1. MSC7110 Features (Continued)

Feature	Description
Software Support	Real-Time Operating Systems (RTOS) that fully supports MSC7110 device architecture (multi-core, memory hierarchy, ICache, timers, DMA, interrupts, peripherals): • High-performance and deterministic, delivering predictive response time. • Optimized to provide low interrupt latency with high data throughput. • Preemptive and priority-based multitasking. • Fully interrupt/event driven. • Small memory footprint. • Comprehensive set of APIs. • Fully supports MSC7110 DMA, interrupts, and timer schemes. Distributed system support, enables transparent inter-task communications: • Messaging mechanism between tasks using mailboxes and semaphores. • Networking support; data transfer between tasks running inside and outside the device using networking protocols. • Includes integrated device drivers for such peripherals as TDM, UART, and external buses.
	Additional features: • Incorporates task debugging utilities integrated with compilers and vendors. • Board support package (BSP) for MSC7110 ADS.
	CodeWarrior® Integrated Development Environment (IDE): • C/C++ compiler with in-line assembly. Enables the developer to generate highly optimized DSP code. It translates code written in C/C++ into parallel fetch sets and maintains high code density. • Librarian. Enables the user to create libraries for modularity. • C libraries. A collection of C/C++ functions for the developer's use. • Linker. Highly efficient linker to produce executables from object code. • Debugger. Seamlessly integrated real-time, non-intrusive multi-mode debugger that enables debugging of highly optimized DSP algorithms. The developer can choose to debug in source code, assembly code, or mixed mode. • Profiler. An analysis tool using a patented Binary Code Instrumentation (BCI) technique that enables the developer to identify program design inefficiencies.
	Boot options: • HDI16. • I^2C.

MetroWerks Application Development System (ADS) Board	• Host debug through single JTAG connector supports both processors.
	• Big Flash memory for stand-alone applications.
	• Support for the following communications ports:
	  • 10/100Base-T.
	  • T1/E1 TDM interface.
	  • H.110.
	  • Voice codec.
	  • RS-232.
	  • High-density (MICTOR) logic analyzer connectors to monitor MSC7110 signals
	  • 6U cPCI form factor.
	• Emulates MSC7110 DSP farm by connecting to three other ADS boards.

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Product Documentation

The documents listed in **Table 2** are required for a complete description of the MSC7110 device and are necessary to design properly with the part. Documentation is available from a local Freescale distributor, a Freescale semiconductor sales office, or a Freescale Literature Distribution Center. For documentation updates, visit the Freescale DSP website. See the contact information on the back of this document.

Table 2. MSC7110 Documentation

Name	Description	Order Number
MSC7110 Technical Data	MSC7110 features list and physical, electrical, timing, and package specifications	MSC7110
MSC711x Reference Manual	Detailed functional description of memory and peripheral configuration, operation, and register programming	MSC711xRM
SC1000 Family Processor Core Reference Manual	Detailed description of the SC1000 family processor cores, including the SC1400, and instruction set	10180-01 See the StarCore LLC website at www.starcore-dsp.com
Application Notes	Documents describing specific applications or optimized device operation including code examples	See the MSC7110 product website

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