MSC8102 Packet Telephony Farm Card (MSC8102PFC)

The MSC8102 packet telephony farm card (MSC8102PFC) is a PCI telephony mezzanine card (PTMC) for evaluating media gateway products. This card is designed around the StarCore™ MSC8102 16-bit fixed-point DSP device. On the MSC8102PFC is a DSP farm consisting of five MSC8102 devices and one MSC8101 device to aggregate the data to/from the DSP farm. Each MSC8102 device has an associated 4M × 32 (16 MB) SDRAM. The MSC8101 aggregator has a separate 2 M × 32 (8 MB) SDRAM.

The MSC8102PFC interfaces with a baseboard platform via its PTMC site (see **Figure 1**). The PTMC is a PCI Mezzanine Card (PMC) module that conforms to the PMC standard for Jn1 and Jn2 but uses Jn3 and Jn4 to support a variety of telecommunications interfaces. The PTMC site on the media gateway is configured similar to a PT3MC, a subset of the PTMC specification that supports UTOPIA, Ethernet Reduced Media-Independent Interface (RMII), and computer telephony bus interfaces on Jn3/4. An optional fifth connector (Jn5) is added to support the two MII interfaces supported by the MSC8101 device. Jn5 is a proprietary connector, effectively supporting an enhanced PTMC that is backward-compatible with existing PTMCs.

Data transfer on the board occurs primarily through 10/100 Mbps Ethernet (single RMII or dual MII interfaces) or UTOPIA and a computer telephony local bus through the PTMC connectors. Also, an I^2C management interface is implemented through the PTMC J3 connector. Additional I/O interfaces

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include an HDI16, RS-232 port, and EOnCE JTAG TAP for debug. The MSC8102PFC interfaces with Freescale packet telephony enhanced PTMC baseboards such as the PDK demonstration system, as well as with standard customer PTMC type III baseboards.

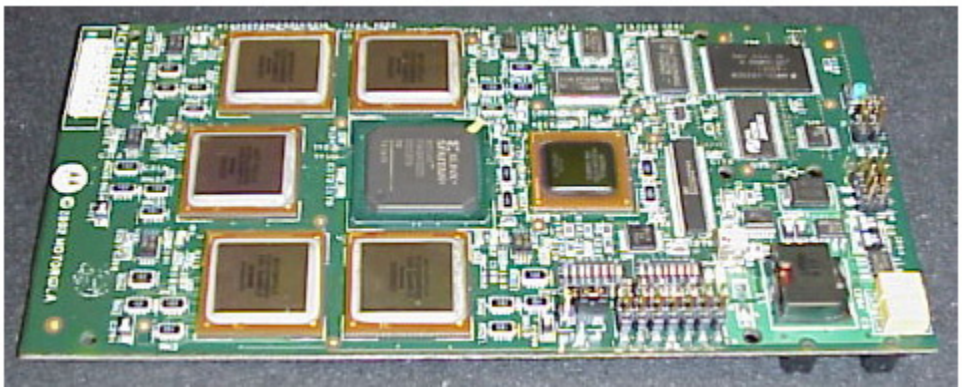


Figure 1. MSC8102 Packet Telephony Farm Card (MSC8102PFC)

Features of the MSC8102PFC are as follows (see **Figure 2**):

- MSC8102PFC platform:
  - Digital support for up to 672 channels
  - PTMC Type 3 form card for interfacing to standard subsystems
- MSC8101 aggregator
  - MSC8101 DSP communications processor with:
  - 10/100BaseT fast Ethernet via PTMC interface
  - RMII Ethernet via PTMC interface
  - UTOPIA interface via PTMC interface
  - Host interface to enable host control of aggregator via the PTMC interface
  - 64-bit/32-bit interface to the MSC8102 DSI port for on-board data distribution to DSP farm
  - RS-232 interface on-board
  - 4 MB of Flash memory for system bootstrap
  - 8 MB SDRAM
- MSC8102 farm consists of five MSC8102 devices, each with the following features:
  - TDM interface (CT Bus) via PTMC interface
  - 64-bit/32-bit DSI Slave port interfacing to the MSC8101 PPC (via FPGA) for data distribution
  - DSI-Asynchronous mode of operation
  - DSI-Synchronous mode of operation
  - 16 MB SDRAM
  - MSC8102 DSP1 has RS-232 interface on board
- FPGA

— PPC-to-DSI translation for synchronous DSI
— Transparent mode for asynchronous DSI
— Routing of MSC8102 to MSC8101 interrupts
— CPORT cluster interface
— MII-to-RMII conversion

- Debug
  — Chained DSP EOnCE port with the option to configure the full five MSC8102 devices and MSC8101 chain or only the MSC8101 DSP.
  — SMC2 RS-232 connection to the MSC8101
  — UART connection to one MSC8102
  — Breakout card access to UTOPIA interfaces via connectors
- Power supply
  — For stand-alone operation, 5 V/3.3 V is supplied externally via a base card with the option to supply 1.6 V externally or via on-board PFC 5 V to 1.6 V step down

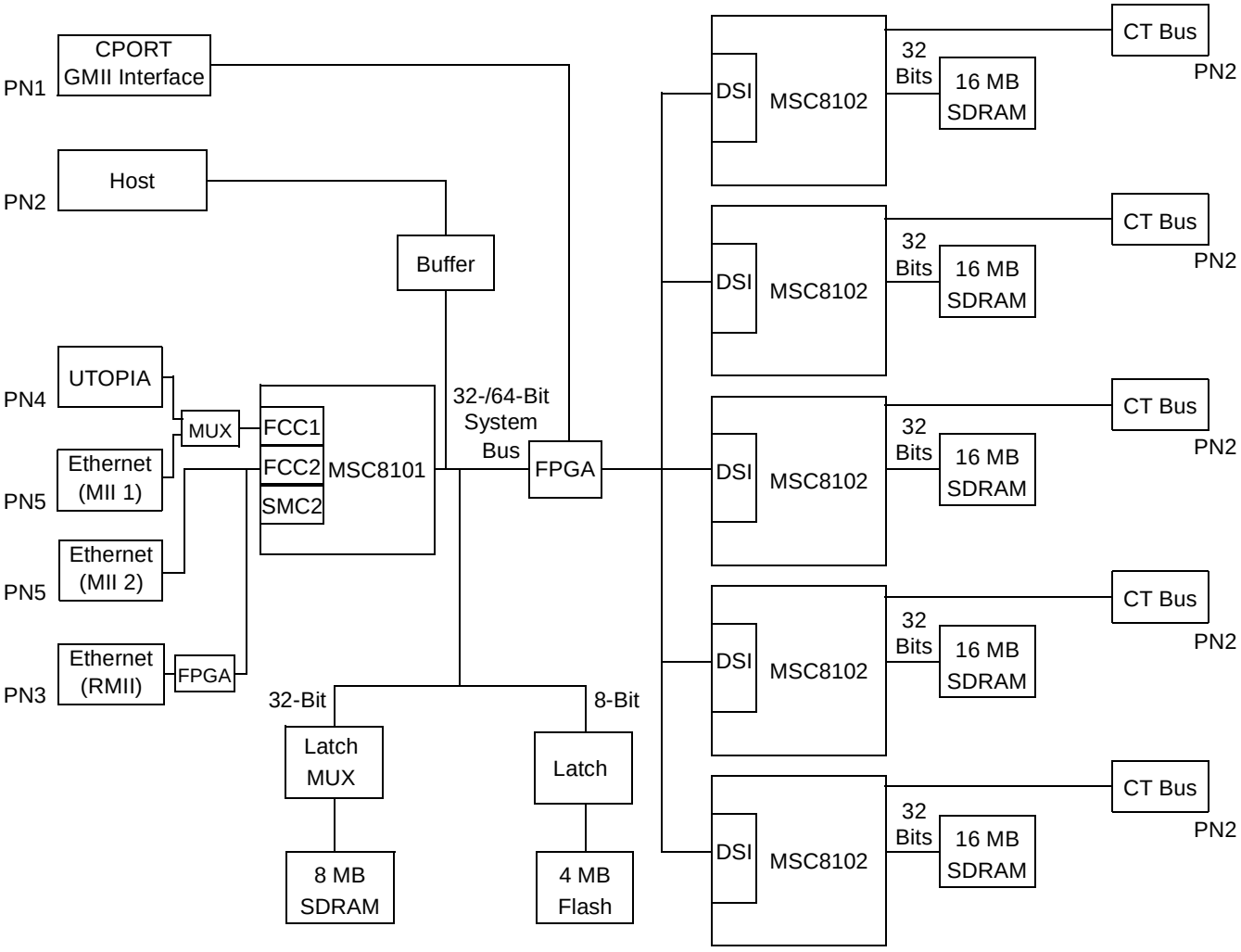


Figure 2. MSC8102PFC Architecture

1 Packet Telephony Development Kit

The Packet Telephony Development kit (PDK) is a platform for evaluating and developing voice-over packet applications. The PDK has an MPC8260 host network processor that runs Linux, StarCore DSP resource cards that run DSP code, and a Public Switched Telephone Network (PSTN) card with interfaces such as E1/T1 and analog telephone lines (see **Figure 3**).

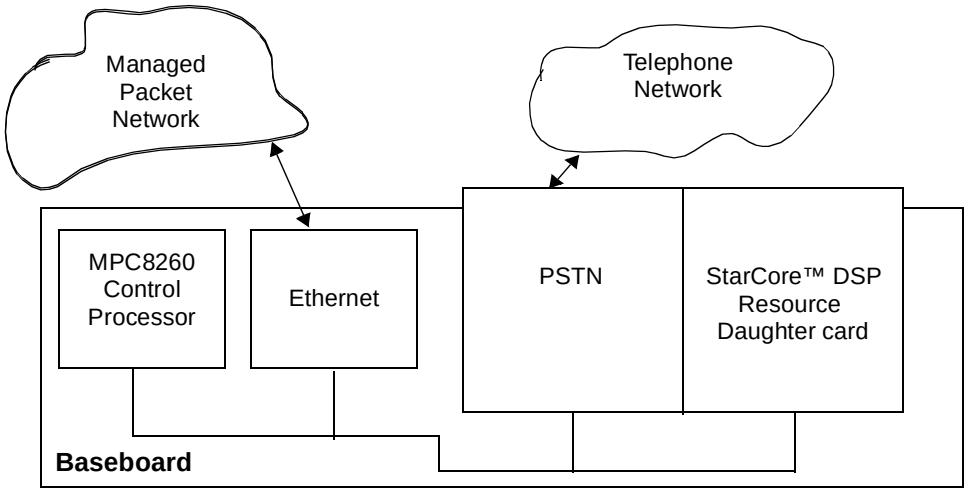


Figure 3. Components of the Packet Telephony Development Kit (PTK)

The documentation for the kit components is listed in **Table 1**. Reference documents for the MSC8102PDC are listed in **Table 3**.

Table 1. PTK Components and Their Associated Documents

Component	Document	Document ID
Baseboard	Packet Development Kit Baseboard Hardware User's Guide	PTKITBASEUG
MPC8260 Control Processor	*MPC8260 PowerQUICC II™ Family Reference Manual* (Available at the web site listed on the back page of this user's guide.)	MPC8260UM
PSTN Card	*Packet Development Kit PSTN Mezzanine User's Guide*	PTKITPSTNUG
StarCore DSP Resource Daughter card	• *MSC8102 Packet Telephony Farm Card (MSC8102PFC) User's Guide* • *MSC8101 Packet Telephony Farm Card (MSC8101PFC) User's Guide*	PTKIT8101UG PTKIT8102UG
MSC8102 Processor	*MSC8102 Reference Manual* and other MSC8102 documentation are located at the web site listed on the back page of this user's guide.	MSC8102RM
Software	*Packet Telephony Development Kit Software User's Guide*	PTKITSOFTUG

CAUTION: *The Packet Telephony Development Kit includes open-construction printed circuit boards that contain static-sensitive components. These boards are subject to damage from electrostatic discharge (ESD). To prevent such damage, you must use static-safe work surfaces and grounding straps, as defined in ANSI/EOS/ESD S6.1 and ANSI/EOS/ESD S4.1. All handling of these boards must be in accordance with ANSI/EAI 625.*

Table 2. Reference Documents

Document	Revision	Date	Document ID
Standard Physical and Environmental layers for PCI Mezzanine Cards: PMC	Draft 2.4	January 12, 2001	IEEE: P1386.1
Standard for a Common Mezzanine Card Family: CMC	Draft 2.4a	March 21, 2001	IEEE: P1386
CompactPCI PCI Telecom Mezzanine Card Specification	R1.0	April 11, 2001	PICMG 2.15
H.100 Hardware Compatibility Specification: CT Bus	1.0		H.100

2 Getting Started With the MSC8102PFC

The procedure for bringing up the MSC8102PFC is as follows:

1. Start the CodeWarrior® tools and ensure that the command converter is running.
2. Place the PFC onto the PDK as shown in **Figure 2**.
3. Ensure that the parallel command converter is connected to P3 on the MSC8102PFC to enable JTAG access, with power connected to JP1 on the PDK.

Figure 4. MSC8102PFC Set-up on the PDK

4. Set the switch settings as shown in **Table 3**, **Table 4**, and **Table 5**:

Table 3. MSC8101 Boot From Flash Memory

Feature	Settings	Comments	
SW3.1	OFF	A_MODCK1 = 1 A_MODCK2 = 1 A_MODCK3 = 0	MODCK 46 [101–110] CLKIN = 34.5 MHz Core/CPM/Bus = 275/138/69 MHz
SW3.2	OFF		
SW3.3	ON		
SW3.4	ON	Boot = 0, Host port disabled; boot from external memory.	
SW3.8	ON	$\overline{\text{RSTCONF}}$ = 0, Reset Configuration Master	

Table 4. MSC8101 Boot Through DSI

Feature	Settings	Comments
SW2.1	OFF	CNFGS = 1 (MSC8102 Boot Over DSI). Keeps MSC8102 devices in reset until the Hardware Reset Configuration Word (HRCW) is received.

Table 4. MSC8101 Boot Through DSI (Continued)

Feature	Settings	Comments	
SW2.2	ON	MODCK2 = 0 MODCK1 = 1	MODCK 10 [010–10] CLKIN = 41.6 MHz Core/Bus = 250/83 MHz
SW2.3	OFF		
SW2.4	ON	DSI64 = 0, DSI is 32 bits	
SW2.5	ON	DSISYNC = 0, DSI operates in asynchronous mode	
SW2.6	ON	SWTE = 0, Software WDT disabled	
SW2.7	ON	$\overline{\text{RSTCONF}}$ = 0 (MSC8102 Boot over DSI). Keeps MSC8102 devices in reset until the HRCW is received.	
SW3.6	OFF	BM2: MSC8102 Boot Sequence through DSI	
SW3.7	ON	BM1	

Table 5. Full Chain (JTAG of 21)

Feature	Setting	Comments
JP1	Pos 1–2	Full chain
SW2.8	ON	Full chain

5. Power up the MSC8102PFC, which automatically bootstraps in the following modes:
   - MSC8101 boot from Flash memory. Operating frequency is 275 MHz Core/138 MHz CPM/69 MHz system bus.
   - MSC8102 boot through 32-bit asynchronous DSI. Operating frequency is 250 MHz core/83 MHz system bus.
   - JTAG of 21 cores.

     Each DSP LED lights after a delay of approximately four seconds (due to FPGA programming) to indicate a successful bootstrap. You can now use the StarCore CodeWarrior® tools to access the DSPs. You should ensure that the JTAG `PFCjtag21.cfg` file is selected. The file listing and core JTAG numbering is detailed in **Appendix A**, *Supporting Information*, on page 41.

2.1 Board Configuration Options

This section outlines the configuration options for the MSC8102PFC.

2.1.1 Single MSC8101 with Default Configuration

To initialize the MSC8101 with its default HRCW, set the switch settings detailed in **Table 6** and **Table 9** (MSC8101 only). This mode allows tools access only to the MSC8101 device (the MSC8102 devices remain in reset) and should be used when the Flash memory is blank or corrupted.

Table 6. MSC8101 Default Hardware Reset Configuration Word

Feature	Settings	Comments	
SW3.1	OFF	A_MODCK1 = 1 A_MODCK2 = 1 A_MODCK3 = 0	MODCK 6 [000–110] CLKIN = 34.5 MHz Core/CPM/Bus = 138/69/34.5 MHz
SW3.2	OFF		
SW3.3	ON		
SW3.4	ON	Boot = 0, Host port disabled; boot from external memory.	

2.1.2 MSC8101 Boot through HDI16

To bootstrap the MSC8102PFC through the MSC8101 HDI16 interface, set the switch settings detailed in **Table 7** and Table 4, “MSC8101 Boot Through DSI,” on page 6.

Table 7. MSC8101 HDI16 Boot

Feature	Setting	Comments	
SW3.1	OFF	A_MODCK1 = 1 A_MODCK2 = 1 A_MODCK3 = 0	MODCK 46 [101–110] CLKIN = 34.5 MHz Core/CPM/Bus = 275/138/69 MHz
SW3.2	OFF		
SW3.3	ON		
SW3.4	OFF	Boot = 1, Host port enabled; boot from HDI16.	
SW3.8	OFF	$\overline{\text{RSTCONF}}$ = 1, Reset Configuration Slave	

2.1.3 MSC8101 Ethernet/UTOPIA Options

Switch SW3.5 can be used to select the required MSC8101 CPM options, as shown in **Table 8**.

Table 8. MSC8101 Ethernet/UTOPIA Options

Feature	Setting	Comments	
SW3.5	ON	FCC1 UTOPIA	FCC2 Ethernet (MII2)
SW3.5	OFF	FCC1 Ethernet (MII1)	FCC2 Ethernet (MII2)

2.1.4 MSC8102 DSI Options

The MSC8102 DSI port can be configured into one of the following modes:

- 32-bit wide Asynchronous mode
- 64-bit wide Asynchronous mode
- 32-bit wide Synchronous mode
- 64-bit wide Synchronous mode

The MSC8102PFC is delivered with 32-bit wide Asynchronous mode as the standard, which is preprogrammed in Flash memory. To implement a different mode, contact Freescale Semiconductor, Inc. to obtain the required firmware.

2.1.5 JTAG Options

Two JTAG options are available as detailed in **Table 9**. The JTAG configuration file for 21 cores is listed in **Appendix A**, *Supporting Information*, on page 41.

Table 9. JTAG Options

Description	Feature	Setting
MSC8101 only	JP1	Pos 2–3
	SW2.8	OFF
Full chain (21 cores)	JP1	Pos 1–2
	SW2.8	ON

2.2 Flash Memory Programming

The MSC8102PFC uses the same Flash memory (AM29LV320DB) as the MSC8102ADS, so you can use either the Metrowerks CodeWarrior or PFC-specific Flash programmer. Consult Freescale Semiconductor, Inc. for additional details on programming Flash memory.

3 MSC8102PFC Hardware Components

The MSC8102PFC hardware architecture consists of the MSC8101 aggregator, DSP processing array of MSC8102 devices, general board configuration, firmware, and PFC base card.

3.1 MSC8101 Aggregator

Under typical operating conditions, the MSC8101 is used to terminate ATM or 10/100BaseT Ethernet packet traffic from a host card via its PTMC interface. The subsequent data is placed into the MSC8101 internal SRAM or external SDRAM. The data is then distributed to the MSC8102 farm for processing via the MSC8102 DSI port, and the FPGA performs the system bus-to-DSI translation.[1] After MSC8102 processing, the data is dispatched through the MSC8102 TDM interfaces to the PTMC CT bus.

3.1.1 MSC8101 System Bus Interface

The aggregator terminates the packet protocol and transfers media data to and from the DSP array through its system bus. The system bus interface to the MSC8102 DSI can be configured as 32 or 64 bits wide. For 32-bit operations, an external host can access the host port (HDI16) of the MSC8101 aggregator for bootstrap and ongoing data exchange and control. 4 MB of 8-bit wide Flash memory is connected to the MSC8101 system bus for configuration, boot, and execution code (for all 6 DSP devices). 8 MB of 32-bit wide SDRAM also connects to the MSC8101 system bus to provide adequate storage during real-time operation. The address bus is latched to the SDRAM and Flash memories because of the 60x-compatible mode used in DSI Synchronous mode. The data bus is not buffered to the memories and FPGA but buffered for the HDI16 port. The SDRAM is not required for normal aggregation functions and is included purely for maximum flexibility. **Table 10** details the MSC8101chip selects used for the system bus devices.

Table 10. MSC8101 Memory Controller Resources

Chip Select	Peripheral
$\overline{CS0}$	Flash memory (boot)
$\overline{CS2}$	SDRAM
$\overline{CS3}$	DSI Asynchronous (individual chip selects)
$\overline{CS4}$	DSI Asynchronous (Broadcast mode)

3.1.2 MSC8101 SDRAM Interface

The aggregator system bus incorporates a 64 M-bit × 32-bit wide × 4 bank Micron MT48LC2M32B2 SDRAM surface mounted onto the board to provide 8 MB of general-purpose system RAM. The MSC8101 Chip Select 2 is used to select the SDRAM devices through the SDRAM controller, which can interface to JEDEC-compatible SDRAM:

1. The FPGA is incorporated to allow synchronous DSI transfers. It is not required for asynchronous DSI transfers.

- SDRAM size is 512 KB × 32 × 4 banks = 8 MB, which requires 23 address lines.
- Device has 8 column and 11 row lines and 2 bank selects. The 32-bit port size means that addresses 30 and 31 are not used.

For page-based interleaving, the system bus is arranged as shown in **Table 11**.

Table 11. Page-Based Interleaving and the System Bus

A[0–8]	A[9–19]	A[20–21]	A[22–29]	A[30–31]
MSB of Start Address	Row (x11)	Bank Select	Column (x8)	LSB

Page-based interleaving requires the following MSC8101 register settings:

- PSDMR[PBI] = 1, page-based interleaving
- ORx[BPD] = 01, four banks per device
- ORx[ROWST] = 1001, row starts at A9
- ORx[NUMR] = 010, SDRAM has 11 row lines

While an ACTIVATE command executes, the SDRAM address port appears as shown in **Table 12**.

Table 12. SDRAM Address Port

A[0–16]	A[17–18]	A[19–29]	A[30–31]
—	Internal Bank Select (A[20–21])	Row (A[9–19])	LSB

A read/write appears as shown in **Table 13**.

Table 13. Read/Write

A[0–16]	A[17–18]	A[19–21]	A[22–29]	A[30–31]
—	Internal Bank Select (A[20–21])	Don’t care	Column (A[22–29])	LSB

The register settings are as follows:

- PSDMR[SDAM] = 010, A[9–19] multiplexed to A[19–29].
- PSMDR[BSMA] = 100, A[17–18] are used as bank select signals.
- PSMDR[SDA10] = 001, A9 maps to the A10/AP pin.

The full PSDMR settings are described in **Table 14**.

Table 14. MSC8101 PSDMR Settings

PSDMR Setting	Description
PBI = 1	Page-based interleaving
RFEN = 1	Refresh services required
OP = 000	Normal operation
SDAM = 010	A[9–19] multiplexed to A[19–29]

Table 14. MSC8101 PSDMR Settings

PSDMR Setting	Description
BSMA = 100	A[17–18] are used as bank select signals
SDA10 = 001	A9 maps to the A10/AP pin
RFRC = 110	Eight clock cycles of refresh recovery
PRETOACT = 011	Precharge to activate a 3-cycle interval
ACTTORW= 011	Activate to read/write 3 clock cycles
BL 23 = 1	Burst Length is 8
LDOTOPRE = 10	Precharge can be set two cycles before last data is read from SDRAM
WRC = 10	Precharge is set two cycles after the last data is written to SDRAM
EAMUX = 0	External address multiplexing is switched off for fastest timing
BUFCMD = 0	Normal timing for the control lines
CL = 11	Cycle $\overline{\text{CAS}}$ Latency = 3
PSDMR = 0xC28737A3: MSC8101 SDRAM	

These SDRAM settings are conservative and can be optimized for future configurations and bus frequencies. The OR and BR settings are described in **Table 15**.

Table 15. MSC8101 BR and OR Settings

Register Setting	Description
BA = 0x2000_0	Base Address = 0x20000000
PS = 11	32-bit port size
MSEL = 010	SDRAM machine
BR = 0x20001841	
SDAM= 1111 1111 1000	
LSDAM = 0000 0	8 MB SDRAM
BPD = 01	Four banks per device
ROWST = 1001	Row starts at A9
NUMR = 010	SDRAM has 11 row lines
PMSEL = 0	Back-to-back page mode (Normal operation)
IBID= 1	Bank interleaving disabled
OR = 0xFF803290	

After power-on, a JEDEC standard initialization sequence is performed to configure the SDRAM. Software uses the SDRAM controller PSDMR to perform this task, as follows:

1. Apply power and start the clock. Maintain a No Operation (NOP) condition at the inputs.
2. Maintain stable power, stable clock, and NOP input conditions at the inputs.
3. Issue a Precharge All command (PALL) to all banks of the device. Program the PSDMR[OP] bits to a value of 0b101 and then perform an access to the SDRAM bank.
4. Issue eight or more CBR Refresh (REF) commands. Program the PSDMR[OP] bits to a value of 0b001 and then perform eight accesses to the SDRAM bank.

5. Issue a Mode Register Set (MRS) command to initialize the mode register. Program the PSDMR[OP] bits to a value of 0b011 and then perform an access to the SDRAM bank at an address offset to 0x0CC as shown in **Figure 5**.

	A10/AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		
SDRAM Address Lines	RSVD	WB	Op Mode		CAS Latency			BT	Burst Length				
	0	0	0	0	0	1	1	0	0	1	1		
MSC8101 Address Lines	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31
	0	0	0	0	0	1	1	0	0	1	1	0	0
	Legend:		SDRAM views only this part of the bus.									NC	

BL = Burst Length 8 for 32-Bit Bus.
BT = 0 Sequential Bursts
CAS Latency = 2
Op Mode = Standard Operation
WB = 0 Programmed Burst Length

Figure 5. MSC8101 SDRAM Mode Register Settings

The SDRAM requires 4096 refresh cycles per 64 ms or one refresh cycle per 15.625 µs. The MSC8101 device can be programmed to carry out the refresh *cycle periodi*cally using the SDRAM Refresh Timer (PSRT). Setting the Memory Refresh Timer Prescaler Register MPTPR[PTP] bits to divide by 32 and the PSRT to a value of 0x30 gives a timer period of 15.625 µs for a 100 MHz system clock. For a 69 MHz system clock, PSRT = 0x17. The refresh calculations are as follows:

$$PSRT = F_{MPTC} \times TimerPeriod$$

$$PSRT = \frac{100\ MHz}{32} \times 15.625\ \mu s - 1$$

$$PSRT = 0x30$$

$$PSRT = F_{MPTC} \times TimerPeriod$$

$$PSRT = \frac{69\ MHz}{32} \times 15.625\ \mu s - 1$$

$$PSRT = 0x20$$

3.1.3 MSC8101 Flash Memory Interface

The aggregator incorporates an AM29LV320DB-120E 4Mx 8-bit Flash memory for stand-alone reset configuration and boot. To enable bootstrapping from reset, the Flash memory is mapped to GPCM $\overline{CS0}$ and uses the signals shown in **Table 16**.

Table 16. MSC8102 DSI Addresses

MSC8102	GPCM Signal
A_CS_FLASH	$\overline{CS0}$
A_PSDRAS	$\overline{POE}$
A_PSDDQMO	$\overline{WE}$

Table 16. MSC8102 DSI Addresses

MSC8102	GPCM Signal
A_BADDR[27–30]	A[3–0]
A_BADDR[31]	A–1

On the Flash memory, the BYTE signal is pulled down for byte mode, which enables DQ[0–7] but tri-states DQ[8–14]. DDQ15/A-1 is used as an input for the LSB address bit, A_BADDR31. The memory controller uses the BADDR[27–31] signals to interface to the memories in Multi-Master mode.

3.1.4 MSC8101 System Bus-to-DSI Interface

The system bus-DSI interface is the main means of communication between the aggregator and the DSP array. The DSI interface can be either 32 or 64 bits wide and operates in Synchronous or Asynchronous modes:

- *Synchronous mode*. This SSRAM-like interface enables host single or burst accesses of 256 bits (8 accesses of 32 bits or 4 accesses of 64 bits) with its external clock decoupled from the MSC8102 internal bus clock. Data is transferred onto the external system bus to be handled by the FPGA.
- *Asynchronous mode*. This SRAM-like interface enables host single accesses with no external clock. Data is transferred via the MSC8101 memory controller user-programmable machine (UPM).

  The DSI gives external hosts direct access to the MSC8102 internal memory space, including internal memories and the registers of the internal modules. The DSI write buffer stores the address and the data of the accesses until they are performed. The external host can therefore perform multiple writes without waiting for those accesses to complete. The DSI read prefetch mechanism greatly reduces latencies that are typical during accesses to internal memories. The host addresses each MSC8102 device using a single chip select; the most significant bits on the address bus identify the addressed MSC8102 device. The 4-bit MSC8102 DSI address is hardwired via CHIP_ID[0–3], as shown in **Table 17**.

Table 17. MSC8102 DSI Addresses

MSC8102	CHIP_ID[0–3]
1	0b0000
2	ob0001
3	0b0010
4	ob0011
5	0b0100

The host can also write the same data to multiple MSC8102 devices simultaneously by asserting a dedicated broadcast chip select. In Synchronous mode, an FPGA is required to interface between the MSC8101 system bus and the MSC8102 DSI port. The connectivity is detailed in **Figure 6**.

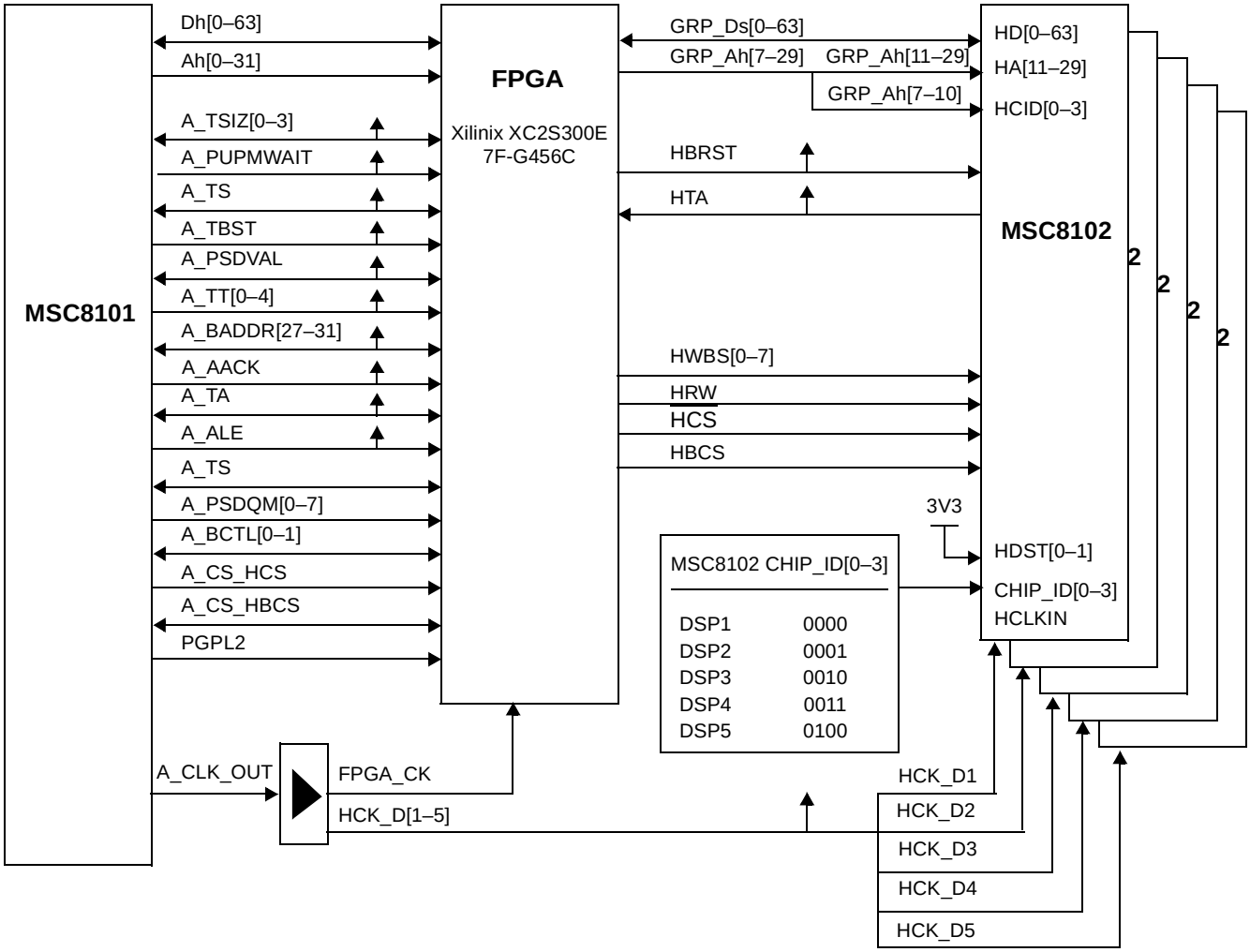


Figure 6. PFC-to-DSI Interface

The DSI can be asynchronously controlled via the UPM signals shown in **Table 18**. These signals are routed through the FPGA, which operates in transparent mode.

Table 18. DSI Asynchronous Signals

UPM Signal	Description
$\overline{\text{CS3}}$	Broadcast chip select
$\overline{\text{CS4}}$	Chip select
PBS[0–7]	Byte strobe
PGPL2	General-purpose
PGPL4/UPMWAIT	UPMWAIT

3.1.5 MSC8101-to-MSC8102 Interrupt Connectivity

The FPGA routes the interrupts/GPIO lines between the MSC8101 and MSC8102 devices. For flexibility, the MSC8101 has five GPIO lines (PC4, PC5, PC24, PC25, and PC30) that are connected to the FPGA and in turn receives seven $\overline{\text{IRQ}}$ inputs from the FPGA. The GPIO30 and INT_OUT of each MSC8102 device is connected to the FPGA, with their respective $\overline{\text{IRQ1}}$ and $\overline{\text{IRQ2}}$ also connected, as shown in **Figure 7**. The standard preprogrammed FPGA interrupt routing is shown in **Figure 8**.

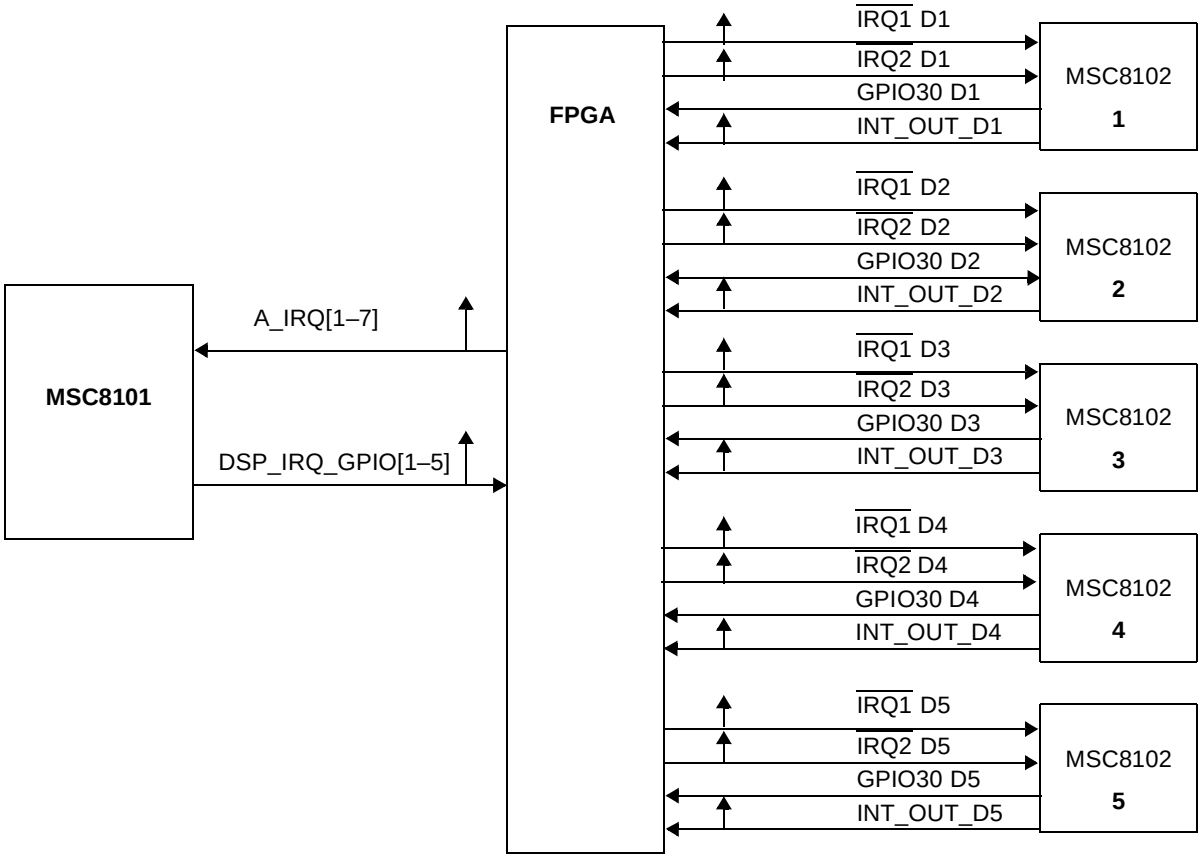


Figure 7. MSC8101-to-MSC8102 Interrupt Connectivity Options

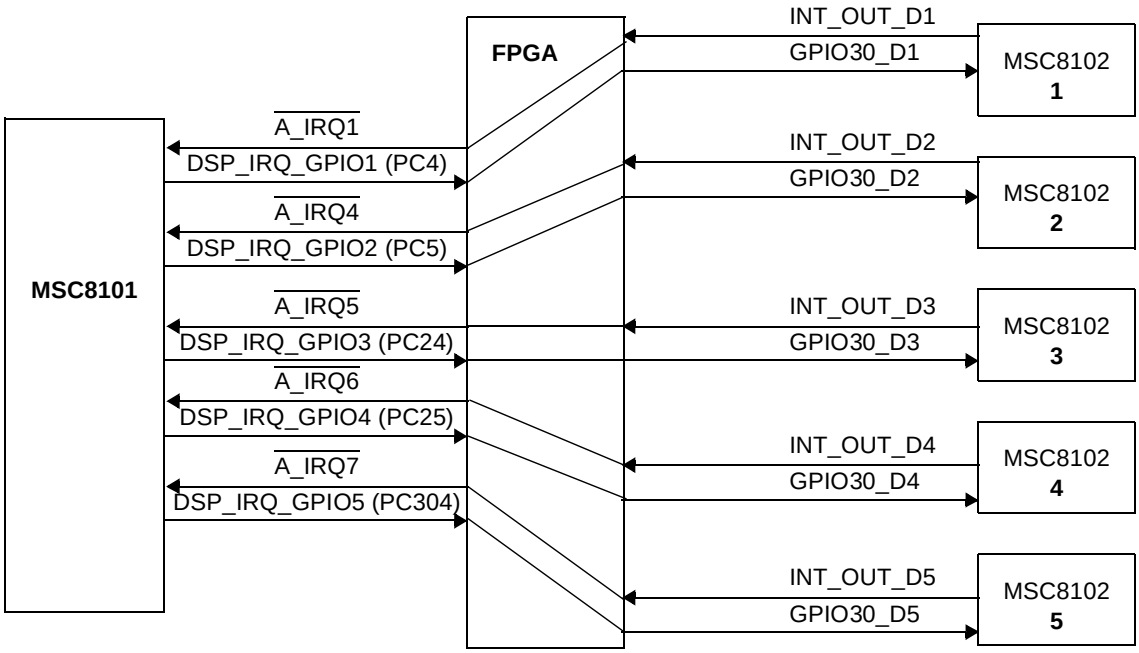


Figure 8. Standard Interrupt Routing

3.1.6 MSC8101 FCC Interface

The MSC8101 device has two FCC interfaces for packet transfers. The packet interfaces are configurable to perform 2 × MII ports (FCC1 and FCC2) or an MII (FCC1) plus a UTOPIA (FCC2) port. Both configurations are routed to the PTMC connector as detailed in **Table 19**. Signals common to UTOPIA FCC1 and MII FCC1 are routed to their connector positions via a PERICOM P13B16233 bus switch.

Table 19. FCC1 Interface

Pin	Signal	Connects to
PA10	UTOPIA II RxD0	Pn4-60
PA11	UTOPIA II RxD1	Pn4-58
PA12	UTOPIA II RxD2	Pn4-54
PA13	UTOPIA II RxD3	Pn4-52
PA14	UTOPIA II Rx4/MII1 RxD3	Pn4-48/Pn5-54
PA15	UTOPIA II Rx5/MII1 RxD2	Pn4-46/Pn5-50
PA16	UTOPIA II Rx6/MII1 RxD1	Pn4-42/Pn5-48
PA17	UTOPIA II Rx7/MII1 RxD0	Pn4-40/Pn5-46
PA18	UTOPIA II Tx7/MII1 TxD0	Pn4-35/Pn5-41
PA19	UTOPIA II Tx6/MII1 TxD1	Pn4-37/Pn5-43
PA20	UTOPIA II Tx5/MII1 TxD2	Pn4-47/Pn5-45
PA21	UTOPIA II Tx4/MII1 TxD3	Pn4-49/Pn5-47
PA22	UTOPIA II Tx3	Pn4-53
PA23	UTOPIA II Tx2	Pn4-55
PA24	UTOPIA II Tx1	Pn4-59
PA25	UTOPIA II Tx0	Pn4-61

Table 19. FCC1 Interface (Continued)

Pin	Signal	Connects to
PA26	UTOPIA II RxCLAV/MII1 RX_ER	Pn4-18/Pn5-56
PA27	UTOPIA II RxSOC/MII1 RX_DV	Pn4-49/Pn5-64
PA28	UTOPIA II RXENB/MII1 TX_EN	Pn4-16/Pn5-53
PA29	UTOPIA II TXSOC/MII1 TX_ER	Pn4-1/Pn5-55
PA30	UTOPIA II TXCLAV/MII1 CRS	Pn4-5/Pn5-58
PA31	UTOPIA II TXENB/MII1 COL	Pn4-49/Pn5-22
PC6	UTOPIA II RXADDR2	Pn4-24
PC7	UTOPIA II TXADDR2	Pn4-19
PC12	UTOPIA II RXADDR1	Pn4-30
PC13	UTOPIA II TXADDR	Pn4-28
PC14	UTOPIA II RXADDR0	Pn4-34
PC15	UTOPIA II TXADDR0	Pn4-29
PC30	UTOPIA II TXCLK/MII1 TCLK	Pn4-2 /Pn5-64
PC31	UTOPIA II RXCLK/MII1 RCLK	Pn4-43/Pn5-60
PD7	UTOPIA II TXADDR3	Pn4-17
PD16	UTOPIA II TXPRTY	Pn4-31
PD17	UTOPIA II RXPRTY	Pn4-36
PD18	UTOPIA II RXADDR4	Pn4-4
PD19	UTOPIA II TXADDR4	Pn4-6
PD29	UTOPIA II RXADDR3	Pn4-7

Table 20. MSC8101 Aggregator FCC2 PTMC Connectivity

Pin	Signal	Connects to
PB18	MII2 RXD3	Pn5-34
PB19	MII2 RXD2	Pn5-30
PB20	MII2 RXD1	Pn5-28
PB21	MII2 RXD0	Pn5-26
PB22	MII2 TXD0	Pn5-21
PB23	MII2 TXD1	Pn5-23
PB24	MII2 TXD2	Pn5-25
PB25	MII2 TXD3	Pn5-27
PB26	MII2 CRS	Pn5-38
PB27	MII2 COL	Pn5-37
PB28	MII2 RX_ER	Pn5-36
PB29	MII2 TX_EN	Pn5-33
PB30	MII2 RX_DV	Pn5-24
PB31	MII2 TX_ER	Pn5-35

3.1.7 MSC8101 RMII Interface

The MSC8101 FCC2 signals are routed to the FPGA to allow conversion of the FCC2 MII interface to a reduced media-independent interface (RMII), giving a connection to the PTMC type III RMII port on connector PN3.

3.1.8 MSC8101 I^2C Controller

An I^2C controller is on the MSC8101 device via the J14 pin 57 (SDA) and the J14 pin 9 (SCL). An optional standard PTMC I^2C (via 0 ohm resistors) is available on Jn1 pin 41 [SCL] and pin 42 (SDA).

3.1.9 MSC8101 RS-232 Interface

A simple RS-232 universal asynchronous receiver/transmitter (UART) through the MSC8101 serial management channel interface (SMC2) gives programmable debug or communications capability. A Maxim MAX3241 provides the level conversion for the interface.

3.1.10 MSC8101 Host Interface (HDI16)

The 16-bit host port on the MSC8101 can be used for bootstrapping and ongoing data and control flow from a host processor. The port connects to PTMC connector PN2 via an IDTQ34XV245Q3 bus switch controlled by the host PTENB signal. By default, this switch is open to isolate any host data signals. A host processor should access the MSC8101 aggregator as shown in **Table 21**. When the host port is used, the DSI interface must be configured for 32-bits.

Table 21. HDI16 Configuration

System Bus Signal	HDI16 Signal	Description
Dh57	HDSP = 0	Single data strobe mode
Dh58	HDDS = 0	Negative data strobe polarity
Dh59	H8BIT = 0	16-bit mode enabled
Dh60	HCS2 = 1	Not used, pulled high

3.2 MSC8102 DSP Processing Array

The DSP processing array contains five MSC8102 DSP devices connected to the MSC8101 via a shared DSI to system bus interface. Each DSP device has access to 16 MB of SDRAM. The DSP devices interface to the PSTN through the PTMC connector via their TDM links. In addition, MSC8102 DSP1 (U19) has an SMC UART connection to an on-board connector.

3.2.1 DSP Array SDRAM Configuration

Each DSP incorporates a 128 M-bit × 32 bits wide × 4 bank Micron MT48LC4M32B2 SDRAM surface mounted onto the board providing 16 MB of general-purpose system RAM. The MSC8102 chip select 2 selects the SDRAM devices through the SDRAM controller, which can interface to JEDEC-compatible SDRAM. SDRAM settings are as follows:

- SDRAM size is 1 M × 32 × 4 Banks = 16 MB, which requires 24 address lines.
- 8 column and 12 row lines as well as 2 bank selects. The 32-bit port size means that addresses 30 and 31 are not used.

For page-based interleaving, the system bus is arranged as shown in **Table 22**.

Table 22. Page-Based Interleaving and the System Bus

A[0–7]	A[8–19]	A[20–21]	A[22–29]	A[30–31]
MSB of Start Address	Row (x12)	Bank Select	Column (x8)	LSB

Page-based interleaving requires the following MSC8101 register settings:

- PSDMR[PBI] = 1, page-based interleaving
- ORx[BPD] = 01, four banks per device
- ORx[ROWST] = 1000, row starts at A8
- ORx[NUMR]= 011, SDRAM has 12 row lines

While an ACTIVATE command executes, the SDRAM address port appears as shown in **Table 23**.

Table 23. SDRAM Address Port

A[0–15]	A[16–17]	A[18–29]	A[30–31]
—	Internal Bank Select (A[20–21])	Row (A[8–19])	LSB

A read/write appears as shown in **Table 24**.

Table 24. Read/Write

A[0–15]	A[16–17]	A[18–21]	A[22–29]	A[30–31]
—	Internal Bank Select (A[20–21])	Don’t care	Column (A[22–29])	LSB

Read/write accesses require the following register settings:

- PSDMR[SDAM] = 010, A[9–19] multiplexed to A[19–29].
- PSMDR[BSMA] = 011, A[16–17] are used as bank selects signals.
- PSMDR[SDA10] = 001, A9 maps to the A10/AP pin.

The full PSDMR settings are described in **Table 25**.

Table 25. MSC8102 PSDMR Settings

PSDMR Setting	Description
PBI = 1	Page-based interleaving
RFEN = 1	Refresh services required
OP = 000	Normal operation
SDAM = 010	A[9–19] multiplexed to A[19–29]
BSMA = 011	A[16–17] are used as bank select signals
SDA10 = 001	A9 maps to the A10/AP pin
RFRC = 110	Eight clock cycles of refresh recovery

Table 25. MSC8102 PSDMR Settings (Continued)

PSDMR Setting	Description
PRETOACT = 011	Precharge to activate a 3-cycle interval
ACTTORW= 011	Activate to read/write 3 clock cycles
BL 23 = 1	Burst Length is 8
LDOTOPRE = 10	Precharge can be set two cycles before last data is read from SDRAM
WRC = 10	Precharge is set two cycles after the last data is written to SDRAM
EAMUX = 0	No external address multiplexing
BUFCMD = 0	Normal timing for the control lines
CL = 11	Cycle $\overline{\text{CAS}}$ Latency = 3
PSDMR = 0xC26737A3: MSC8102 SDRAM	

These SDRAM settings are conservative and can be optimized for future configurations and bus frequencies. **Table 26** shows the BR and OR settings.

Table 26. MSC8102 BR and OR Settings

Register Setting	Description
BA = 0x2000_0	Base Address = 0x20000000
PS = 11	32-bit port size
MSEL = 010	SDRAM machine
BR = 0x20001841	
SDAM= 1111 1111 0000	
LSDAM = 0000 0	16 MB SDRAM
BPD = 01	Four banks per device
ROWST = 1000	Row starts at A8
NUMR = 011	SDRAM has 12 row lines
PMSEL = 0	Back-to-back page mode (Normal operation)
IBID= 1	Bank interleaving disabled
OR = 0xFF0030D0	

After power-on, software performs a JEDEC-standard initialization sequence to configure the SDRAM using the SDRAM controller PSDMR. The SDRAM initialization command sequence proceeds as follows:

1. Apply power and start the clock. Maintain a No Operation (NOP) condition at the inputs.
2. Maintain stable power, a stable clock, and NOP input conditions at the inputs.
3. Issue a Precharge All command (PALL) to all banks of the device. Program the PSDMR[OP] bits to a value of 0b101 and then perform an access to the SDRAM bank.
4. Issue eight or more CBR Refresh (REF) commands. Program the PSDMR[OP] bits to a value of 001 and then perform eight accesses to the SDRAM bank.
5. Issue a Mode Register Set (MRS) command to initialize the mode register. Program the PSDMR[OP] bits to a value of 0b011 and then access the SDRAM bank at an address offset to 0x0CC. See **Figure 9**.

	A10/AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		
SDRAM Address Lines	RSVD	WB	Op Mode		CAS Latency			BT	Burst Length				
	0	0	0	0	0	1	1	0	0	1	1		
MSC8101 Address Lines	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31
	0	0	0	0	0	1	1	0	0	1	1	0	0
	SDRAM views only this part of the bus.											NC	

Legend:

BL = Burst Length 8 for 32-Bit Bus.
BT = 0 Sequential Bursts
CAS Latency = 2
Op Mode = Standard Operation
WB = 0 Programmed Burst Length

Figure 9. SDRAM Mode Register Settings

The SDRAM requires 4096 refresh cycles per 64 ms or one refresh cycle per 15.625 µs. The MSC8101 can be programmed to perform the refresh cycle periodically using the SDRAM Refresh Timer (PSRT). Setting the memory refresh timer prescaler register, MPTPR[PTP] to divide by 32 and the PSRT to 0x30 gives a timer period of 15.625 µs for a 100 MHz system clock. For an 83MHz system clock, PSRT = 0x17. The refresh calculations are as follows:

$$PSRT = F_{MPTC} \times TimerPeriod$$

$$PSRT = \frac{100\ MHz}{32} \times 15.625\ \mu s - 1$$

$$PSRT = 0x30$$

$$PSRT = F_{MPTC} \times TimerPeriod$$

$$PSRT = \frac{83\ MHz}{32} \times 15.625\ \mu s - 1$$

$$PSRT = 0x27$$

3.2.2 MSC8102 DSI Interface

The MSC8102 DSI interface is the main means of packet media transfers to and from the DSP array. The DSI is configured for either 32- or 64-bit modes of operation via Dip Switch SW2.

3.2.3 MSC8102 TDM Interface

The CT bus is split into 32 streams of 128 time slots each, giving 4096 timeslots. Each MSC8102 TDM link is unidirectional, so two CT Streams are required to interface with the MSC8102 TDM.The P3TMC specification further restricts the number of CT lines to 20 streams. Each MSC8102 has four TDM interfaces. **Figure 10** shows how the TDM streams are routed.

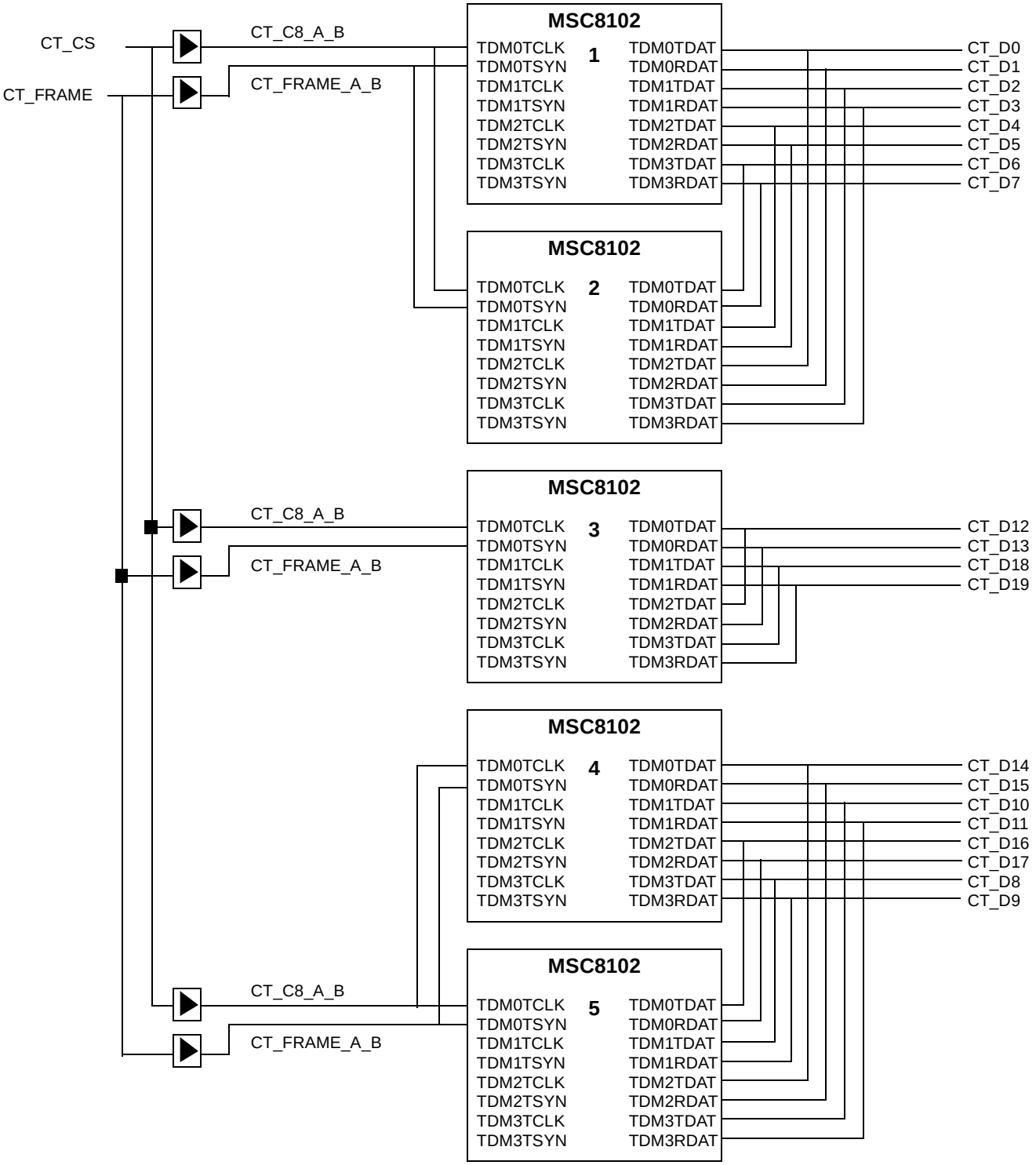


Figure 10. Routing of TDM Streams

Table 27. TDM to CT Routing

MSC8102	TDM	MSC8102 Signal	CT Stream Signal
MSC8102 Device **1**	TDM0	TDM0TDAT TDM0RDAT	CT_D0 CT_D1
	TDM1	TDM1TDAT TDM1RDAT	CT_D2 CT_D3
	TDM2	TDM2TDAT TDM2RDAT	CT_D4 CT_D5
	TDM3	TDM3TDAT TDM3RDAT	CT_D6 CT_D7
MSC8102 Device **2**	TDM0	TDM0TDAT TDM0RDAT	CT_D6 CT_D7
	TDM1	TDM1TDAT TDM1RDAT	CT_D4 CT_D5
	TDM2	TDM2TDAT TDM2RDAT	CT_D0 CT_D1
	TDM3	TDM3TDAT TDM3RDAT	CT_D2 CT_D3
MSC8102 Device **3**	TDM0	TDM0TDAT TDM0RDAT	CT_D12 CT_D13
	TDM1	TDM1TDAT TDM1RDAT	CT_D18 CT_D19
	TDM2	TDM2TDAT TDM2RDAT	CT_D12 CT_D13
	TDM3	TDM3TDAT TDM3RDAT	CT_D18 CT_D19
MSC8102 Device **4**	TDM0	TDM0TDAT TDM0RDAT	CT_D14 CT_D15
	TDM1	TDM1TDAT TDM1RDAT	CT_D10 CT_D11
	TDM2	TDM2TDAT TDM2RDAT	CT_D16 CT_D17
	TDM3	TDM3TDAT TDM3RDAT	CT_D8 CT_D9
MSC8102 Device **5**	TDM0	TDM0TDAT TDM0RDAT	CT_D16 CT_D17
	TDM1	TDM1TDAT TDM1RDAT	CT_D8 CT_D9
	TDM2	TDM2TDAT TDM2RDAT	CT_D14 CT_D15
	TDM3	TDM3TDAT TDM3RDAT	CT_D10 CT_D11

The MSC8102 devices are configured in a four-pin set-up with common clock and frame syncs for receive and transmit. The clock and frame sync signals routed from the PTMC CT bus are CT_8_A and CT_FRAME_A, respectively.

3.2.4 MSC8102 RS-232 Interface

A simple RS-232 UART through the MSC8102 serial communications interface (SCI) gives programmable debug or communications capability. A Maxim MAX3232CUE provides the level conversion for the interface. The receiver inputs are pulled low internally, and the transmitter inputs have external pull-ups.

3.3 General Board Configuration

The general board configuration involves reset, clock distribution, power, the FPGA, the PTMC connectors on the media gateway platform, and JTAG connectivity.

3.3.1 Reset

As **Figure 11** shows, the MAXIM MAX6828 generates the primary reset for the MSC8102PFC ($\overline{\text{PORESET}}$), which is supplied to the MSC8101 and MSC8102 devices[1], FPGA, and Flash memory. The open-drain output ($\overline{\text{RESET}}$) is pulled low for a minimum time-out period of 140 ms when any of the following conditions occur:

- $\overline{\text{MR}}$ is pulled low via the push button switch SW1.
- The 1V6 voltage monitor trip voltage is reached (1.23V on Reset In pin):

$$Vmonitor\_trip = 0.63(\frac{R10 + R12}{R12})$$

- The threshold voltage on 3V3 is reached (MIN = 2.85 V, MAX = 3.00 V, TYP = 2.93 V).

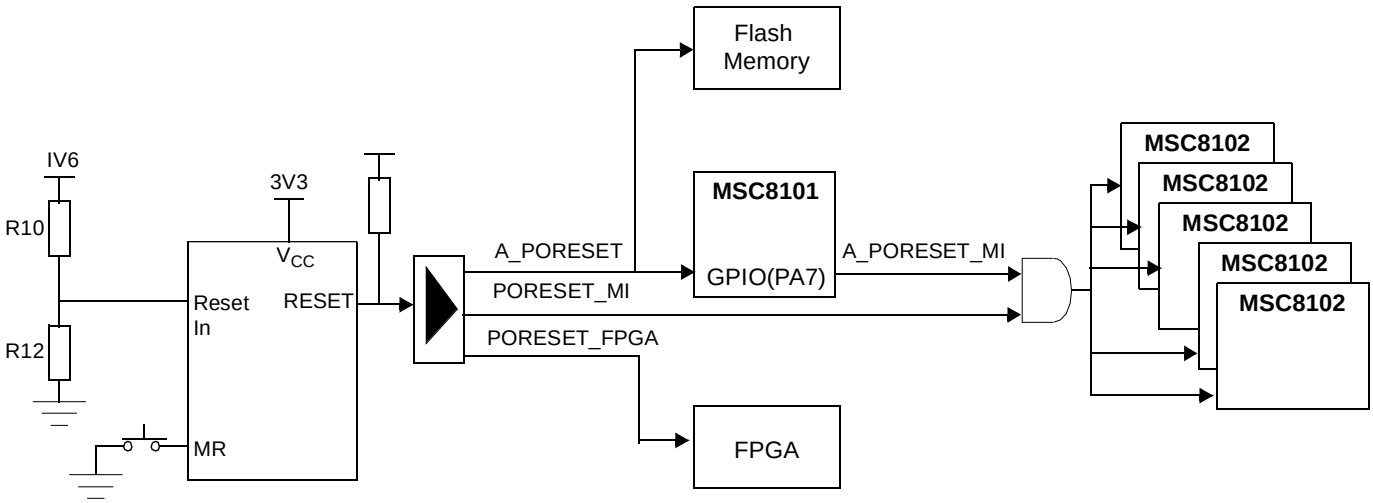


Figure 11. $\overline{\text{PORESET}}$ Scheme

The MSC8101 device controls the generation of individually buffered $\overline{\text{HRESET}}$ signals to the MSC8102 devices through the AND gating of its own $\overline{\text{HRESET}}$ signal and its $\overline{\text{HRESET}}$ GPIO control line PD31. For flexibility, the MSC8102 $\overline{\text{HRESET}}$ signals are routed to the FPGA via 0ohm resistors. An MSC8102PFC base card host can use the PMCC PTMC_RESET signal to control the $\overline{\text{HRESET}}$ of the PFC. The $\overline{\text{SRESET}}$ signals for the MSC8101 and MSC8102s are pulled high.

1. And with MSC8101 GPIO, PA7.

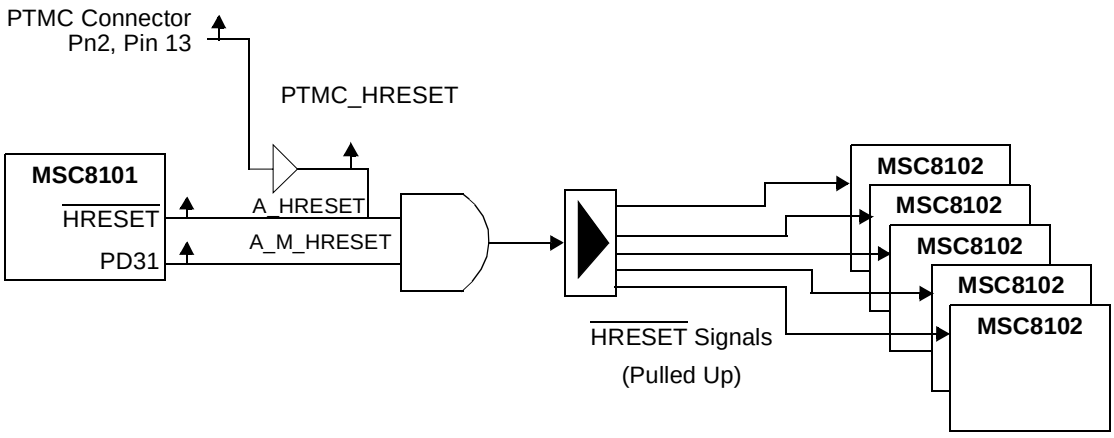


Figure 12. HRESET Scheme

3.3.2 Clock Distribution

The MSC8102PFC has two clock regions:

- MSC8101 aggregator and MSC8102 DSI interface clocking (see **Figure 13**).
- MSC8102 and associated SDRAM clocking (see **Figure 14**).

In the first clock region, the MSC8101 aggregator and MSC8102 DSI interface clocks (HCK) are generated via a single oscillator, which is distributed via an ICS9112-17 low skew buffer. In the second clock region, the MSC8102 CLKIN signals are generated from a single oscillator, which is distributed via the ICS9112-16 low skew output buffer to the MSC8102 DSP array. Each MSC8102 CLKOUT signal is in turn fed back as the DLLIN signal via an additional low-skew buffer. This buffer also generates the associated MSC8102 SDRAM clock. To accommodate debug and board set-up, the clock frequencies listed in **Table 28** are used on the MSC8101 and MSC8102 devices.

Table 28. Clock Frequencies

Processor	Clock Mode	CLKIN	Core	CPM	Bus	DSI
MSC8101	46	34.5 MHz	275 MHz	138 MHz	69 MHz	—
MSC8102	10	41.6 MHz	250 MHz	—	83 MHz	69 MHz

The frequency of operation depends on the revision of silicon used and the required application. Consult the respective data sheets for the latest operating frequency characteristics of the MSC8101 and MSC8102 devices. These data sheets are available at the website listed on the back cover of this user's guide. The following layout constraints ensure synchronous operation:

- The MSC8102 CLKIN_D[1–5] are of equal length.
- The MSC8101 derived clocks: FPGA_CK, SDRAMCKA, A_DLLIN, HCK_D[1–5] are of equal length.
- On the MSC8102 devices, the D1_DLLINx and SDRMCKx signals are of equal length.

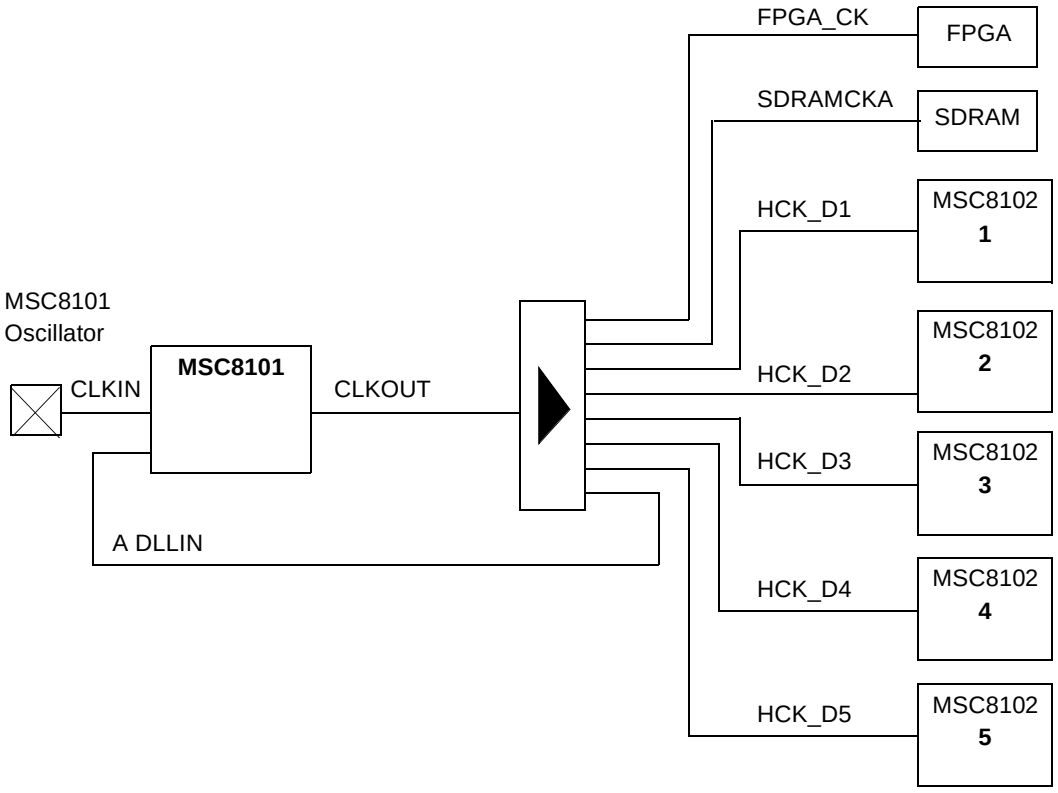


Figure 13. MSC8101 Aggregator Clocking Scheme

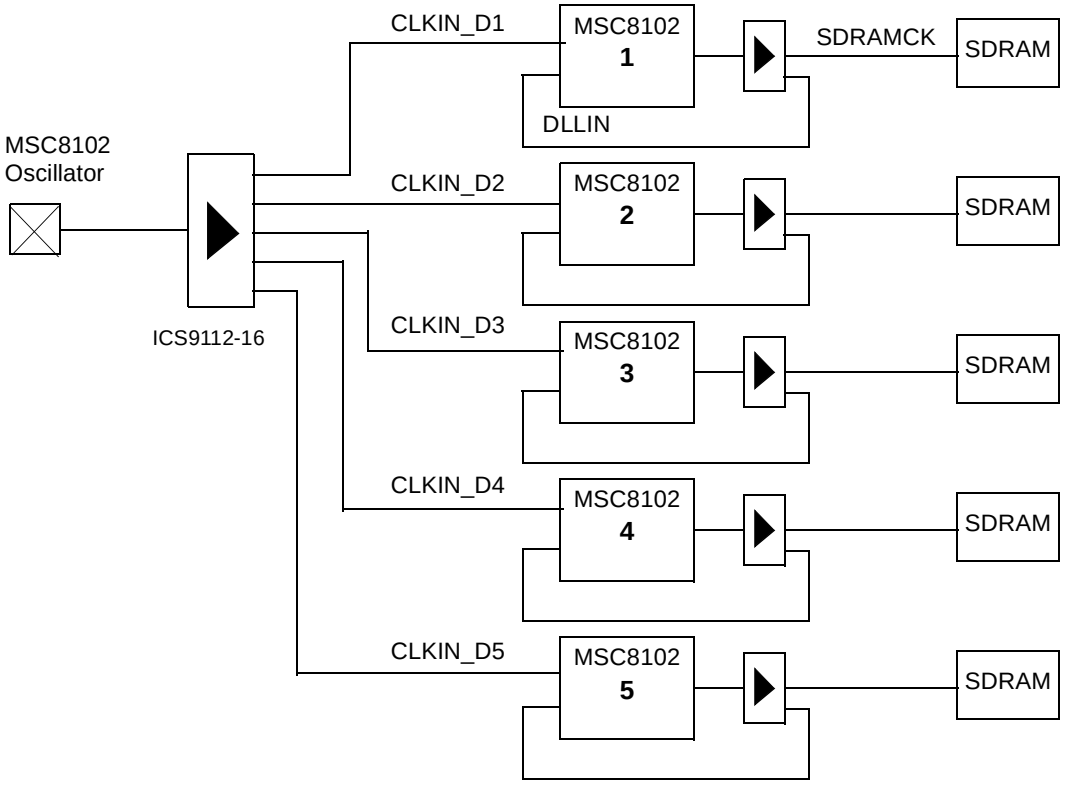


Figure 14. MSC8102 and SDRAM Clocking

3.3.3 Power

The PICMG 2.15 standard stipulates that 5 V, 3.3 V and GND be provided through the PTMC connectors. The optional connector, Pn5/Jn5, can supply the core voltage, 1.6V, to the card. There is no need for additional regulation on the card. However, to interface with standard PTMC cards, Pn5/Jn5 may not be populated, so the core voltage cannot be obtained through the PTMC connectors. To compensate for this possibility, the MSC8102PFC uses a Maxim MAX1714 Buck Controller to step down from 5 V (supplied via Jn1/Pn1) to 1.6 V, which can supply 8A. There is a link to isolate this 1V6 supply when required. A resistor pad is provided to pull the MAX1714 SHDN pin low and disable the 1V6. The 1V6 output voltage can be adjusted from 1.3V to 2.0V, as shown in **Figure 15**. The equation for adjusting the output voltage is:

$$Vout = Vfb\left(1 + \frac{R4}{R5 + VR1}\right) \quad : Vtb = 1.0V, R4 = R5 = 1K \text{ and } VR = 2K$$

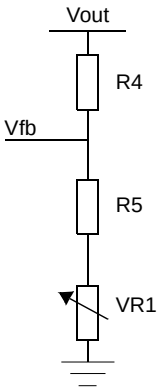


Figure 15. Setting Vout with Resistor-Divider

The FPGA requires a 1V8 supply and a minimum 500 mA (for a few millisecs) on power-up. The operating power requirements of the FPGA are application-specific. A Maxim MAX8869EU18 linear regulator, which can give a guaranteed 1A, supplies the 1V8.

3.3.4 FPGA

The FPGA is configured as follows:

- M[0–2] = 110, Slave Serial mode with preconfiguration pull-ups.
- CCLK. Input clock in slave mode.
- $\overline{\text{PROGRAM}}$. Initiates a configuration sequence when low.

3.3.5 PTMC Connectors

The MSC8102PFC interfaces with the PTMC connectors on a media gateway platform. The MSC8102PFC implements an enhanced PTMC type III or P3TMC configuration, incorporating an additional optional connector, Pn5, to allow the inclusion of 2x MII capabilities. The 5 connector interface is organized as follows:

- Pn1. CPORT interface
- Pn2. Host port interface

- Pn3. CT bus, Ethernet (RMII)
- Pn4. UTOPIA interface
- Pn5. Ethernet (MII1 and MII2)

The connector pinout is listed in **Table 29** to **Table 33**.

Table 29. Pn1/Jn1 Connector Pinout (CPORT Interface)

Pin	Signal	Pin	Signal
1	NC	2	NC
3	GND	4	NC
5	NC	6	NC
7	NC	8	+5 V
9	NC	10	NC
11	GND	12	NC
13	GMII_CK	14	GND
15	GND	16	NC
17	NC	18	+5 V
19	VIO	20	NC
21	NC	22	CP14_D0
23	CP13_D6	24	GND
25	GND	26	CP14_D1
27	CP13_D5	28	CP14_D2
29	CP13_D4	30	+5 V
31	CP13_D3	32	CP14_D3
33	CP13_D2	34	GND
35	GND	36	CP14_D4
37	CP13_D1	38	+5 V
39	GND	40	CP14_D5
41	CP13_D0	42	CP14_D6
43	CP12_D6	44	GND
45	VIO	46	CP15_D0
47	CP12_D5	48	CP15_D1
49	CP12_D4	50	+5 V
51	GND	52	CP15_D2
53	CP12_D3	54	CP15_D3
55	CP12_D2	56	GND

Table 29. Pn1/Jn1 Connector Pinout (CPORT Interface) (Continued)

Pin	Signal	Pin	Signal
57	VIO	58	CP15_D4
59	CP12_D1	60	CP15_D5
61	CP12_D0	62	+5 V
63	GND	64	CP15_D6

Table 30. Pn2/Jn2 Connector Pinout (Host Port Interface)

Pin	Signal	Pin	Signal
1	NC	2	NC
3	NC	4	NC
5	NC	6	GND
7	GND	8	NC
9	HD0	10	HA1
11	HD1	12	+3.3 v
13	PMTC_RESET	14	HA2
15	+3.3 v	16	HA3
17	HD2	18	GND
19	HD3	20	HRW
21	GND	22	HDS
23	HD4	24	+3.3 v
25	HA5	26	HTREQ
27	+3.3 v	28	HRREQ
29	HD6	30	GND
31	HD7	32	A_IRQ7
33	GND	34	HCS
35	HD8	36	+3.3 v
37	GND	38	NC
39	HD9	40	GND
41	+3.3 v	42	NC
43	HD10	44	GND
45	HD11	46	NC
47	GND	48	NC
49	HD12	50	+3.3 v

Table 30. Pn2/Jn2 Connector Pinout (Host Port Interface) (Continued)

Pin	Signal	Pin	Signal
51	HD13	**52**	NC
53	+3.3 v	**54**	NC
55	HD14	**56**	GND
57	HD15	**58**	NC
59	GND	**60**	NC
61	HA0	**62**	+3.3 v
63	GND	**64**	NC

Table 31. Pn3/Jn3 Connector Pinout (CT Bus & RMII)

Pin	Signal	Pin	Signal
1	MII_MDIO	**2**	GND
3	GND	**4**	NC
5	MII_MDC	**6**	NC
7	RMII_RX_ER0	**8**	GND
9	NC	**10**	RMII_TXD0
11	NC	**12**	RMII_TXD1
13	REF_CLK	**14**	GND
15	GND	**16**	RMII_RXD0
17	CT_FRAME_A	**18**	RMII_RXD1
19	NC	**20**	GND
21	NC	**22**	RMII_TXEN0
23	NC	**24**	RMII_CRS_DV0
25	CT_C8_A	**26**	GND
27	GND	**28**	CT_D19
29	CT_D18	**30**	CT_D17
31	CT_D16	**32**	GND
33	GND	**34**	NC
35	CT_D14	**36**	NC
37	CT_D12	**38**	GND
39	PTENB	**40**	NC
41	NC	**42**	NC
43	NC	**44**	GND

Table 31. Pn3/Jn3 Connector Pinout (CT Bus & RMII) (Continued)

Pin	Signal	Pin	Signal
45	GND	46	CT_D15
47	CT_D10	48	CT_D13
49	CT_D8	50	CT_D11
51	GND	52	CT_D9
53	CT_D6	54	CT_D7
55	CT_D4	56	GND
57	NC	58	CT_D5
59	CT_D2	60	CT_D3
61	CT_D0	62	GND
63	GND	64	CT_D1

Table 32. Pn4/Jn4 Connector Pinout (UTOPIA)

Pin	Signal	Pin	Signal
1	TxSOC	2	GND
3	GND	4	RXADR4
5	TxCLAV	6	TXADR4
7	RXADR3	8	GND
9	I2C_SCL	10	GND
11	GND	12	5 V
13	5 V	14	GND
15	GND	16	$\overline{\text{RXENB}}$
17	TXADR3	18	RXCLAV
19	TXADR2	20	GND
21	5 V	22	$\overline{\text{TXENB}}$
23	GND	24	RXADR2
25	TXCLK	26	GND
27	GND	28	TXADR1
29	TXADR0	30	RXADR1
31	TXPRTY	32	GND
33	GND	34	RXADR0
35	TXD7	36	RXPRTY
37	TXD6	38	GND

Table 32. Pn4/Jn4 Connector Pinout (UTOPIA) (Continued)

Pin	Signal	Pin	Signal
39	5 V	**40**	RXD7
41	GND	**42**	RXD6
43	RXCLK	**44**	GND
45	GND	**46**	RXD5
47	TXD5	**48**	RXD4
49	TXD4	**50**	GND
51	GND	**52**	RXD3
53	TXD3	**54**	RXD2
55	TXD2	**56**	GND
57	I2C_SDA	**58**	RXD1
59	TXD1	**60**	RXD0
61	TXD0	**62**	GND
63	GND	**64**	RxSOC

Table 33. Pn5/Jn5 Connector Pinout (Ethernet)

Pin	Signal	Pin	Signal
1	NC	**2**	IV6
3	NC	**4**	NC
5	NC	**6**	NC
7	NC	**8**	NC
9	IV6	**10**	NC
11	IV6	**12**	GND
13	NC	**14**	NC
15	NC	**16**	NC
17	NC	**18**	NC
19	GND	**20**	MII2_TCLK
21	MII2_TXD0	**22**	IV6
23	MII2_TXD1	**24**	MII2_RXDV
25	MII2_TXD2	**26**	MII2_RXD0
27	MII2_TXD3	**28**	MII2_RXD1
29	IV6	**30**	MII2_RXD2
31	IV6	**32**	GND

Table 33. Pn5/Jn5 Connector Pinout (Ethernet) (Continued)

Pin	Signal	Pin	Signal
33	MII2_TXEN	34	MII2_RXD3
35	MII2_TXER	36	MII2_RXER
37	MII2_COL	38	MII2_CRS
39	GND	40	MII2_RCLK
41	MII1_TXD0	42	VCC_CORE
43	MII1_TXD1	44	MII1_RXDV
45	MII1_TXD2	46	MII1_RXD0
47	MII1_TXD3	48	MII1_RXD1
49	IV6	50	MII1_RXD2
51	IV6	52	GND
53	MII1_TXEN	54	MII1_RXD3
55	MII1_TXER	56	MII1_RXER
57	MII1_COL	58	MII1_CRS
59	GND	60	MII1_RCLK
61	IV6	62	GND
63	IV6	64	MII1_TCLK

3.3.6 JTAG Connectivity

The MSC810x EOncE module enables you to analyze and examine the SC140 core registers, memory, and peripherals non-intrusively. It interfaces with the debugging system through on-chip JTAG TAP controller pins. The EOnCE JTAG debug ports are connected in a chain configuration so that the complete DSP array and aggregator can be debugged simultaneously. The possible configurations are as follows:

- Set JP1 jumper to position 1-2 and switch 2_8 to ON (short) to debug the full chain.
- Set the JP1 jumper to position 2-3 and switch 2_8 to OFF (open) to debug only the MSC8101 device.
- Remove/add various 0 ohm resistors to remove/add MSC8102 devices to the chain.

An EOnCE connector with the following signals is provided on P3:

- TMS. Pulled up so that after reset five TCK clocks put the TAP into the Test Logic Reset State.
- $\overline{\text{TRST}}$. The reset signal is pulled low to force the JTAG TAP into reset by default.
- TCK. The clock signal is pulled low (pulled high is also OK) to save power in low power stop mode.
- TDI. The input signal is pulled high to save power in low power stop mode. All JTAG ports have a weak internal TDI pull-up.
- TDO. The output signal is pulled high.

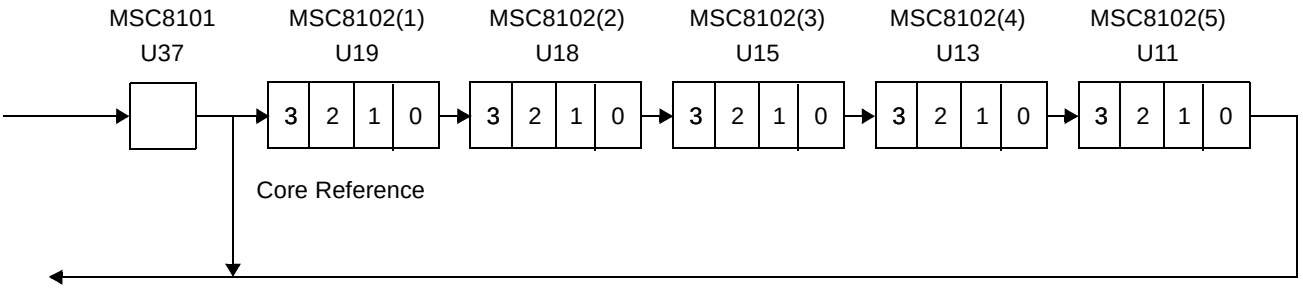


Figure 16. JTAG Chain

3.3.7 LEDs

Surface mount 0603 footprint LEDs are provided on each MSC8102 device, the MSC8101 device, and the FPGA, as follows:

- MSC8101 port line PA6 controls the MSC8101 LED.
- MSC8102 port line GPIO31 controls the MSC8102 LED.
- FPGA pin D3 (IO_82) controls the FPGA LED.

3.4 MSC8102PFC Board Configuration

The MSC8102PFC has two banks of switches for configuring the MSC8101 and MSC8102 devices. The configuration switch options are detailed in **Table 34** and **Table 38**. A switch setting of ON = logic 0 and a setting of OFF = logic 1.

Table 34. Switch 3 Descriptions

Feature	Description	
SW3.1	A_MODCK1 A_MODCK2 A_MODCK3	Sets MSC8101 MODCLK[1–3] and works in conjunction with the HRCW to determine SC140 core/CPM/bus operating frequencies.
SW3.2		
SW3.3		
SW3.4	MSC8101 boot options: • ON = Host port disabled. Boot from external memory. • OFF= Host port enabled. Boot from HDI16.	
SW3.5	I/O SEL for MSC8101 UTOPIA/Ethernet multiplexed selection: • ON = UTOPIA • OFF = MII1 Ethernet	
SW3.6	M1_BM2 M1_BM1	MSC8102 Boot Sequence options: • M1_BM1= ON, M1_BM2= ON → external memory via system bus • M1_BM1= ON, M1_BM2 = OFF → DSI boot
SW3.7		
SW3.8	Reset configuration: • ON = Reset configuration master • OFF = Reset configuration slave	

Table 35. Switch 2 Descriptions

Feature	Description	
SW2.1	Configuration source works in conjunction with SW2.7 ($\overline{\text{RSTCONF}}$).	
SW2.2	MODCK1 MODCK2	Sets MSC8101 MODCLK[1–3] and works in conjunction with the HRCW to determine SC140 core/bus operating frequencies.
SW2.3		
SW2.4	Select DSI bus width (DSI64): • ON = 32 bits. • OFF= 64 bits.	
SW2.5	Select DSI mode of operation (DSISYNC): • ON = Asynchronous mode. • OFF = Synchronous mode.	
SW2.6	Software watchdog timer enable (SWTE): • ON = Timer disabled. • OFF = Timer enabled.	
SW2.7	Reset configuration: SW2.1 SW2.7 • ON ON • ON OFF • OFF ON	• Reset configuration write through system bus. • Reset configuration write through system bus (defaults to all zeros after 1024 clock cycles. • Reset configuration write through the DSI.
SW2.8	JTAG selection (in conjunction with JP1): • ON = (JP1-pos 1–2) full JTAG of 21 SC140 cores. • OFF = (JP1) pos 2–3) single MSC8101 JTAG.	

4 Firmware Implementation

This section describes the firmware implementation on the MSC8102PFC board, including the memory maps, register settings, and bootstrap.

4.1 MSC8101 Host Memory Controller Settings

The MSC8102PFC MSC8101 host DSP uses six chip selects as memory resources. Four of these are used for peripherals (Flash memory, SDRAM, DSI, DSI broadcast) and two are used for internal resources (SRAM and local peripherals). **Table 36** illustrates the memory map. Notice that in Synchronous DSI mode, chips selects are not required for DSI and that the system bus (FPGA) handles DSI broadcast transfers. Also shown is a view of the DSI mapping of the MSC8102 through the DSI port. Only the local bus can view the core-side memory area (that is, local SRAM that is mapped from 0x00000000 to 0x0007FFFF) and peripherals such as the HDI16. The Base and Option Register settings, which define the memory map, are shown in **Table 36**. Chip select 10 and 11 are automatically set up as part of the ROM boot sequence. In addition to these registers, the Bus Configuration Register (BCR) should be set for multi-master mode BCR[EBM] = 1 in Synchronous DSI mode.

Table 36. MSC8101 Memory Controller Resources

Chip Select	Device	Start Address	End Address	Size	BR[x]	OR[x]
$\overline{\text{CS0}}$	Flash (Boot)	0xFE00_0000	0xFE3F_FFFF	4 MB	0xFE000801	0xFFC00EF4
$\overline{\text{CS2}}$	SDRAM	0x2000_0000	0x207F_FFFF	8 MB	0x20001841	0xFF803290

Table 36. MSC8101 Memory Controller Resources (Continued)

Chip Select	Device		Start Address	End Address	Size	BR[x]	OR[x]
$\overline{CS3}$	DSI Broadcast		0x22A0_0000	0x22BF_FFFF	2 MB	0x22A01881	0xFFE00104
$\overline{CS4}$	DSI	DSP 5	0x2280_0000	0x229F_FFFF	2 MB	0x22001881	0xFE000102
		DSP 4	0x2260_0000	0x227F_FFFF	2 MB		
		DSP 3	0x2240_0000	0x225F_FFFF	2 MB		
		DSP 2	0x2220_0000	0x223F_FFFF	2 MB		
		DSP 1	0x2200_0000	0x221F_FFFF	2 MB		
$\overline{CS10}$	Internal SRAM		0x0200_0000	0x0207_FFFF	512 KB	0x020000C1	0xFFF80000
$\overline{CS11}$	Local Bus Peripherals		0x01F0_0000	0x01F0_7FFF	32 KB	0x01F00021	0xFFFF0000

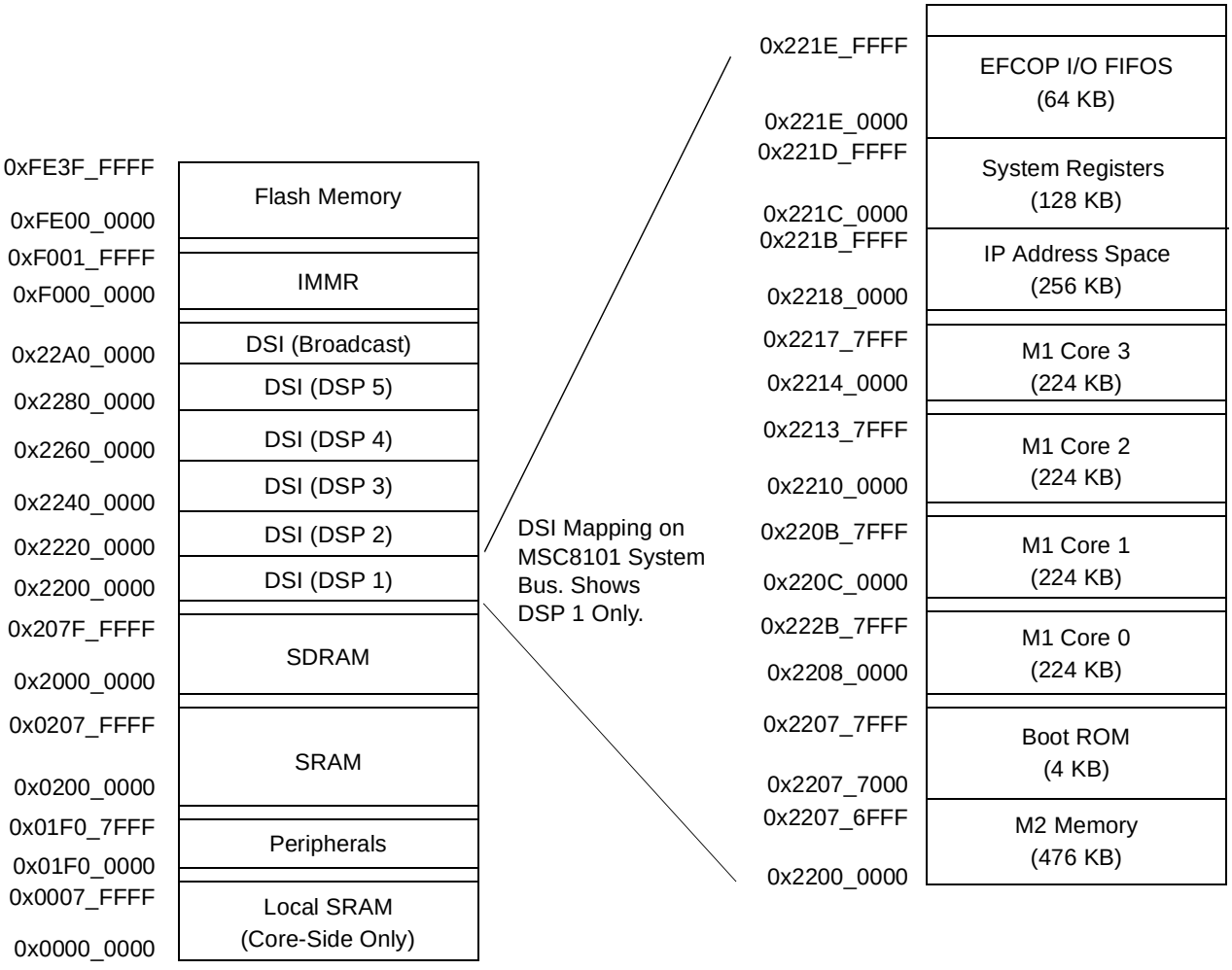


Figure 17. MSC8101 Host Memory Map

4.2 MSC8102 Memory Controller Settings

Each MSC8102PFC MSC8102 slave DSP uses four chip selects as memory resources, one for the SDRAM peripheral and three for internal resources (L1 and L2 SRAM, IPBus peripherals, and DSP peripherals). The Base and Option Register settings, which define the memory map, are detailed in **Table 37**. Chip selects 9–11 are automatically set up as part of the ROM boot sequence.

Table 37. MSC8102 Memory Controller Resources

Chip Select	Device	Start Address	End Address	Size	BR[x]	OR[x]
$\overline{CS2}$	SDRAM	0x2000_0000	0x20FF_FFFF	16 MB	0x20001841	0xFF0030D0
$\overline{CS9}$	IP Peripherals	0x0218_0000	0x021B_FFFF	256 KB	0x02181821	0xFFFC0008
$\overline{CS10}$	DSP Peripherals	0x021E_0000	0x021E_FFFF	64 KB	0x021E002E	0xFFFF0000
$\overline{CS11}$	Internal SRAM	0x0200_0000	0x0217_FFFF	1.5 MB	0x020000C1	0xFFE00000

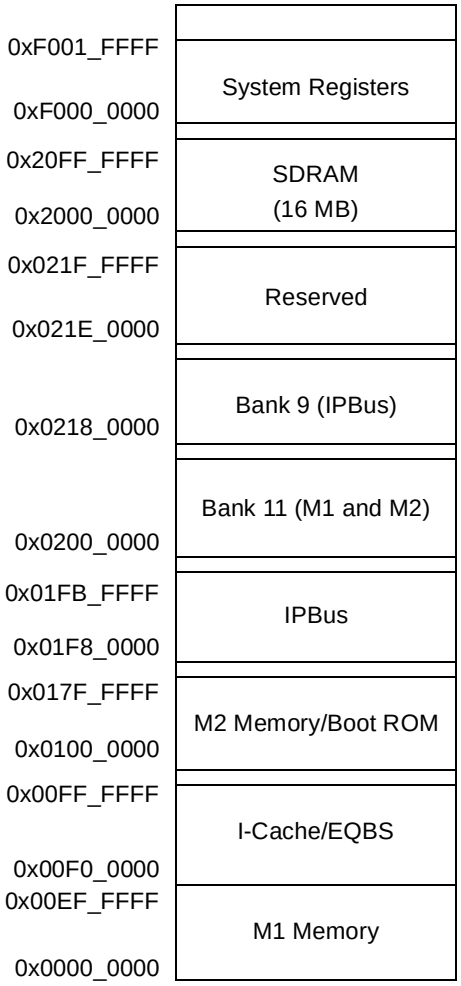


Figure 18. MSC8102 Memory Map

4.3 MSC8102PFC Reset Configuration Word (MSC8101)

When the MSC8101 device is configured to boot from external memory, it accesses the start of Flash memory at address 0xFE000000 (using $\overline{\text{CS0}}$) to read the HRCW. The configuration master (MSC8101) reads the HRCW from the Flash memory with byte-wide accesses. The HRCW defines the initial bus, arbitration, memory controller modes, and clocking modes of the device. **Table 38** lists the bit values of the MSC8101 HRCW.

Table 38. MSC8101 HRCW

Bit	Name	Value	Description
0	EARB	0	Internal arbitration 1
1	EXMC	0	Internal memory controller
2	IRQ7 INT	1	INT_OUT selected
3	EBM	1	Multi-Master mode (set to 1 for synchronous DSI)
4–5	BPS	01	Boot port size is 8 bits
6	SCDIS	0	SC140 core enabled
7	ISPS	1	System bus is 32 bits wide
8–9	IRPC	10	$\overline{\text{IRQ}}$ lines act as BADDR
10–11	DPPC	00	Data parity pins act as $\overline{\text{IRQ}}$ lines
12	NMI OUT	0	$\overline{\text{NMI}}$ is serviced by SC140 core
13–15	ISB	000	Internal space base is 0xF0000000
16	—	0	Reserved
17	BBD	0	Arbitration pins enabled
18–19	MMR	00	Initial bus request inputs to the master are not masked
20–21	—	00	Reserved
22–23	TCPC	00	TC function selected
24–25	BC1PC	00	BCTL1 function selected
26	SWDIS	1	Disable watchdog timer
27	DLLDIS	1	DLL bypass
28–30	MODCK_H	101	Clock Configuration 46 used (MODCK_L = 110)
31	—	0	Reserved
Configuration Word = 0x3580003A			

4.4 MSC8102PFC MSC8102 HRCW

The slave MSC8102 devices are configured to receive their HRCW through the DSI port. **Table 39** lists the bit values for the MSC8102 HRCW.

Table 39. MSC8102 HRCW

Bit	Name	Value	Description
0	EARB	0	Internal arbitration
1	EXMC	0	Internal memory controller
2	INT OUT	1	INT_OUT selected
3	EBM	0	Single MSC8102 bus mode
4–5	BPS	00	Boot port size is 64 bits (not used)
6	SCDIS	0	SC140 core enabled

Table 39. MSC8102 HRCW (Continued)

Bit	Name	Value	Description
7	ISPS	1	Internal space is 32 bits
8	IRPC	0	$\overline{\text{IRQ}}$ selected (not used)
9	—	0	Reserved
10–11	DPPC	00	Data parity pins act as $\overline{\text{IRQ}}$ lines
12	NMI OUT	0	$\overline{\text{NMI}}$ is serviced by SC140 core
13–15	ISB	000	Internal space base is 0xF0000000
16	—	0	Reserved
17	BBD	0	Arbitration pins enabled (not used)
18	MMR	0	No masking on bus request lines
19	—	0	Reserved
20	TTPC	0	Transfer type selected (not used)
21	CS5PC	0	$\overline{\text{CS5}}$ selected (not used)
22–23	TCPC	00	TC function selected
24	LTLEND	0	Big endian
25	PPCLE	0	Not applicable
26	—	0	Reserved
27	DLLDIS	0	No DLL bypass
28–30	MODCK[3–5]	010	Clock configuration (default mode is 10)
31	—	0	Reserved
Configuration Word = 0x21000004			

4.5 MSC8102PFC Bootstrap

The flowchart in **Figure 19** illustrates the bootstrap method of the MSC8102PFC, which proceeds as follows:

1. $\overline{\text{PORESET}}$ is released and the MSC8101 device reads its own HRCW from Flash memory.

   There is a set delay to allow the PLL and DLL to lock after $\overline{\text{HRESET}}$ is released.
2. The MSC8101 device executes its ROM boot code.
3. The MSC8101 device reads the address lookup table at 0xFE000110 and jumps to an address preprogrammed in Flash memory (0xFE000200).
4. At this preprogrammed address, the MSC8101 device begins to execute its start-up code.
5. The start-up code switches off the watchdog timer and jumps to address 0xFE002000 (Sector 1 of Flash memory) where a simple downloader routine resides.
6. The downloader routine copies the main down loader routine, which is stored at 0xFE004000 (Sector 2 of Flash) to SRAM location 0x69000 and then jumps to the start of the routine.
7. The main down loader, which is now running in SRAM rather than in slower Flash memory, copies the MSC8102PFC application code from Flash memory to SRAM, starting at location 0x0.
8. When copying completes, the main downloader jumps to address 0x0 and executes the code.
9. The application code initializes the FPGA, the MSC8101 device, and finally the MSC8102 DSI ports.
10. The application code writes the MSC8102 HRCW to the MSC8102 devices via their DSI port to bring them out of reset.

11. When the MSC8102 devices are out of reset, the MSC8101 downloads the MSC8102 code through the MSC8102 DSI ports into L1/L2 memory.

12. The MSC8101 device instructs the MSC8102 cores to execute the code.

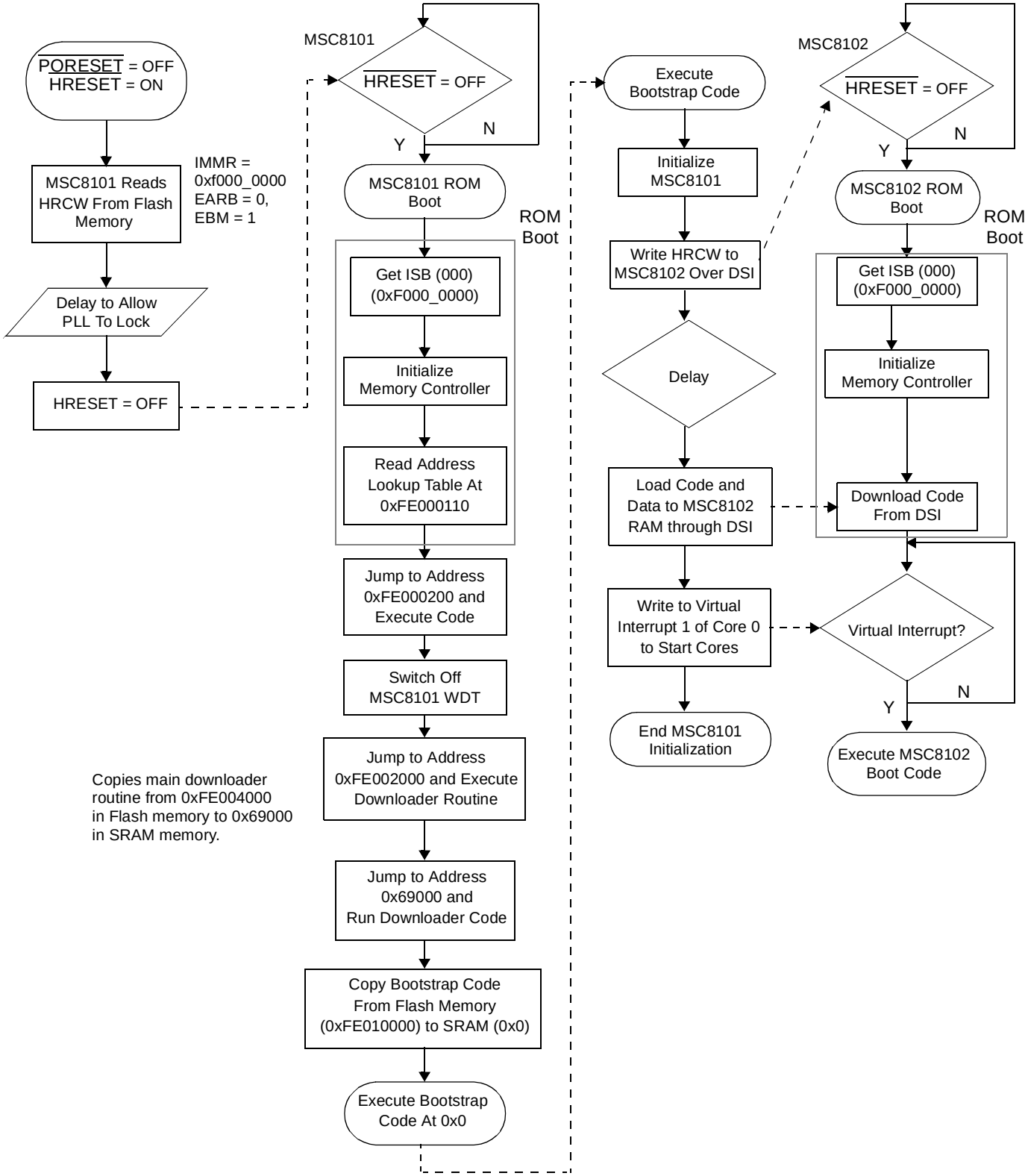


Figure 19. MSC8102PFC Bootstrap Method

Appendix A Supporting Information

This appendix presents information on the MSC8102PFC parts, the JTAG configuration file, and the MSC8102PFC layout. **Table 40** lists the MSC8102PFC parts, including part number.

Table 40. MSC8102PFC Parts

Board Reference	Description	Manufacturer	Part Number
D1, D2, D3, D4, D5, D6, D10	0603 SM YELLOW LED	LiteON	LTST-C190YKT
D7, D8, D9	1A Silicon Rectifier	General Semi	GF1A
JP1	HDR 1X3 SMT 100mil SP 380H Au	SAMTEC	TSM-103-01-S-SV
JP2	Surface Mount 3x2 0.1" pitch header	SAMTEC	TSM-103-01-S-DV
LK1	1mm dia. 5mm shorting link (10A)	Harwin	D3080-05
L1	POWER INDUCTOR 1.5UH 14.0A SMD	SUMIDA	CEP1251R5MC
PN1, PN2, PN3, PN4, PN5	CON 64PIN 1.0MM FH PLUG W/PST 8MM STACK	TYCO	120525-1
P1	Surface Mount 2x2 0.1" pich header	SAMTEC	TSM-102-01-S-DV
P3	HDR 2X7 SMT 100mil CTR 380H Au	SAMTEC	TSM-107-01-S-DV
SW1	SW SPST KEY NO PB SMT 15V 20mA	BOURNS	7914J-1-000E
SW2, SW3	SW 8P SPST DIP NC SMT 24V 25mA	GRAYHILL	97C08S
TP1, TP2	Test Point		
U1	DIO SMT Schottky Power Rectifier	ON Semiconductor	MBRS340T3
U2	CONTROLLER HIGH-SPEED STEP-DOWN	MAXIM	MAX1714BEEE
U3	TRANSISTOR MOSFET N-CHANNEL 28V	International Rectifier	IRF7811A
U4	TRANSISTOR MOSFET N-CHANNEL 30V	Fairchild Semiconductor	FDS6670A
U5	IC RS-232 TRANSCEIVER 3/5.5V 1Mbps	MAXIM	MAX3232CUE
U6	LOGIC GATE QUAD 2-INPUT AND LCX-CMOS TSSOP 14PIN	ON Semiconductor	MC74LCX08DT
U7	IC LOGIC GATE HEX BUFFER TSSOP 14PIN	Philips Semiconductors	74LVC07APW
U8	IC Dual Ultra-Low-Voltage SOT23 µP Supervisors	MAXIM	MAX6828SUT-T
U9, U29	BUFFER/DRIVER DUAL 4-BIT 20PIN SOP	Philips Semiconductors	74LVC244APW
U10	IC Linear Regulator	MAXIM	MAX8869EUE18
U11, U13, U15, U18, U19	IC DSP 431PIN BGA	Freescale Semiconductor	MSC8102
U12, U14, U16, U17, U20, U34	IC MEM DRAM SYNC PC-100 86PIN TSSOP	MICRON	MT48LC2M32B2TG-6
U21, U22, U24, U25, U26, U27	IC BUFFER LOW SKEW ZERO DELAY 8PIN TSSOP	ICS-Integrated Circuit Systems	ICS9112AG-16
U23, U38, U40	OSC CLOCK 50MHZ CMOS 3.3V SMT	EPSON	SG-710ECK50.0000MC

Table 40. MSC8102PFC Parts (Continued)

Board Reference	Description	Manufacturer	Part Number
U28	IC BUFFER LOW SKEW ZERO DELAY 16PIN TSSOP	ICS-Integrated Circuit Systems	ICS9112AF-17
U30	IC 12-bit to 24-bit multiplexed D Type Latches (3state)	Philips Semiconductors	74ALV16260DGG
U31	BUS SWITCH SSOP 80PIN	IDT	IDTQS34XV245Q3
U32, U33	16-bit transparent D-type latch	Philips Semiconductors	74ALVT16373DGG
U35	BUS EXCHANGER TSSOP 56PIN	Pericom Semiconductor	PI3B16233A
U36	EEPROM FLASH 2MX16/4MX8 TSSOP 48PIN	AMD	AM29LV320DB120EI
U37	IC DSP 332PIN BGA	Freescale Semiconductor	MSC8101
U39	IC FPGA 1.8V Spartan-IIE	Xilinix	XC2S300E-7FG456C
VR1	2K2 variable resolution	Bourns	3214W-1-222E

The JTAG configuration file (for 21 SC140 cores) is as follows:

```
       MSC8102Sync
MSC8102                        # DSP5 Core 0       1
MSC8102                        # DSP5 Core 1       2
MSC8102                        # DSP5 Core 2       3
MSC8102                        # DSP5 Core 3       4
       MSC8102Sync
MSC8102                        # DSP4 Core 0       6
MSC8102                        # DSP4 Core 1       7
MSC8102                        # DSP4 Core 2       8
MSC8102                        # DSP4 Core 3       9
       MSC8102Sync
MSC8102                        # DSP3 Core 0       11
MSC8102                        # DSP3 Core 1       12
MSC8102                        # DSP3 Core 2       13
MSC8102                        # DSP3 Core 3       14
       MSC8102Sync
MSC8102                        # DSP2 Core 0       16
MSC8102                        # DSP2 Core 1       17
MSC8102                        # DSP2 Core 2       18
MSC8102                        # DSP2 Core 3       19
       MSC8102Sync
MSC8102                        # DSP1 Core 0       21
MSC8102                        # DSP1 Core 1       22
MSC8102                        # DSP1 Core 2       23
MSC8102                        # DSP1 Core 3       24
SC140                          # MSC8101           25
```

Figure 20 and **Figure 21** show top and bottom views of the MSC8102PFC layout.

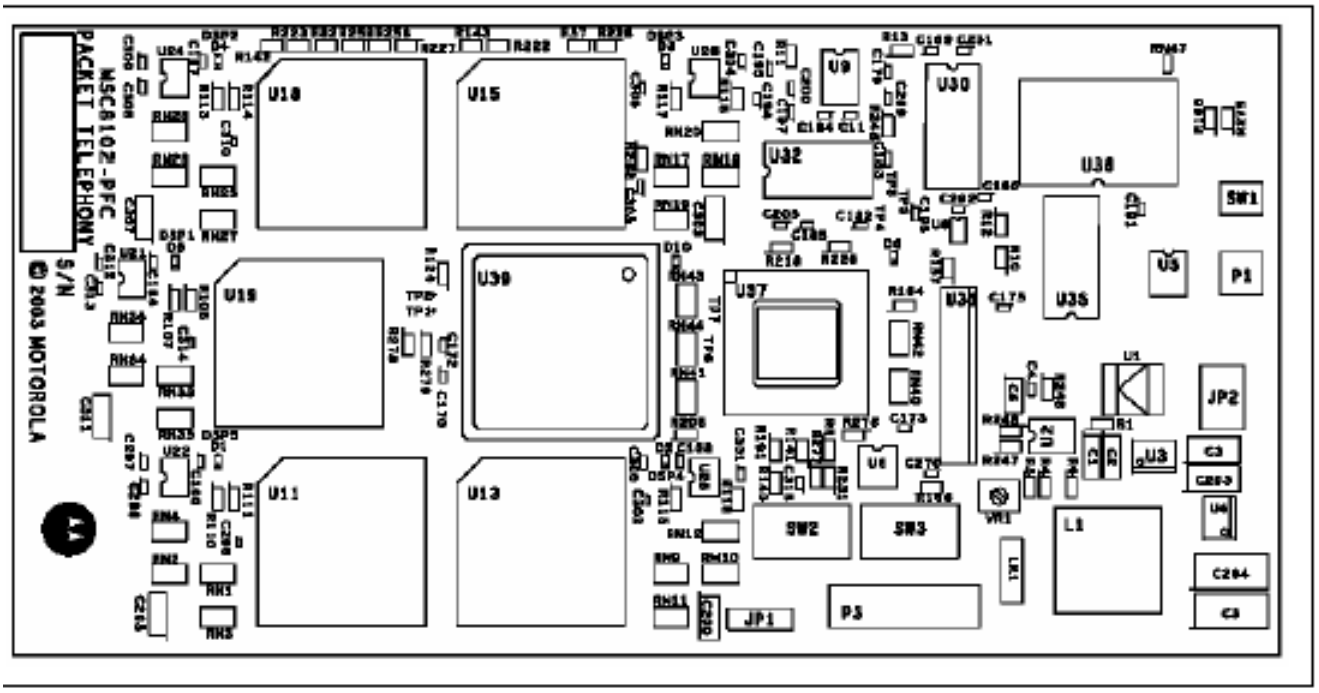


Figure 20. MSC8102PFC Layout, Top

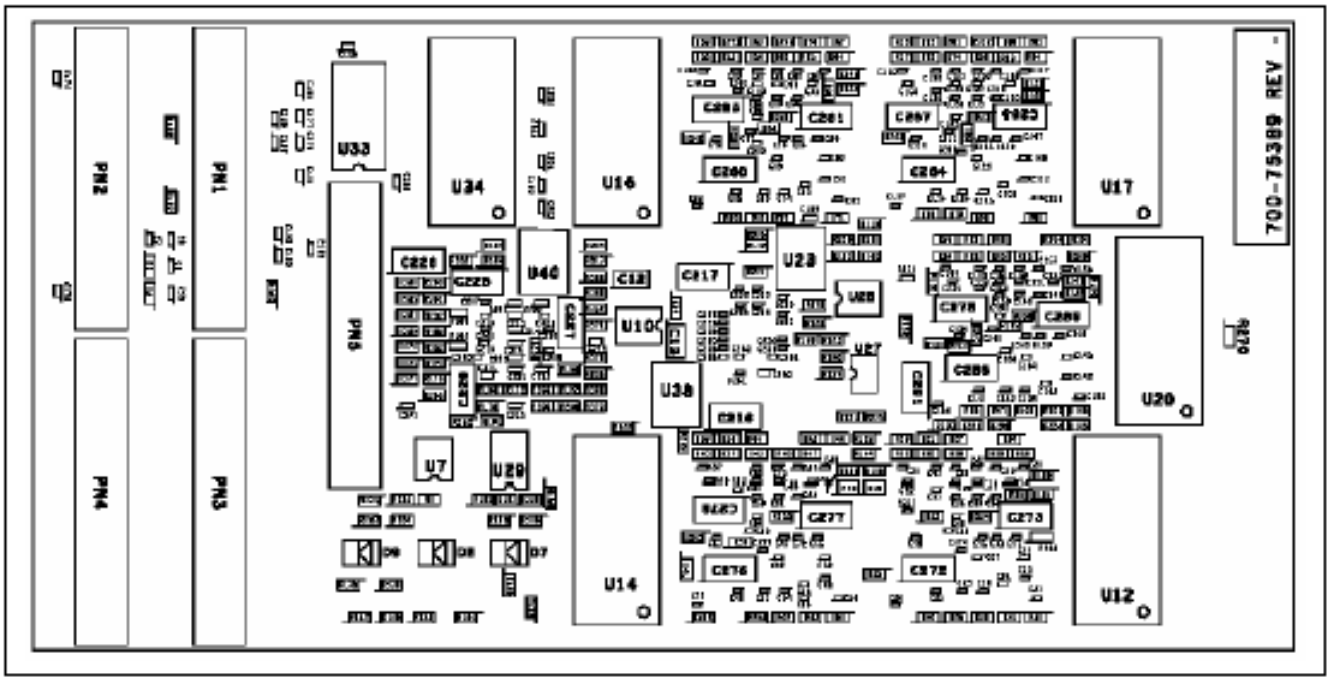


Figure 21. MSC8102PFC Layout, Bottom

Appendix B Schematics

The following pages show the schematics for the MSC8102PFC.

MSC8102 - PACKET TELEPHONT FARMCARD (PFC)

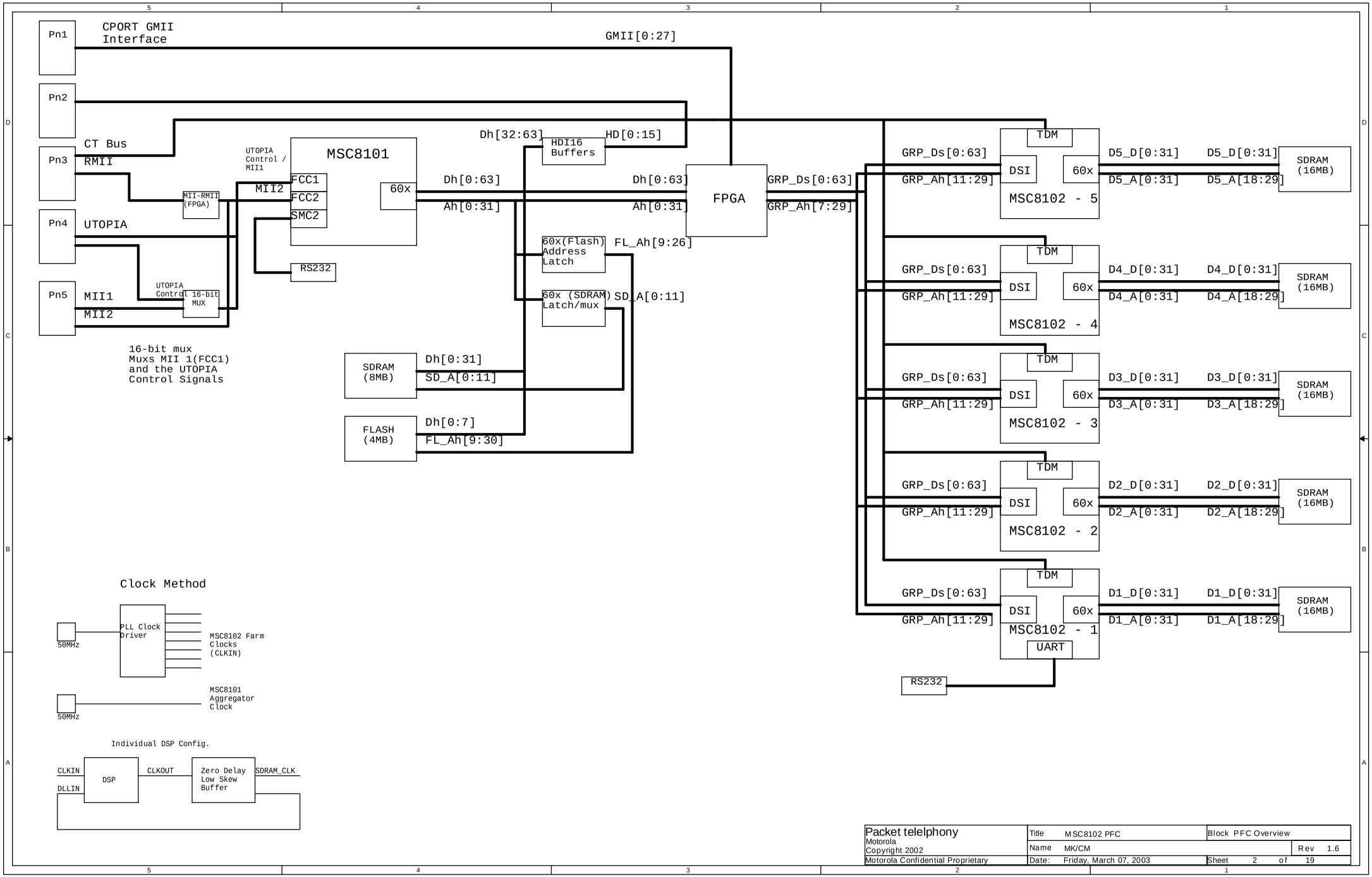
Table of Contents

Revision History

0.1	Release for Manufacturing Quotation
1.0	First Release
1.1	Minor Updates
1.2	CPORT Interface added to FPGA
1.3	Minor Updates
1.4	Reset Scheme & FPGA power up mode altered. MRP renamed PFC
1.5	Pilot Production Release
1.6	MSC8102 SDRAM increased to 16MByte

Digital DNA from Motorola

Title	MSC8102 PFC	Block	Front Page
Name	MK/CM	Rev	1.6
Date:	Friday, March 07, 2003	Sheet	1 of 19



Packet telelphony	Title MSC8102 PFC	Block PFC Overview	
Motorola	Name MK/CM		Rev 1.6
Copyright 2002 Motorola Confidential Proprietary	Date: Friday, March 07, 2003	Sheet 2 of 19	

Note
1. MSC8101 Click Mode 46 (CLKIN=34.5MHz,
Bus=69MHz, CPM= 138MHz, Core=275MHz).

DSP_CORE

MSC8101

U37B

Parallel I/O

MSC8101

BOOT MODE:

A_RSTCONF	EE1	EE4	EE5	MODE
1	0	0	0	Default
0	0	0	0	Boot From Flash
0	1	0	1	Boot From HDI16

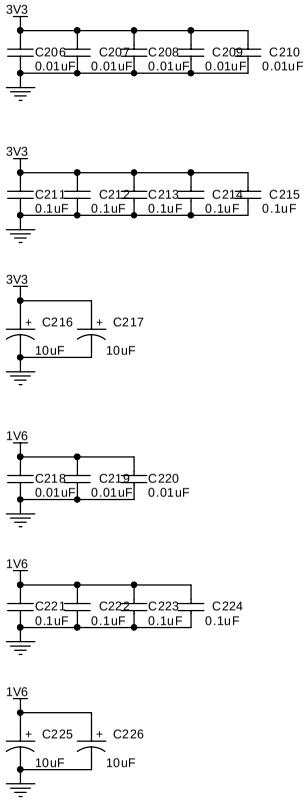
Note:
[1] If DREQs required then DREQ3/4 can be enabled in the SIUMCR. This only leaves IRQ1 functioning. If more IRQs are need then ABB and DBB can be used for IRQ 2 & 3. IRQ7/INT_OUT can be used as IRQ7. BADDR pins are used for flash and cannot be used as IRQsIRQs

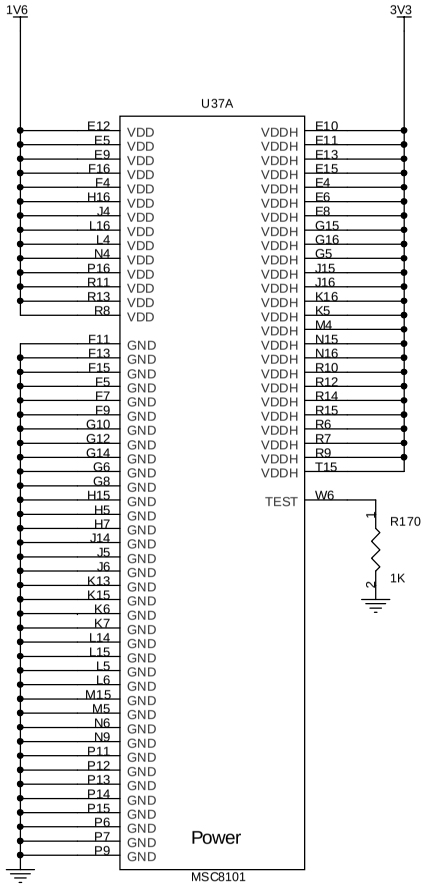
[2] UTOPIA Address may be removed from future designs

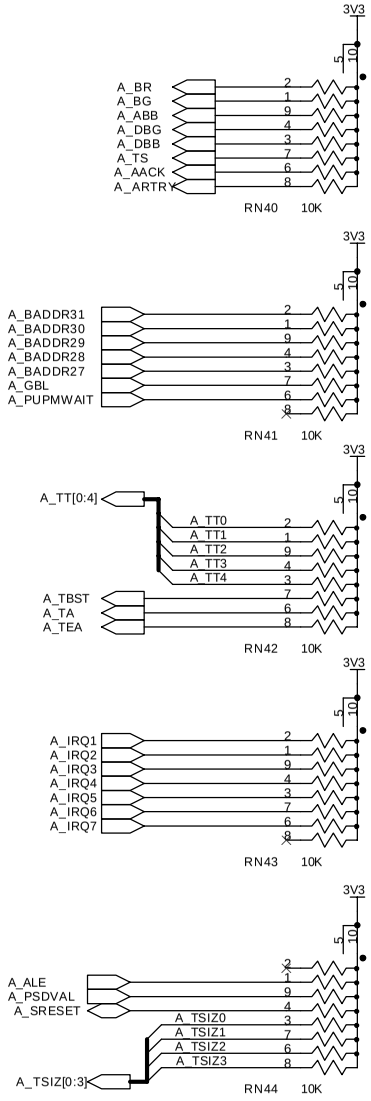
Notes
1. Pulls up can be removed if provided by carrier card

Packet telephony Motorola Copyright 2002 Motorola Confidential Proprietary	Title MSC8102 PFC	Block MSC8101 Core
	Name MK/CM	Rev 1.6
	Date: Friday, March 07, 2003	Sheet 3 of 19

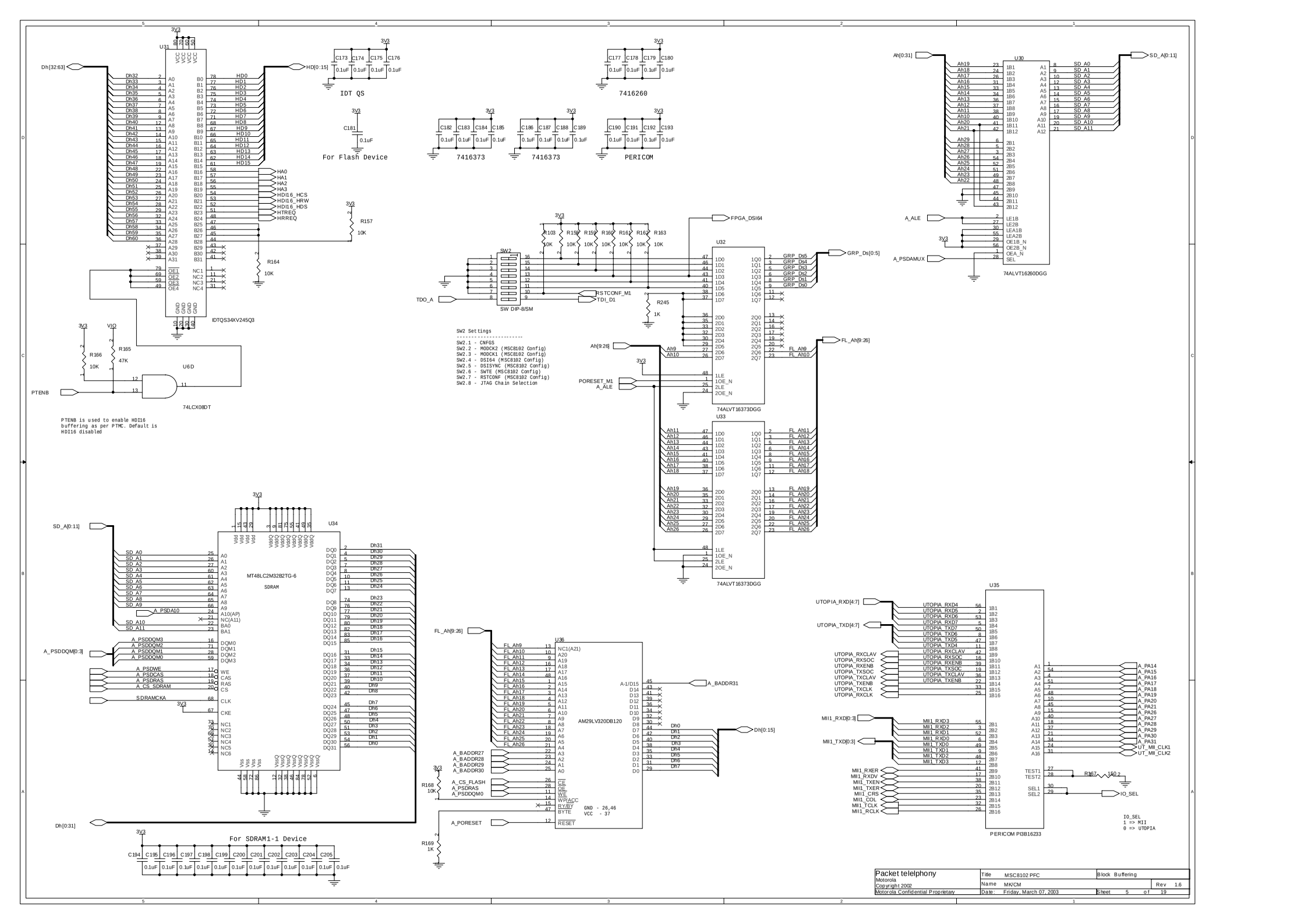
Place caps as close to device as possible.







Packet telelphony Motorola Copyright 2002 Motorola Confidential Proprietary	Title MSC8102 PFC	Block MSC8101 Power	
	Name MK/CM		Rev 1.6
	Date: Friday, March 07, 2003	Sheet 4 of 19	



Packet telelphony	Title MSC8102 PFC		Block Buffering
Motorola	Name MK/CM		Rev 1.6
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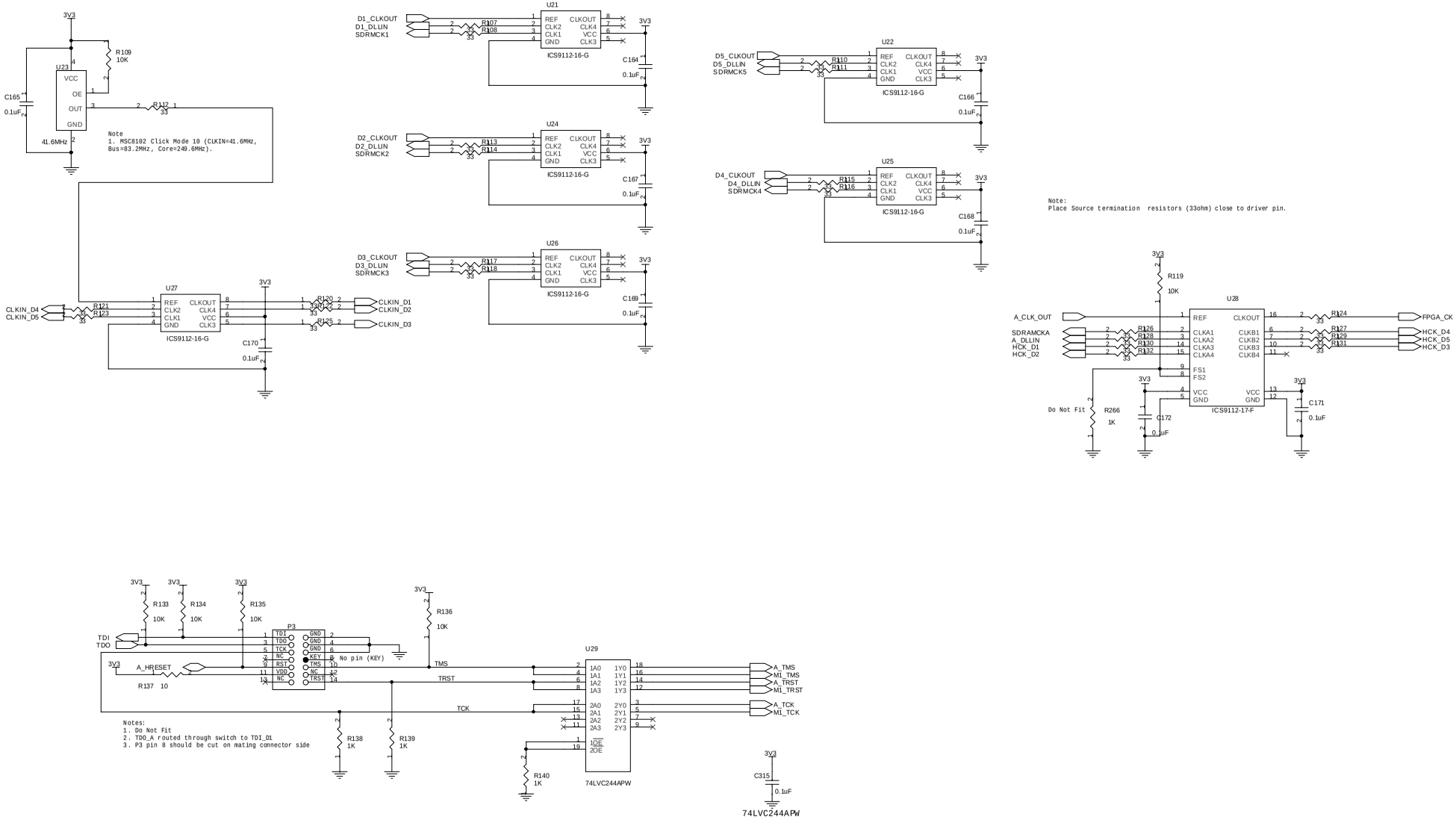
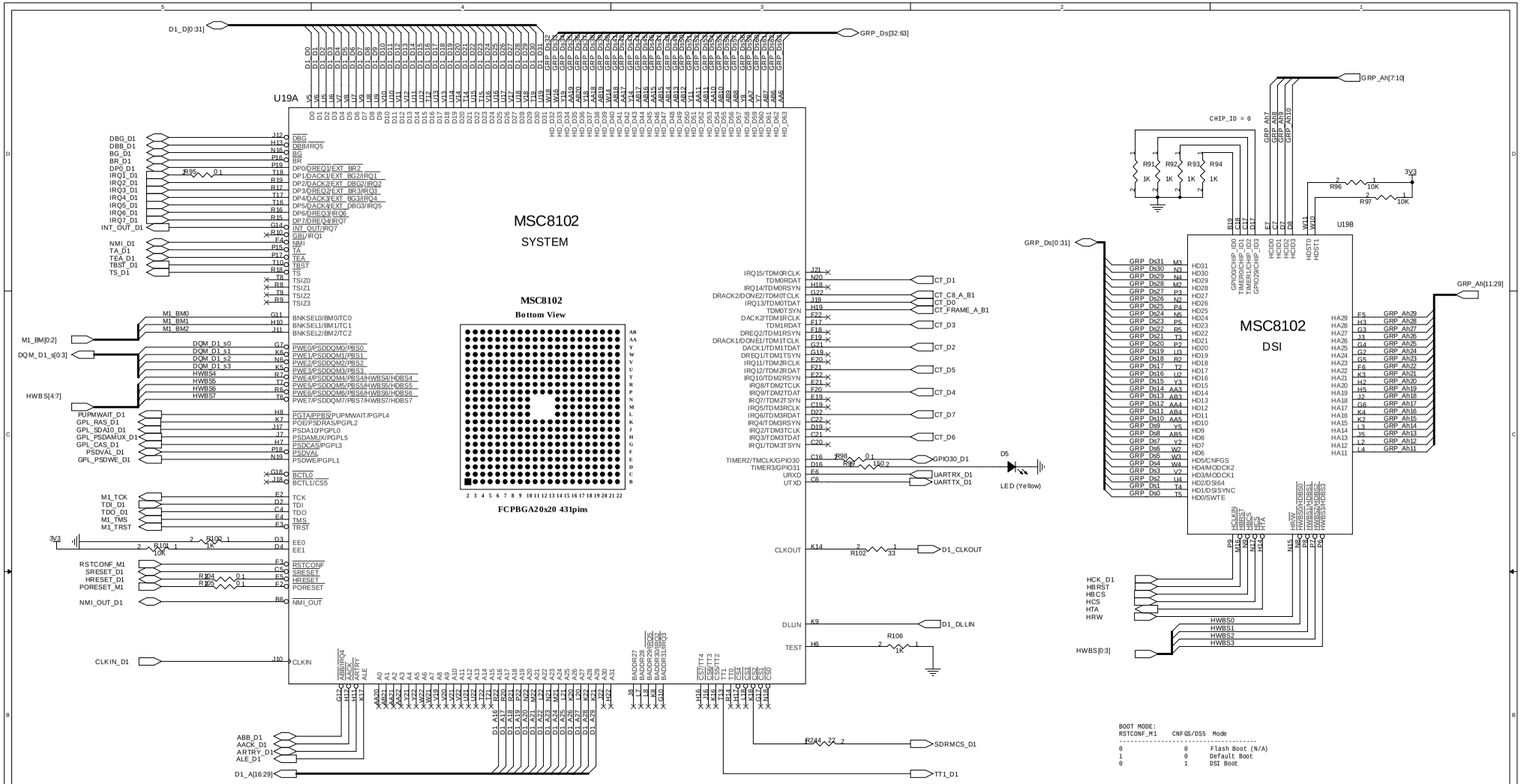


Packet telelphony	Title MSC8102 PFC	Block Clocks	
Motorola	Name MK/CM		Rev 1.6
Copyright 2002			
Motorola Confidential Proprietary	Date: Friday, March 07, 2003	Sheet 6 of 19	


MSC8102
SYSTEM
U19A
MSC8102
Bottom View
FCPBGA20x20 431pins
MSC8102
DSI
U19B
CHIP_ID = 0
BOOT MODE:
RSTCONF_M1 CNFGS/DS5 Mode
0 0 Flash Boot (N/A)
1 0 Default Boot
0 1 DSI Boot
Packet telelphony
Motorola
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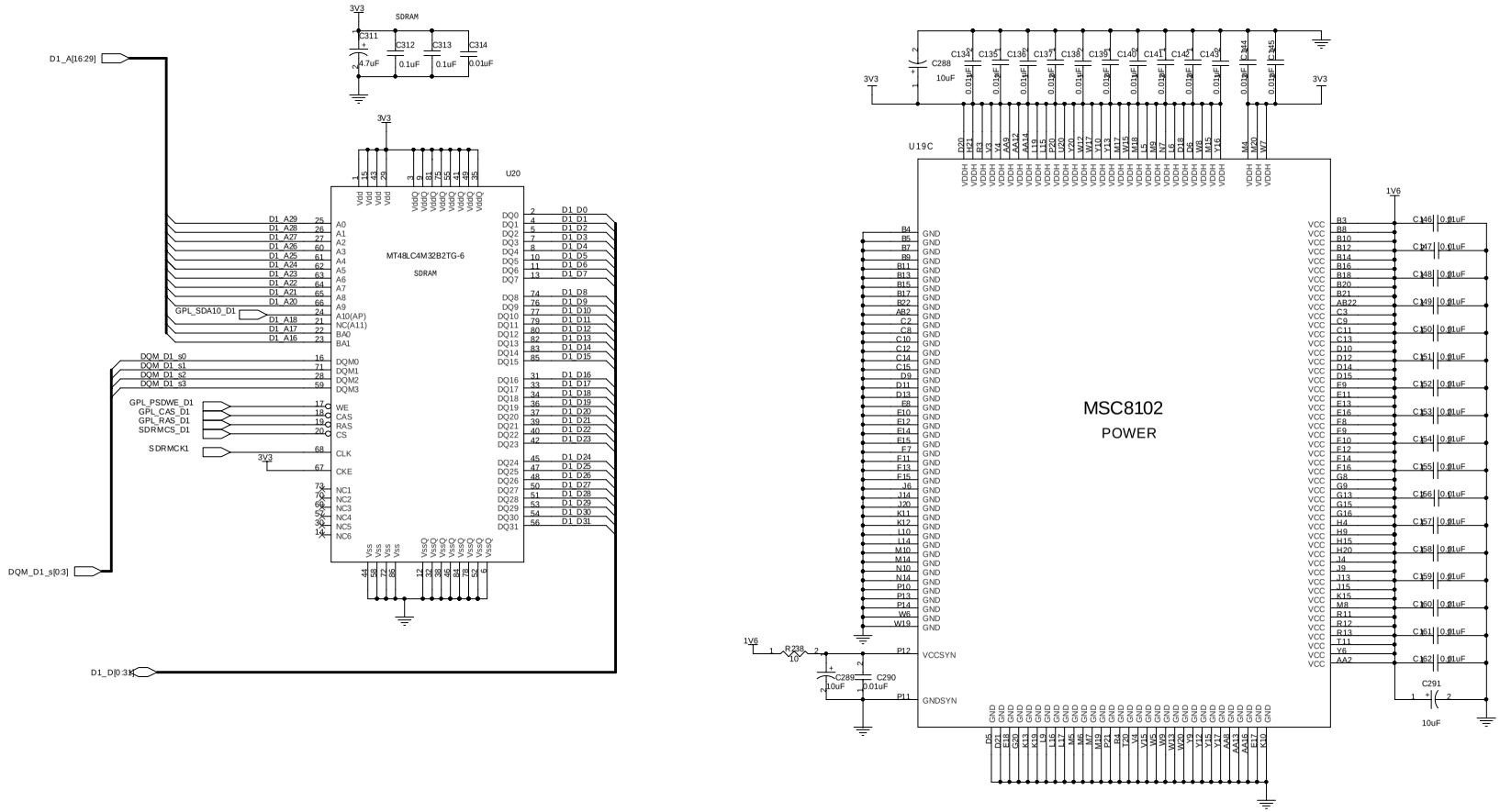
Title MSC8102 PFC
Block D1 Core
Name MK/CM
Rev 1.6
Date: Friday, March 07, 2003
Sheet 7 of 19



Packet telelphony	Title MSC8102 PFC	Block D1 Mem	
Motorola	Name MK/CM		Rev 1.6
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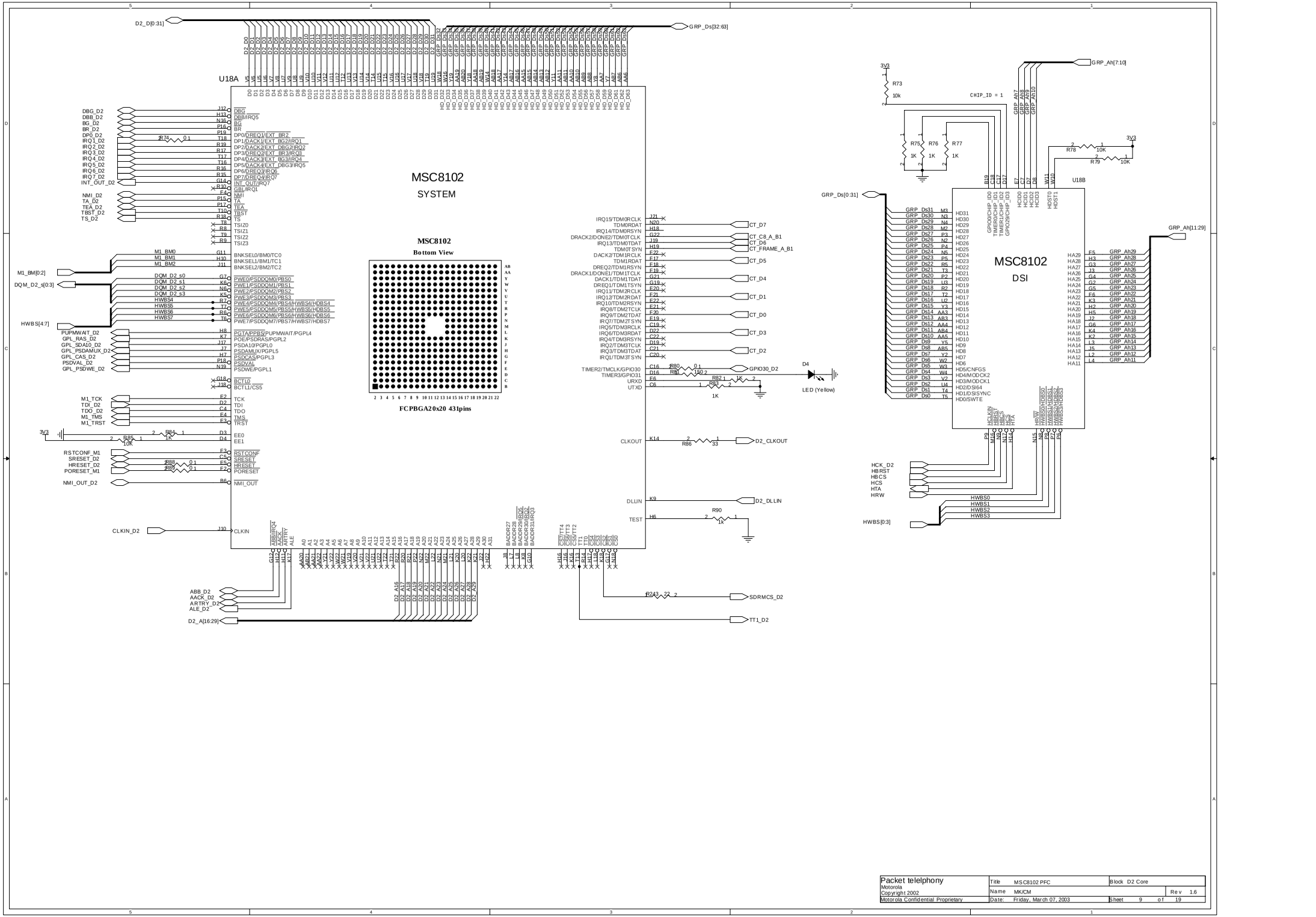
MSC8102
SYSTEM
MSC8102
Bottom View
FCPBGA20x20 431pins
U18A
U18B
MSC8102
DSI
D2_D[0:31]
GRP_Ds[32:63]
GRP_Ah[7:10]
GRP_Ah[11:29]
GRP_Ds[0:31]
M1_BM[0:2]
DQM_D2_s[0:3]
HWBS[4:7]
HBRST
HBCS
HCS
HTA
HRW
HWBS0
HWBS1
HWBS2
HWBS3
HWBS[0:3]
HCK_D2
CHIP_ID = 1
3V3
R73
10k
R75
R76
R77
1K
R78
R79
10K
LED (Yellow)
GPIO30_D2
D2_CLKOUT
D2_DLLIN
SDRMCS_D2
TT1_D2
CLKIN_D2
ABB_D2
AACK_D2
ARTRY_D2
ALE_D2
D2_A[16:29]
Packet telelphony
Motorola
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Title MSC8102 PFC
Block D2 Core
Name MK/CM
Rev 1.6
Date: Friday, March 07, 2003
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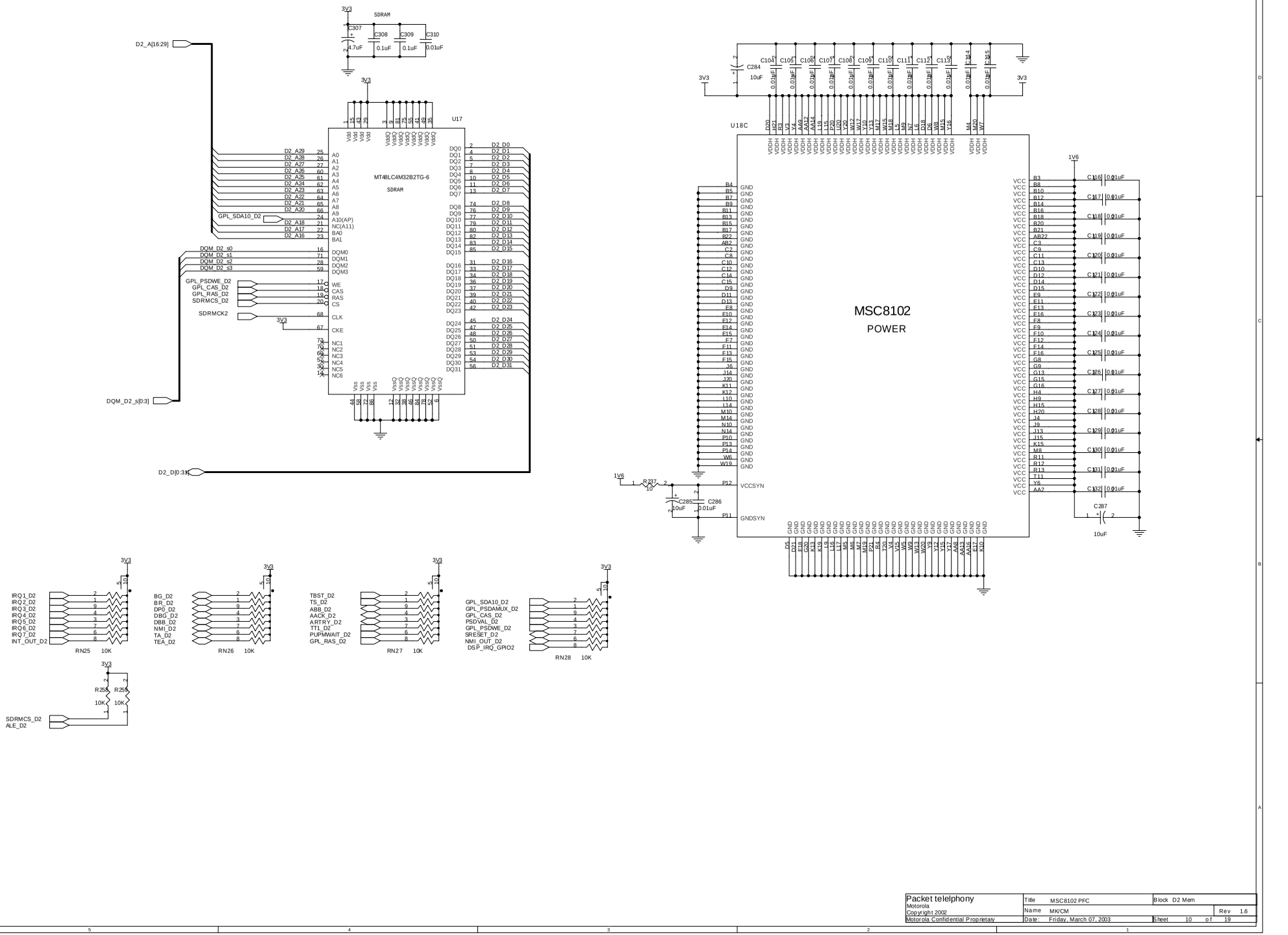

Packet telelphony	Title MSC8102 PFC		Block D2 Mem
Motorola	Name MK/CM		Rev 1.6
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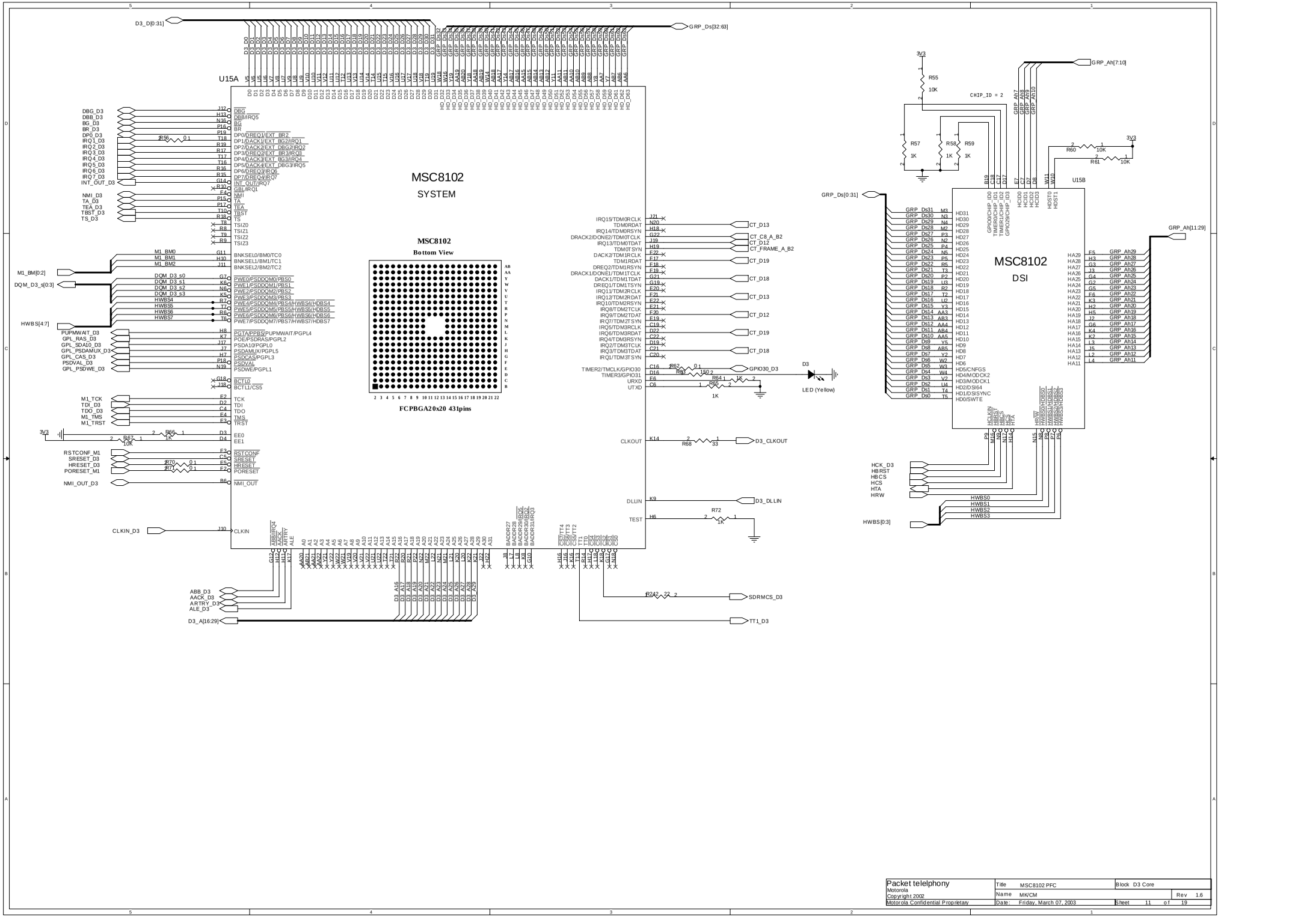
MSC8102
SYSTEM
U15A
MSC8102
Bottom View
FCPBGA20x20 431pins
MSC8102
DSI
U15B
D3_D[0:31]
GRP_Ds[32:63]
GRP_Ah[7:10]
GRP_Ah[11:29]
GRP_Ds[0:31]
CHIP_ID = 2
DBG_D3
DBB_D3
BG_D3
BR_D3
DP0_D3
IRQ1_D3
IRQ2_D3
IRQ3_D3
IRQ4_D3
IRQ5_D3
IRQ6_D3
IRQ7_D3
INT_OUT_D3
NMI_D3
TA_D3
TEA_D3
TBST_D3
TS_D3
M1_BM[0:2]
DQM_D3_s[0:3]
HWBS[4:7]
PUPMWAIT_D3
GPL_RAS_D3
GPL_SDA10_D3
GPL_PSDAMUX_D3
GPL_CAS_D3
PSDVAL_D3
GPL_PSDWE_D3
M1_TCK
TDI_D3
TDO_D3
M1_TMS
M1_TRST
RSTCONF_M1
SRESET_D3
HRESET_D3
PORESET_M1
NMI_OUT_D3
CLKIN_D3
ABB_D3
AACK_D3
ARTRY_D3
ALE_D3
D3_A[16:29]
SDRMCS_D3
TT1_D3
CLKOUT
D3_CLKOUT
DLLIN
D3_DLLIN
TEST
GPIO30_D3
LED (Yellow)
HCK_D3
HBRST
HBCS
HCS
HTA
HRW
HWBS[0:3]
HWBS0
HWBS1
HWBS2
HWBS3
3V3
R55
10K
R57
1K
R58
1K
R59
1K
R60
10K
R61
10K
R56
0.1
R62
0.1
R63
150.2
R64
1K
R65
1K
R66
1K
R67
10K
R68
33
R70
0.1
R71
0.1
R72
1K
R242
22
IRQ15/TDM0RCLK
TDM0RDAT
IRQ14/TDM0RSYN
DRACK2/DONE2/TDM0TCLK
IRQ13/TDM0TDAT
TDM0TSYN
DACK2/TDM1RCLK
TDM1RDAT
DREQ2/TDM1RSYN
DRACK1/DONE1/TDM1TCLK
DACK1/TDM1TDAT
DREQ1/TDM1TSYN
IRQ11/TDM2RCLK
IRQ12/TDM2RDAT
IRQ10/TDM2RSYN
IRQ8/TDM2TCLK
IRQ9/TDM2TDAT
IRQ7/TDM2TSYN
IRQ5/TDM3RCLK
IRQ6/TDM3RDAT
IRQ4/TDM3RSYN
IRQ2/TDM3TCLK
IRQ3/TDM3TDAT
IRQ1/TDM3TSYN
TIMER2/TMCLK/GPIO30
TIMER3/GPIO31
URXD
UTXD
CT_D13
CT_C8_A_B2
CT_D12
CT_FRAME_A_B2
CT_D19
CT_D18
CT_D13
CT_D12
CT_D19
CT_D18
Packet telelphony
Motorola
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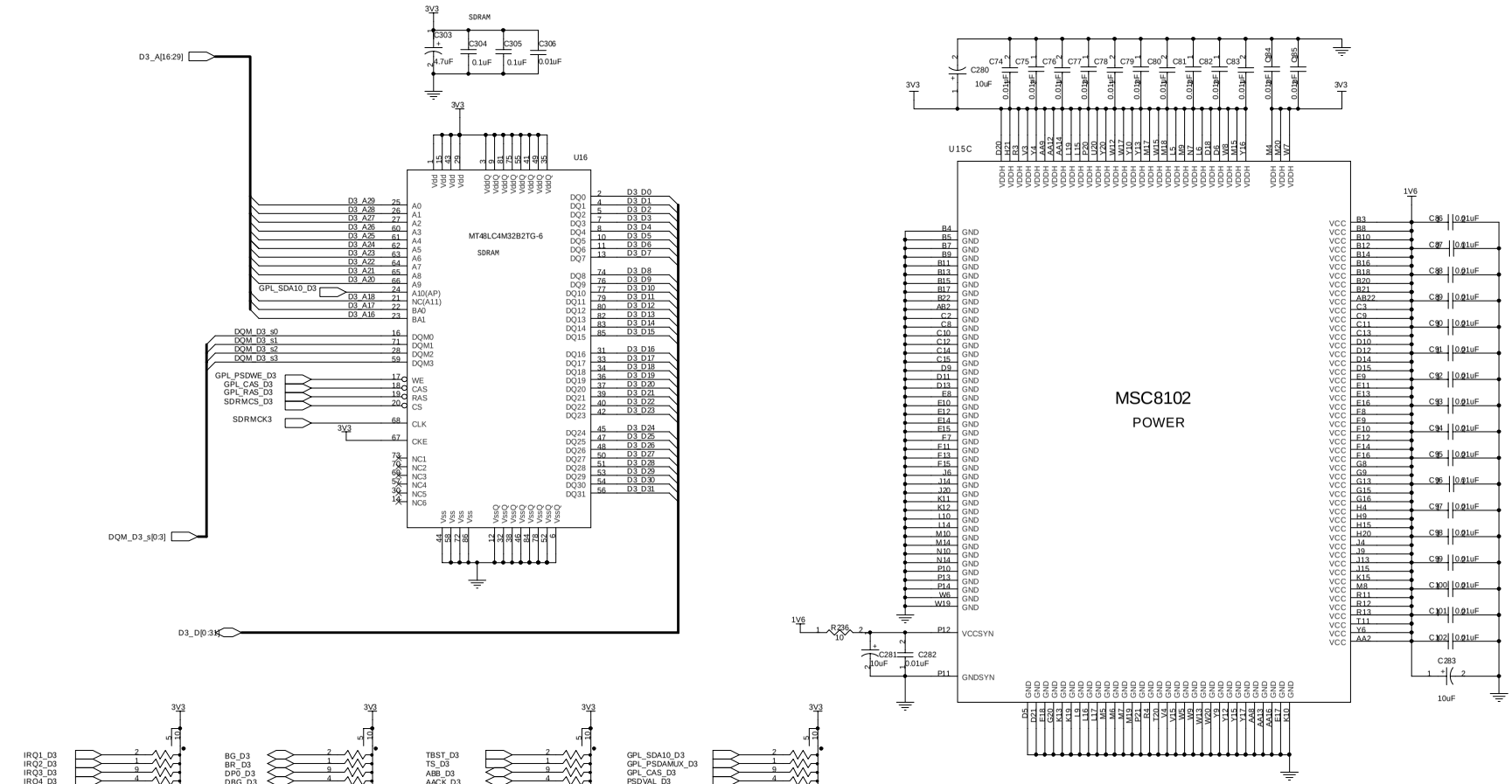
Title MSC8102 PFC
Block D3 Core
Name MK/CM
Rev 1.6
Date: Friday, March 07, 2003
Sheet 11 of 19



Packet telelphony	Title MSC8102 PFC		Block D3 Mem
Motorola	Name MK/CM		Rev 1.6
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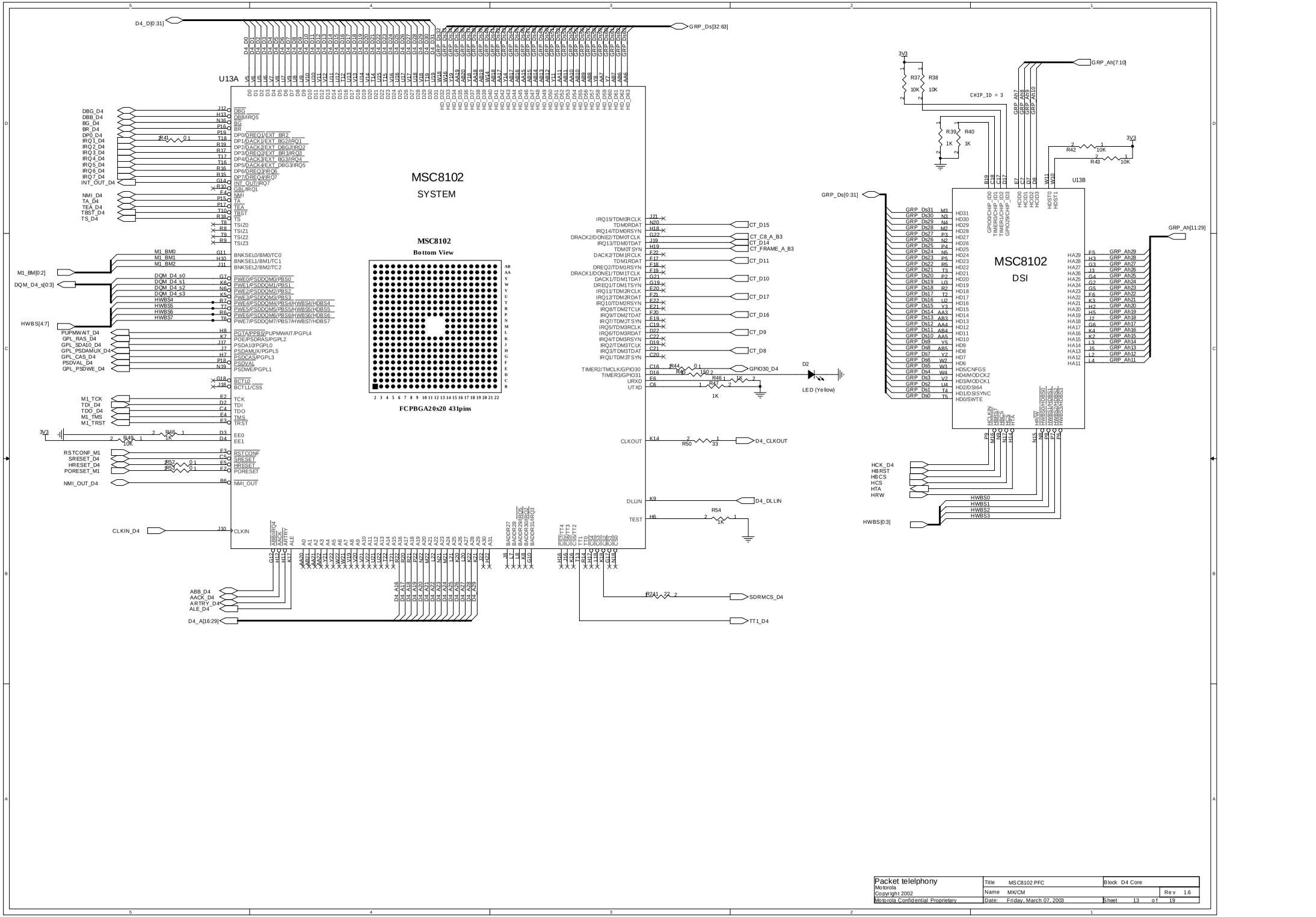
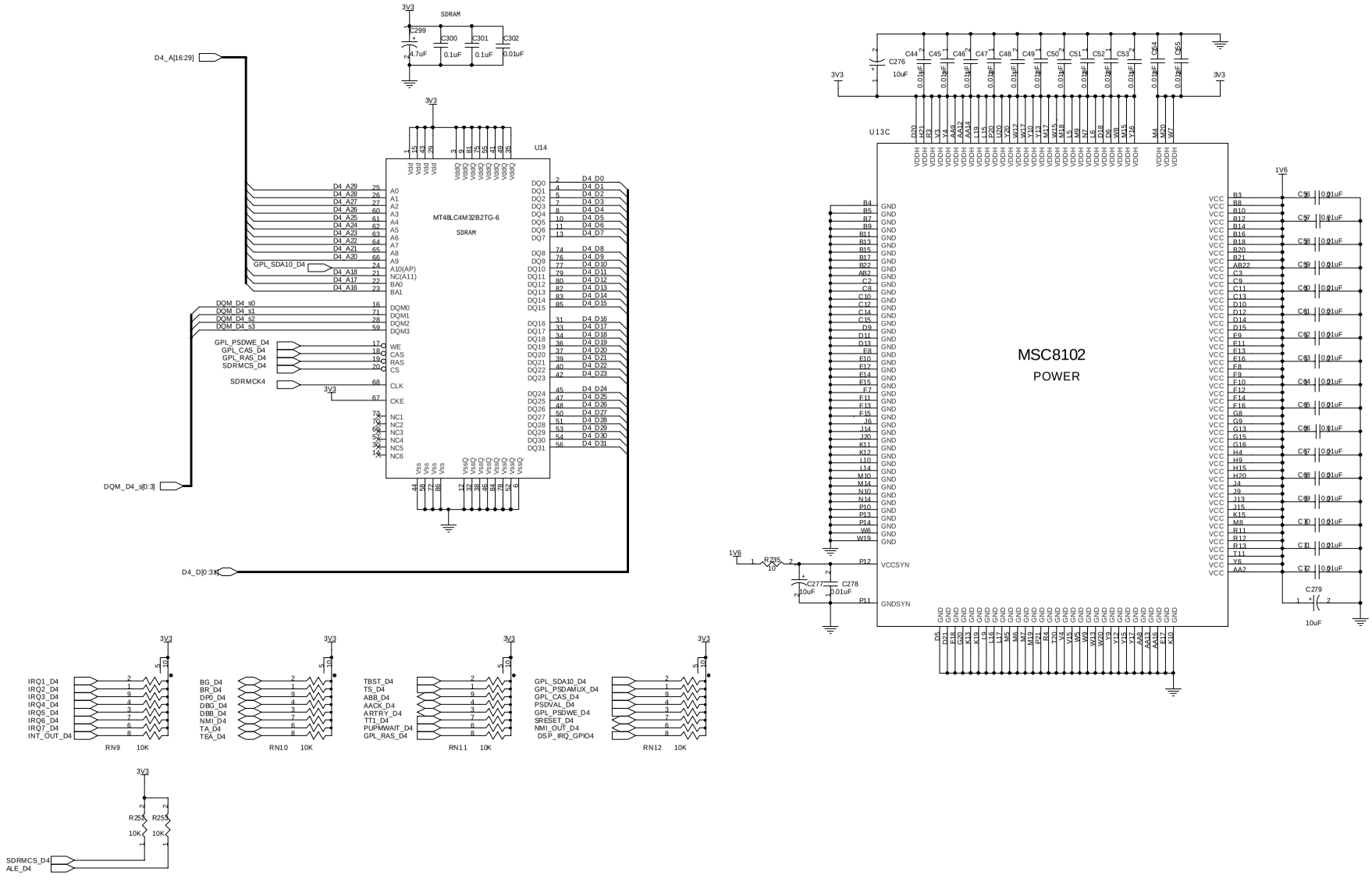


Packet telelphony Motorola Copyright 2002 Motorola Confidential Proprietary	Title MSC8102 PFC		Block D4 Core
	Name MK/CM		Rev 1.6
	Date: Friday, March 07, 2003	Sheet 13	of 19



Packet telelphony	Title MSC8102 PFC		Block D4 Mem
Motorola	Name MK/CM		Rev 1.6
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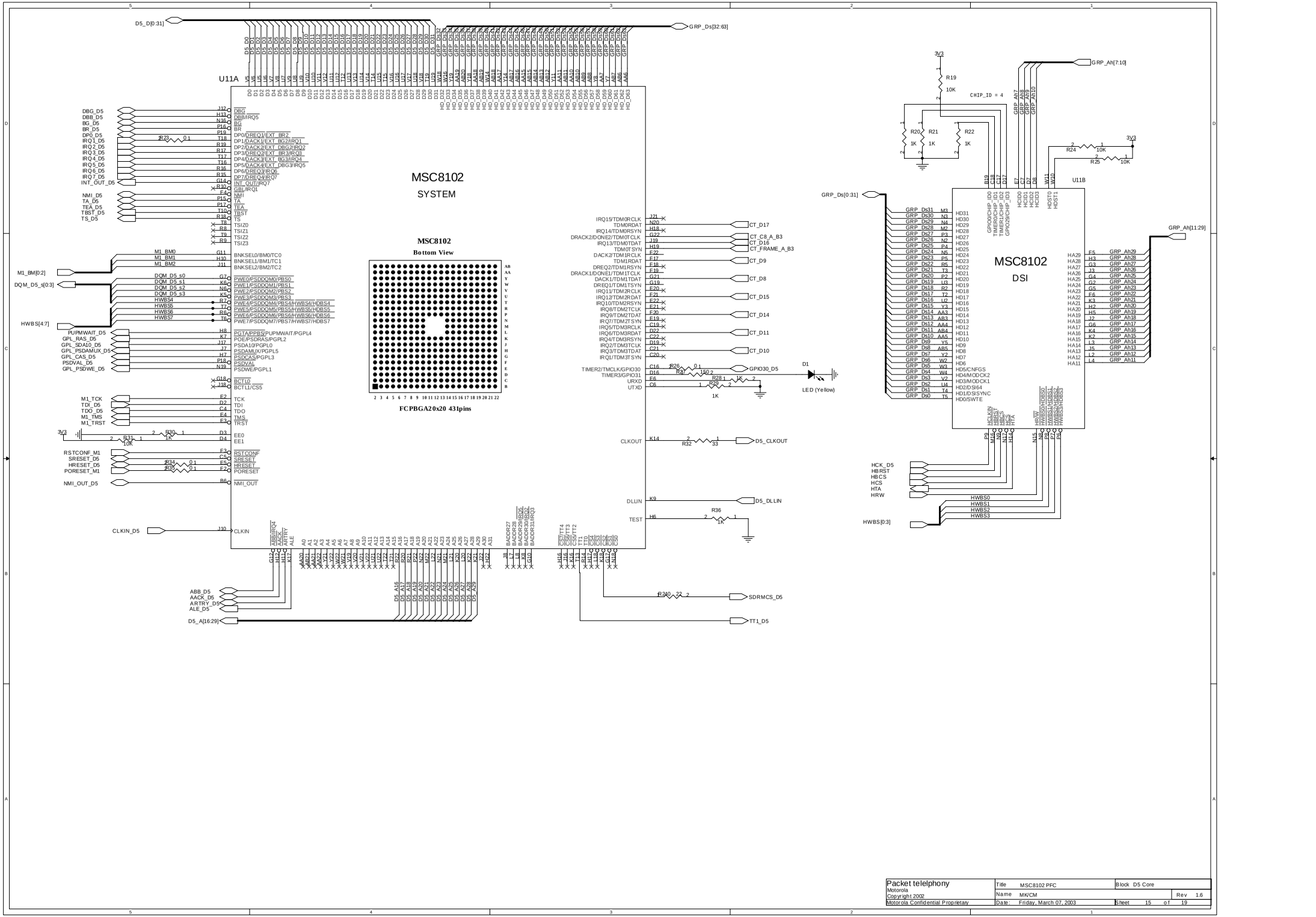
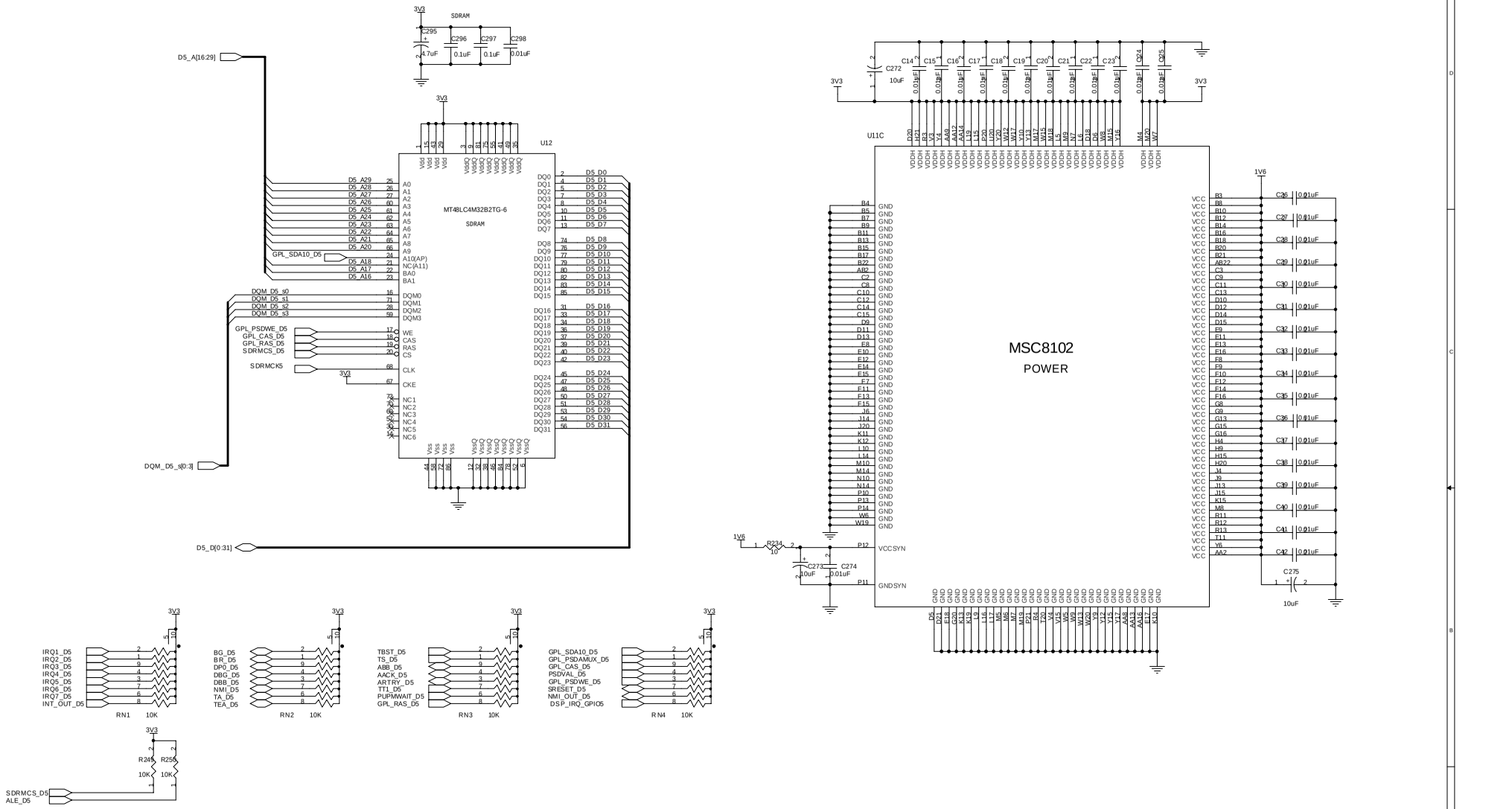
Motorola Confidential Proprietary	Date: Friday, March 07, 2003	Sheet 14 of 19	



Packet telelphony	Title MSC8102 PFC		Block D5 Core
Motorola	Name MK/CM		Rev 1.6
Copyright 2002 Motorola Confidential Proprietary	Date: Friday, March 07, 2003	Sheet 15 of 19	



Packet telelphony	Title MSC8102 PFC		Block D5 Mem
Motorola	Name MK/CM		Rev 1.6
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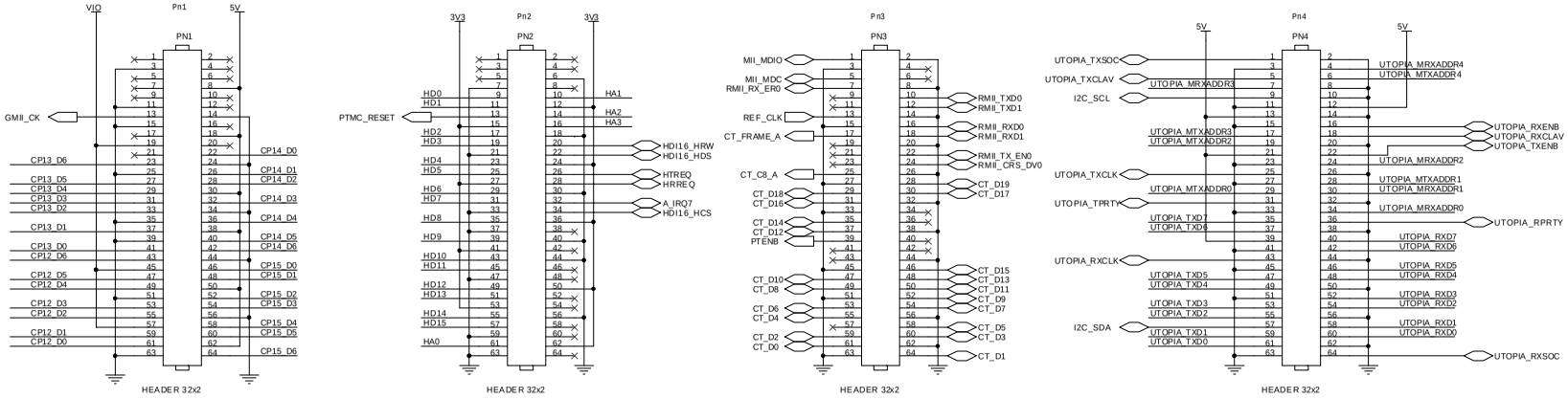
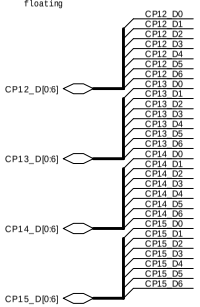
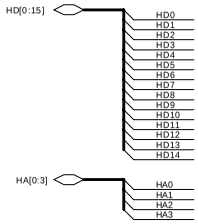
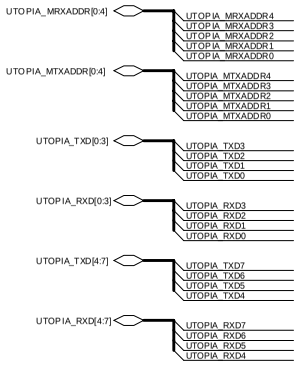
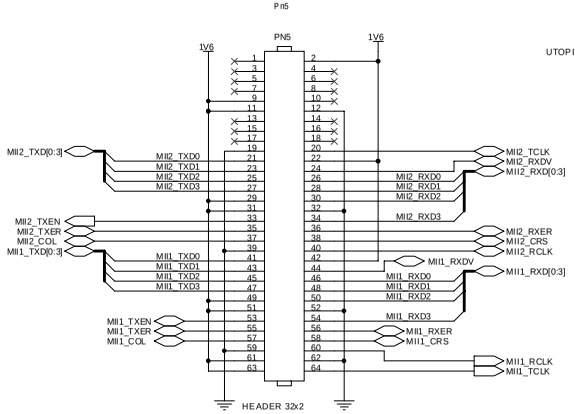


PTMC Type III enabled by tying PTID1/2 to V(IO) and leaving PTID0 floating

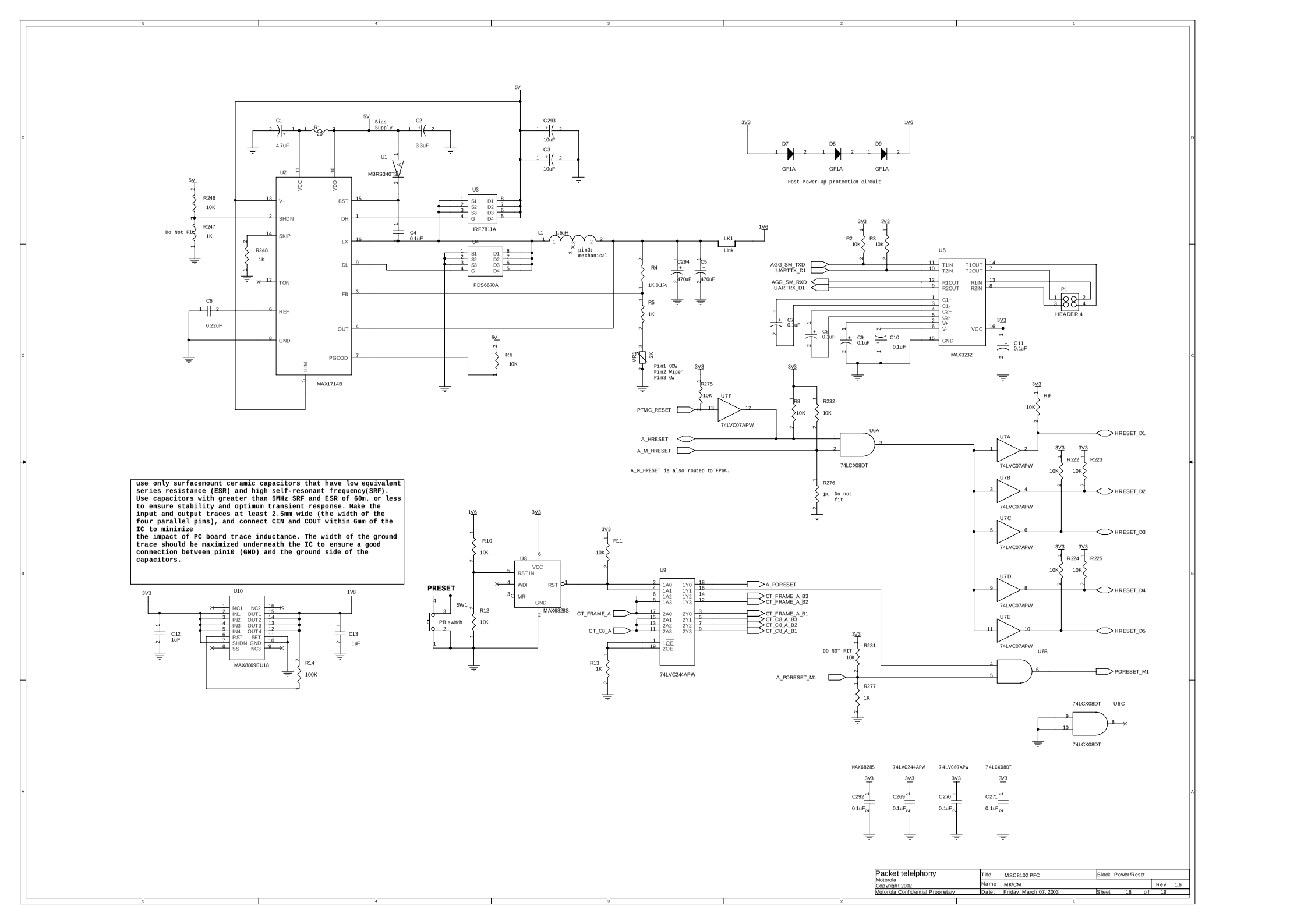








Packet telelphony Motorola Copyright 2001 Motorola Confidential Proprietary	Title MSC8102 PFC	Block PTMC Connectors	
	Name MK/CM		Rev 1.6
	Date: Friday, March 07, 2003	Sheet 17 of 19	


5V
C1
4.7uF
R1
20
Bias Supply
C2
3.3uF
U1
MBRS340T3
C293
10uF
C3
10uF
U2
VCC
VDD
V+
SHDN
SKIP
TON
REF
GND
BST
DH
LX
DL
FB
OUT
PGOOD
ILIM
MAX1714B
R246
10K
R247
1K
Do Not Fit
R248
1K
C6
0.22uF
C4
0.1uF
U3
IRF7811A
U4
FDS6670A
L1
1.5uH
pin3: mechanical
LK1
Link
1V6
R4
1K 0.1%
R5
1K
VR1
2K
Pin1 CCW
Pin2 Wiper
Pin3 CW
C294
470uF
C5
470uF
R6
10K
3V3
D7
D8
D9
GF1A
Host Power-Up protection circuit
R2
10K
R3
10K
U5
AGG_SM_TXD
UARTTX_D1
AGG_SM_RXD
UARTRX_D1
T1IN
T2IN
R1OUT
R2OUT
T1OUT
T2OUT
R1IN
R2IN
C1+
C1-
C2+
C2-
V+
V-
VCC
GND
MAX3232
C7
0.1uF
C8
0.1uF
C9
0.1uF
C10
0.1uF
C11
0.1uF
P1
HEADER 4
R275
10K
U7F
74LVC07APW
PTMC_RESET
A_HRESET
A_M_HRESET
R8
10K
R232
10K
U6A
74LCX08DT
A_M_HRESET is also routed to FPGA.
R276
1K
Do not fit
R9
10K
U7A
U7B
U7C
U7D
U7E
U6B
R222
10K
R223
10K
R224
10K
R225
10K
HRESET_D1
HRESET_D2
HRESET_D3
HRESET_D4
HRESET_D5
R231
10K
R277
1K
DO NOT FIT
A_PORESET_M1
PORESET_M1
U6C
74LCX08DT
use only surfacemount ceramic capacitors that have low equivalent series resistance (ESR) and high self-resonant frequency(SRF). Use capacitors with greater than 5MHz SRF and ESR of 60m. or less to ensure stability and optimum transient response. Make the input and output traces at least 2.5mm wide (the width of the four parallel pins), and connect CIN and COUT within 6mm of the IC to minimize the impact of PC board trace inductance. The width of the ground trace should be maximized underneath the IC to ensure a good connection between pin10 (GND) and the ground side of the capacitors.
U10
MAX8869EU18
NC1
NC2
IN1
OUT1
IN2
OUT2
IN3
OUT3
IN4
OUT4
RST
SET
SHDN
GND
SS
NC3
C12
1uF
C13
1uF
R14
100K
1V8
PRESET
SW1
PB switch
R10
10K
R12
10K
U8
MAX6828S
VCC
RST IN
WDI
RST
MR
GND
R11
10K
U9
74LVC244APW
1A0
1A1
1A2
1A3
2A0
2A1
2A2
2A3
1Y0
1Y1
1Y2
1Y3
2Y0
2Y1
2Y2
2Y3
1OE
2OE
A_PORESET
CT_FRAME_A_B3
CT_FRAME_A_B2
CT_FRAME_A_B1
CT_C8_A_B3
CT_C8_A_B2
CT_C8_A_B1
CT_FRAME_A
CT_C8_A
R13
1K
MAX6828S
74LVC244APW
74LVC07APW
74LCX08DT
C292
0.1uF
C269
0.1uF
C270
0.1uF
C271
0.1uF
Packet telelphony
Motorola
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Title MSC8102 PFC
Block Power/Reset
Name MK/CM
Rev 1.6
Date: Friday, March 07, 2003
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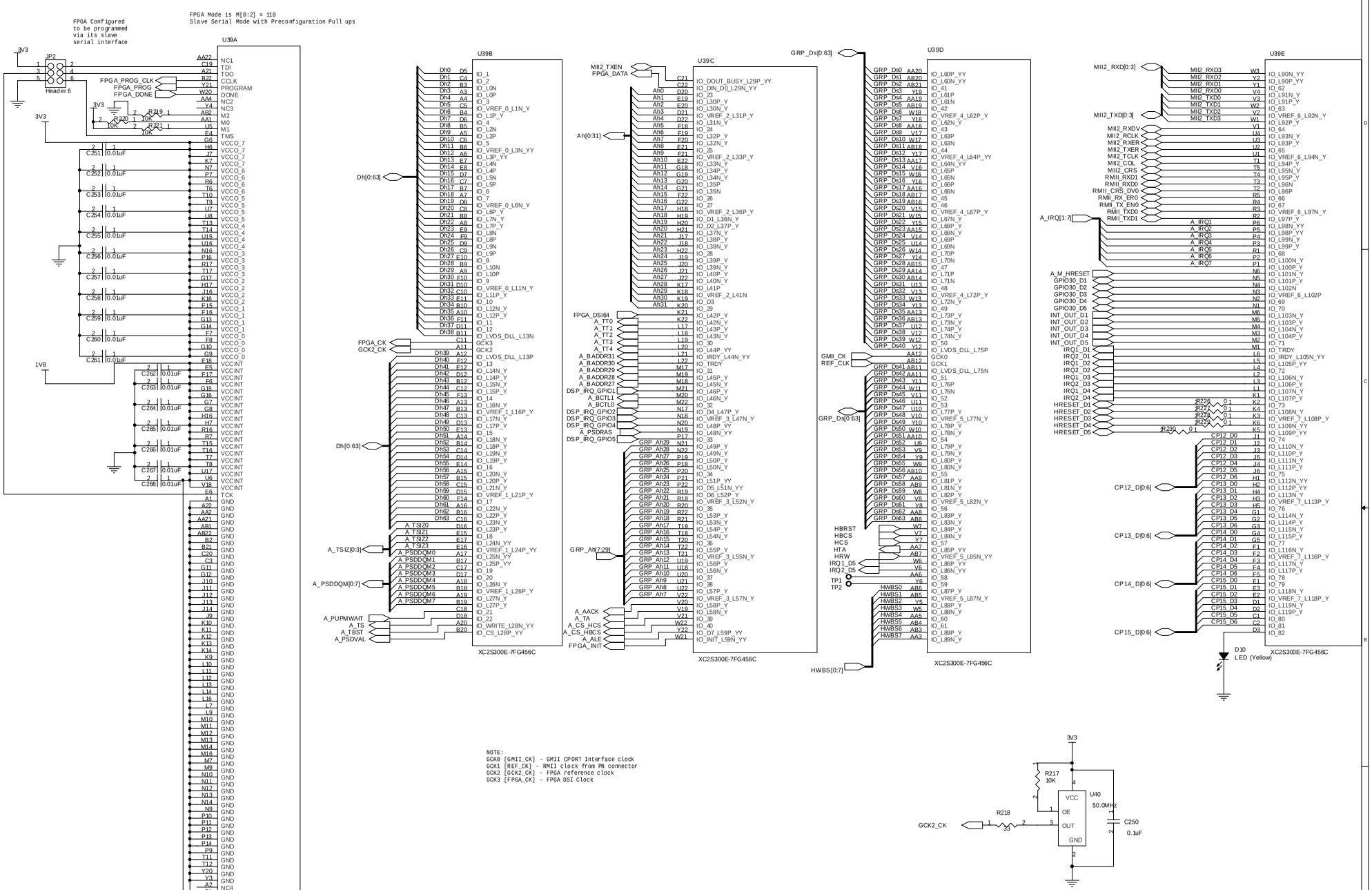

Packet telelphony	Title MSC8102 PFC	Block FPGA	
Motorola	Name MK/CM		Rev 1.6
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