

MSF18N50

500V N-Channel MOSFET

Description

The MSF18N50 is a N-channel enhancement-mode MOSFET, providing the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost effectiveness. The ITO-220AB package is universally preferred for all commercial-industrial applications.

Features

- Originative New Design
- Very Low Intrinsic Capacitances
- Excellent Switching Characteristics
- 100% EAS Test
- Extended Safe Operating Area
- RoHS compliant package

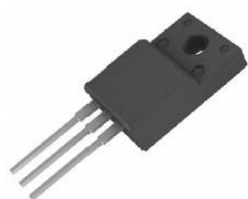
Application

- High current, High speed switching
- PFC (Power Factor Correction)

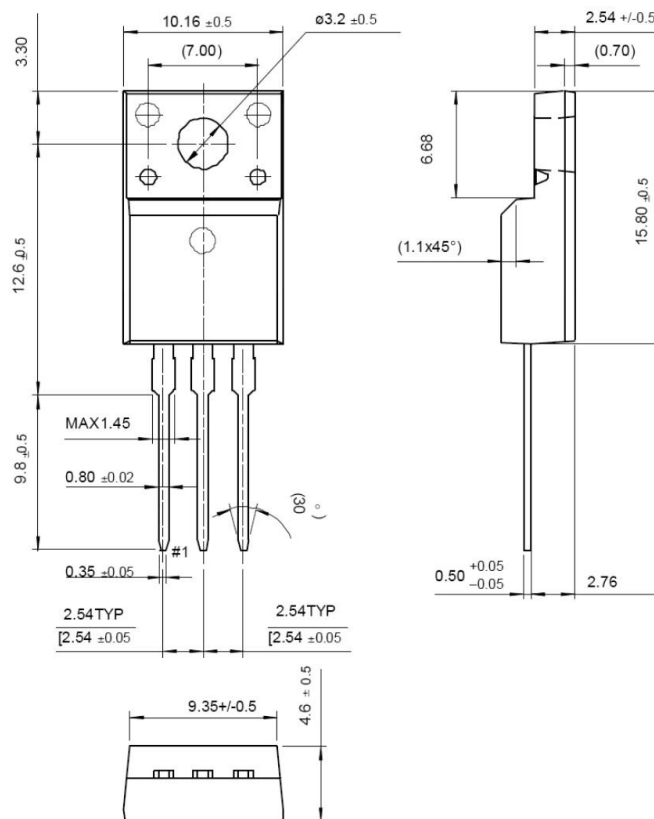
Package type : ITO220-AB

Packing & Order Information

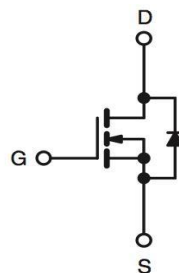
50/Tube ; 1,000/Box



**RoHS
COMPLIANT**



Graphic symbol



MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (Tc=25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V _{DS}	Drain-Source Voltage	500	V
V _{GS}	Gate-Source Voltage	±30	V
I _D	Drain Current -Continuous (TC=25°C)	18	A
	Drain Current -Continuous (TC=100°C)	10.8	A
I _{DM}	Drain Current Pulsed	72	A
E _{AS}	Single Pulsed Avalanche Energy	990	mJ
E _{AR}	Repetitive Avalanche Energy	23.5	mJ
dV/dt	Peak Diode Recovery dV/dt	4.5	V/ns
P _D	Power Dissipation (TC = 25 °C)	235	W
	Power Dissipation (TC=100°C)	1.8	W/°C

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Absolute Maximum Ratings (Tc=25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C

NOTE:

1. Repetitive Rating: Pulse width limited by maximum junction temperature

Thermal characteristics (Tc=25°C unless otherwise noted)

Symbol	Parameter	Max.	Units
R _{thjc}	Typical thermal resistance	0.53	°C/W
R _{θJA}		62.5	

Static Characteristics

Symbol	Test Conditions	Min	Typ.	Max.	Units
V _{GS}	V _{DS} = V _{GS} , I _D =250μA	3.0		5.0	V
*R _{DS(ON)}	V _{GS} =10V, I _D =9.0A	--	0.25	0.32	Ω
BV _{DSS}	V _{GS} =0 V, I _D =250μA	500	--	--	V
ΔBV _{DSS} / ΔT _J	I _D =250μA, Referenced to 25°C		0.6		
I _{DSS}	V _{DS} =500V, V _{GS} = 0 V V _{DS} =400V, V _{GS} = 0 V, T _J = 125°C	--	--	1 10	uA
I _{GSSF}	V _{DS} =30V, V _{DS} =0 V			100	nA
I _{GSSR}	V _{DS} =-30V, V _{DS} =0 V	--	--	-100	nA

Dynamic Characteristics

Symbol	Test Conditions	Min	Typ.	Max.	Units
Q _g	V _{DS} =400V, I _D =18A, V _{GS} =10 V	--	48.5	--	nC
Q _{gs}		--	14	--	
Q _{gd}		--	22	--	
t _{d(on)}	V _{DS} =250 V, I _D =18A, R _G =25Ω	--	70	--	ns
t _r		--	190	--	ns
t _{d(off)}		--	100	--	ns
t _f		--	100	--	ns
C _{ISS}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz	--	2500	--	pF
C _{OSS}		--	400	--	pF
C _{RSS}		--	40	--	pF

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Source-Drain Diode Characteristics					
Symbol	Test Conditions	Min	Typ.	Max.	Units
I_S		--	--	18	A
I_{SM}		--	--	72	
V_{SD}	$I_F=18A, V_{GS}=0$	--	--	1.5	V
t_{rr}	$I_F=18A, V_{GS}=0, di/dt=100A/\mu s$	--	550	--	ns
Q_{rr}		--	5.5	--	uC

Notes;

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $L=5.5mH, I_{AS}=18A, V_{DD}=50V, R_G=25\Omega$, Starting $T_J=25^\circ C$
3. $I_{SD} \leq 16A, di/dt \leq 200A/\mu s, V_{DD} \leq BV_{DSS}$, Starting $T_J=25^\circ C$
4. Pulse Test: Pulse Width $\leq 300 \mu s$, Duty Cycle $\leq 2\%$
5. Essentially Independent of Operating Temperature

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■ Characteristics Curve

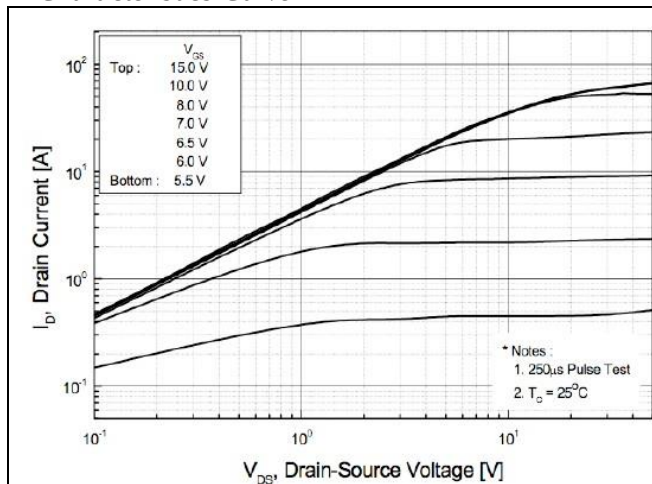


FIG.1-ON REGION CHARACTERISTICS

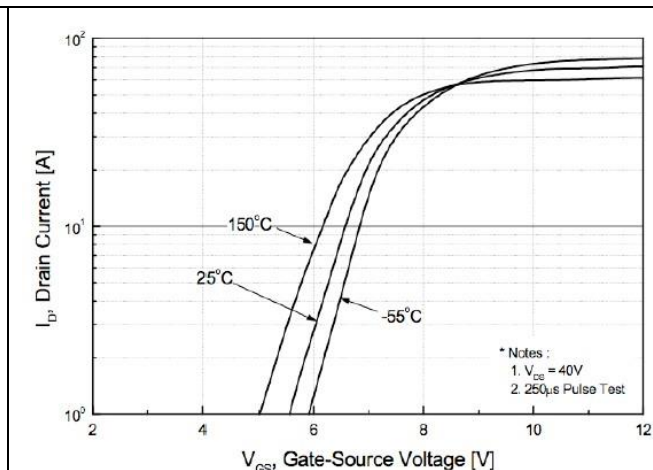


FIG.2-TRANSFER CHARACTERISTICS

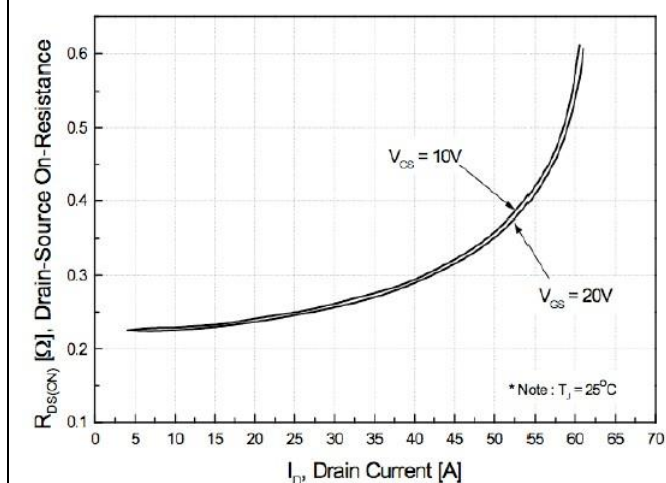


FIG.3-ON RESISTANCE VARIATION VS DRAIN CURRENT AND GATE VOLTAGE

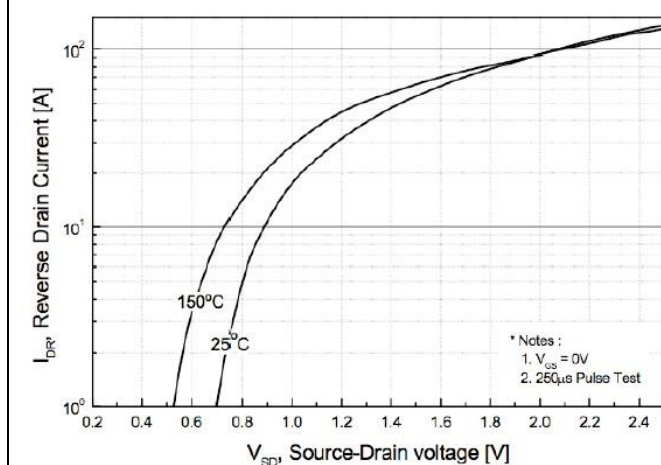


FIG.4-BODY DIODE FORWARD VOLTAGE VARIATION WITH SOURCE CURRENT AND TEMPERATURE

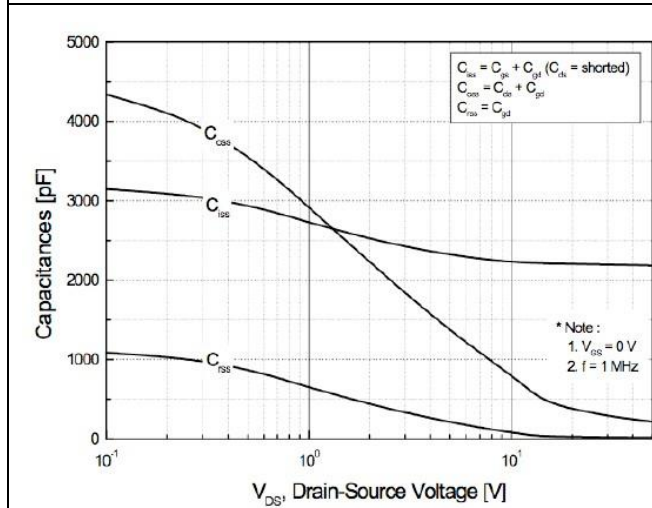


FIG.5-CAPACITANCE CHARACTERISTICS

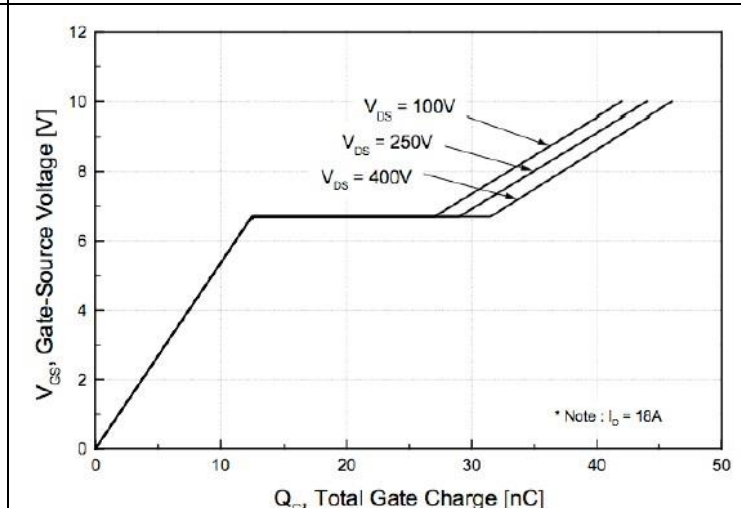


FIG.6-GATE CHARGE CHARACTERISTICS

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■ Characteristics Curve

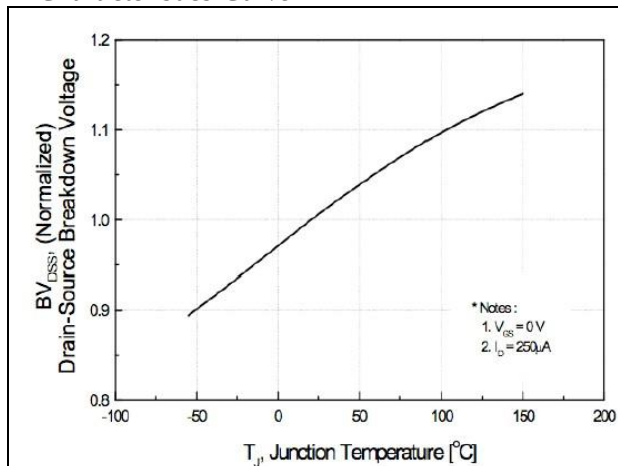


FIG.7-BREAKDOWN VOLTAGE VARIATION VS TEMPERATURE

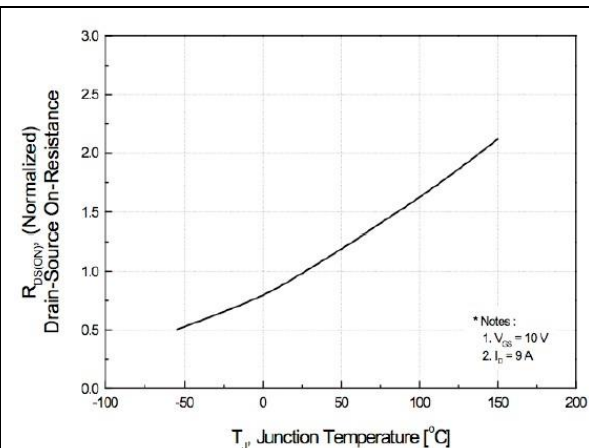


FIG.8-ON-RESISTANCE VARIATION VS TEMPERATURE

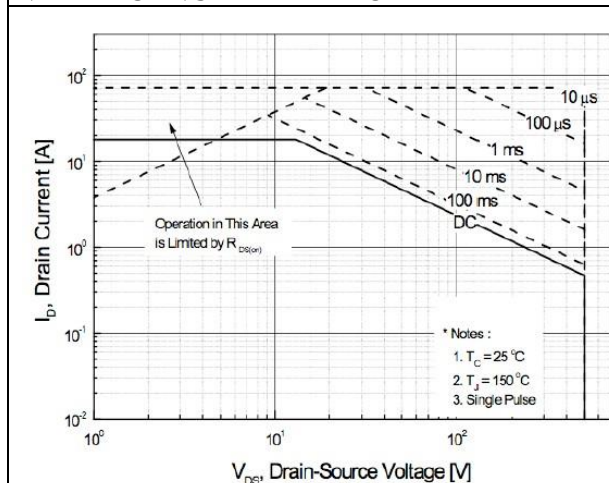


FIG.9-MAXIMUM SAFE OPERATING AREA

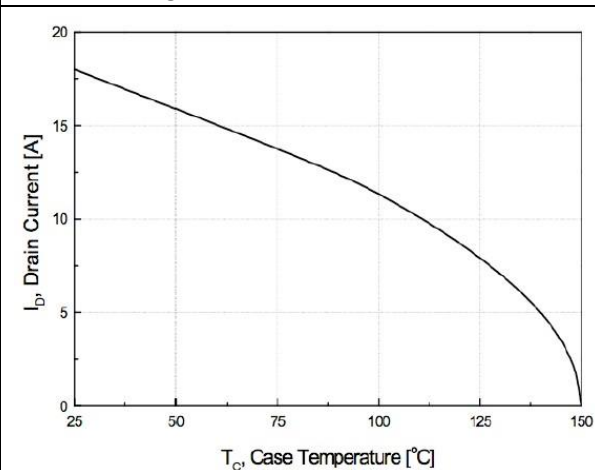


FIG.10-MAXIMUM DRAIN CURRENT VS CASE TEMPERATURE

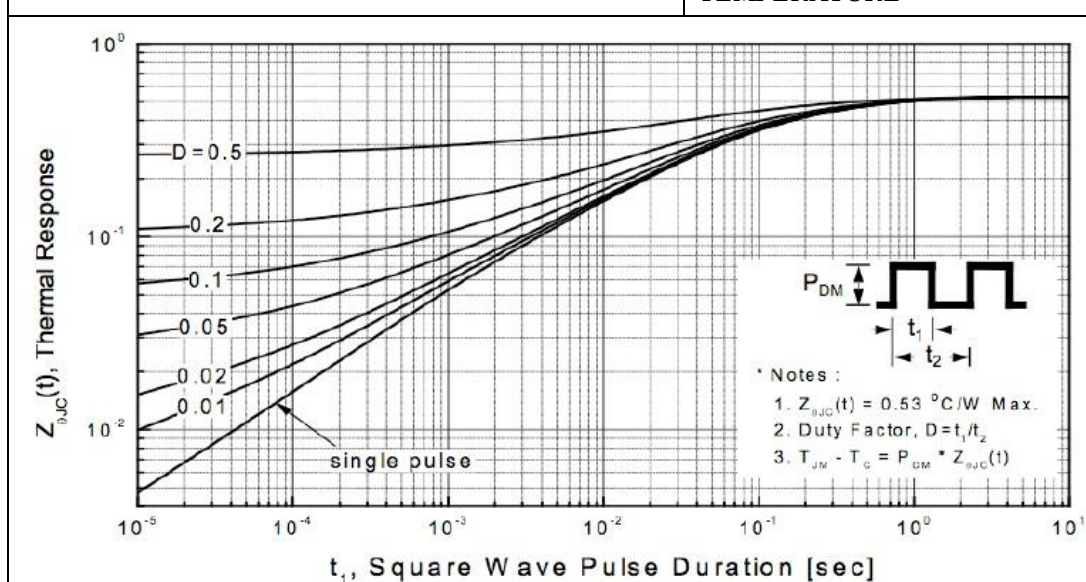


FIG.11-TRANSIENT THERMAL RESPONSE CURVE

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■ Characteristics Test Circuit & Waveform

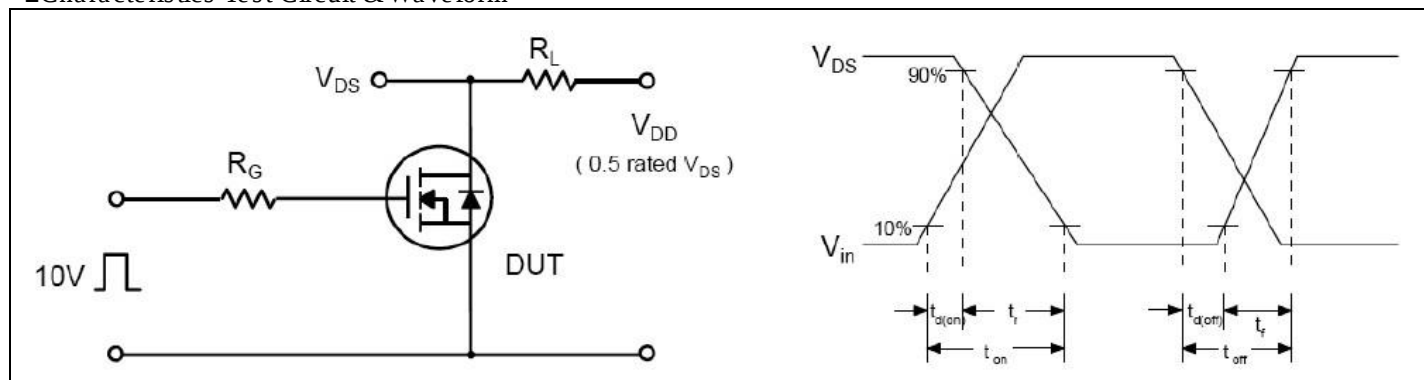


Fig 12. Resistive Switching Test Circuit & Waveforms

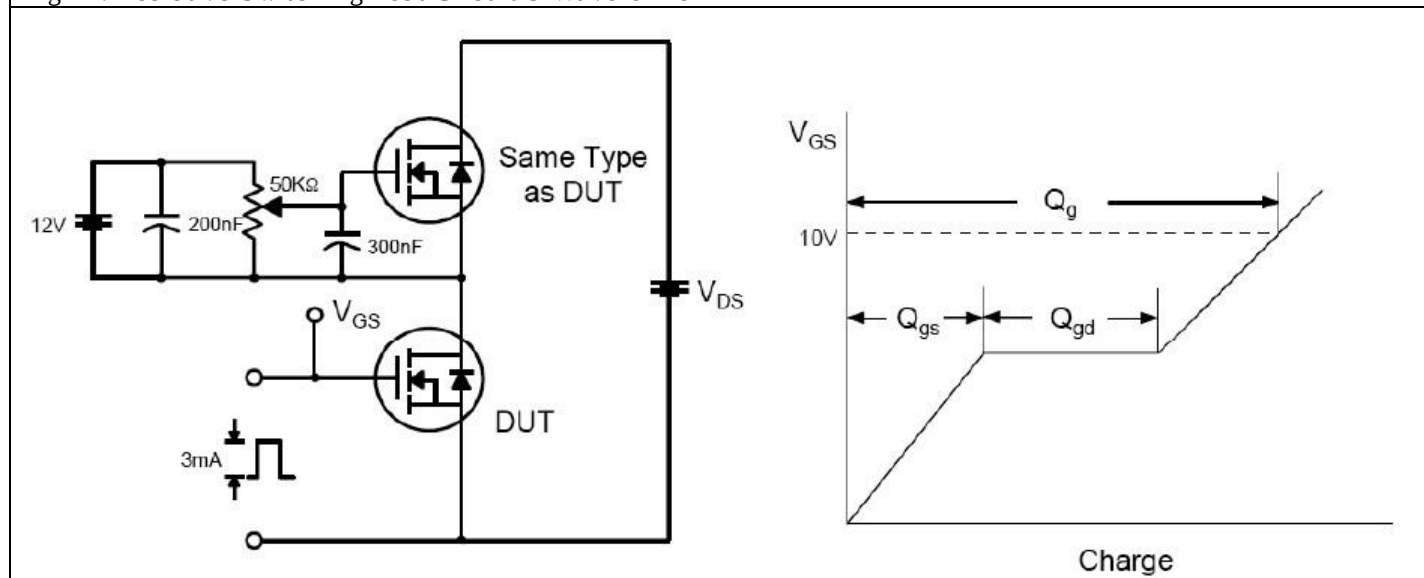


Fig 13. Gate Charge Test Circuit & Waveform

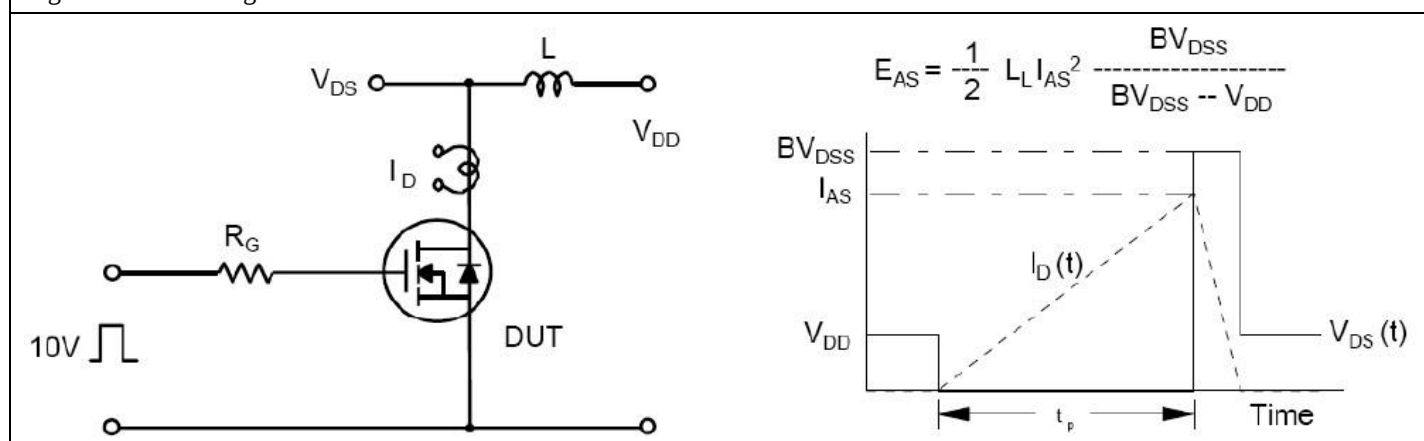


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

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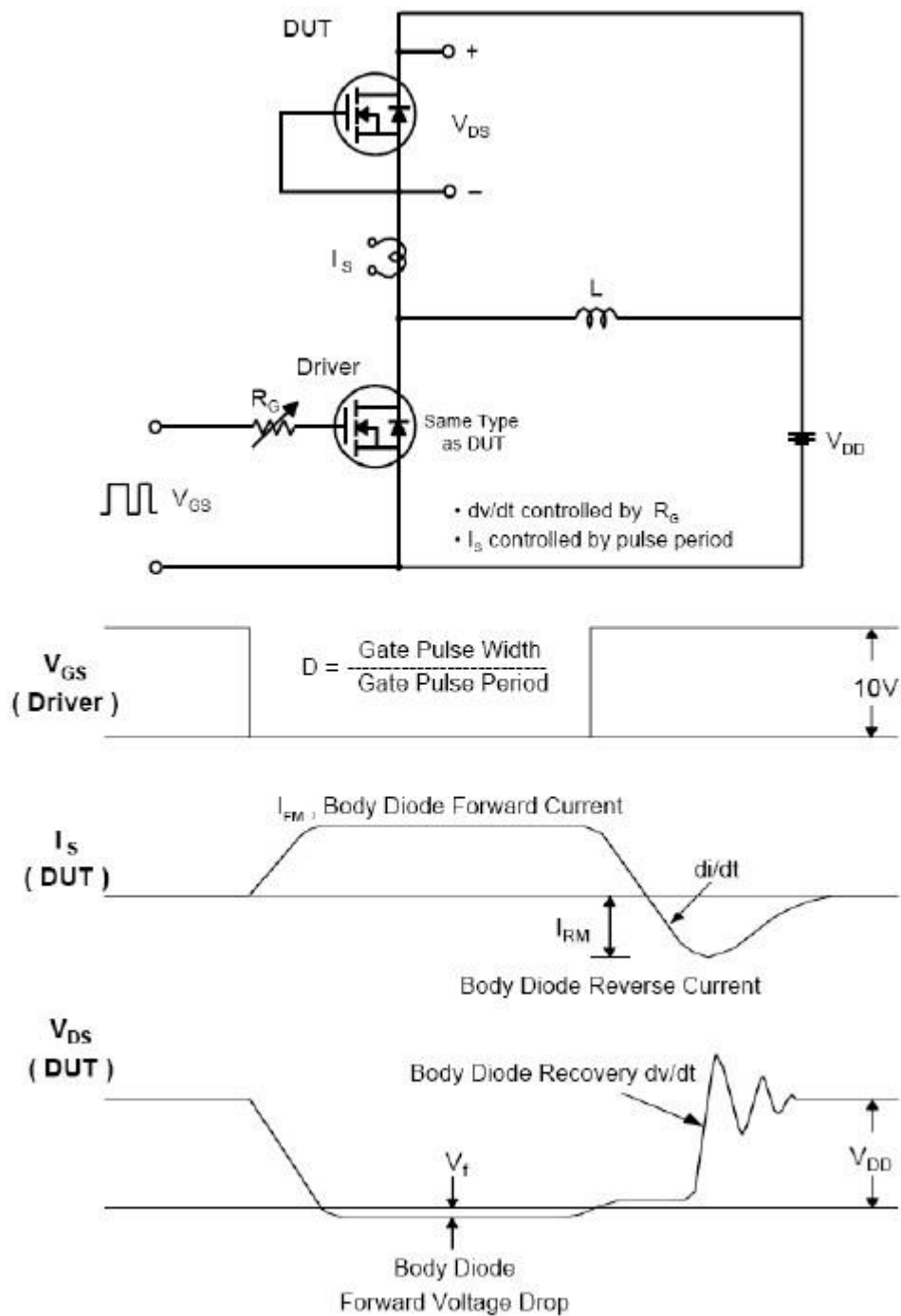


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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