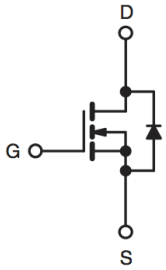
MSF8N80-G 800V N-Channel MOSFET

GENERAL DESCRIPTION

This Power MOSFET is produced using the advanced planar stripe, DMOS technology. This latest technology has been especially designed to minimize on-state resistance, have high rugged avalanche characteristics. These devices are well suited for high efficiency switch mode power supplies, active power factor correction, and electronic lamp ballasts based on half bridge topology.



RoHS
COMPLIANT

HALOGEN
FREE
Avaliable

FEATURES

- RDS(on) (typ 1.3 Ω)@VGS=10V
- Gate Charge (Typical 39nC)
- Improved dv/dt Capability, High Ruggedness
- 100% Avalanche Tested
- Maximum Junction Temperature Range (150°C)
- Halogen Free

Absolute Maximum Ratings (Tc=25°C unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-Source Voltage	800	V
I_D	Drain Current -Continuous (T_C=25°C)	8	A
	Drain Current -Continuous (T_C=100°C)	5.0	A
I_{DM}	Drain Current -Pulsed	32	A
V_{GS}	Gate-Source Voltage	±30	V
E_{AS}	Single Pulsed Avalanche Energy	850	mJ
E_{AR}	Repetitive Avalanche Energy	17.8	mJ
d_v/d_t	Peak Diode Recovery dv/dt	4.5	V/ns
P_D	Power Dissipation (T_C=25°C)	59	W
	- Derate above 25°C	0.48	W/°C
T_J,T_{STG}	Operating and Storage Temperature Range	–55 to + 150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	°C

• Drain current limited by maximum junction temperature

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Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	2.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	62.5	

Electrical Characteristics (Tc=25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Type	Max	Units
On Characteristics						
V_{GS}	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	3.0	--	5.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V,I_D=4.0A	—	1.3	1.6	Ω
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0 V , I_D=250μA	800	—	—	V
$\triangle BV_{DSS}$ /$\triangle T_J$	Breakdown Voltage Temperature Coefficient	I_D=250μA, Referenced to 25°C	—	0.6	—	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=800V , V_{GS}= 0 V	—	—	10	μA
		V_{DS}=640V , V_C= 125°C	—	—	100	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS}=30V , V_{DS}=0 V	—	—	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS}=-30V , V_{DS}=0 V	—	—	–100	nA
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS}=25V, V_{GS}=0V, f=1.0MHz	—	1700	—	pF
C_{oss}	Output Capacitance		—	140	—	pF
C_{rss}	Reverse Transfer Capacitance		—	15	—	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Time	V_{DS}=400 V, I_D=8.0A, R_G=25Ω	—	50	--	ns
t_r	Turn-On Rise Time		—	100	--	ns
$t_{d(off)}$	Turn-Off Delay Time		—	70	--	ns
tf	Turn-Off Fall Time		—	70	--	ns
Q_g	Total Gate Charge	V_{DS}=640V,I_D=8.0A, V_{GS}=10 V	—	37	--	nC
Q_{gs}	Gate-Source Charge		—	11	—	nC
Q_{gd}	Gate-Drain Charge		—	15	—	nC

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Source-Drain Diode Maximum Ratings and Characteristics

I_S	Continuous Source-Drain Diode Forward Current		—	—	8.0	A
I_{SM}	Pulsed Source-Drain Diode Forward Current		—	—	32.0	
V_{SD}	Source-Drain Diode Forward Voltage	I_S=8A, V_{GS}=0V	—	—	1.4	V
trr	Reverse Recovery Time	I_S=8 A , V_{GS}= 0V	—	0.7	—	us
Qrr	Reverse Recovery Charge	di_F/dt=100A/μs	—	8.0	—	μC

Notes:

1. Repeativity rating : pulse width limited by junction temperature
2. L = 25.0mH, IAS =8.0A, VDD = 50V, RG = 25Ω , Starting TJ = 25°C
3. ISD ≤ 8.0A, di/dt ≤ 200A/us, VDD ≤ BVDSS, Starting TJ = 25°C
4. Pulse Test : Pulse Width ≤ 300us, Duty Cycle ≤ 2%
5. Essentially independent of operating temperature.

- **Characteristic Curves**

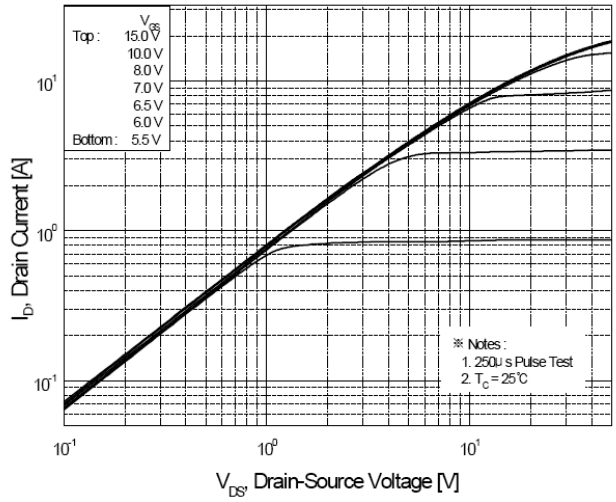

Figure 1. On Region Characteristics

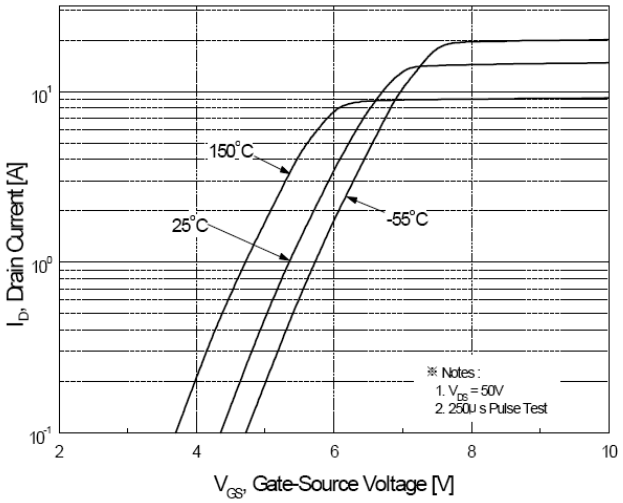

Figure 2. Transfer Characteristics

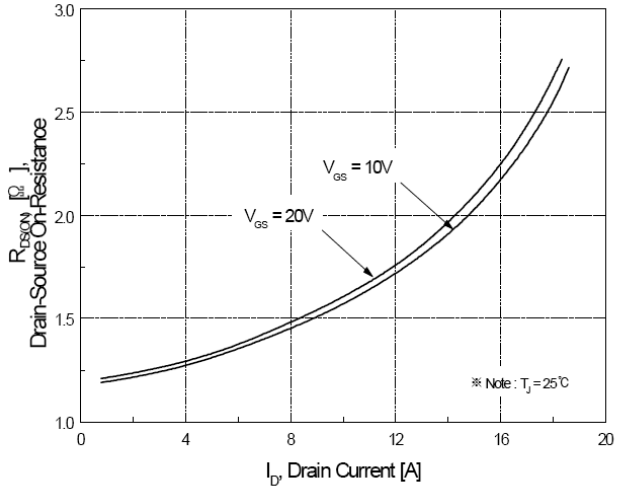

Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

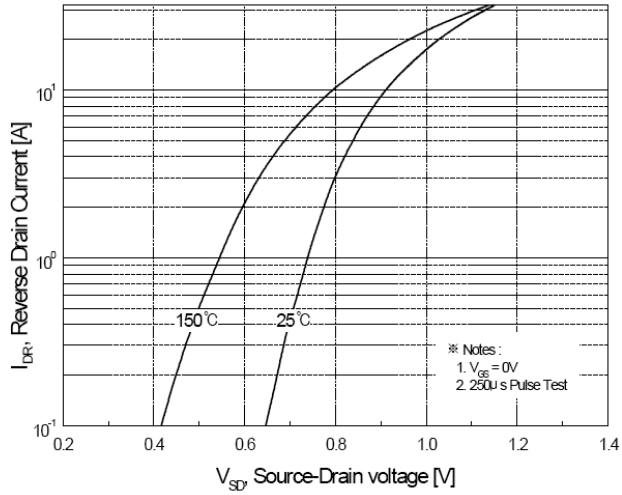

Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

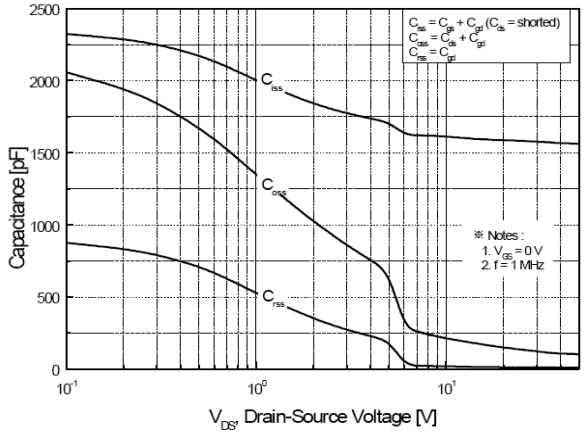

Figure 5. Capacitance Characteristics

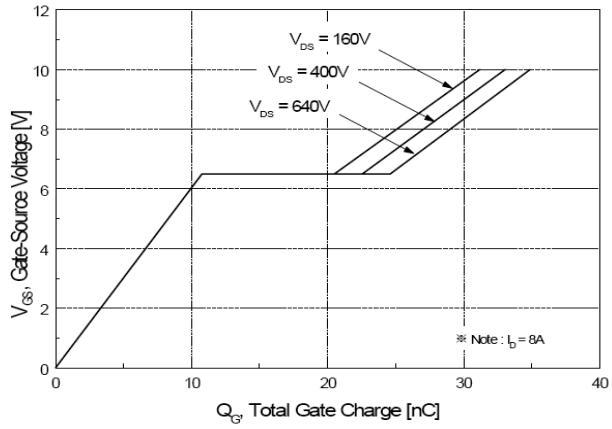

Figure 6. Gate Charge Characteristics

- **Characteristic Curves**

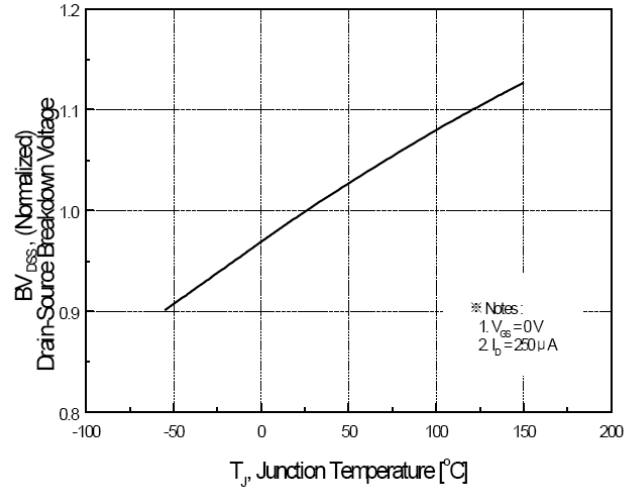

Figure 7. Breakdown Voltage Variation vs Temperature

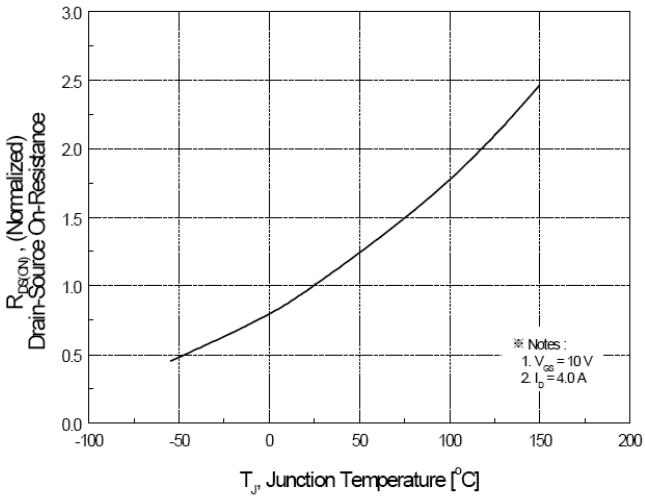

Figure 8. On-Resistance Variation vs Temperature

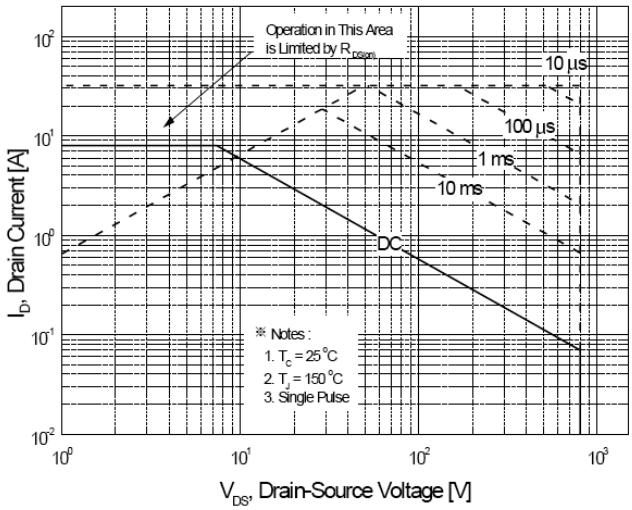

Figure 9. Maximum Safe Operating Area

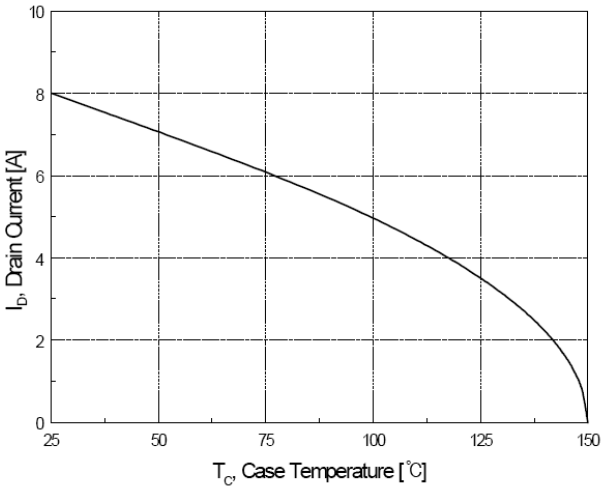

Figure 10. Maximum Drain Current vs Case Temperature

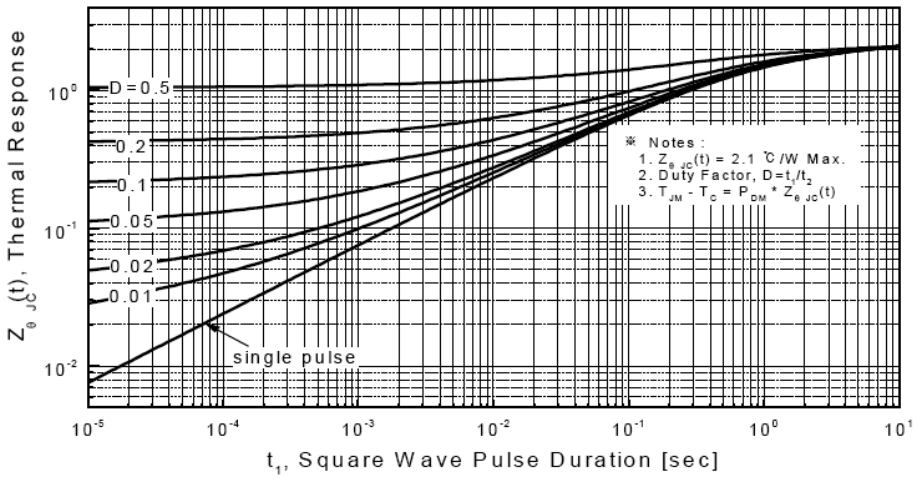

Figure 11. Transient Thermal Response Curve

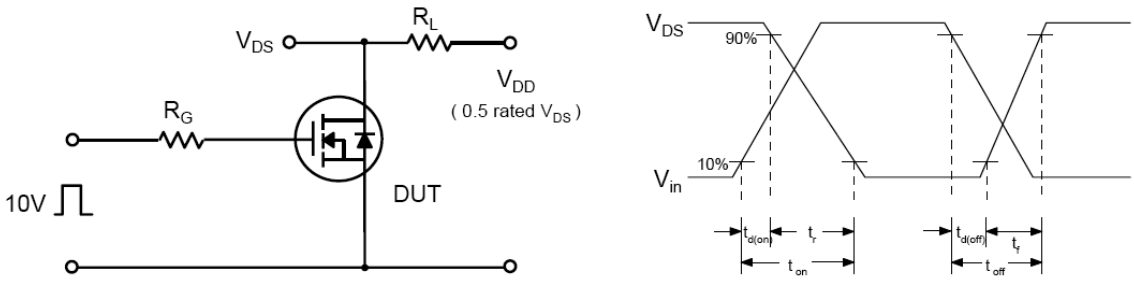

Fig 12. Resistive Switching Test Circuit & Waveforms

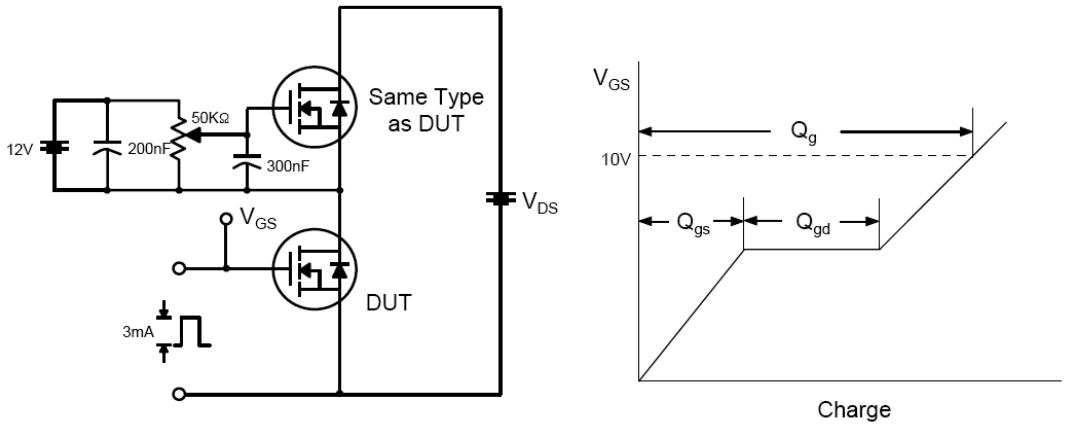

Fig 13. Gate Charge Test Circuit & Waveform

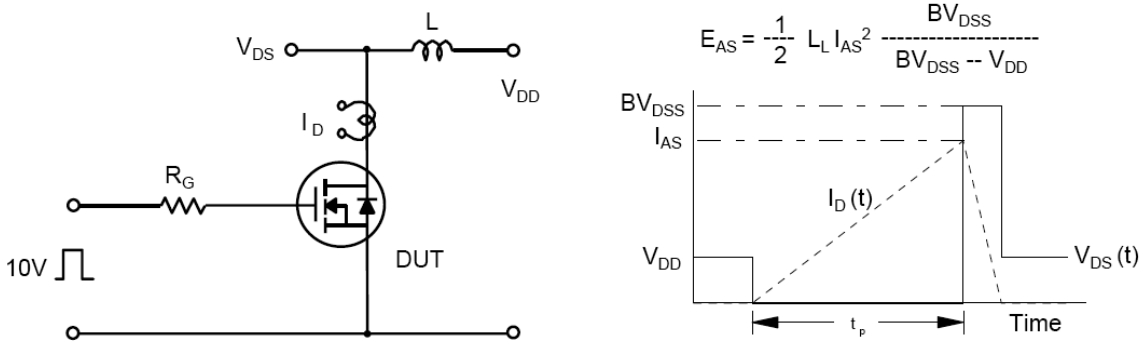

Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

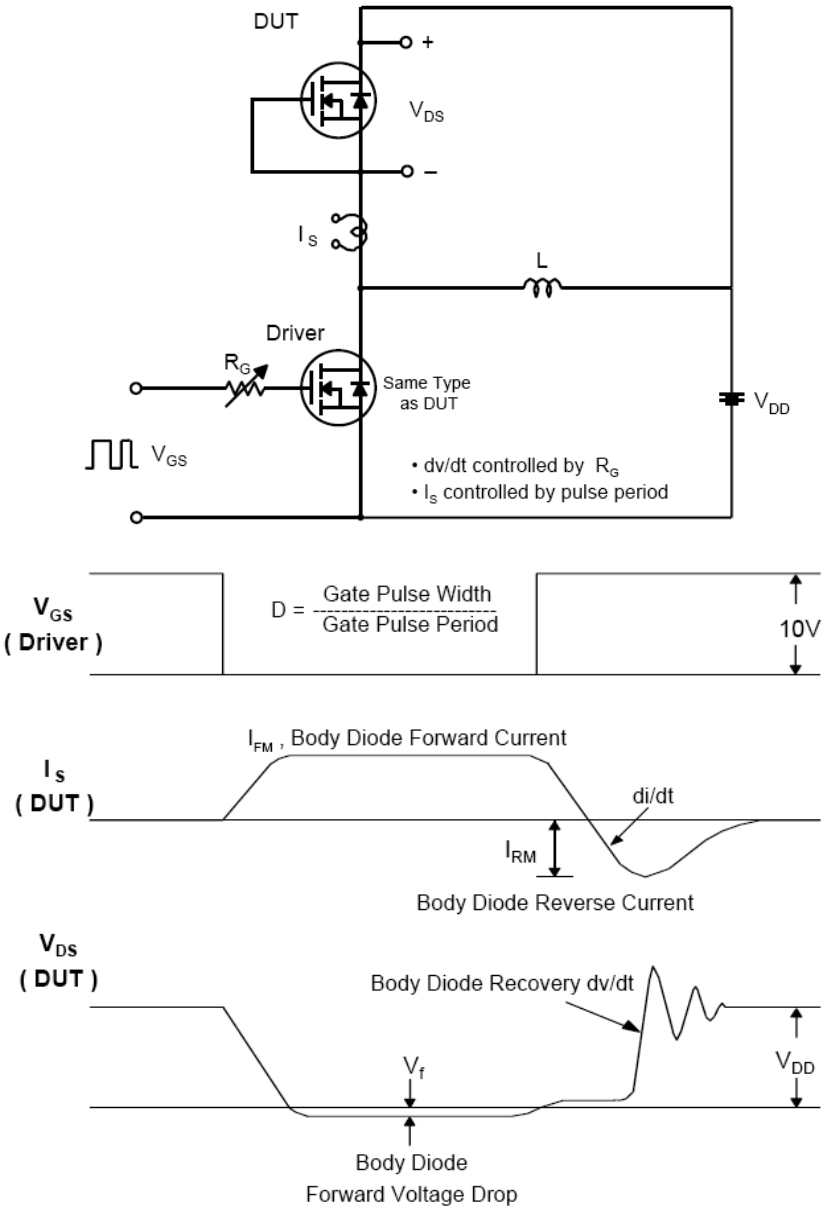

Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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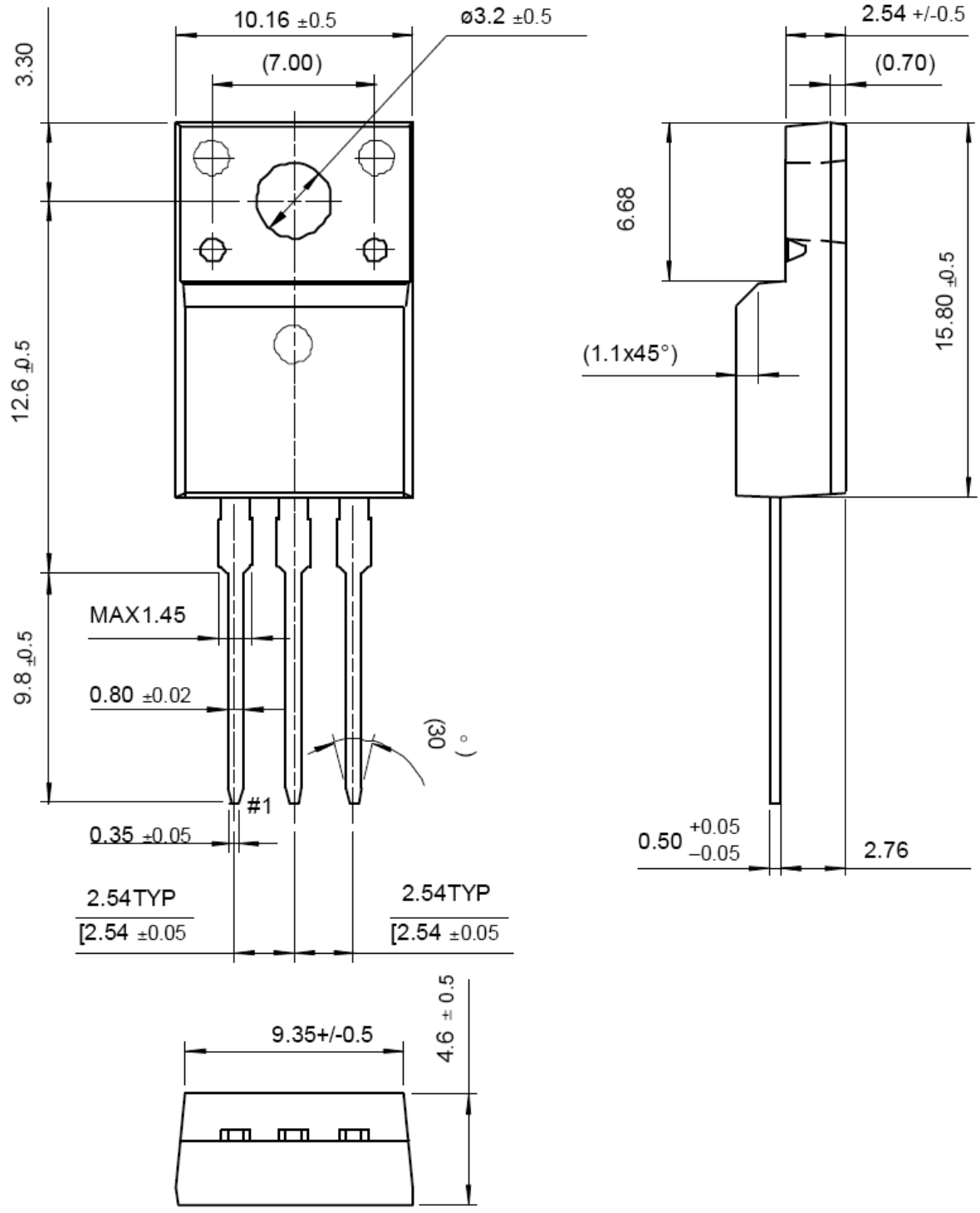
Package Dimensions

Dimensions in Millimeters



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