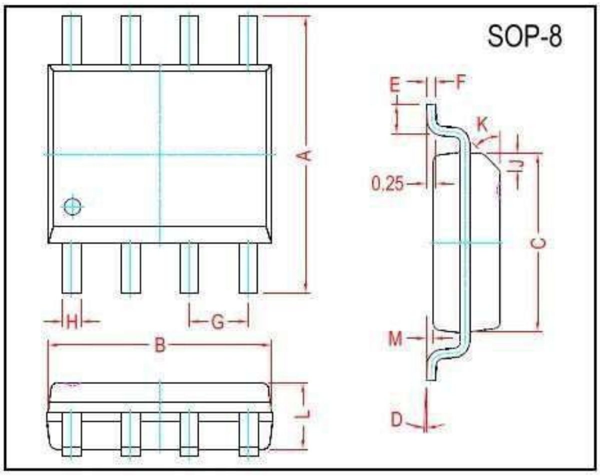
MSL4435A

Chip Integration Technology Corporation

P-Channel ENHANCEMENT MODE POWER MOSFET



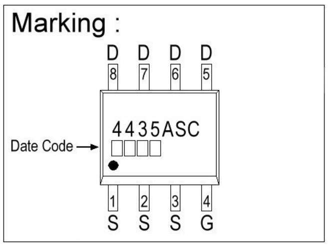
Features:

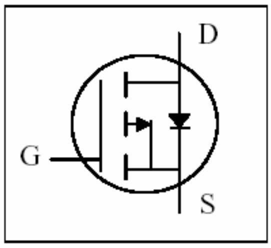
- Advanced high cell density Trench technology
- Excellent CdV/dt effect decline
- Green Device Available
- Super Low Gate Charge
- 100% EAS Guaranteed

Description:

The MSL4435A is the high cell density trenched P-ch MOSFETs, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

The MSL4435A meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.





BV_{DSS}	-30V
$R_{DS(ON)}$	20mΩ
I_D	-7.5A

REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	5.80	6.20	M	0.10	0.25
B	4.80	5.00	H	0.35	0.51
C	3.80	4.00	L	1.35	1.75
D	0°	8°	J	0.40 REF.	
E	0.40	0.90	K	45° REF	
F	0.19	0.25	G	1.27 TYP.	

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current[1], @V_{GS}= -10V	I_D @T_A=25℃	-7.5	A
	I_D @T_A=70℃	-5.8	A
Pulsed Drain Current[2]	I_{DM}	-50	A
Total Power Dissipation[4]	P_D @T_A=25℃	2.5	W
	P_D @T_A=70℃	1.6	W
Single Pulse Avalanche Energy[3], L=0.1mH	E_{AS}	72.2	mJ
Single Pulse Avalanche Current, L=0.1mH	I_{AS}	-38	A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 ~ +150	℃

Thermal Data

Parameter	Symbol	Max. Value	Unit
Thermal Resistance Junction-ambient[1]	$R_{\theta JA}$	85	℃/W
Thermal Resistance Junction-ambient[1]	$R_{\theta JA}$	36	℃/W

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Electrical Characteristics (Tj = 25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV_{DSS}	-30	-	-	V	V_{GS}=0, I_D=-250uA
Gate Threshold Voltage	$V_{GS(th)}$	-1.0	-	-2.5	V	V_{DS}=V_{GS}, I_D=-250uA
Forward Transconductance	g_{fs}	-	17	-	S	V_{DS}=-5V, I_D=-6A
Gate-Source Leakage Current	I_{GSS}	-	-	±100	nA	V_{GS}= ?20V
Drain-Source Leakage Current(Tj=25°C)	I_{DSS}	-	-	-1	uA	V_{DS}=-24V, V_{GS}=0
Drain-Source Leakage Current(Tj=55°C)		-	-	-5	uA	V_{DS}=-24V, V_{GS}=0
Static Drain-Source On-Resistance[2]	$R_{DS(ON)}$	-	-	20	mΩ	V_{GS}=-10V, I_D=-6A
		-	-	32		V_{GS}=-4.5V, I_D=-4A
Total Gate Charge	Q_g	-	12.6	-	nC	I_D=-6A V_{DS}=-15V V_{GS}=-4.5V
Gate-Source Charge	Q_{gs}	-	4.8	-		
Gate-Drain (“Miller”) Change	Q_{gd}	-	4.8	-		
Turn-on Delay Time	$T_{d(on)}$	-	4.6	-	ns	V_{DS}=-15V I_D=-6A V_{GS}=-10V R_G=3.3Ω
Rise Time	T_r	-	14.8	-		
Turn-off Delay Time	$T_{d(off)}$	-	41	-		
Fall Time	T_f	-	19.6	-		
Input Capacitance	C_{iss}	-	1345	-	pF	V_{GS}=0V V_{DS}=-15V f=1.0MHz
Output Capacitance	C_{oss}	-	194	-		
Reverse Transfer Capacitance	C_{rss}	-	158	-		
Gate Resistance	R_g	-	13	-	Ω	f=1.0MHz

Guaranteed Avalanche Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Single Pulse Avalanche Energy[5]	EAS	36.45	-	-	mJ	V_{DD}=-25V, L=0.1mH, I_{AS}=-27A

Source-Drain Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Diode Forward Voltage[2]	V_{SD}	-	-	-1.2	V	I_S=-1A, V_{GS}=0V, T_J=25°C
Continuous Source Current[1,6]	I_S	-	-	-7.5	A	V_G=V_D=0V, Force Current
Pulsed Source Current[2,6]	I_{SM}	-	-	-50	A	
Reverse Recovery Time	t_{rr}	-	16.3	-	ns	I_F=-6A, dI/dt=100A/us, T_J=25°C
Reverse Recovery Charge	Q_{rr}		5.9	-	nC	

Notes: 1. Surface mounted on a 1 inc h^2 FR-4 board with 2OZ copper.

2. The data tested by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%.

3. The EAS data shows Max. rating. The test condition is VDD= -25V, VGS= -10V, L=0.1mH, IAS= -38A.

4. The power dissipation is limited by 150°C junction temperature.

5. The Min. value is 100% EAS tested guarantee.

6. The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.

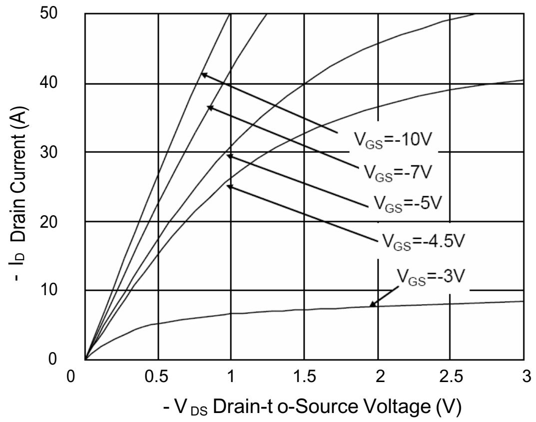

Fig.1 Typical Output Characteristics

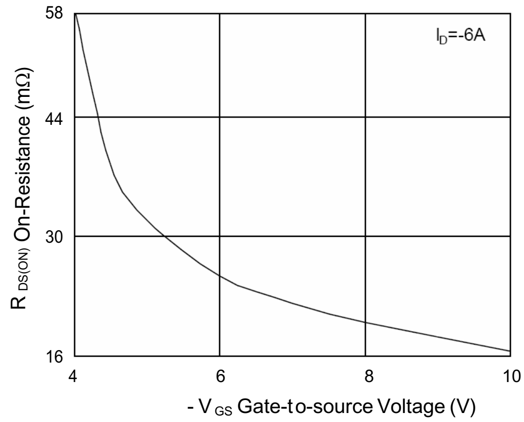

Fig.2 On-Resistance vs. G-S Voltage

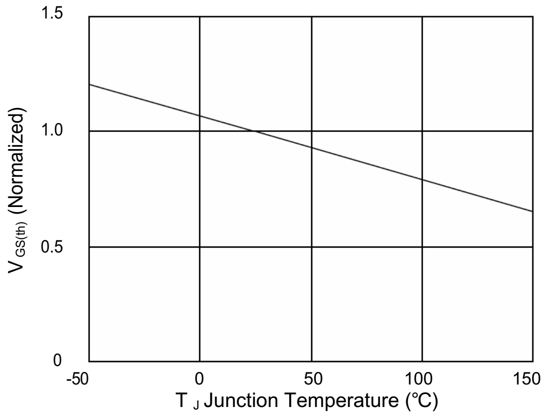

Fig.3 Normalized $V_{GS(th)}$ vs. T_J

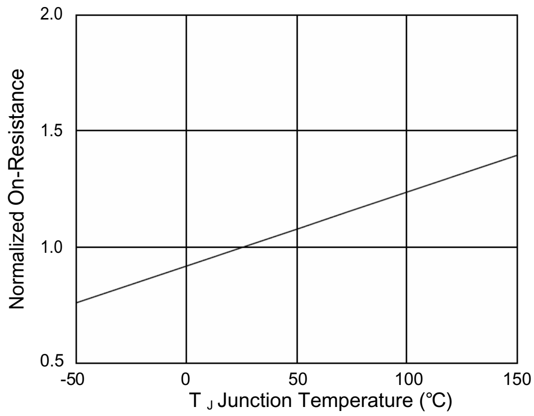

Fig.4 Normalized R_{DSON} vs. T_J

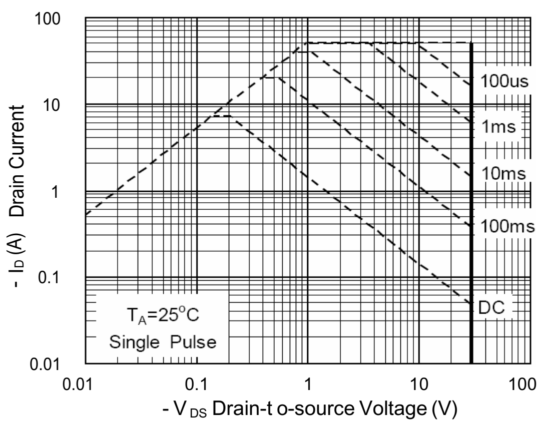

Fig.5 Safe Operating Area

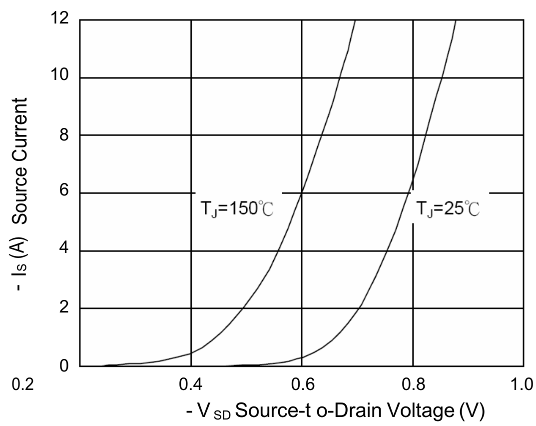

Fig.6 Forward Characteristics of Reverse

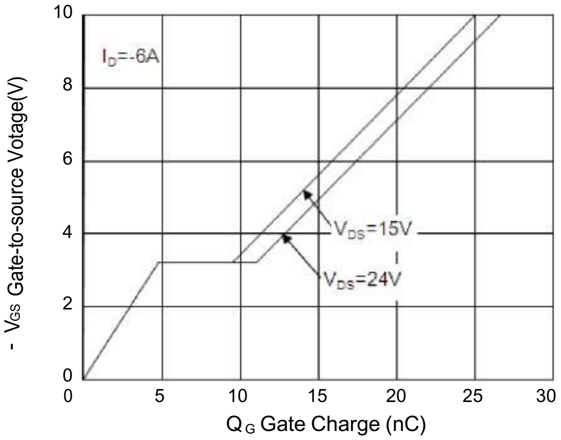

Fig.7 Gate Charge Characteristics

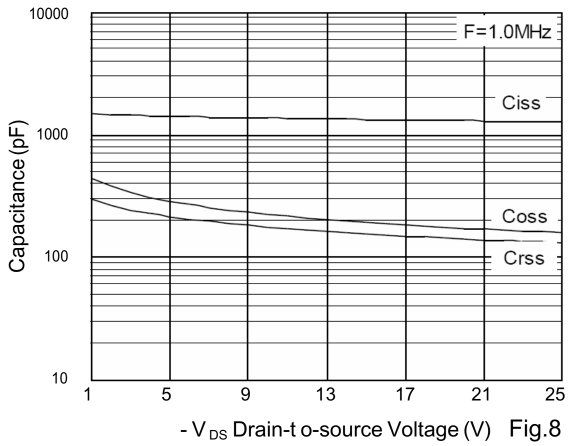

Fig.8 Capacitance Characteristics

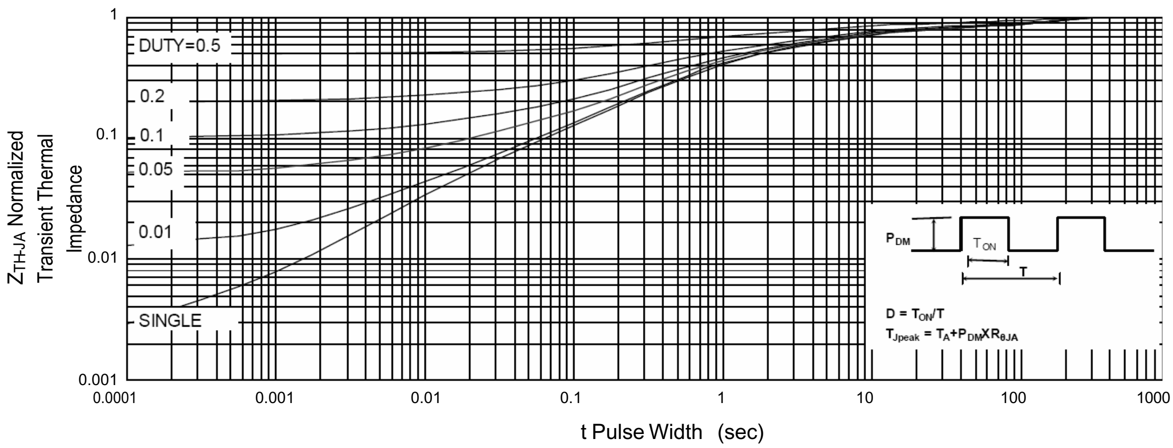

Fig.9 Normalized Transient Thermal Impedance

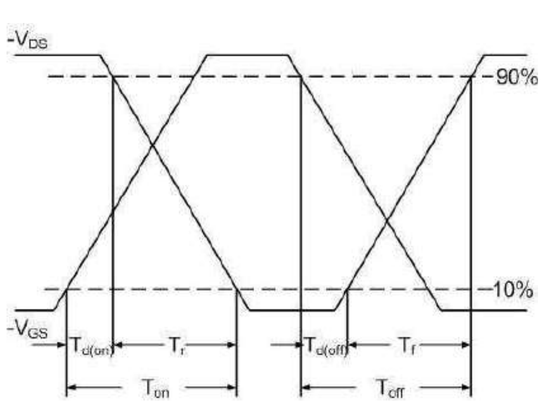

Fig.10 Switching Time waveform

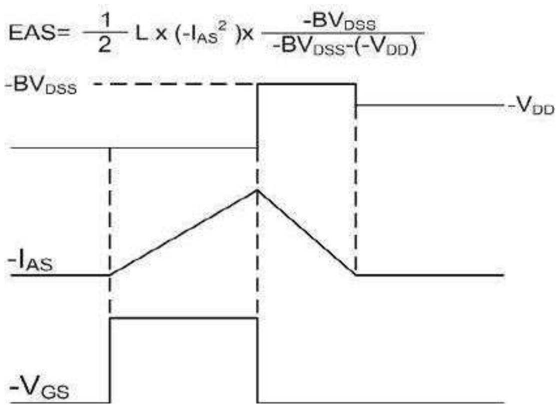

Fig.11 Unclamped Inductive Switching Waveform

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