OKI semiconductor

Preliminary

MSM6951B

ANALOG FRONT END LSI FOR MULTI-STANDARD MODEM

GENERAL DESCRIPTION

The MSM6951B is an analog front-end LSI which is fabricated by OKi's low power consumption CMOS silicon gate technology for modem chip set based on Bell 212A, CCITT V.21, V.22, V.23 and V.22 bis standard. The MSM6951 consists of two BPFs, for low band and high band, an A/D converter with 8-bit parallel output, a D/A converter with 8-bit parallel input, an AGC circuit controlled by external digital signals, a guard tone generator (550 Hz/1800 Hz selectable) and some analog signal control switches for various applications.

The MSM6951B communicates with a modulator and a demodulator via each 8 bits parallel digital line.
This chip does not contain a carrier detect function but it will be performed with a digital signal processor dedicated to implement a demodulator by using digital signals from the A/D converter.

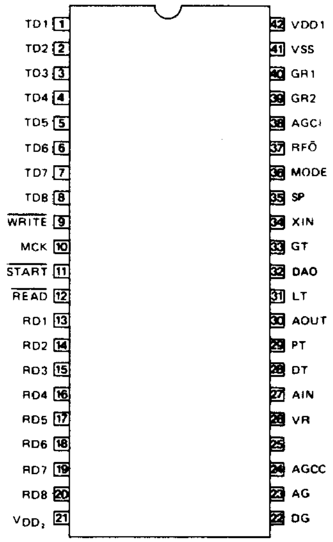
This device provides an analog signal input, an analog signal output and some signal-loop control inputs, and requires a 3.6864 MHz clock input to generate the operating time-base.

FEATURES

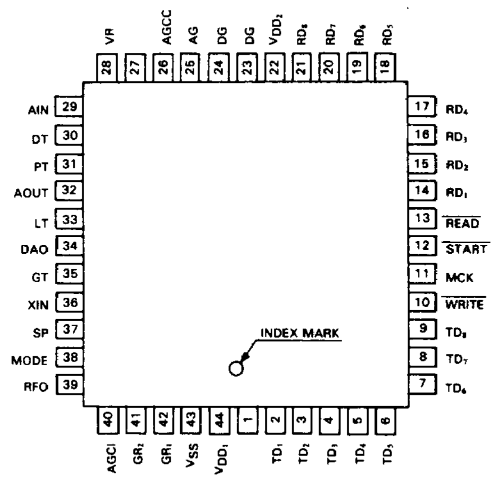
- Conforms to Bell 212A, CCITT V.21, V.22, V.23 and V.22 bis
- 8-bit parallel output A/D converter and 8-bit parallel input D/A converter on chip.
- On-chip voltage reference.
- On-chip AGC circuit controlled by 8-bit external digital signal, over the received signal level range of 48 dB with 0.19 dB step.
- Dynamic range: 70 dB
- Guard tone mixing function: 550 Hz or 1800 Hz.
- On-chip multi-purpose LPF for tone transmitting and call progress detection.
- Provides AC loop test function, a transmitting analog signal can be looped back as a receive analog signal within the chip.
- Supply voltage: ±5V.
- Low power dissipation: 115 mW.
- 3.6864 MHz external clock for operation.
- 42-pin plastic DIP MSM6951BRS
  56-pin plastic FLAT
  . . . . MSM6951BGS-VK
  44-pin PLCC. MSM6951BJS

PIN CONFIGURATION (Top view)

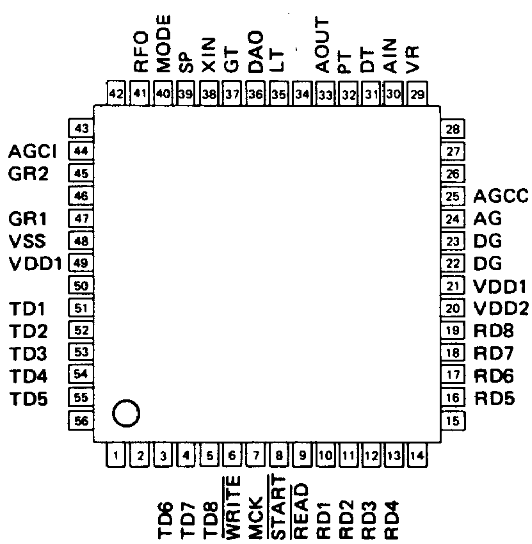
42 pin DIP (MSM6951BRS)



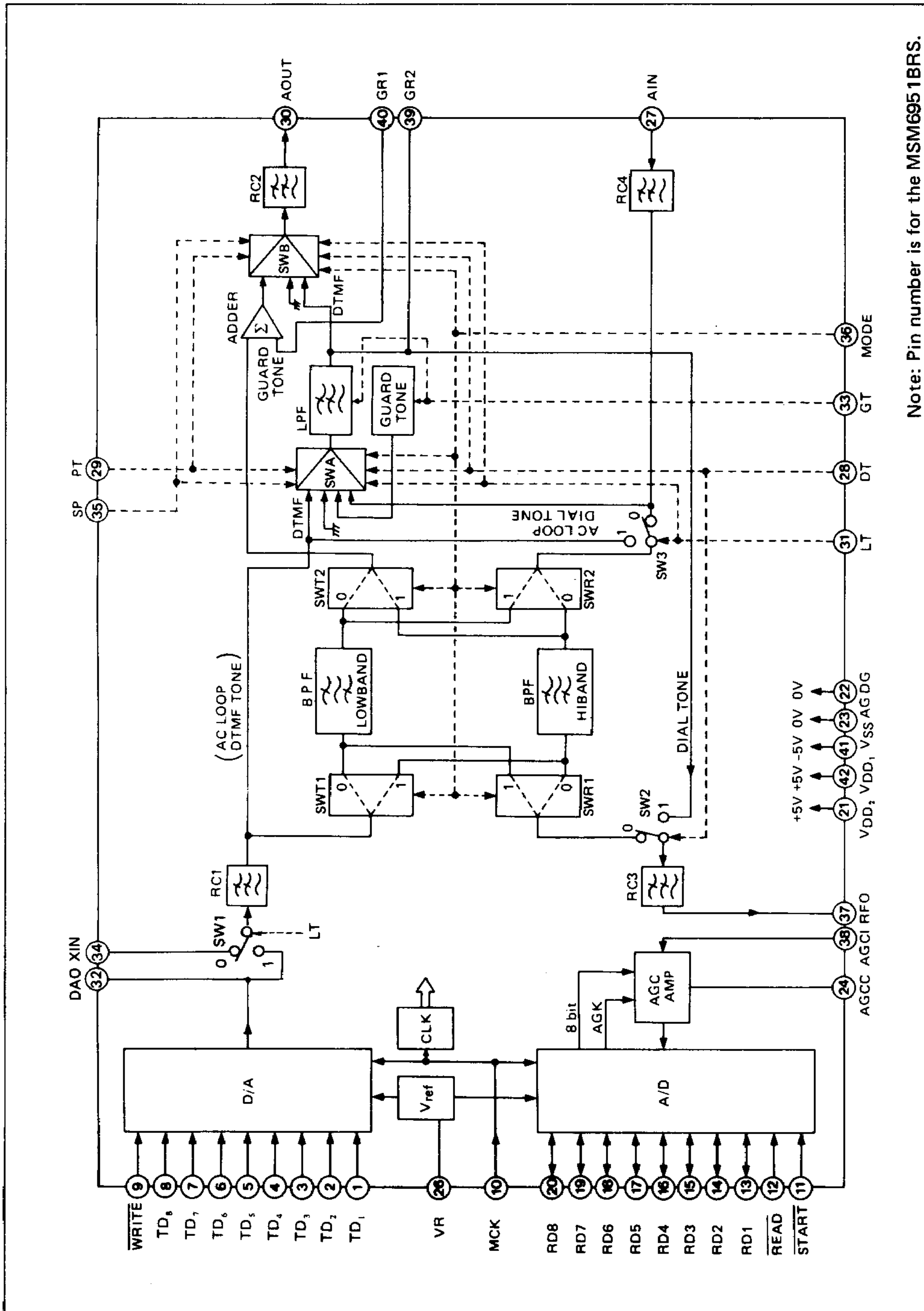
44 pin PLCC (MSM6951BJS)



56 pin FLAT (MSM6951BGS-VK)



BLOCK DIAGRAM



Note: Pin number is for the MSM6951BRS.

Pin Assignment

Pin Name	Pin No.			In/Out	Function
	RS	GS	JS		
TD1	1	51	2	Input	Transmit signal digital data input to DA (LSB)
TD2	2	52	3	Input	Transmit signal digital data input to DA
TD3	3	53	4	Input	Transmit signal digital data input to DA
TD4	4	54	5	Input	Transmit signal digital data input to DA
TD5	5	55	6	Input	Transmit signal digital data input to DA
TD6	6	3	7	Input	Transmit signal digital data input to DA
TD7	7	4	8	Input	Transmit signal digital data input to DA
TD8	8	5	9	Input	Transmit signal digital data input to DA (MSB)
$\overline{\text{WRITE}}$	9	6	10	Input	TD writing control signal for DA
MCK	10	7	11	Input	Master clock input 3.6864 MHz
$\overline{\text{START}}$	11	8	12	Input	Control signal for starting of AD conversion
$\overline{\text{READ}}$	12	9	13	Input	RD reading control signal for AD
RD1	13	10	14	In/Out	Receive signal digital data output from AD (LSB)
RD2	14	11	15	In/Out	Receive signal digital data output from AD
RD3	15	12	16	In/Out	Receive signal digital data output from AD
RD4	16	13	17	In/Out	Receive signal digital data output from AD
RD5	17	16	18	In/Out	Receive signal digital data output from AD
RD6	18	17	19	In/Out	Receive signal digital data output from AD
RD7	19	18	20	In/Out	Receive signal digital data output from AD
RD8	20	19	21	In/Out	Receive signal sigital data output from AD (MSB)
VDD2	21	20	22		Positive power supply (+5 V)
DG	22	22, 23	23, 24		Digital ground (0 V)
AG	23	24	25		Analog ground (0 V)
AGCC	24	25	26		External capacitor terminal for AGC
VR	26	29	28	Output	External capacitor terminal for reference voltage
AIN	27	30	29	Input	Receive analog signal input
DT	28	31	30	Input	Dial tone detecting loop
PT	29	32	31	Input	DTMF signal transmitting loop
AOUT	30	33	32	Output	Transmit analog signal output
LT	31	35	33	Input	AC loop test
FT	32	36	34	Input	XIN enable (Filter test or External input)
GT	33	37	35	Input	Guard tone select (1800/550 Hz)
XIN	34	38	36	Input	External transmit analog signal input
SP	35	39	37	Input	V.23 transmitting loop
MODE	36	40	38	Input	Originate/Answer mode select
RF$\overline{\text{O}}$	37	41	39	Output	Receive filter output
AGCI	38	44	40	Input	AGC circuit input
GR2	39	45	41	Output	External resistor terminal for Guard tone level
GR1	40	47	42	Input	External resistor terminal for Guard tone level
VSS	41	48	43		Negative power supply (−5 V)
VDD1	42	21,49	44		Positive power supply (+5 V)

ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	VDD	Ta = 25°C with respect to AG or DG	-0.3 ~ +7	V
	VSS		+0.3 ~ -7	
Analog input voltage	VIA		VSS - 0.3 ~ VDD + 0.3	
Digital input voltage	VID		-0.3 ~ VDD + 0.3	
Operating temperature	T_{OP}	—	-40 ~ + 85	°C
Storage temperature	T_{STG}	—	-55 ~ +150	

2. Recommended Operating Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	With Respect to AG or DG	4.75	5.00	5.25	V
	V_{SS}		-5.25	-5.00	-4.75	
	AG, DG	–	–	0	–	
Operating temperature	T_{OP}	–	0	–	70	°C
R_0	–	–	–	51	–	kΩ
R_1	–	Transformer Impedance (Hybrid) $\begin{bmatrix} 600\ \Omega \\ 600\ \Omega \end{bmatrix}$: 600 Ω	–	600	–	Ω
R_2	–		–	600	–	
R_3	–		–	300	–	
R_4	–	–	–	51	–	kΩ
R_5	–		–	51	–	
R_6	–		–	51	–	
R_7	–		–	51	–	
R_8	–		–	51	–	
R_9	–		–	51	–	
R_{10}	–		–	100	–	
C_0	–	–	–	0.1	–	μF
C_1	–		–	2.2	–	
C_2	–		–	1	–	
C_3	–		–	0.1	–	
C_4	–		–	1	–	
C_5, C_7, C_9	–		–	10	–	
C_6, C_8	–		–	1	–	
$R_{11} \sim R_{18}$	–	–	–	20	–	kΩ
Master Clock Frequency	F_{MCK}	–	3.6860	3.6864	3.6867	MHz
MCK Duty Cycle	D_{MCK}	50% to 50%	30	50	70	%
Digital Input Rise Time	T_R	$T_{D1} \sim T_{D8}$, $\overline{WRITE}$, $\overline{START}$, $\overline{READ}$, $R_{D1} \sim R_{D8}$, See Figure 1	0	–	50	nS
Digital Input Fall Time	T_F		0	–	50	nS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
$\overline{\text{WRITE}}$ Period	T_{PW}	See Figure 2, 3	104	–	143	μS
$\overline{\text{WRITE}}$ Width	T_{WW}		0.55	–	85	μS
$\overline{\text{START}}$ Period	T_{PS}		98.2	–	143	μS
$\overline{\text{START}}$ Width	T_{WS}		1.1	–	79	μS
$\overline{\text{READ}}$ Width	T_{WR}		3.2	–	*	μS
$\overline{\text{START}} \rightarrow \overline{\text{READ}}$ Timing	T_{SR}		80	–	*	μS
$\overline{\text{READ}} \rightarrow \overline{\text{START}}$ Timing	T_{RS}		15	–	*	μS
Allowable XIN Input DC Offset Voltage	V_{OSXIN}	–	-100	–	+100	mV
Allowable AIN Input DC Offset Voltage	V_{OSAIN}	–	-100	–	+100	mV

* $T_{WR}\ MAX = T_{PS} - T_{SR} - T_{RS}$
$T_{SR}\ MAX = T_{PS} - T_{WR} - T_{RS}$
$T_{RS}\ MAX = T_{PS} - T_{WR} - T_{SR}$

3. Power Dissipation

(V_{DD} = +5 V ±5%, V_{SS} = -5 V ±5%, T_a = 0 ~ 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Positive Power Supply Current	I_{DD}	–	–	12	20	mA
Negative Power Supply Current	I_{SS}	–	–	11	20	mA

Note: $I_{DD} = I_{DD1}$ (V_{DD1} pin) + I_{DD2} (V_{DD2} pin)

4. Digital Interface

(V_{DD} = +5 V ±5%, V_{SS} = -5 V ±5%, T_a = 0 ~ 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	–	–	–	0.6	V
Input High Voltage	V_{IH}	–	2.2	–	–	V
Output Low Voltage	V_{OL}	I_{OL} = 0.36 mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH} = 20 μA	2.4	–	–	V
Input Low Current	I_{IL}	DG $\leq V_{IN} \leq V_{IL}$	-10	–	10	μA
Input High Current	I_{IH}	$V_{IH} \leq V_{IN} \leq V_{DD}$	-10	–	10	μA
DA Data Set-up Time	T_{SD}	See Figure 3	0	–	–	μS
DA Data Hold Time	T_{HD}		1.2	–	–	μS
AGC Data Set-up Time	T_{SA}	See Figure 2	0	–	–	μS
AGC Data Hold Time	T_{HA}		2.2	–	–	μS
AD Data Output Delay Time	T_{D1}	Pull-up Resistor = 20 KΩ See Figure 2	0	–	3	μS
	T_{D2}		0.5	–	3	μS

5. ANALOG INTERFACE (VDD = +5V ± 5%, −5V ± 5%, Ta = 0~70°C)

Reference Voltage (VR)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Reference Voltage	VR		2.40	2.50	2.60	V

Transmit Modem Signal Characteristics (XIN, AOUT)

Parameter		Symbol	Condition		Min	Typ	Max	Unit
Input Resistance		RXIN	XIN $f_{XIN} \leqq 5KHz$		500			KΩ
Input Voltage		VXIN	XIN				5	V_{PP}
Output Voltage		VAOUT	RAOUT ≧ 20KΩ, CAOUT ≦ 100PF		5			V_{PP}
Load Resistance		RAOUT			20			KΩ
Load Capacitance		CAOUT					100	PF
DC Offset Voltage		VOST	AOUT, XIN = 0V		−500	0	+500	mV
*1 Absolute Voltage Gain	Bell 212A/ V.22/V.22bis	GT1	Originate	1200Hz, 0dBm	−1.5	0	+1.5	dB
		GT2	Answer	2400Hz, 0dBm	−1.5	0	+1.5	dB
	Tone Transmit	GT3	GT = 1, 1020Hz, 0dBm		−1.5	0	+1.5	dB
Gain Tracking		TGT1	GT1 − GT2		−1.0	0	+1.0	dB
*2 AOUT Signal Level	Bell 212A/ V.22/V.22bis	VT1	Originate	1200Hz		6.5/6.6		dBm
		VT2	Answer	2400Hz		5.2/6.0		dBm
	Tone Transmit	VT3	GT = 1, 1020Hz			6.6/6.7		dBm
*3 Idle Channel Noise	Bell 212A/ V.22/V.22bis	NIDLT1	Originate	0.3~3.4KHz		−60	−55	dBm
		NIDLT2	Answer	0.3~3.4KHz		−56	−50	dBm
		NIDLT3	Originate	1.8~3KHz		−76	−65	dBm
		NIDLT4	Answer	0.6~1.8KHz		−73	−65	dBm
	Tone Transmit	NIDLT5	GT = 1	0.3~3.4KHz		−66	−60	dBm

Parameter		Symbol	Condition		Min	Typ	Max	Unit
Clock Noise		NCLKT	All modes, at 57.6KHz				−50	dBm
Total Harmonic Distortion	Bell 212A/ V.22/V.22bis	THDT1	Originate	1200Hz, 0dBm		−52	−50	dB
		THDT2	Answer	2400Hz, 0dBm		−45	−43	dB
	Tone Transmit	THDT3	GT = 1, 1020Hz, 0dBm			−48	−45	dB

*1 GT = 20 log (VAOUT/VXIN)
*2 DA input level is maximum, XIN = DA0

$\boxed{① \ / \ ②}$ ①; $\overline{\text{WRITE}}$ = 7.2KHz, ②; $\overline{\text{WRITE}}$ = 9.6KHz

*3 Idle Channel Noise is defined with no weighted filter.

Note) 0dBm = 0.775Vrms

Guard Tone (AOUT)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Tone Frequency	FGT1	GT = 0	530	553.8	570	Hz
	FGT2	GT = 1	1780	1800	1820	Hz
Tone Amplitude	VGT1	GT = 0, R8 = Opened	−1.0	0	1.0	dBm
	VGT2	GT = 1, R8 = Opened	−1.0	0	1.0	dBm
Total Harmonic Distortion (2nd and 3rd) *	THDGT1	GT = 0, VGT1 = −4dBm		−63	−57	dB
	THDGT2	GT = 1, VGT2 = −4dBm		−51	−45	dB

* Harmonics above 3rd harmonic are negligible.

V.21/V.23 Transmit Signal Characteristics (XIN, AOUT)

Parameter		Symbol	Condition		Min	Typ	Max	Unit
*1 Absolute Voltage Gain	CCITT V.21	GT4	Originate	1080Hz, 0dBm	– 1.5	0	+ 1.5	dB
		GT5	Answer	1750Hz, 0dBm	– 1.5	0	+ 1.5	dB
	CCITT V.23	GT6	Main	1700Hz, 0dBm	– 1.5	0	+ 1.5	dB
		GT7	Backward	420Hz, 0dBm	– 1.5	0	+ 1.5	dB
Gain Tracking	CCITT V.21	TGT2	GT4 – GT5		– 1	0	1	dB
	CCITT V.23	TGT3	GT6 – GT7		– 1.5	0	1.5	dB
*2 AOUT Signal Level	CCITT V.21	VT4	Originate	1080Hz		6.5/6.7		dBm
		VT5	Answer	1750Hz		6.0/6.4		dBm
	CCITT V.23	VT6	Main	1700Hz		6.1/6.4		dBm
		VT7	Backward	420Hz		6.8/6.8		dBm
*3 Idle Channel Noise	CCITT V.21	NIDLT6	Originate	0.3~ 3.4KHz		– 59	– 55	dBm
		NIDLT7	Answer			– 56	– 50	dBm
	CCITT V.23	NIDLT8	Main			– 63	– 55	dBm
		NIDLT9	Backward			– 67	– 60	dBm
Total Harmonic Distortion	CCITT V.21	THDT4	Originate	1080Hz, 0dBm		– 53	– 50	dB
		THDT5	Answer	1750Hz, 0dBm		– 48	– 43	dB
	CCITT V.23	THDT6	Main	1700Hz, 0dBm		– 50	– 45	dB
		THDT7	Backward	420Hz, 0dBm		– 59	– 55	dB

*1 GT = 20 log (VAOUT/VXIN)
*2 DA input level is maximum, XIN = DA0
$\boxed{① \ / \ ②}$ ①; $\overline{\text{WRITE}}$ = 7.2KHz, ②; $\overline{\text{WRITE}}$ = 9.6KHz
*3 Idle Channel Noise is defined with no weighted filter.

Note) 0dBm = 0.775Vrms

Receive Modem Signal Characteristics (AIN, RFO)

Parameter		Symbol	Condition		Min	Typ	Max	Unit
Input Resistance		RAIN	AIN $f_{XIN} \leqq 5KHz$		500			KΩ
Input Voltage Swing		VAIN	AIN				5	V_{PP}
Output Voltage		VRFO	RRFO ≧ 20KΩ, CRFO ≦ 100PF		5			V_{PP}
Load Resistance		RRFO	RFO		20			KΩ
Load Capacitance		CRFO	RFO				100	PF
DC Offset Voltage		VOSR	RFO		-500	0	+500	mV
*1 Absolute Voltage Gain	Bell 212A/ V.22/V.22bis	GR1	Answer	1200Hz, 3dBm	-1.5	0	+1.5	dB
		GR2	Originate	2400Hz, 3dBm	-1.5	0	+1.5	dB
	Tone Receive	GR3	GT = 0, 300Hz, 3dBm		-1.5	0	+1.5	dB
Gain Tracking		TGR1	GR1 - GR2		-1.0	0	+1.0	dB
*2 Idle Channel Noise	Bell 212A/ V.22/V.22bis	NIDLR1	Answer	0.3~ 3.4KHz		-63	-57	dBm
		NIDLR2	Originate			-63	-57	dBm
	Tone Receive	NIDLR3	GT = 0			-69	-57	dBm
Clock Noise		NCLKR1	All modes, at 57.6KHz				-45	dBm
		NCLKR2	GT = 0, at N x 14.4KHz				-45	dBm
Total Harmonic Distor- tion	Bell 212A/ V.22/V.22bis	THDR1	Answer	1200Hz, +3dBm		-47	-43	dB
		THDR2	Originate	2400Hz, +3dBm		-41	-37	dB
		THDR3	Originate	1200Hz, 0dBm		-58	-53	dB
		THDR4	Answer	2400Hz, 0dBm		-90	-55	dB
	Tone Receive	THDR5	GT = 0, 300Hz, +3dBm			-57	-49	dB

*1 GR = 20 log (VRFO/VAIN)
*2 Idle Channel Noise is defined with no weighted filter.

V.21/V.23 Receive Signal Characteristics (AIN, RFO)

Parameter		Symbol	Condition		Min	Typ	Max	Unit
*1 Absolute Voltage Gain	CCITT V.21	GR4	Answer	1080Hz, 3dBm	– 1.5	0	+ 1.5	dB
		GR5	Originate	1750Hz, 3dBm	– 1.5	0	+ 1.5	dB
	CCITT V.23	GR6	Main	1700Hz, 3dBm	– 1.5	0	+ 1.5	dB
		GR7	Backward	420Hz, 3dBm	– 1.5	0	+ 1.5	dB
Gain Tracking	CCITT V.21	TGR2	GR4 – GR5		– 1	0	1	dB
	CCITT V.23	TGR3	GR6 – GR7		– 1.5	0	1.5	dB
*2 Idle Channel Noise	CCITT V.21	NIDLR4	Answer	0.3~ 3.4KHz		– 62	– 57	dBm
		NIDLR5	Originate			– 62	– 57	dBm
	CCITT V.23	NIDLR6	Main			– 66	– 57	dBm
		NIDLR7	Backward			– 69	– 57	dBm
Total Harmonic Distor-tion	CCITT V.21	THDR6	Answer	1080Hz, + 3dBm		– 47	– 43	dB
		THDR7	Originate	1750Hz, + 3dBm		– 43	– 40	dB
		THDR8	Answer	1750Hz, 0dBm		– 100	– 50	dB
		THDR9	Originate	1080Hz, 0dBm		– 67	– 50	dB
	CCITT V.23	THDR10	Main	1700Hz, + 3dBm		– 43	– 40	dB
		THDR11	Backward	420Hz, + 3dBm		– 58	– 50	dB
		THDR12	Main	420Hz, 0dBm		– 60	– 50	dB
		THDR13	Backward	1700Hz, 0dBm		– 90	– 50	dB

*1 GR = 20 log (VRFO/VAIN)

*2 Idle Channel Noise is defined with no weighted filter.

6. Filter Transfer Characteristics

Low-band BPF

(V_{DD} = +5 V ±5%, V_{SS} = -5 V ±5%, T_a = 0 ~ 70°C)

Relative Voltage Gain to G_{FL_4}	G_{FL_1}	508 Hz/406 Hz*	–	-44	-40	dB
	G_{FL_2}	555 Hz/444 Hz	–	-60	-45	dB
	G_{FL_3}	898 Hz/718 Hz	– 1.5	0	+ 1.5	dB
	G_{FL_4}	1,008 Hz/806 Hz	Referred Gain 0			dB
	G_{FL_5}	1,148 Hz/918 Hz	– 1.5	0	+ 1.5	dB
	G_{FL_6}	1,352 Hz/1,082 Hz	– 1.5	0	+ 1.5	dB
	G_{FL_7}	1,508 Hz/1,206 Hz	– 2	0	+ 1	dB
	G_{FL_8}	1,805 Hz/1,444 Hz	–	-65	-45	dB
	G_{FL_9}	2400 Hz/1,920 Hz	–	-55	-50	dB
Group Delay Distortion	G_{DL}	900 ~ 1,500 Hz/ 720 ~ 1,200 Hz	–	–	100/120	μS

* Bell212A, V.22, V.22 bis/V.21

High-band BPF

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Relative Voltage Gain to G_{FH_4}	G_{FH_1}	1,195 Hz/956 Hz*	–	-55	-50	dB
	G_{FH_2}	1,641 Hz/1,313 Hz	–	-55	-50	dB
	G_{FH_3}	2,055 Hz/1,644 Hz	−1.5	0	+1.5	dB
	G_{FH_4}	2,195 Hz/1,756 Hz	Referred Gain 0			dB
	G_{FH_5}	2,398 Hz/1,918 Hz	−1.5	0	+1.5	dB
	G_{FH_6}	2,602 Hz/2,082 Hz	−1.5	0	+1.5	dB
	G_{FH_7}	2,742 Hz/2,194 Hz	−1.2	0	+1.8	dB
	G_{FH_8}	3,211 Hz/2,569 Hz	–	-43	−38	dB
	G_{FH_9}	3,398 Hz/2,718 Hz	–	-35	−29	dB
Group Delay Distortion	G_{DH}	2,100~2,700 Hz/ 1,680~2,160 Hz	–	–	200/240	µS

* Bell212A, V.22, V.22 bis/V.21

Multi-purpose LPF

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Relative Voltage Gain to G_{LPF_1}	G_{FLF_1}	211 Hz	GT=0	−1	0	+1	dB
	G_{FLF_2}	305 Hz		Referred Gain 0			dB
	G_{FLF_3}	617 Hz		−1	0	+1	dB
	G_{FLF_4}	898 Hz		–	−50	−40	dB
	G_{FLF_5}	1,695 Hz		–	−50	−46	dB
Relative Volgate Gain to G_{LPF_2}	G_{FHF_1}	211 Hz	GT=1	−1	0	+1	dB
	G_{FHF_2}	305 Hz		Referred Gain 0			dB
	G_{FHF_3}	2,477 Hz		−1.5	0	+0.5	dB
	G_{FHF_4}	3,898 Hz		–	−51	−46	dB

BPF for CCITT V.23

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Relative Voltage Gain to G_{FB_4}	G_{FB_1}	414 Hz	–	−49	−44	dB
	G_{FB_2}	602 Hz	–	−32	−27	dB
	G_{FB_3}	789 Hz	−1.5	0	+1.5	dB
	G_{FB_4}	1,695 Hz	Referred Gain 0			dB
	G_{FB_5}	2,602 Hz	−1.5	0	+1.5	dB
	G_{FB_6}	3,008 Hz	–	−15	−12	dB
	G_{FB_7}	3,398 Hz	–	−36	−32	dB

7. AGC Circuit and DA, AD Converters

(V_{DD} = +5 V ±5%, V_{SS} = -5 V ±5%, T_a = 0 ~ 70°C)

Parameter		Symbol	Condition	Min	Typ	Max	Unit
AGC Amplifier							
Input Resistance		R_{AGCI}	–	–	1	–	MΩ
Variable Voltage Gain Range		G_{AGC}	–	-4	–	+43.8	dB
Voltage Gain Accuracy		G_E	–	-0.4	+0.03 ~ -0.17	+0.4	dB
Output DC Offset Voltage		V_{OSAGC}	–	-60 (-3)	–	+60 (+3)	mV (LSB)
Transmit Digital to Analog Converter							
Bits of Resolution		B_{REST}	–	–	8	–	bit
End-point Linearity		NL_{DA}	–	–	0.36	0.5	%
Differential Non-linearity		DNL_{DA}	–	–	1/5	1/2	LSB
Full Scale	Plus Full Scale	PFV_{DA}	–	–	+2,481	–	mV
	Minus Full Scale	NFV_{DA}	–	–	-2,500	–	mV
DC Offset Voltage		V_{OSDA}	–	-10	-1.5	+10	mV
Receive Analog to Digital Converter							
Bits of Resolution		B_{RESR}	–	–	8	–	bit
End-point Linearity		NL_{AD}	–	–	0.24	0.5	%
Differential Non-linearity		DNL_{AD}	–	–	1/5	1/2	LSB
Full Scale	Plus Full Scale	PFV_{AD}	–	–	+2,481	–	mV
	Minus Full Scale	NFV_{AD}	–	–	-2,500	–	mV
DC Offset Voltage*		V_{OSAD}	–	-1/2	–	+1/2	LSB

* This specification does not include the DC offset voltage at the input of the AD converter.

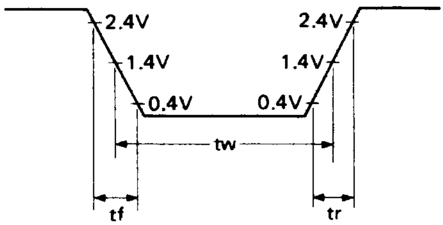


Figure 1 Definition of Rise/Fall Time

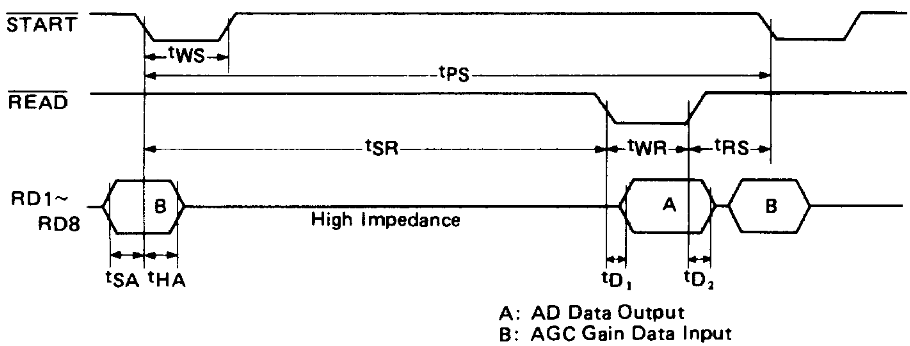


Figure 2 Receive Data Timing Chart

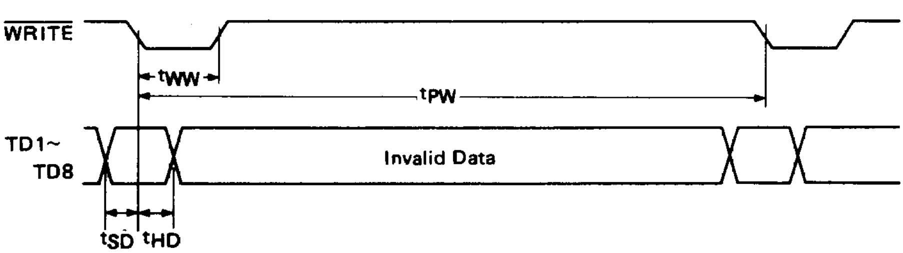


Figure 3 Transmit Data Timing Chart

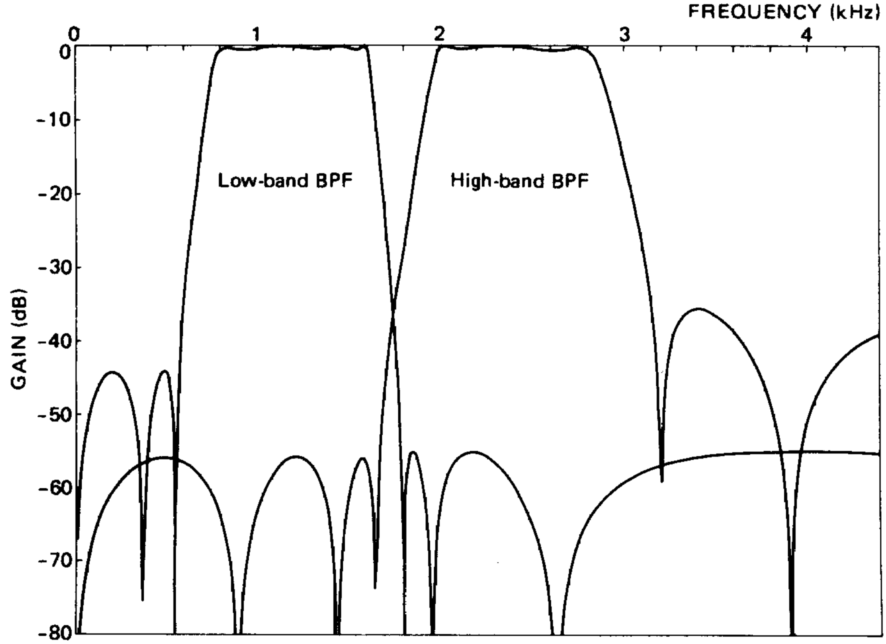


Figure 4 Low/High – band BPF FREQUENCY CHARACTERISTICS

Note) For CCITT V.21 mode, the passband of these BPFs is shifted down to 80% for the original.

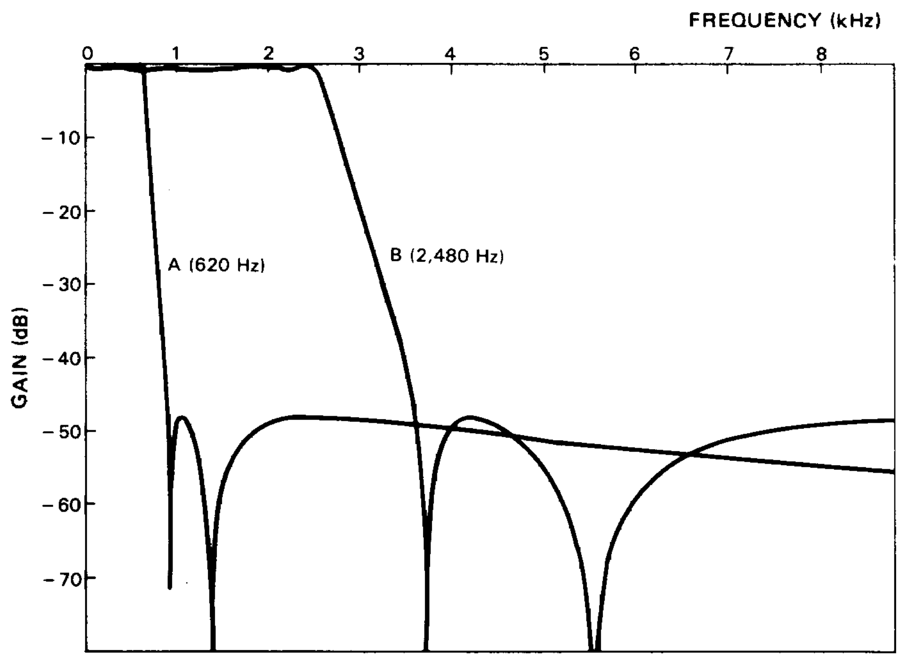


Figure 5-1 MULTI-PURPOSE LPF FREQUENCY CHARACTERISTICS

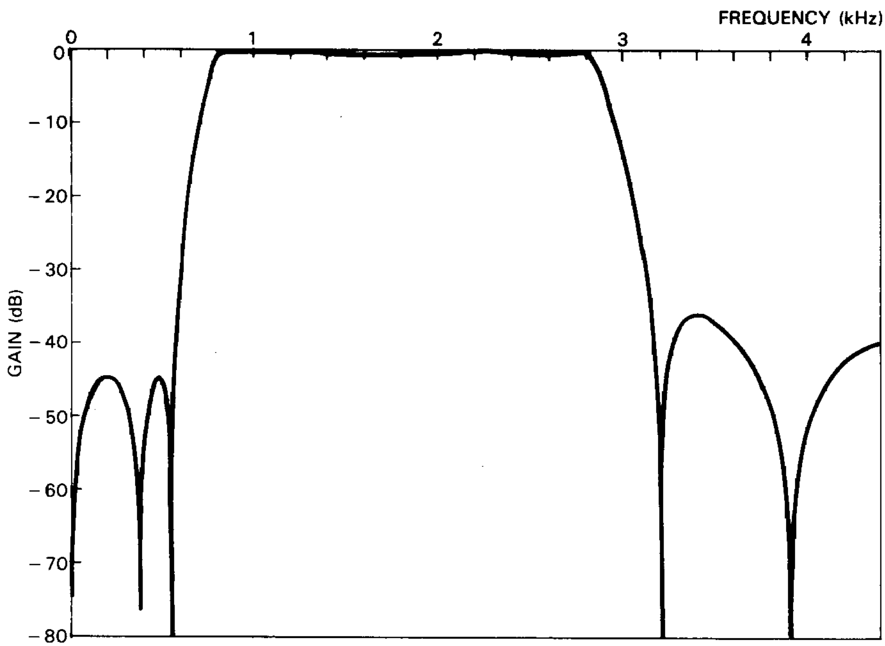


Figure 5-2 BPF for V.23 (1200 BPS) FREQUENCY CHARACTERISTICS

PIN DESCRIPTION

Pin Name	Pin No. RS	Pin No. GS	Pin No. JS	Function
TD1~TD8	1~8	3~5, 51~55	2~9	Transmit signal digital data input for DA conversion. These pins are 8 bit parallel two's complement data input pins. The data is loaded to the DA converter at the falling edge of $\overline{\text{WRITE}}$. TD1 is the LSB and TD8 is the MSB. Refer to Table 1 below.

TD	8	7	6	5	4	3	2	1	Total Value	Nominal Output Voltage*
Plus Full Scale	0	1	1	1	1	1	1	1	+127	+2,172.1 mV
⋮				⋮					+126 ~ 1	⋮
Plus 0	0	0	0	0	0	0	0	0	0	0
Minus 0	1	1	1	1	1	1	1	1	-1	-17.1 mV
⋮				⋮					-2 ~ 127	⋮
Minus Full Scale	1	0	0	0	0	0	0	0	-128	-2,189.2 mV

Table 1 *The reference voltage for DA conversion is +2.5 V. This output voltage is defined at AOUT, and does not care of its polarity.

Pin Name	Pin No. RS	Pin No. GS	Pin No. JS	Function
$\overline{\text{WRITE}}$	9	6	10	This signal enables TD1 ~ TD8 pins to write data into DA converter. The digital input from TD1 ~ TD8 is latched to the DA converter at the falling edge of $\overline{\text{WRITE}}$ signal, and then converted to analog signal. The analog output signal is renewed about 9 μsec after the falling edge of $\overline{\text{WRITE}}$ signal. The cycle of this signal can be chosen out of 104 μsec ∿ 143 μsec (7 ∿ 9.6 KHz). It is desirable for the noise performance that the $\overline{\text{WRITE}}$ is synchronous to the MCK.
MCK	10	7	11	A 3.6864 MHz clock signal should be applied to this pin. This is the time base for the operation of the MSM6951B.
$\overline{\text{START}}$	11	8	12	This signal enables MSM6951B to start the AD conversion. This signal is also used to latch the input data used for setting the amplitude of the AGC circuit. The input data is supplied from a demodulating chip, the general performance of which is digital signal processing. These two operations are performed at the falling edge of $\overline{\text{START}}$. The cycle of this signal can be chosen out of 98 μsec ~ 143 μsec.
$\overline{\text{READ}}$	12	9	13	This is a control signal for 3-state output data bus line, RD1 ~ RD8. While this pin is at digital 0 state, the output bus is activated and the result of the AD conversion is output from RD1 ~ RD8 terminals. While this pin is at digital 1 state, the output bus is inactivated and RD1 ~ RD8 become input terminals.

(to be continued)

Pin Name	Pin No.			Function
	RS	GS	JS	
RD1 ~ RD8	13 ~ 20	10 ~ 13, 16 ~ 19	14 ~ 21	These are I/O terminals controlled by $\overline{\text{START}}$ and $\overline{\text{READ}}$ terminals. When $\overline{\text{READ}}$ is set at digital 0 state, RD1 ~ RD8 become output terminals and the AD conversion result is output from these pins with 8 bit parallel two's compliment format. Refer to Table 2. When $\overline{\text{READ}}$ is set at digital 1 state, RD1 ~ RD8 become input terminals. The data input to these pins is loaded into the registers at the falling edge of $\overline{\text{START}}$ signal. In this case, this data is used at the gain setting data for AGC circuit. Nominal absolute voltage gain of AGC circuit is described in Table 3. The dynamic range of the AGC circuit is about 48 dB as shown in Table 3.

$\overline{\text{READ}}$ = Digital 0

RD_8	RD_7	RD_6	RD_5	RD_4	RD_3	RD_2	RD_1	Nominal Corresponding Voltage on the Input of AGC Circuit (AGCI)
0	1	1	1	1	1	1	1	+2,480.5 mV
			∫					~ 19.5 mV Step
0	0	0	0	0	0	0	1	+19.5 mV
0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	-19.5 mV
			∫					~ 19.5 mV Step
1	0	0	0	0	0	0	0	-2,500 mV

Table 2

$\overline{\text{READ}}$ = Digital 1

RD_8	RD_7	RD_6	RD_5	RD_4	RD_3	RD_2	RD_1	Nominal Absolute Voltage Gain of AGC Circuit (dB)
1	1	1	1	1	1	1	1	+43.8
1	1	1	1	1	1	1	0	+43.6
			∫					0.1875 dB Step
0	0	0	0	0	0	1	0	-3.63
0	0	0	0	0	0	0	1	-3.81
0	0	0	0	0	0	0	0	-4.00

Table 3

Pin Name	RS	GS	JS	Function
V_{DD_2}	21	20	22	Positive power supply, +5 V. This power supply is internally connected to the digital output logical circuitry RD1 ~ RD8 to avoid the deterioration to the noise performance. Same power supply as to V_{DD_1} should be used.
DG	22	22, 23	23, 24	Digital ground, 0 V.
AG	23	24	25	Analog ground, 0 V.
AGCC	24	25	26	An external capacitor of 1 μF should be connected between AGCC and AG. This capacitor is necessary to compensate the DC offset voltage generated in the AGC circuit.

(to be continued)

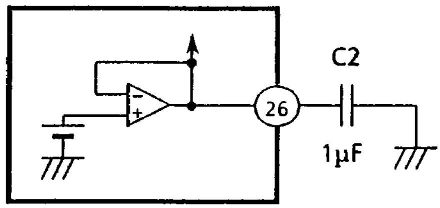
<table>
<tr><th rowspan="2">Pin Name</th><th colspan="3">Pin No.</th><th rowspan="2">Function</th></tr>
<tr><th>RS</th><th>GS</th><th>JS</th></tr>
<tr><td>VR</td><td>26</td><td>29</td><td>28</td><td>The MSM6951 provides the voltage reference which is used for AD and DA convertions and the guard tone generator.
The electrical potential is stabilized to variations of temperature or supply voltages.


Figure 6 (MSM6951BRS)
A bypass capacitor is required to keep this reference electrical in the silent condition. A capacitor with the value of 1 μF is recommended.</td></tr>
<tr><td>AIN</td><td>27</td><td>30</td><td>29</td><td>Receive analog signal input pin. The maximum input level is about +7.2 dBm (5 Vp-p).</td></tr>
<tr><td>DT, PT</td><td>28, 29</td><td>31, 32</td><td>30, 31</td><td>These pins control the transmit and receive analog signal paths for AC loop test, DTMF tone, guard tone and call progress tone. For details, refer to Table 8. When the chip is used for the V. 21 or V. 23 modem, DT and PT should be in digital 1 state.</td></tr>
<tr><td>AOUT</td><td>30</td><td>33</td><td>32</td><td>This is the transmit analog signal output terminal. The output resistance is about 10 Ω and the load resistance should be more than 20 kΩ. The higher the road resistor is, the lower the power dissipation of MSM6951B becomes.
When the full scale digital data is input to DA, the output voltage on AOUT becomes as follows. The polarity of the output voltage and DC offset are not cared in this table.
<table>
<tr><th>Input Data to DA</th><th>Reference Voltage</th><th>Output Voltage (AOUT)</th></tr>
<tr><td>Plus Full Scale</td><td rowspan="2">+2.5 V</td><td>+2.17 V</td></tr>
<tr><td>Minus Full Scale</td><td>-2.19 V</td></tr>
</table>
Table 4</td></tr>
</table>

(to be continued)

<table>
<tr><th rowspan="2">Pin Name</th><th colspan="3">Pin No.</th><th rowspan="2">Function</th></tr>
<tr><th>RS</th><th>GS</th><th>JS</th></tr>
<tr><td>LT</td><td>31</td><td>35</td><td>33</td><td>LT is used to provide the local AC loop test function.
When digital 1 is input to LT, the transmit analog signal bypasses the transmit analog filter and is directly routed to the receive analog filter. At this time, the transmit analog signal must be of the same channel with the receiver. The passband of the receive analog filter is selected by LT and MODE as shown in Table 5.
<table>
<tr><th rowspan="2">LT</th><th rowspan="2">MODE</th><th colspan="3">Receive Filter Passband</th><th rowspan="2">AIN</th><th rowspan="2">AOUT</th></tr>
<tr><th>*</th><th>V.21</th><th>V.23</th></tr>
<tr><td rowspan="2">1</td><td>0</td><td>2000 ~ 2800 Hz</td><td>1600 ~ 2240 Hz</td><td>800 ~ 2800 Hz</td><td rowspan="2">Open</td><td rowspan="2">Shorted to AG (OV)</td></tr>
<tr><td>1</td><td>800 ~ 1600 Hz</td><td>640 ~ 1280 Hz</td><td>0 ~ 620 Hz</td></tr>
<tr><td>0</td><td>×</td><td colspan="5">Normal Operating State</td></tr>
</table>
Table 5
* Bell 212A, CCITT V.22, V22 bis</td></tr>
<tr><td>DAO</td><td>32</td><td>36</td><td>34</td><td>DAO is the output of the digital to analog converter. Normally, this pin is connected to the XIN pin directly. As the output impedance is low and the minimum input impedance of XIN is 500 KΩ, the transferred signal level from DAO to XIN can be adjusted by the external resistors.</td></tr>
<tr><td>GT</td><td>33</td><td>37</td><td>35</td><td>GT selects the frequency of the guard tone, which is a necessary function for this chip to be used internationally.
At the same time, the passband of LPF is decided according to the guard tone frequency.
LPF is useful also for DTMF or extra tone transmitting with its wider passband.
<table>
<tr><th>GT</th><th>Guard Tone Frequency</th><th>LPF's Passband</th></tr>
<tr><td>0</td><td>550 Hz</td><td>0 ~ 620 Hz</td></tr>
<tr><td>1</td><td>1,800 Hz</td><td>0 ~ 2480 Hz</td></tr>
</table>
Table 6
LPF plays a role of rejecting harmonic components from the original tone. In addition to it, this LPF can be also used in the receiver as the band limiting filter during call progress tone detection.
GT is used to provide the receive and the transmit filter for CCITT V.21 or V.23 modem function. Refer to Table 8.</td></tr>
<tr><td>XIN</td><td>34</td><td>38</td><td>36</td><td>XIN is the transmit analog signal input. As described in the paragraph for DAO, XIN is normally connected to DAO directly. The maximum input level is about +7.2 dBm (5 Vp-p).</td></tr>
</table>

(to be continued)

Pin Name	Pin No.			Function
	RS	GS	JS	
SP	35	39	37	This pin controls the transmit and receive analog signal paths for V.23 and the other standards. When the chip is used for the V.23 modem, SP should be in digital 1 state. For details, refer to Table 8.
MODE	36	40	38	MODE determines the role of each BPF by controlling SWT and SWR as shown in the circuit configuration. When digital 0 is applied to this pin, the low channel BPF is assigned to the transmitter and the high channel BPF is assigned to the receiver. This condition is called as "Originate mode". When digital 1 is input to MODE, the positions of BPFs are reversed and this is called as "Answer mode". During the AC loop back test, the frequency band used for this test becomes the receiver's channel determined by MODE.

MODE	Mode	Transmit Band (Hz)			Receive Band (Hz)		
		*	V.21	V.23	*	V.21	V.23
0	Originate	800 ~ 1600	640 ~ 1280	0 ~ 620	2000 ~ 2800	1600 ~ 2240	800 ~ 2800
1	Answer	2000 ~ 2800	1600 ~ 2240	800 ~ 2800	800 ~ 1600	640 ~ 1280	0 ~ 620

* Bell 212A, CCITT V.22, V.22 bis

Table 7

Pin Name	RS	GS	JS	Function
RFO	37	41	39	RFO is the analog signal output of the receive filter. This signal is to be connected to the AGC circuit through an external capacitor of 0.1 μF. The load resistance should be more than 20 kΩ. The maximum voltage swing is about 5 Vp-p.
AGCI	38	44	40	AGCI is the input pin of the AGC circuit and is connected to RFO through an external capacitor as shown in Figure 7. The role of the capacitor is to avoid a bad influence by the DC offset voltage generated in the receive filter. The input resistance is high and the maximum input voltage swing is about 5 Vp-p.

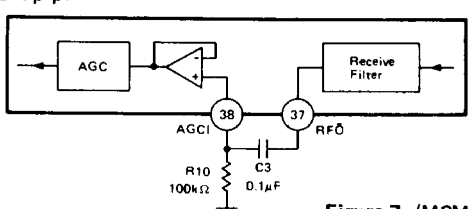


Figure 7 (MSM6951BRS)

(to be continued)

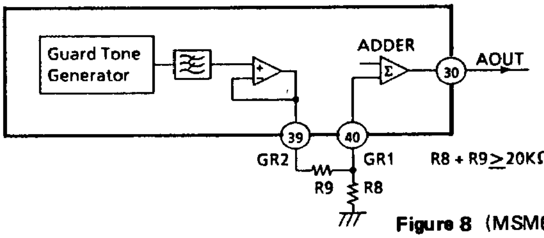
<table>
<tr><th rowspan="2">Pin Name</th><th colspan="3">Pin No.</th><th rowspan="2">Function</th></tr>
<tr><th>RS</th><th>GS</th><th>JS</th></tr>
<tr><td>GR2, GR1</td><td>39,
40</td><td>45,
47</td><td>41,
42</td><td>The output guard tone level can be adjusted by using external resistors as shown in Figure 8.


Figure 8 (MSM6951BRS)
The approximate output tone level is determined by the following equation.
$$V_{AOUT} = 20 \cdot \log \frac{R_8}{R_8 + R_9} \quad [\text{dBm}]$$
In Bell's standard sets, the guard tone function is not applied.</td></tr>
<tr><td>VSS</td><td>41</td><td>48</td><td>43</td><td>Negative power supply, −5 V.</td></tr>
<tr><td>V_{DD1}</td><td>42</td><td>21,
49</td><td>44</td><td>Positive power supply, +5 V.</td></tr>
</table>

MSM6951BRS CIRCUIT WIRING ILLUSTRATION

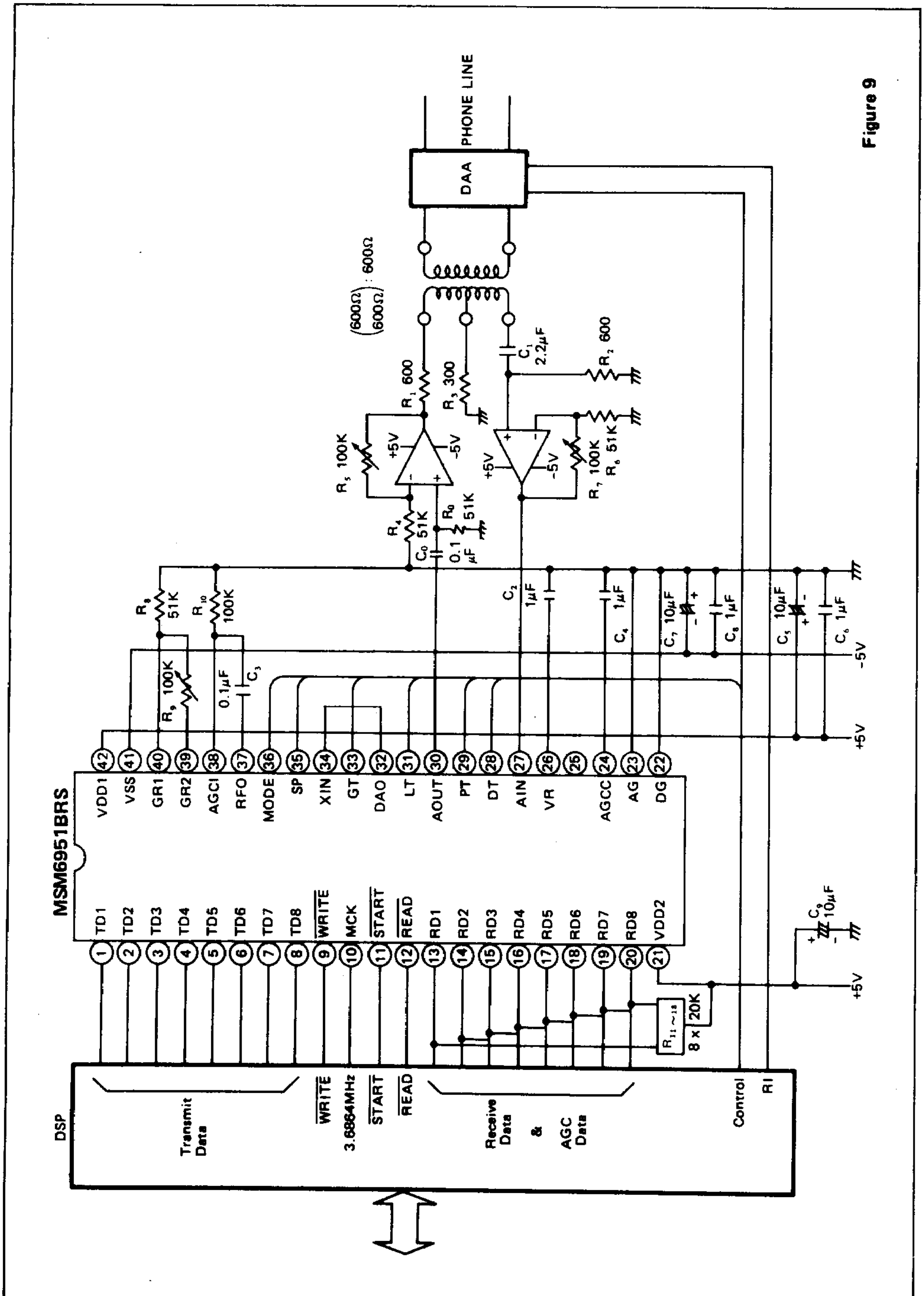


Figure 9

APPLICATION INFORMATIONS

1. Typical Master Clock (MCK) Frequency and $\overline{\text{WRITE}}$, $\overline{\text{START}}$, $\overline{\text{READ}}$ signals.

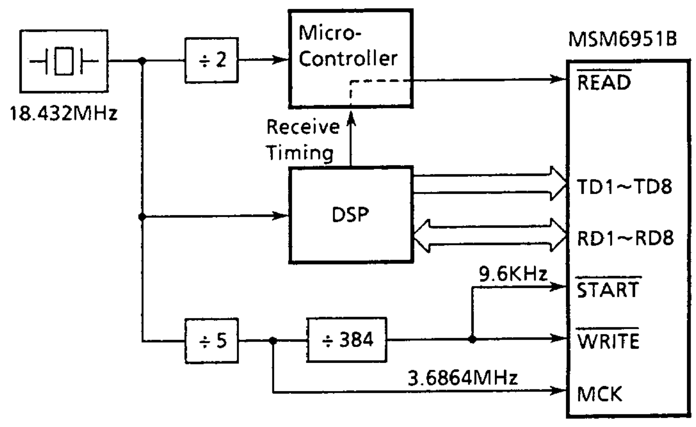


Figure 10 Clock and Control Signals

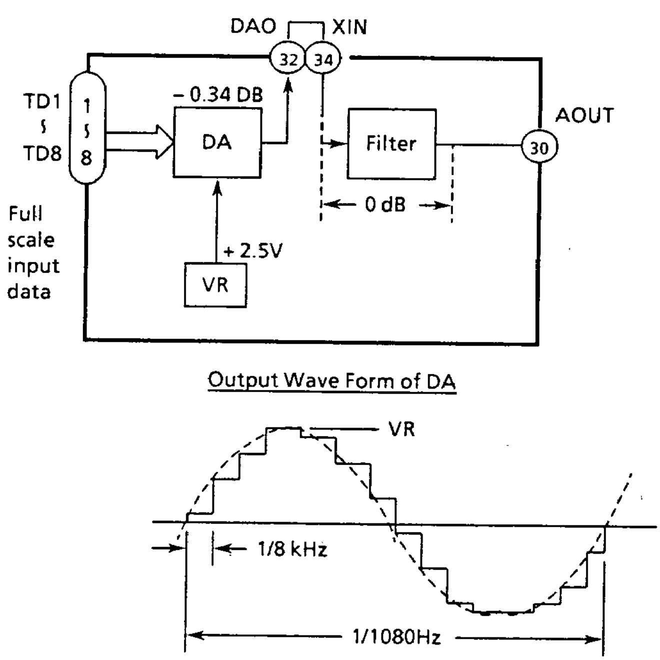
Figure 10 shows the typical design for the operating clock and control signals.

It is desirable to use one time base for the noise performance of the modem system.

2. Consideration for Transmit Signal Level Diagram

The consideration is difficult to be described because of the Aperture Effect* depending on the sampling period and the peak factor in PSK (1200 bps) and QAM (2400 bps) modes. *See Figure 12.
To make easy understandings, the following model should be defined here.

Sampling period	;	8KHz
Modem mode	;	CCITT V.21, CH.1 (FSK, 1080 ± 100Hz)
Input data to TD1~TD8	;	± Full scale
Reference voltage (VR)	;	+ 2.50V



$$20 \log \frac{2.5}{1.095} = +7.17 \text{ dBm, } 0 \text{ dBm} = 1.095 \text{ Vop}$$

$$20 \log \frac{\sin X}{X} = -0.26 \text{ dB, } X = \frac{\pi . 1080}{8000} \quad \text{[Aperture effect]}$$

Figure 11 Transmit Signal Level

As a result of this case, the transmit signal (1080Hz) amplitude at AOUT becomes as follows.

$$+7.17 \underbrace{-0.26}_{A} \underbrace{-0.34}_{B} = +6.57 \text{ dBm}$$

A : Aperture effect at 1080Hz

B : Loss of the DA converter

In the actual applications, there is not a design by such level diagram. This is just a sample for understandings.

Normally, the amplitude at AOUT may be designed to be around 0dBm. Particularly for PSK or QAM modulation, since the modulated analog signal has the peak factor, to consider it into the design of the output signal amplitude is very important.

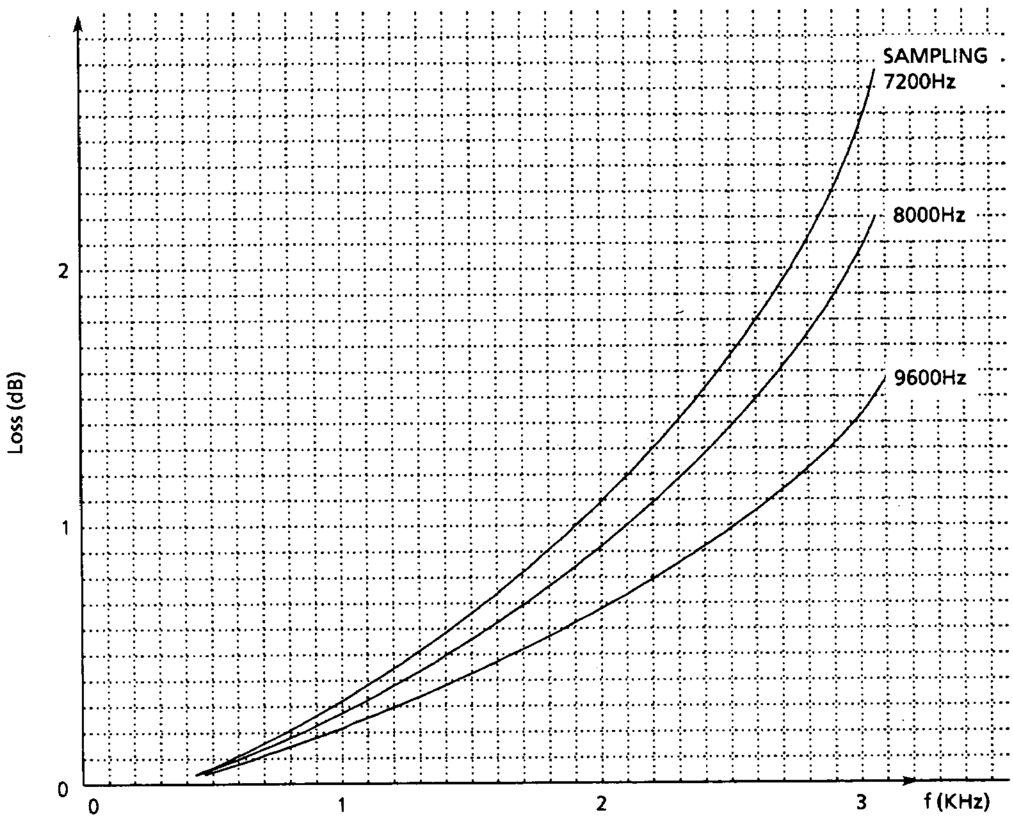


Figure 12 Aperture effect

3 Original Transmission Mode

The signal pass in this mode is shown in Figure 13.

The low band signal must be transmitted and the high band signal must be received. MODE determines the positions of two BPFs by controlling SWT1, SWT2, SWR1 and SWR2. When MODE is in digital 0 state, the low channel BPF is assigned to the transmitter and the high channel BPF is assigned to the receiver. Both DT and PT should be in digital 1 state so that the guard tone function should be disabled.

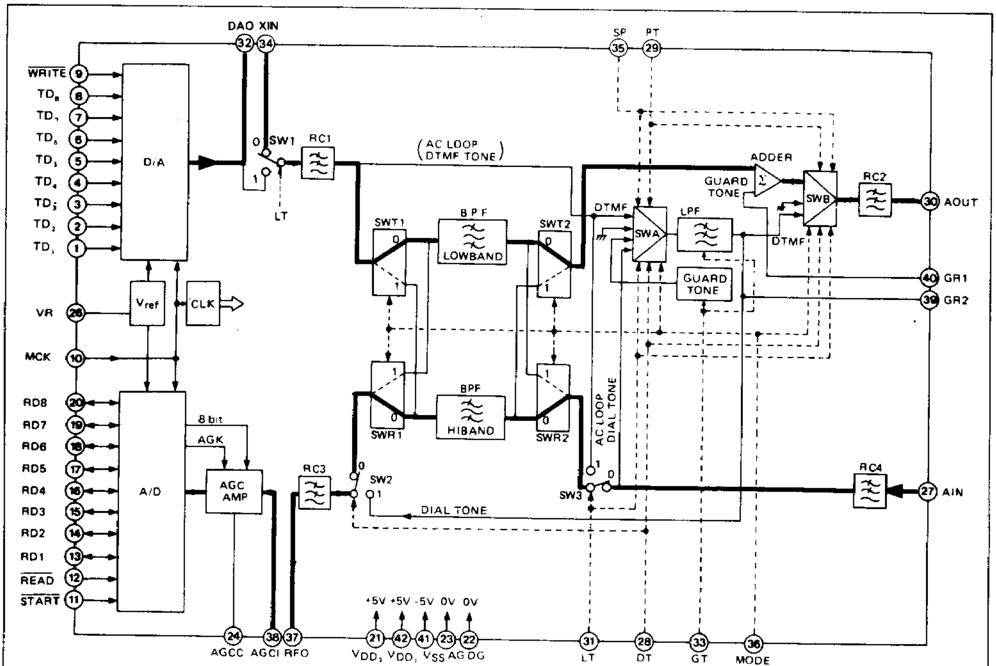


Figure 13 (MSM6951BRS)

4 Answer Transmission Mode

The signal path in this mode is shown in Figure 14.

The high band signal must be transmitted and the low band signal must be received. When MODE is in digital 1 state, the high channel BPF is assigned to the transmitter and the low channel BPF is assigned to the receiver. In some applications, it is required to mix a guard tone to the high channel transmit signal in the answer mode. The control signals on DT, PT and GT determine the guard tone function. When DT and PT are in digital 1 state, the guard tone function is disabled and only the high channel transmitter is enabled. When DT, PT and GT are in digital 0 state, the guard tone, the frequency of which is 550 Hz, is mixed to the transmit signal.

When GT is changed to digital 1 keeping DT and PT in digital 0 state, another guard tone, the frequency of which is 1800 Hz, is mixed to the transmit signal.

The original guard tone is filtered through LPF and only its fundamental component is extracted and mixed to the transmit signal. The cut-off frequency of LPF is about 620Hz while GT is in digital 0 state and becomes about 2480Hz while GT is in digital 1 state.

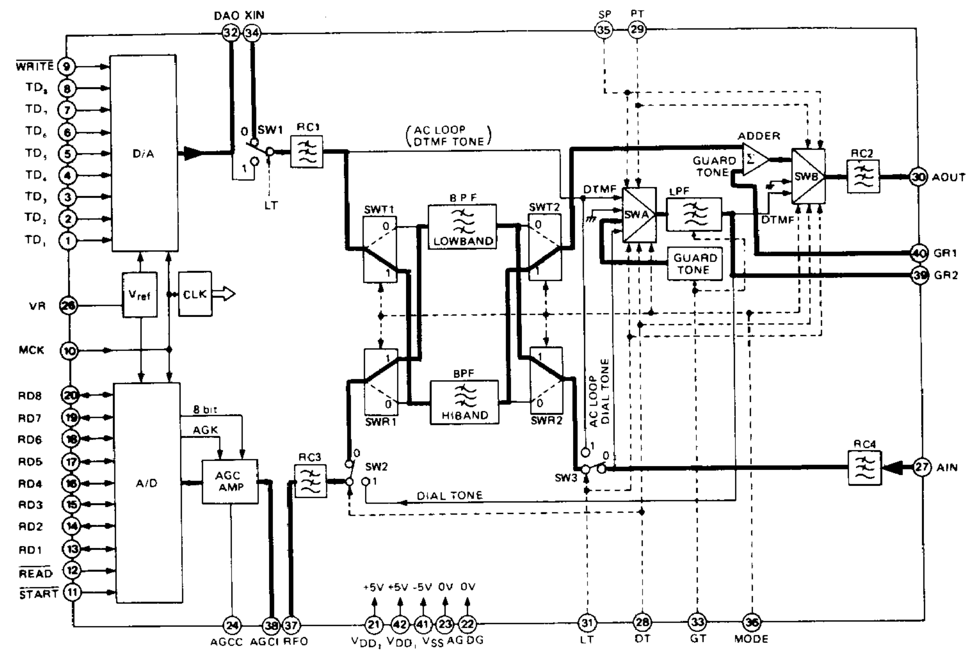


Figure 14 (MSM6951BRS)

5 Tone Transmit Mode

The signal path in this mode is shown in Figure15.

LPF put on this path has two kinds of its cut-off frequency (620 Hz/2480 Hz). This mode is useful for DTMF signaling and so forth. Refer to Table 8.

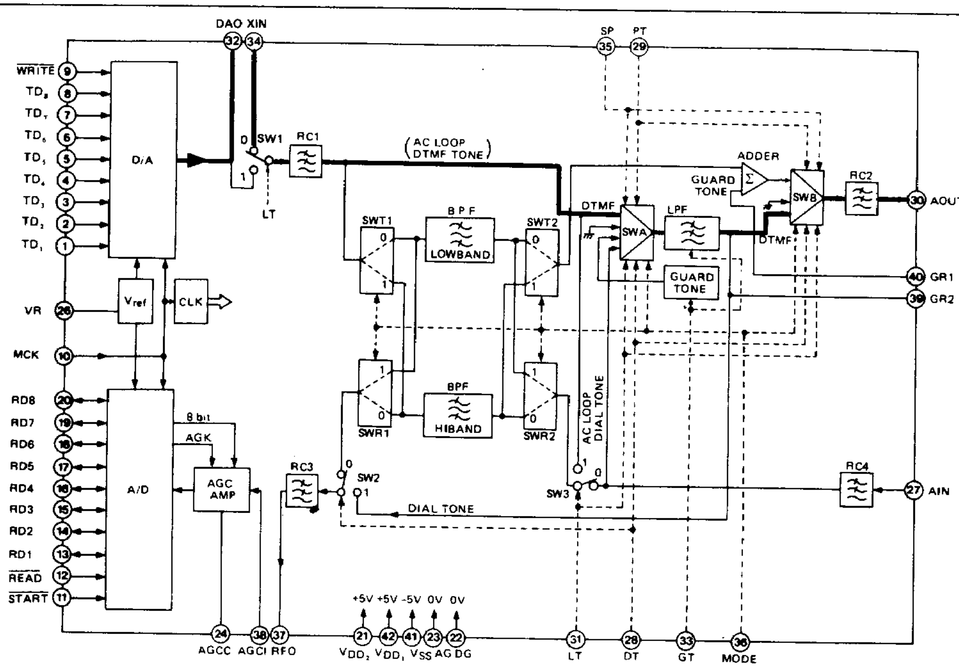


Figure 15 (MSM6951BRS)

6 Tone Receive Mode

The signal path in this mode is shown in Figure 16.

LPF put on this path has two kinds of cut-off frequency — 620 Hz and 2480 Hz. This mode is useful for call progress tone monitoring, such as for dial tone. Refer to Table 9-1. In this mode, AOUT is connected to AG (0V) internally.

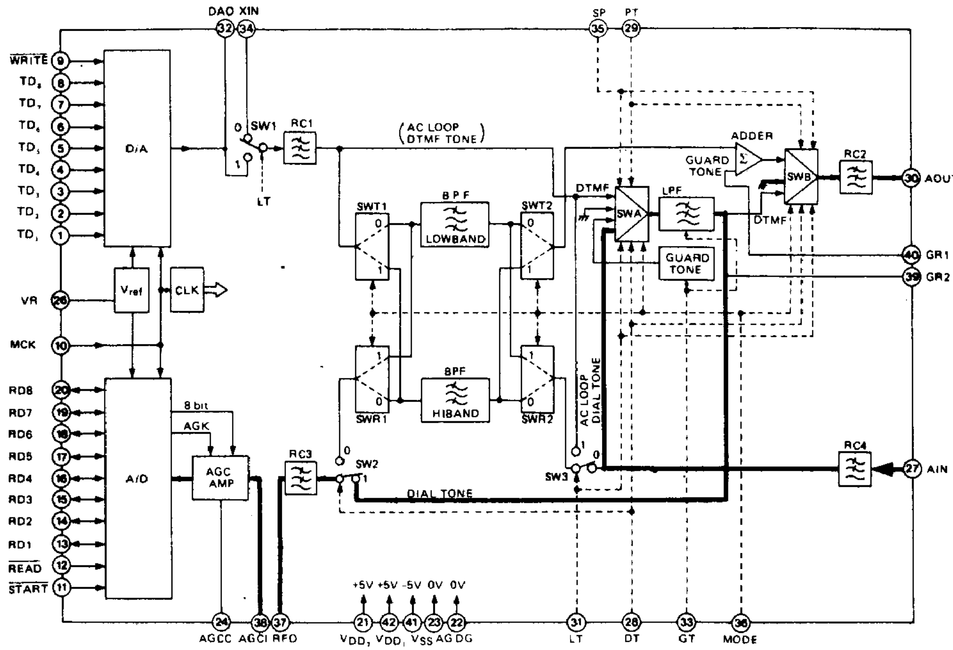


Figure 16 (MSM6951BRS)

7 AC Loop-back Test Mode

The signal path in this mode is shown in Figure 17.

The modem system has to receive its own transmit signal to check the modem operation.

In this mode, the transmit filter is skipped from the signal route and the channel used for AC Loop-back test is determined by the receiver's channel assigned by MODE. Refer to Table 8.

AOUT is connected to AG (0V) internally.

During AC Loop back test (LT = 1), the output of the DA converter is connected to the forward signal route internally, and XIN is disconnected from the signal path.

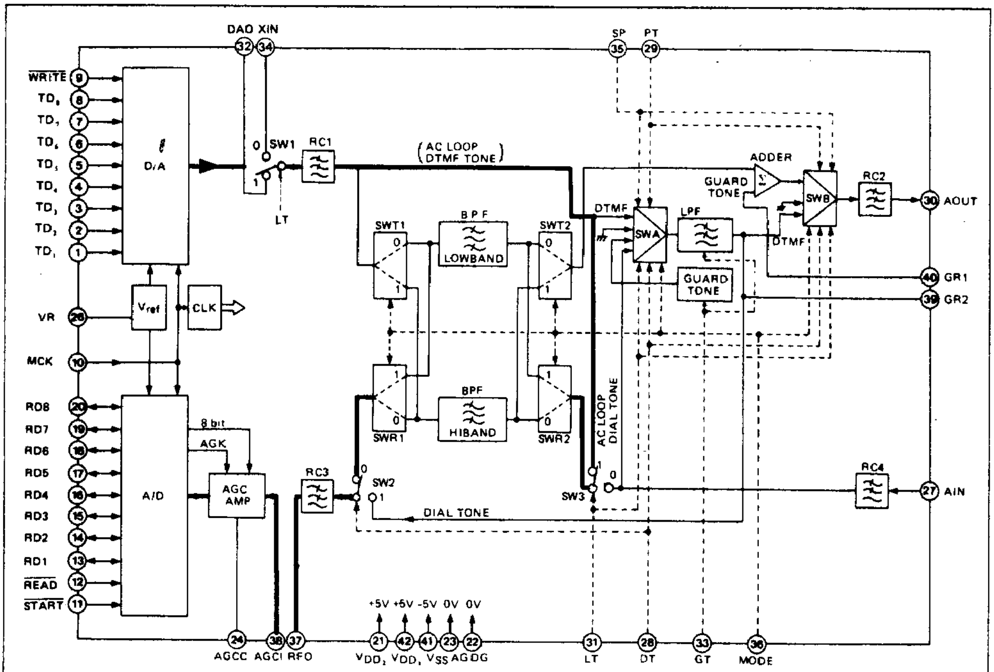


Figure 17 (MSM6951BRS)

8 CCITT V.21 Transmission Mode

The chip provides the V.21 filtering function.
V.21 is the 300BPS full duplex modem standard and applies the different frequency bands from other standards — Bell 212A, CCITT V.22, V.22 bis —. In V.21, 1080 Hz (Low band) and 1750 Hz (High band) are FSK carriers, and the required bandwidth is about 300 Hz.

To realize this filtering function, the clock frequency for on-chip BPFs is set at 80% of its original value when V.21 mode is selected.
Refer to Table 8.

9 CCITT V.23 Transmission Mode

As another function, the chip provides the V.23 filtering function including the 75BPS backward channel filter.

The BPF for the main 1200BPS channel is realized by combining second order filters which are originally designed for Bell 212A or CCITT V.22/V.22 bis. For the LPF for the optional 75BPS backward channel, multi-purpose LPF can be commonly applied with its narrow bandwidth.

The signal path in this mode are shown in Figure 18 and 19. Figure 18 shows the path for the main channel (1200 BPS) transmitting and the backward channel (75 BPS) receiving. Figure 19 shows the reverse case.

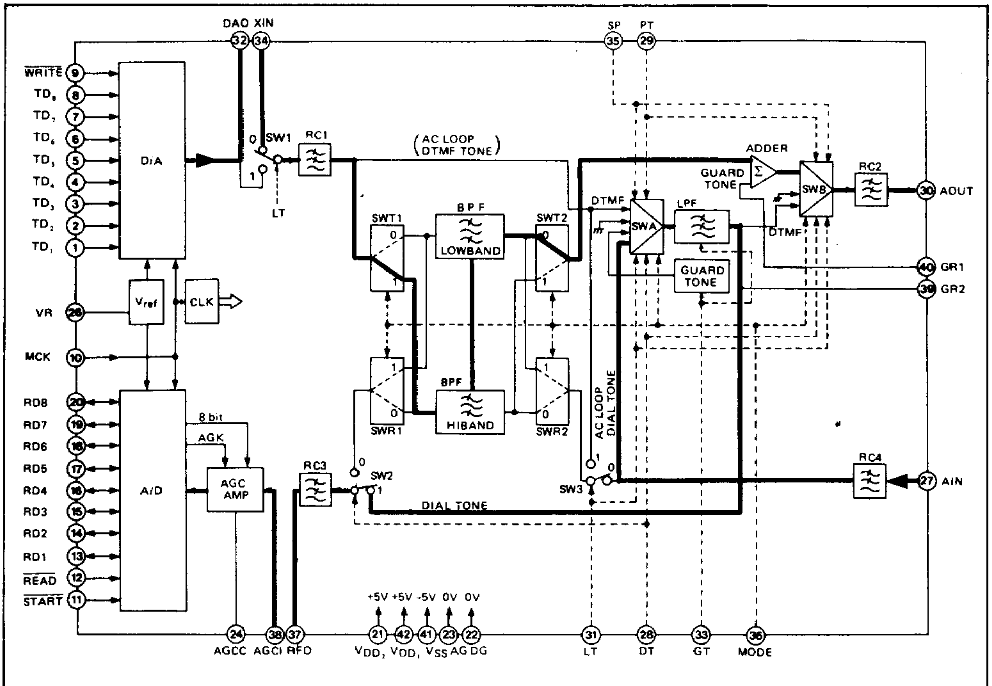


Figure 18 (MSM6951BRS)

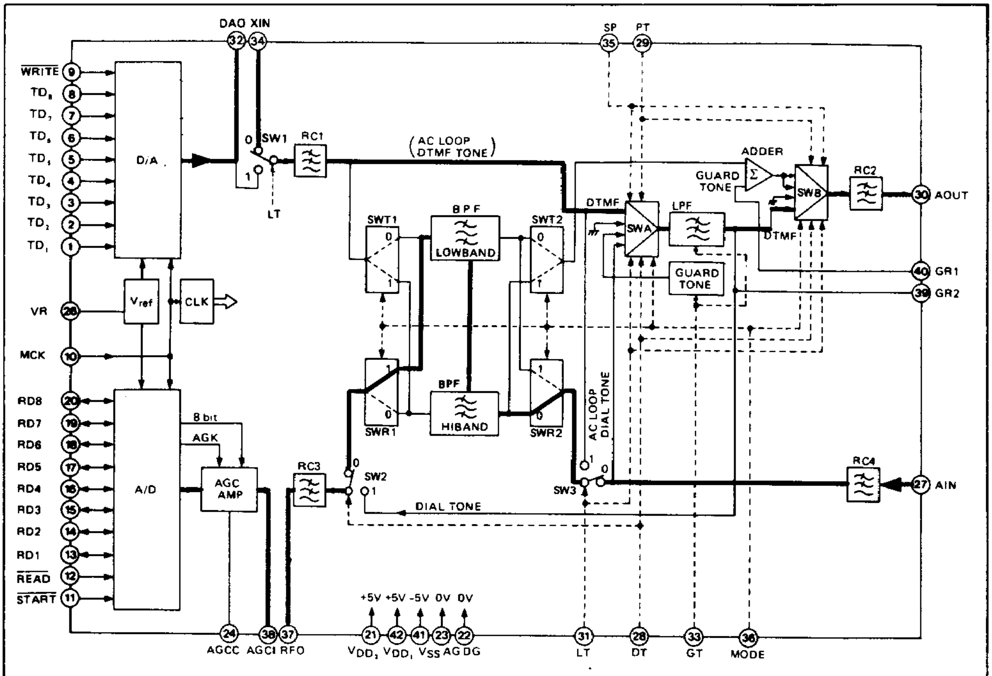


Figure 19 (MSM6951BRS)

Control Signal						Transmitter			Receiver		Note	
DT	PT	MODE	GT	SP	LT	Pass Band*1	Gain*1	Guard Tone	Pass Band*2	Gain*2		
1	1	0	0	0	0	800~1600Hz	0dB		2000~2800Hz	0dB	Originate	FSK DPSK
1	1	1	0	0	0	2000~2800Hz	0dB		800~1600Hz	0dB	Answer	
0	0	1	0	0	0	2000~2800Hz	0dB	550Hz	800~1600Hz	0dB	Answer with Guard Tone	
0	0	1	1	0	0	2000~2800Hz	0dB	1800Hz	800~1600Hz	0dB		
0	1	0	0	0	0	0~ 620Hz	0dB		2000~2800Hz	0dB	Extra Tone/DTMF Tone Transmitting	
0	1	1	0	0	0	0~ 620Hz	0dB		800~1600Hz	0dB		
0	1	0	1	0	0	0~2480Hz	0dB		2000~2800Hz	0dB		
0	1	1	1	0	0	0~2480Hz	0dB		800~1600Hz	0dB		
1	0	X	0	0	0	*3			0~ 620Hz	0dB	Filtering for Call Progress Tone	
1	0	X	1	0	0	*3			0~2480Hz	0dB		
1	1	0	0	0	1	*3			2000~2800Hz	0dB	AC Loop-back	FSK DPSK
0	0	0	X	0	1	*3			2000~2800Hz	0dB		
1	1	1	0	0	1	*3			800~1600Hz	0dB		
0	0	1	X	0	1	*3			800~1600Hz	0dB		

*1 XIN → AOUT
*2 AIN → RFO
*3 AOUT is connected to Ground.

Table 8-1 Various Operating Modes

Control Signal						Transmitter			Receiver		Note	
DT	PT	MODE	GT	SP	LT	Pass Band*1	Gain*1	Guard Tone	Pass Band*1	Gain*2		
1	1	0	1	0	0	640～1280Hz	0dB		1600～2240Hz	0dB	Originate	CCITT V.21
1	1	1	1	0	0	1600～2240Hz	0dB		640～1280Hz	0dB	Answer	
1	1	0	1	0	1	*3			1600～2240Hz	0dB	AC Loop-back	
1	1	1	1	0	1	*3			640～1280Hz	0dB		
1	1	0	1	1	0	0～620Hz	0 dB		800～2800Hz	0dB		CCITT V.23 wtih Backward Channel
1	1	1	1	1	0	800～2800Hz	0dB		0～620Hz	0dB		
1	1	0	1	1	1	*3			800～2800Hz	0dB	AC Loop-back	
1	1	1	1	1	1	*3			0～620Hz	0dB		

Table 8-2 Various Operating Modes