OKI Semiconductor

This version: Aug. 1998
Previous version: Nov. 1996

MSM6996H/6996V/6997H/6997V/6998/6999

Single Chip CODEC

GENERAL DESCRIPTION

The MSM6996H/MSM6996V/MSM6997H/MSM6997V/MSM6998/MSM6999 are a single-channel CODEC CMOS ICs containing filters for A/D and D/A converting of the voice signal ranging from 300 Hz to 3400 Hz.

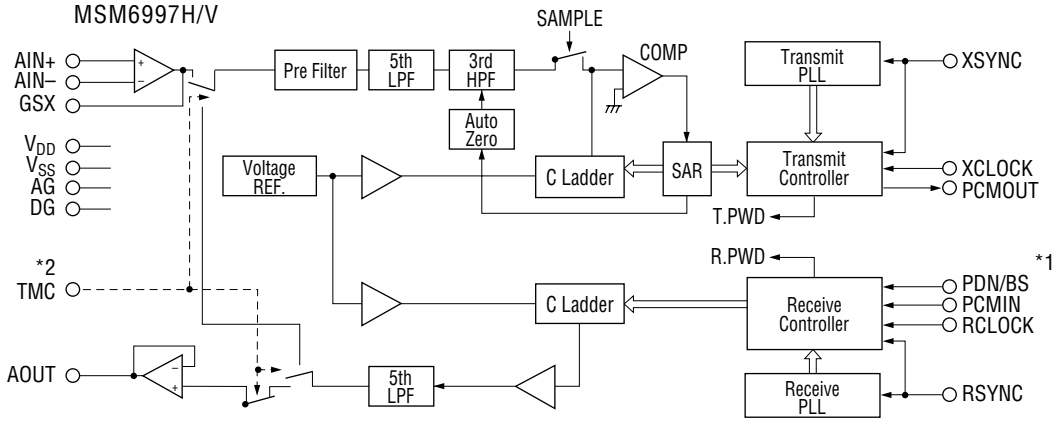
FEATURES

- Compliance with ITU-T companding Law
  MSM6996H/MSM6996V/MSM6998 : A-law
  MSM6997H/MSM6997V/MSM6999 : μ-law
- Capable of independent operation of transmission and reception
- Transmission clock in the range of 64 kHz to 2048 kHz
- Adjustable transmit gain
- 600 Ω drive for analog output
  MSM6996H/MSM6996V/MSM6997H/MSM6997V single end drive
  MSM6998/MSM6999 Push-pull drive
- Built-in analog loop back fanction
  MSM6996V/MSM6997V
- Built-in reference voltage source
- Low Power Dissipation (60 mW to 70 mW Typ.)
- Package options :

16-pin plastic DIP (DIP16-P-300-2.54)	(Product name : MSM6996HRS/MSM6997HRS)
	(Product name : MSM6996VRS/MSM6997VRS)
	(Product name : MSM6998RS/MSM6999RS)
16-pin cer DIP (DIP16-G-300-2.54-1)	(Product name : MSM6996HAS/MSM6997HAS)
	(Product name : MSM6996VAS/MSM6997VAS)
	(Product name : MSM6998AS/MSM6999AS)
24-pin plastic SOP (SOP24-P-430-1.27-K)	(Product name : MSM6996HGS-K/MSM6997HGS-K)
	(Product name : MSM6996VGS-K/MSM6997VGS-K)
	(Product name : MSM6998GS-K/MSM6999GS-K)

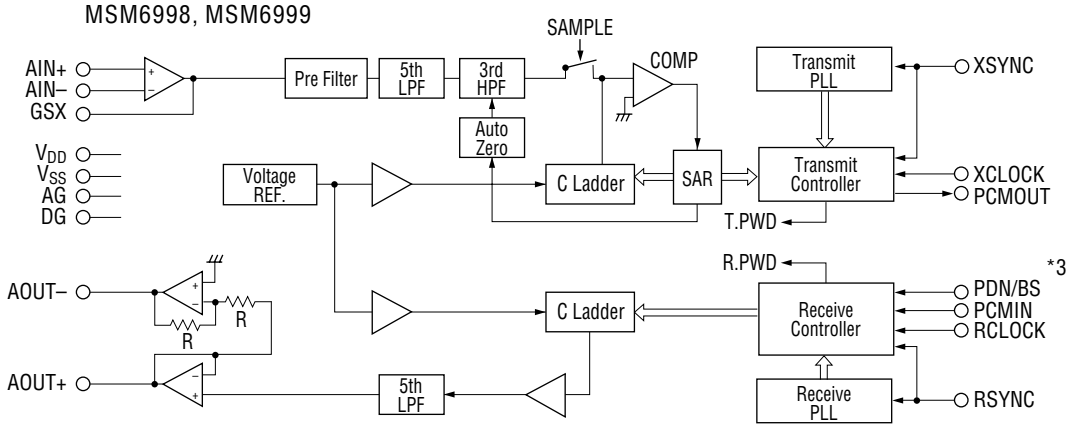
BLOCK DIAGRAM

MSM6996H/V
MSM6997H/V



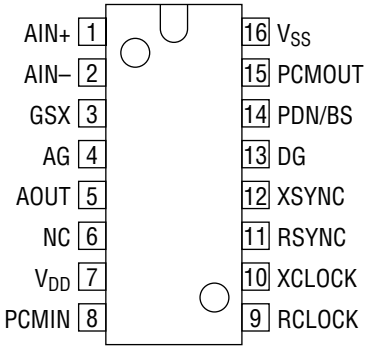
*1 BS : Only MSM6997H/V
*2 Only MSM6996V, MSM6997V

MSM6998, MSM6999



*3 BS : Only MSM6999

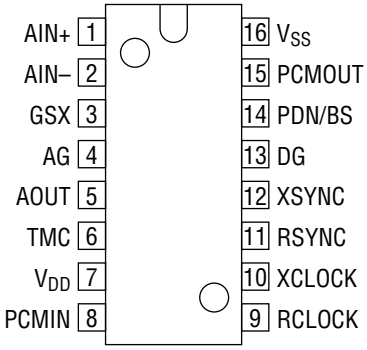
PIN CONFIGURATION (TOP VIEW)



NC : No connect pin

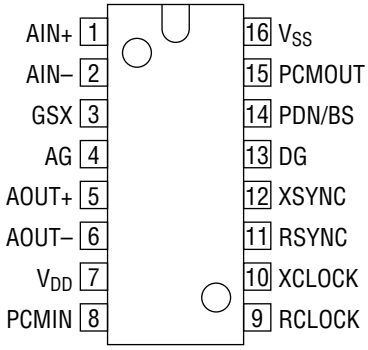
16-Pin Plastic DIP

MSM6996HRS
MSM6997HRS



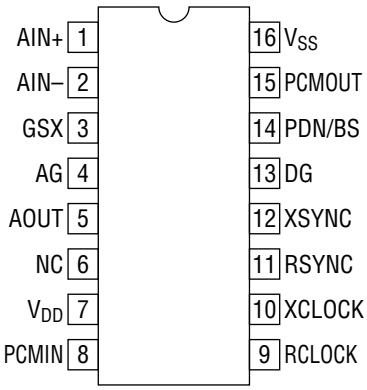
16-Pin Plastic DIP

MSM6996VRS
MSM6997VRS



16-Pin Plastic DIP

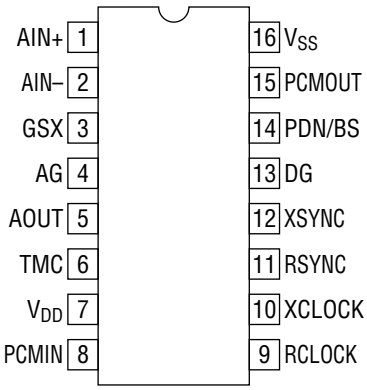
MSM6998RS
MSM6999RS



NC : No connect pin

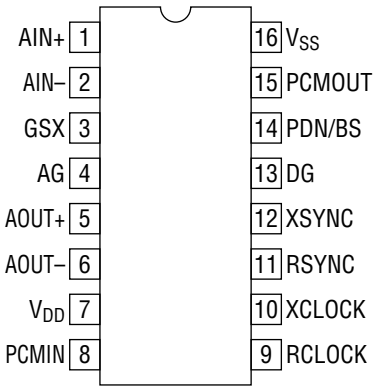
16-Pin Cer DIP

MSM6996HAS
MSM6997HAS



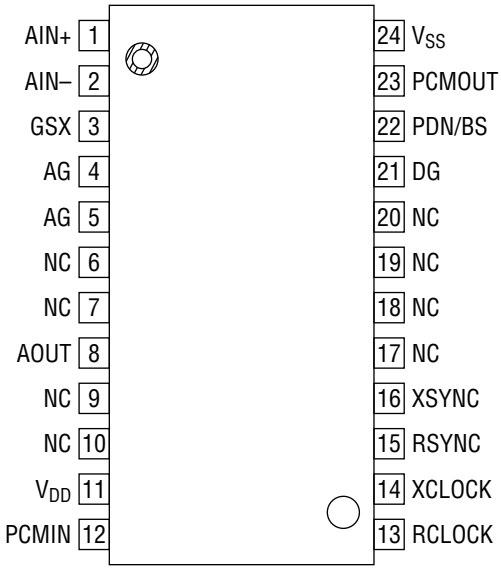
16-Pin Cer DIP

MSM6996VAS
MSM6997VAS



16-Pin Cer DIP

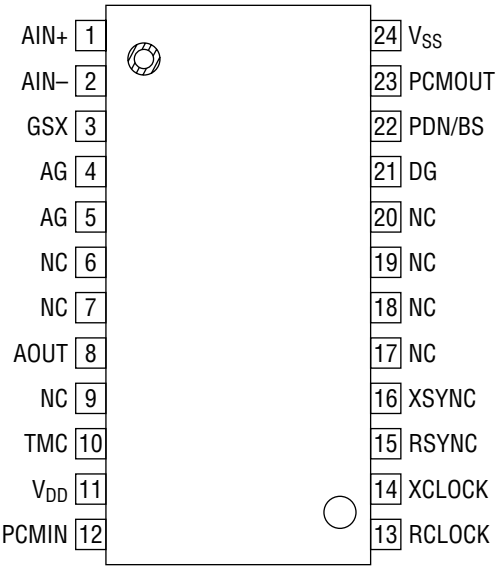
MSM6998AS
MSM6999AS



NC : No connect pin

24-Pin Plastic SOP

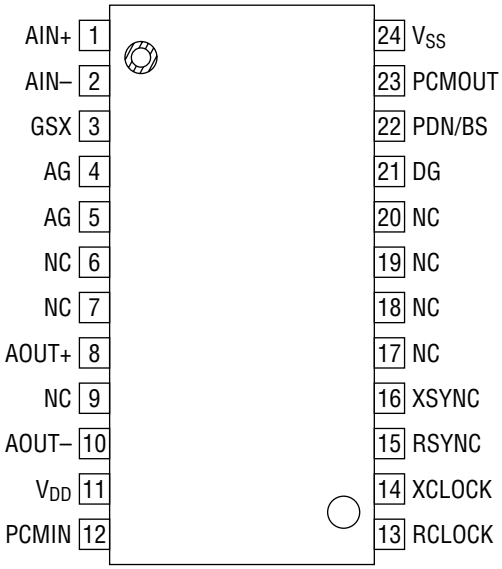
MSM6996HGS-K
MSM6997HGS-K



NC : No connect pin

24-Pin Plastic SOP

MSM6996VGS-K
MSM6997VGS-K



NC : No connect pin

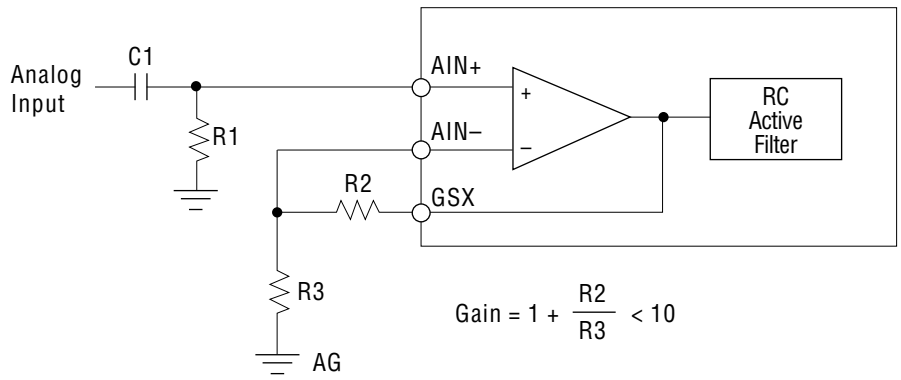
24-Pin Plastic SOP

MSM6998GS-K
MSM6999GS-K

PIN AND FUNCTIONAL DESCRIPTIONS

AIN+, AIN–, GSX

These three pins are used for the transmit level adjustment.
AIN+ is a non-inverting analog input pin which is connected to the non-inverting input of a transmit amplifier.
AIN– is an inverting analog input pin which is connected to the inverting input of the transmit amplifier.
GSX is a transmit amplifier output pin.
Adjustment can be done by following method.



Notes: 1. $R_2 + R_3 > 10\ k\Omega$
2. When the DC off-set voltage of analog input is more than 20 mV, C1 and R1 should provide for DC blocking.
In this case, cut-off frequency of HPF, composed by R_1 and C_1, should be less than 30 Hz.
3. R_1 should be less than 20 kΩ

AG

AG is an analog ground.
AG is connected to the analog system ground.

AOUT

AOUT is the analog signal output pin for the MSM6996H/V and MSM6997H/V.
The output voltage range is 5 V_{PP}. This output can drive the 600 Ω resistor.

AOUT+, AOUT–

Analog output for the MSM6998 and MSM6999.
The output signal amplitudes are 5 V_{PP}. The AOUT– output is inverted to the AOUT+ output. These outputs can drive a 600 Ω impedance.

V_{DD}

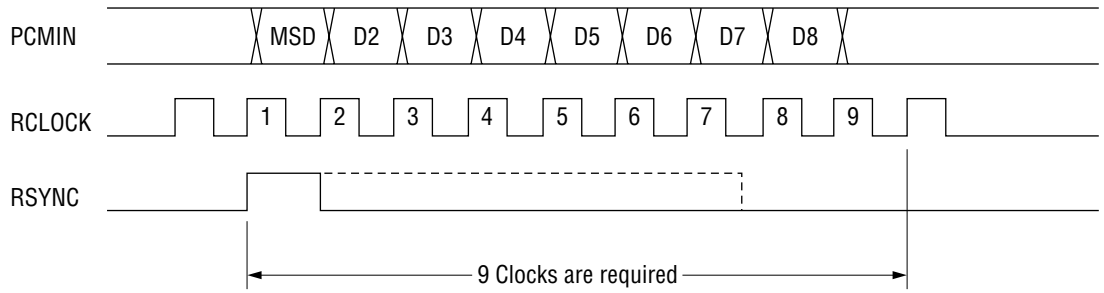
V_{DD} is the positive power supply.
The voltage supplied to this pin should be +5 V ±5%.

PCMIN

PCM signal input.
The serial input PCM signal is converted from digital to analog, synchronizing with the synchronous signal RSYNC and clock signal RCLOCK.
The data rate of PCM signal ranges from 64 kbps to 2048 kbps.
The PCM signal is read at the falling edge of the clock signal and latched into the internal register when finished to read eight bits data.
The top of the PCM data is specified by RSYNC pulse timing.

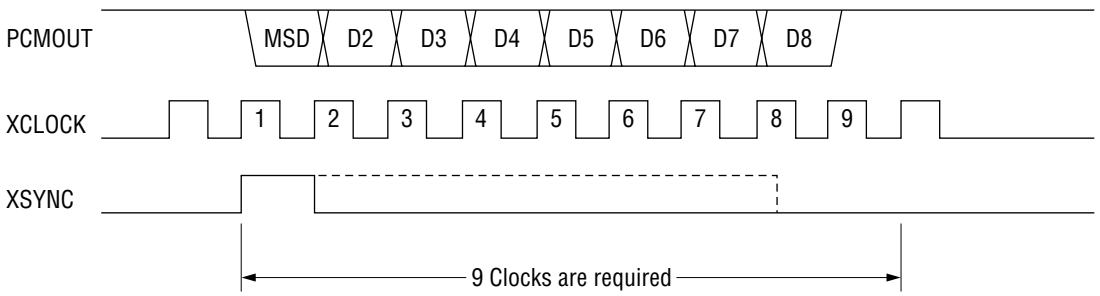
RCLOCK

Receive clock pulse input.
The frequency of this clock pulse should be identified with the data rate of PCM input signal at the PCMIN pin.
This RCLOCK signal can be a continuous clock or a burst clock with nine bits or more.
In the case of a burst clock, input the following timing.



XCLOCK

Transmit clock input.
The PCM output data rate from the PCMOUT pin is set by this clock frequency.
The applicable clock frequencies range from 64 kHz to 2048 kHz.
This XCLOCK signal can be a continuous clock or a burst clock with nine bits or more.
In the case of a burst clock, input the following timing.



RSYNC

Receive synchronizing signal input.
Eight required bits are selected from serial PCM signals on the PCMIN pin by the receive synchronizing signal.
The whole timing signal in the receive section are synchronize by this synchronizing signal.
This signal must be synchronize in phase with RCLOCK.
The frequency should be 8 kHz ±50 ppm to guarantee the AC characteristics of receive section.
However, same as the RCLOCK frequency, this device can operate in the range of 8 kHz ±2 kHz, with no guarantee of adherence to the electrical characteristics in this specification as a catalogue value.
Fixing this signal to logic "1" or "0", the receive circuit is driver in a power down state.

XSYNC

Transmit synchronizing signal input.
The PCM output signal from the PCMOUT pin is output in synchronization with this transmit synchronizing signal.
All transmit timing signals are triggered to synchronize with this signal. This signal should be synchronized in phase with XCLOCK pulse.
The frequency should be 8 kHz ±50 ppm to guarantee the AC characteristics of transmit section.
Fixing this signal to logic "1" or "0", the transmit circuit is driver in a power down state.

DG

Ground of digital signal.
This pin is electrically separated from the AG pin in this device.
The DG pin must be connected to the AG pin on the printed circuit board to make common to the AG pin.

PDN/BS

Power down signal input.
When this input is held at low level more than 1 ms, the device is put into the power-down mode.

PCMOUT

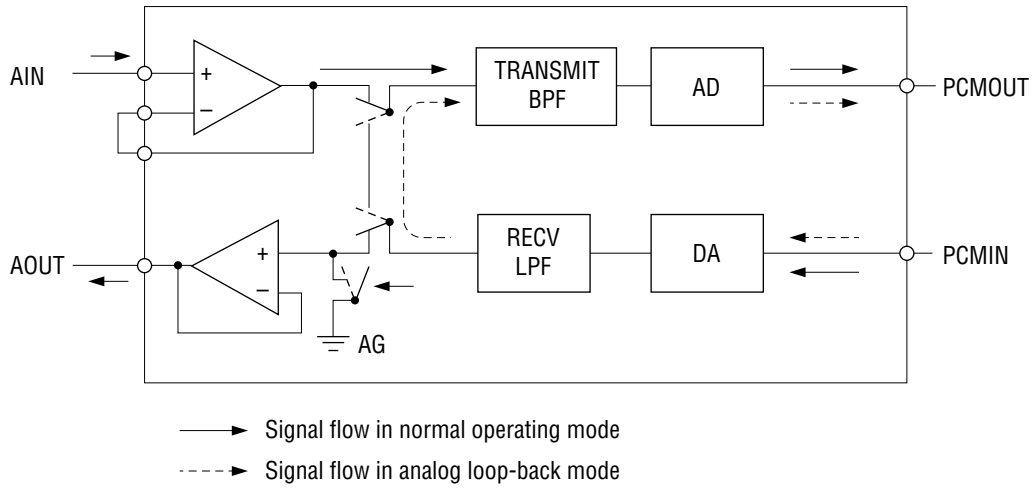
PCM signal output.
The PCM output signal is output in synchronization with the rising edge of XCLOCK pulse orderly from MSD first. (The first bit of the PCM signal may output at the rising edge of XSYNC pulse, according to the timing of XSYNC and XCLOCK pulse.). During the PCMOUT signal output except the 8-bit pulses, the pin is in an open state, therefore, multiple connections by wired-OR are easily possible at this pin.
The code companding law and output code format depend on ITU-T Recommendation G.711, and for the MSM6996H, MSM6996V, and MSM6998 (A-law) the output PCM signals are obtained by inverting the even bits of signals.

Input/Output Level	PCMIN/PCMOUT															
	MSM6996 (A-law) MSM6998 (A-law)								MSM6997 (μ-law) MSM6999 (μ-law)							
+Full scale	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0
+0	1	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1
–0	0	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1
–Full scale	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0

TMC

Control signal input for mode selection.
This pin select the normal operating mode or analog loop-back mode.

TMC Input	Mode
> 2.0 V	Normal operation
< 0.8 V	Analog loop-back



V_{SS}

Negative voltage power supply.
The range of power supply voltage is –5 V ±5%.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	—	0 to 7	V
	V_{SS}	—	–7 to 0	V
Analog Input Voltage	V_{AIN}	—	V_{DD} –0.3 to V_{DD} + 0.3	V
Digital Input Voltage	V_{DIN}	—	–0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(Ta = 0°C to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	—	4.75	5	5.25	V
	V_{SS}	—	–5.25	–5	–4.75	V
Operating Temperature	Ta	—	0	25	70	°C
Analog Input Voltage	V_{AIN}	Connect AIN– and GSX	—	—	5	V_{P-P}
Input High Voltage	V_{IH}	XSYNC, XCLOCK, PCMIN,	2.0	—	V_{DD}	V
Input Low Voltage	V_{IL}	RSYNC, RCLOCK, TMC, PDN/BS	0	—	0.8	V
Clock Frequency	f_C	XCLOCK, RCLOCK	64	—	2048	kHz
Sync Pulse Frequency	f_S	XSYNC, RSYNC	—	8	—	kHz
Clock Duty Ratio	D_L	XCLOCK, RCLOCK	40	50	60	%
Digital Input Rise Time	t_{Ir}	XSYNC, XCLOCK, PCMIN,	—	—	50	ns
Digital Input Fall Time	t_{If}	RSYNC, RCLOCK (Fig. 1)	—	—	50	ns
Transmit Sync Timing	t_{XS}	XCLOCK→XSYNC (Fig. 2)	50	—	—	ns
	t_{SX}	XSYNC→XCLOCK (Fig. 2)	100	—	—	ns
Receive Sync Timing	t_{RS}	RCLOCK→RSYNC (Fig. 2)	50	—	—	ns
	t_{SR}	RSYNC→RCLOCK (Fig. 2)	100	—	—	ns
Transmit Sync Pulse Width	t_{WX}	—	1/fc	—	—	µs
Receive Sync Pulse Width	t_{WR}	—	1/fc	—	—	µs
PCMIN Set-up Time	t_{DS}	—	100	—	—	ns
PCMIN Hold Time	t_{DH}	—	100	—	—	ns
BS Set-up Time *	t_{BS}	—	200	—	—	ns
BS Hold Time *	t_{BH}	—	200	—	—	ns
Analog Output Load	R_{AL}	AOUT, AOUT+, AOUT–	600	—	—	Ω
		GSK	10	—	—	kΩ
	C_{AL}	—	—	—	100	pF
Digital Output Load	R_{DL}	—	1	—	—	kΩ
	C_{DL}		—	—	100	pF
Allowable Analog Input Offset Voltage	V_{IO}	Transmit gain stage, Gain = 1	–200	—	+200	mV
		Transmit gain stage, Gain = 10	–20	—	+20	

* : The value for the MSM6997 and MSM6999

ELECTRICAL CHARACTERISTICS

DC and Digital Interface Characteristics

(V_{DD} = +5 V ±5%, V_{SS} = –5 V ±5%, Ta = 0°C to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current (Operating)	I_{DD1}	XCLOCK, RCLOCK 2048 kHz *	—	7.0	12	mA
					14	
	I_{SS1}	*	—	6.5	12	
					14	
Power Supply Current (Stand-by)	I_{DD2}	—	—	—	3.0	mA
	I_{SS2}		—	—	1.5	
Input High Voltage	V_{IH}	—	2.2	—	—	V
Input Low Voltage	V_{IL}		—	—	0.8	V
Input Leakage Current	I_{IH}		—	< 0.5	2.0	µA
	I_{IL}		—	< 0.2	0.5	
Output Low Voltage	V_{OL}		—	0.1	0.4	V
Output Leakage Current	I_{OH}		—	< 5	10	µA
Analog Output Offset Voltage	V_{OFF}		–150	0	+150	mV
Input Capacitance	C_{IN}	—	—	5	—	pF
Analog Input Resistance	R_{IN}	f_{IN} < 3.4 kHz	—	1	—	MΩ

* : The upper is specified for the MSM6996/MSM6997 and the lower for the MSM6998/MSM6999

AC Characteristics

(V_{DD} = +5 V ±5%, V_{SS} = –5 V ±5%, Ta = 0°C to 70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
		Freq. (Hz)	Level (dBm0)				
Transmit Frequency Response	L_{OSS} T1	60	0	20	—	—	dB
	L_{OSS} T2	300		–0.15	—	+0.25	
	L_{OSS} T3	820		Reference			
	L_{OSS} T4	2020		–0.15	—	+0.25	
	L_{OSS} T5	3000		–0.15	—	+0.25	
	L_{OSS} T6	3400		0	—	0.8	
Receive Frequency Response	L_{OSS} R1	300	0	–0.1	—	+0.2	dB
	L_{OSS} R2	820		Reference			
	L_{OSS} R3	2020		–0.1	—	+0.2	
	L_{OSS} R4	3000		–0.1	—	+0.2	
	L_{OSS} R5	3400		0	—	0.8	
Transmit Signal to Noise Ratio *1	SD T1	1020 or 820	3	36	—	—	dB
	SD T2		0	36	—	—	
	SD T3		–30	36	—	—	
	SD T4		–40	31	—	—	
	SD T5		–45	26	—	—	
Receive Signal to Noise Ratio *1	SD R1	1020 or 820	3	36	—	—	dB
	SD R2		0	36	—	—	
	SD R3		–30	36	—	—	
	SD R4		–40	31	—	—	
	SD R5		–45	26	—	—	
Transmit Gain Tracking	GT T1	1020 or 820	3	–0.2	—	+0.2	dB
	GT T2		–10	Reference			
	GT T3		–40	–0.2	—	+0.2	
	GT T4		–50	–0.4	—	+0.4	
	GT T5		–55	–0.8	—	+0.8	
Receive Gain Tracking	GT R1	1020 or 820	3	–0.2	—	+0.2	dB
	GT R2		–10	Reference			
	GT R3		–40	–0.2	—	+0.2	
	GT R4		–50	–0.4	—	+0.4	
	GT R5		–55	–0.8	—	+0.8	

Note: *1 The measurement is taken with P-message filter

AC Characteristics (Continued)

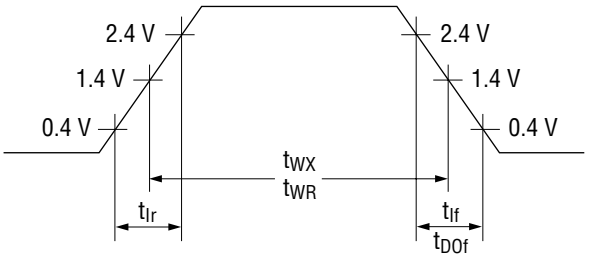
(V_{DD} = +5 V ±5%, V_{SS} = –5 V ±5%, Ta = 0°C to 70°C)

Parameter		Symbol	Condition		Min.	Typ.	Max.	Unit
			Freq. (Hz)	Level (dBm0)				
Idle Channel Noise *1	Transmit	N_{IDL} T	—	—	—	—	–75	dBmOp
	Receive	N_{IDL} R	—	—	—	—	–75	
Absolute Gain *2	Transmit	AV T	1020 or 820	0	–0.5	0	+0.5	dB
	Receive	AV R	1020 or 820	0	–0.5	0	+0.5	
Absolute Delay Time		t_D	—	0	—	—	0.52	ms
Transmit Group Delay Time *3		t_{GD} T1	500	0	—	—	0.75	ms
		t_{GD} T2	600		—	—	0.35	
		t_{GD} T3	1000		—	—	0.125	
		t_{GD} T4	2600		—	—	0.125	
		t_{GD} T5	2800		—	—	0.75	
Receive Group Delay Time *3		t_{GD} R1	500	0	—	—	0.75	ms
		t_{GD} R2	600		—	—	0.35	
		t_{GD} R3	1000		—	—	0.125	
		t_{GD} R4	2600		—	—	0.125	
		t_{GD} R5	2800		—	—	0.75	
Crosstalk Attenuation	T to R	C_R T	1020 or 820	—	—	—	66	dB
	R to T	C_R R	1020 or 820		—	—	66	
Out-of-Band Spurious		S	300 to 3400	0	—	—	–30	dBmO
Intermodulation Distortion		IMD 1	f_a = 470 f_b = 320	–4	—	—	–35	dBmO
Discrimination		DIS	4.6 kHz to 72 kHz	0	30	—	—	dB
V_{DD} Noise Rejection Ratio	Transmit	PPSR T	0 to 300 kHz	200 mVp-p	—	30	—	dB
	Receive	PPSR R			—	30	—	
V_{SS} Noise Rejection Ratio	Transmit	NPSR T			—	30	—	
	Receive	NPSR R			—	30	—	
Digital Output Delay Time		t_{SD}	R_{DL} = 2 kΩ C_{DL} = 100 pF		50	150	300	ns
		t_{XD1}			50	100	300	
		t_{XD2}			50	100	300	
		t_{XD3}			50	180	300	
Digital Output Fall Time		t_{DO}			—	20	100	ns

Notes: *1 The measurement is taken with P-message filter
*2 MSM6996/MSM6998 0 dB = 1.231 Vrms
MSM6997/MSM6999 0 dB = 1.227 Vrms
*3 Reference : 1800 Hz

TIMING DIAGRAM

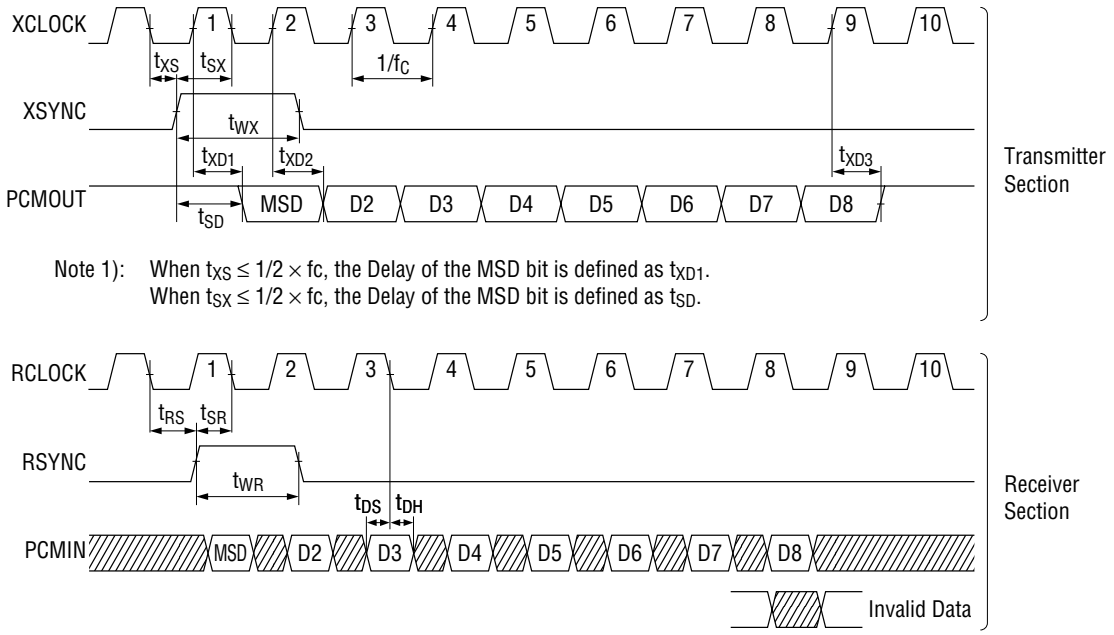
Wave Time Measurement Level



Note: Timing between signal waves is judged at 1.4 V

Figure 1

Basic Timing



Note 1): When $t_{XS} \leq 1/2 \times fc$, the Delay of the MSD bit is defined as t_{XD1}.
When $t_{SX} \leq 1/2 \times fc$, the Delay of the MSD bit is defined as t_{SD}.

Note 2): Transmit synchronizing and clock pulse, and Receive synchronizing and clock pulse may be asynchronous mutually.

Note 3): The threshold level is 1.4 V.

Figure 2

Timing for 7 bits Decode (Specified for MSM6997/6999)

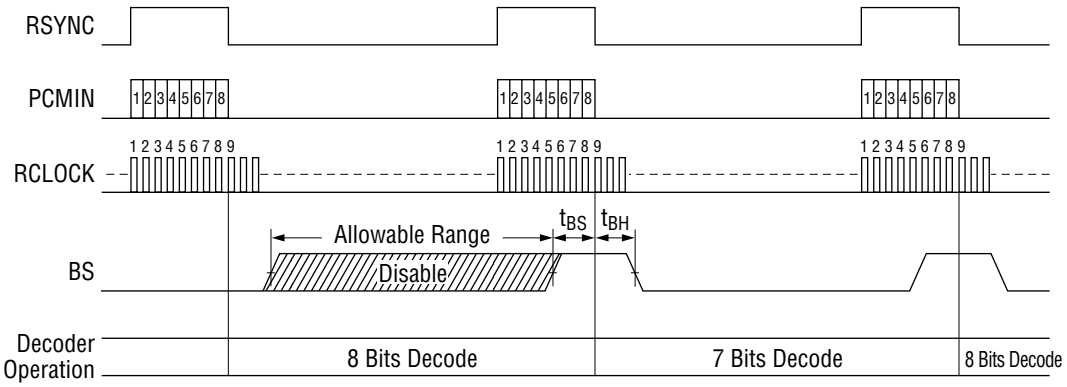
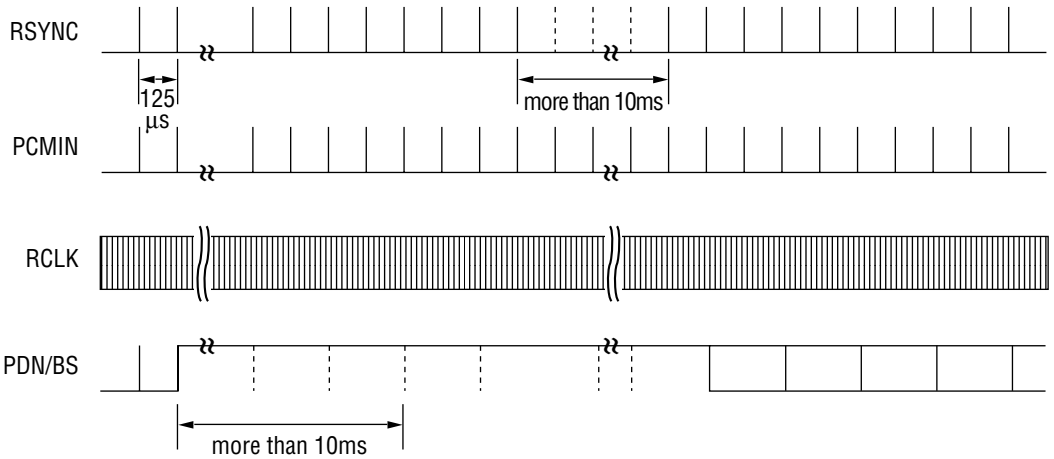


Figure 3

Timing for Bit-steal Function Setting

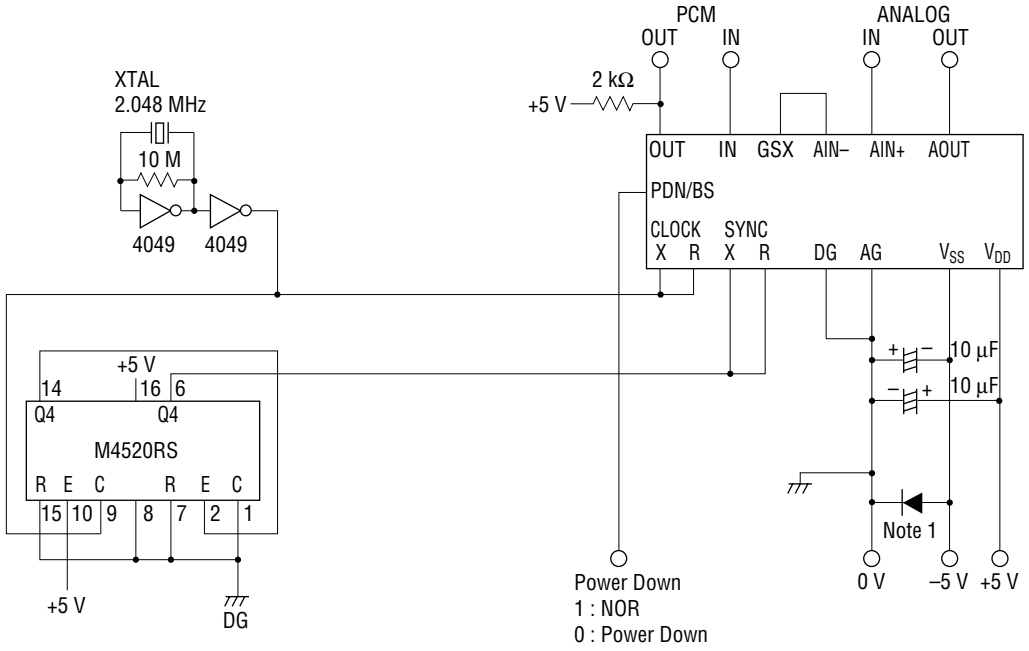


Notes: Follow these procedures when the Bit-steal function is used:

1. Set the RSYNC pin to OFF ("L") after the PDN/BS pin is set at "H" for 10ms or more.
2. Set the RSYNC to ON after a pulse is input at the PDN/BS pin.
3. The Bit-steal function starts to operate.

APPLICATION CIRCUIT

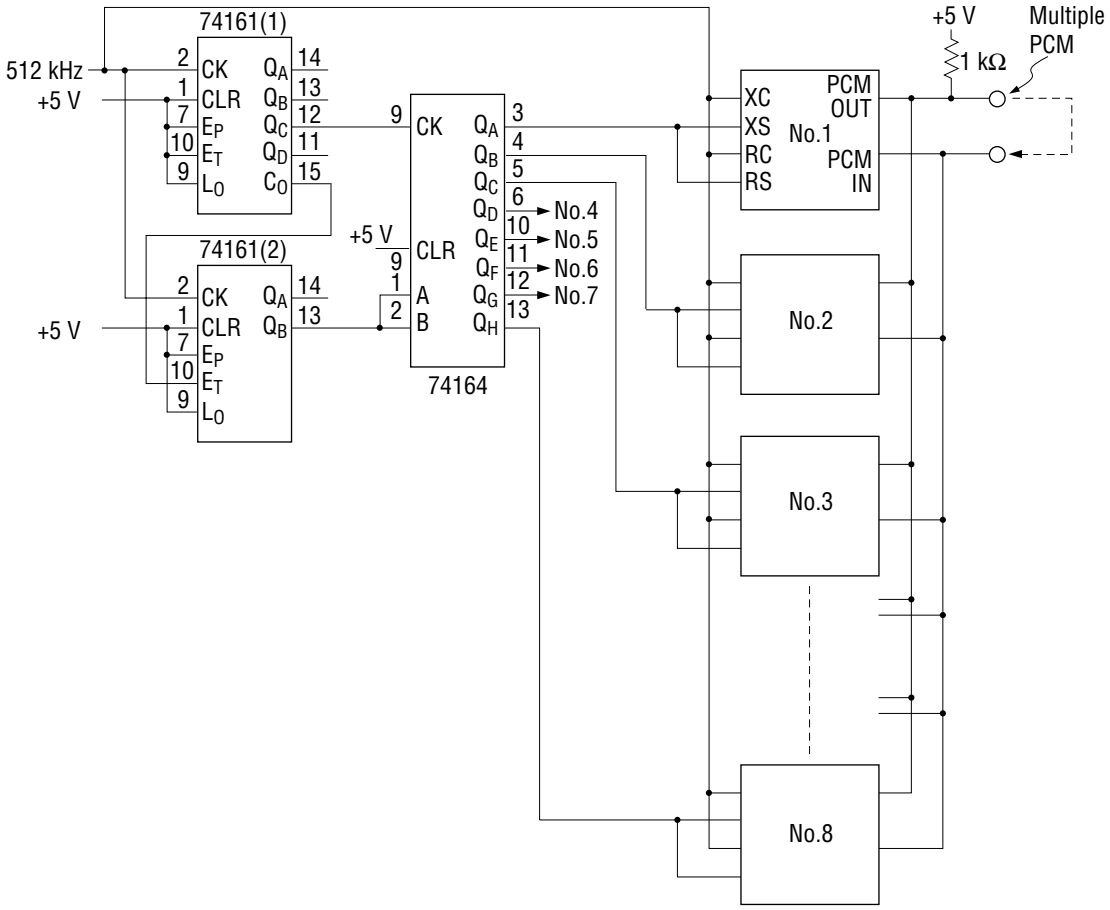
Basic Circuit



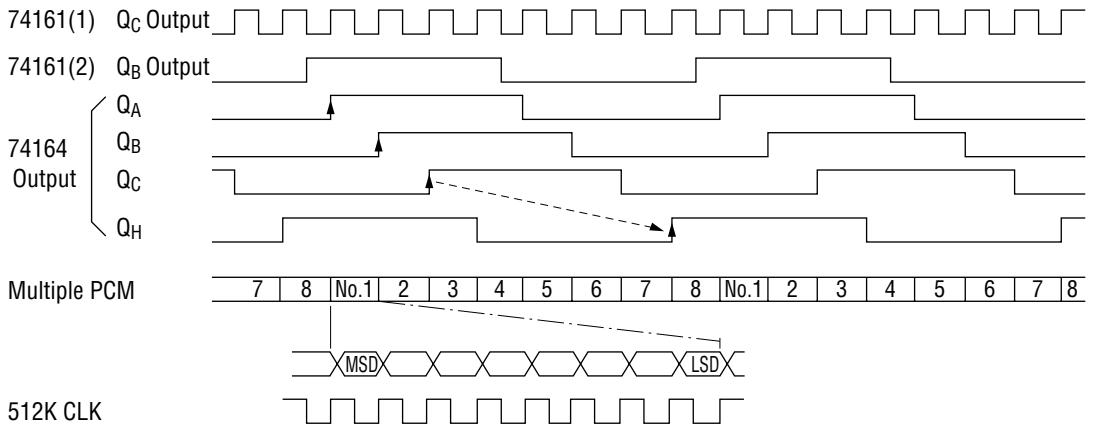
Notes: 1. Insert diode for preventing from Latch-Up at turn on Power.
Recommended Diode Specification.
- High Speed Switching
- Allowerable Power dissipation 250 mW to 300 mW
- Forward Voltage Drop < 1.3 V (at 100 mA)

2. AG and DG must be connected in the printed circuit board mounted this device, for preventing from Latch-Up.

Example of Multi-Channel Connections (8ch)

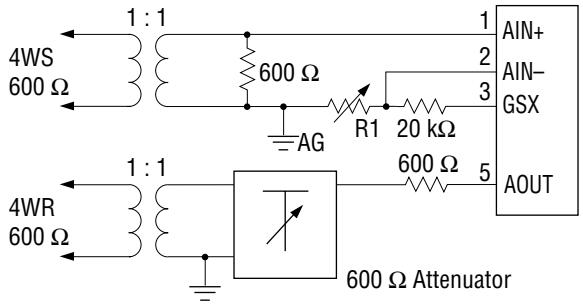


Example of Multi-Channel Timing



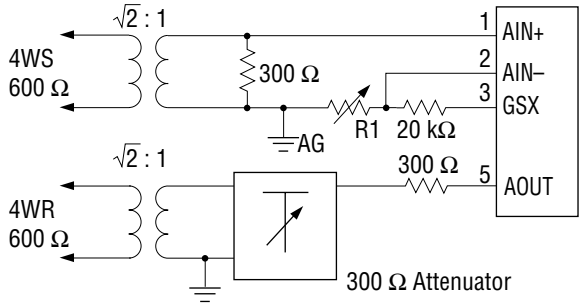
Transmit and Receive Level Adjustment (MSM6996H/V, MSM6997H/V)

a. Transformer of turns ratio 1 : 1



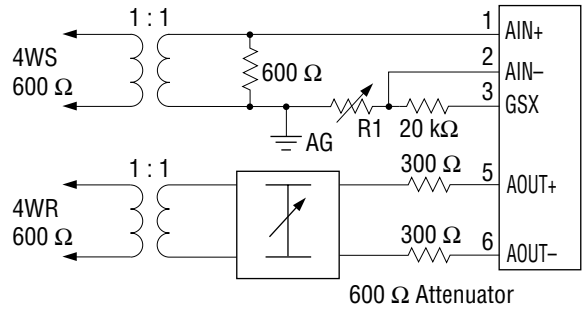
When R1 is open and the attenuator is set at 0 dB,
4 WS maximum input level = +7.17 + L_T (dBm)
4 WR maximum output level = +1.15 – L_T (dBm)
L_T : Transformer loss

b. Transformer of turns ratio 1 :$\sqrt{2}$



When R1 is open and the attenuator is set at 0 dB,
4 WS maximum input level = +10.18 + L_T (dBm)
4 WR maximum output level = +4.16 – L_T (dBm)
L_T : Transformer loss

Transmit and Receive Level Adjustment (MSM6998, MSM6999)



When R1 is open and the attenuator is set at 0 dB,
4 WS maximum input level = +7.17 + L_T (dBm)
4 WR maximum output level = +7.17 – L_T (dBm)
L_T : Transformer loss

RECOMMENDATIONS FOR ACTUAL DESIGN

- To assure proper electrical characteristics, use bypass capacitors with excellent high frequency characteristics for the power supply and keep them as close as possible to the device pins.

- Connect the AG pin and the DG pin each other as close as possible.
  Connected to the system ground with low impedance.

- Mount the device directly on the board when mounted on printed circuit board.
  Do not use IC sockets.
  If an IC socket is unavoidable, use the short lead type socket.

- When mounted on a frame, use electro-magnetic shielding, if any electro-magnetic wave source such as power supply transformers surround the device.

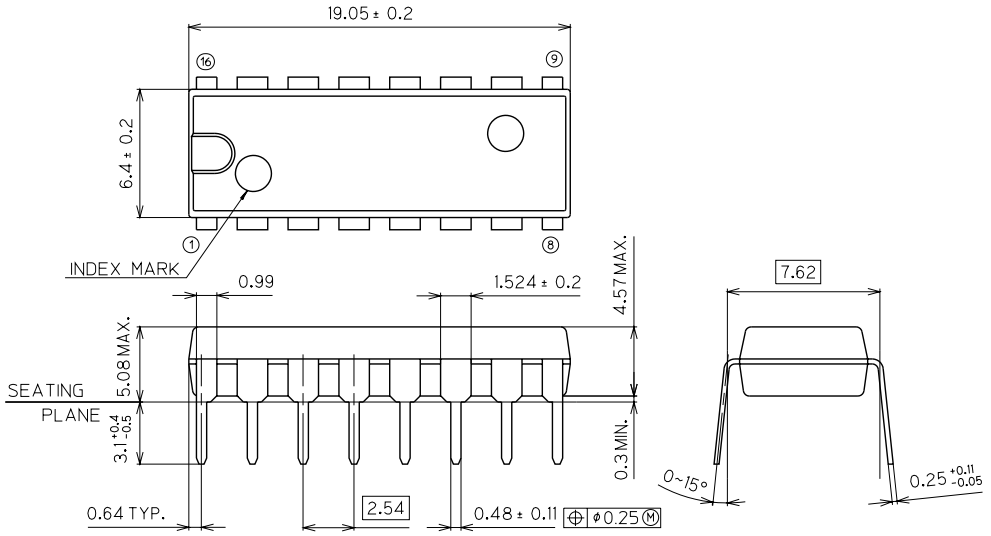
- Keep the voltage on the V_{DD} pin not lower than –0.3 V and the voltage on the V_{SS} pin more than +0.3 V even instantaneously to avoid latch-up phenomenon when turning the power on.

- Use a low noise (particularly, low level type of high frequency spike noise or pulse noise) power supply to avoid erroneous operation and the degradation of the characteristics of these devices.

PACKAGE DIMENSIONS

(Unit : mm)

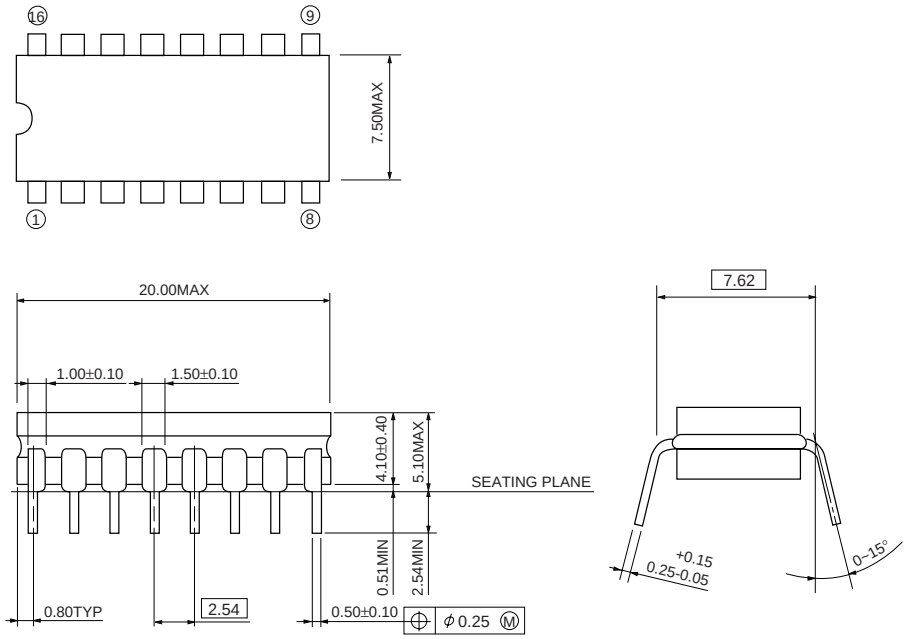
DIP16-P-300-2.54



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.99 TYP.

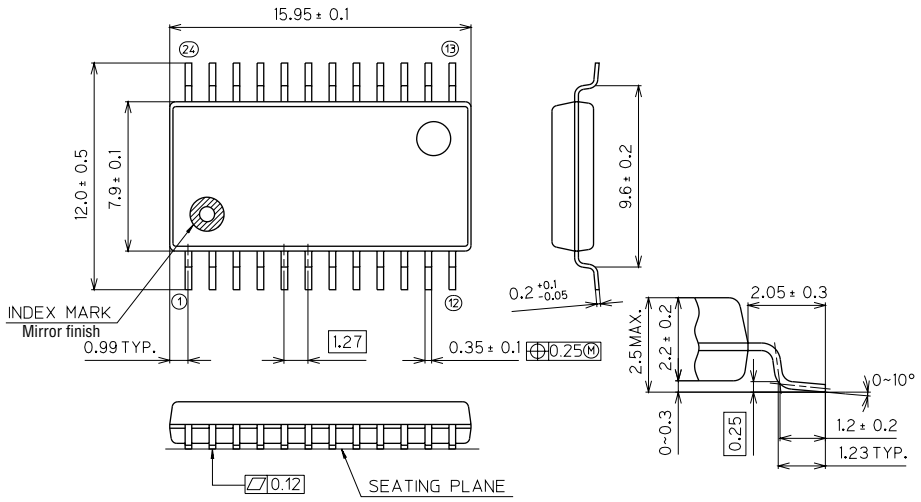
(Unit : mm)

DIP16-G-300-2.54



(Unit : mm)

SOP24-P-430-1.27-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.58 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).