OKI Semiconductor

This version: Mar. 1995

MSM80C31F/MSM80C51F

CMOS 8-Bit Microcontroller

GENERAL DESCRIPTION

The OKI MSM80C31F/MSM80C51F microcontroller is a low-power, 8-bit device implemented in OKI's silicon-gate complementary metal-oxide semiconductor process technology. The device includes 4K bytes of mask programmable ROM (MSM80C51F only), 128 bytes of data RAM, 32 I/O lines, two 16-bit timer/counters, a five-source two-level interrupt structure, a full duplex serial port, and an oscillator and clock circuitry. In addition, the device has two software selectable modes for further power reduction — Idle and Power Down. Idle mode freezes the CPU's in-struction execution while maintaining RAM and allowing the timers, serial port and interrupt system to continue functions. Power Down mode saves the RAM contents but freezes the oscillator causing all other device functions to be inoperative.

FEATURES

- Low power consumption by 2 µm silicon gate CMOS process technology
- Fully static circuit
- Internal program memory : 4K bytes (MSM80C51F)
- External program memory space : 64K bytes
- Internal data memory (RAM) : 128 bytes
- External data memory (RAM) space : 64K bytes
- I/O ports : 8-bit × 4 ports
- Two 16-bit timer/counters
- Multifunctional serial port (UART)
- Five interrupt sources (Priority can be set)
- Four sets of working registers (R0-7 × 4)
- Stack : Internal data memory (RAM)
  128-byte area can be used arbitrarily (by SP specified)
- Two CPU power-down modes
  (1) Idle mode : CPU stopped while oscillation continued. (Software setting)
  (2) PD mode : CPU and oscillation all stopped. (Software setting) (Setting I/O ports to floating status possible)
- Operating temperature : –40 to +85°C (@ 12 MHz, V_{CC} = 5 V ±20%)
  –20 to +70°C (@ 16 MHz, V_{CC} = 5 V ±5%)
- 2-byte 1-machine cycle instructions : 1 µsec. @ 12 MHz
  0.75 µsec. @ 16 MHz
- Multiplication/division instructions : 4 µsec. @ 12 MHz
  3 µsec. @ 16 MHz
- Instruction code addressing method
  Byte specification : Data addressing (direct)
  Bit specification : Bit addressing

- Package options

40-pin plastic DIP (DIP40-P-600-2.54)	:	(MSM80C31F-×××RS) (MSM80C51F-×××RS)
44-pin plastic QFP (QFP44-P-910-0.80-2K)	:	(MSM80C31F-×××GS) (MSM80C51F-×××GS)
44-pin plastic QFJ (PLCC) (QFJ44-P-S650-1.27)	:	(MSM80C31F-×××JS) (MSM80C51F-×××JS)

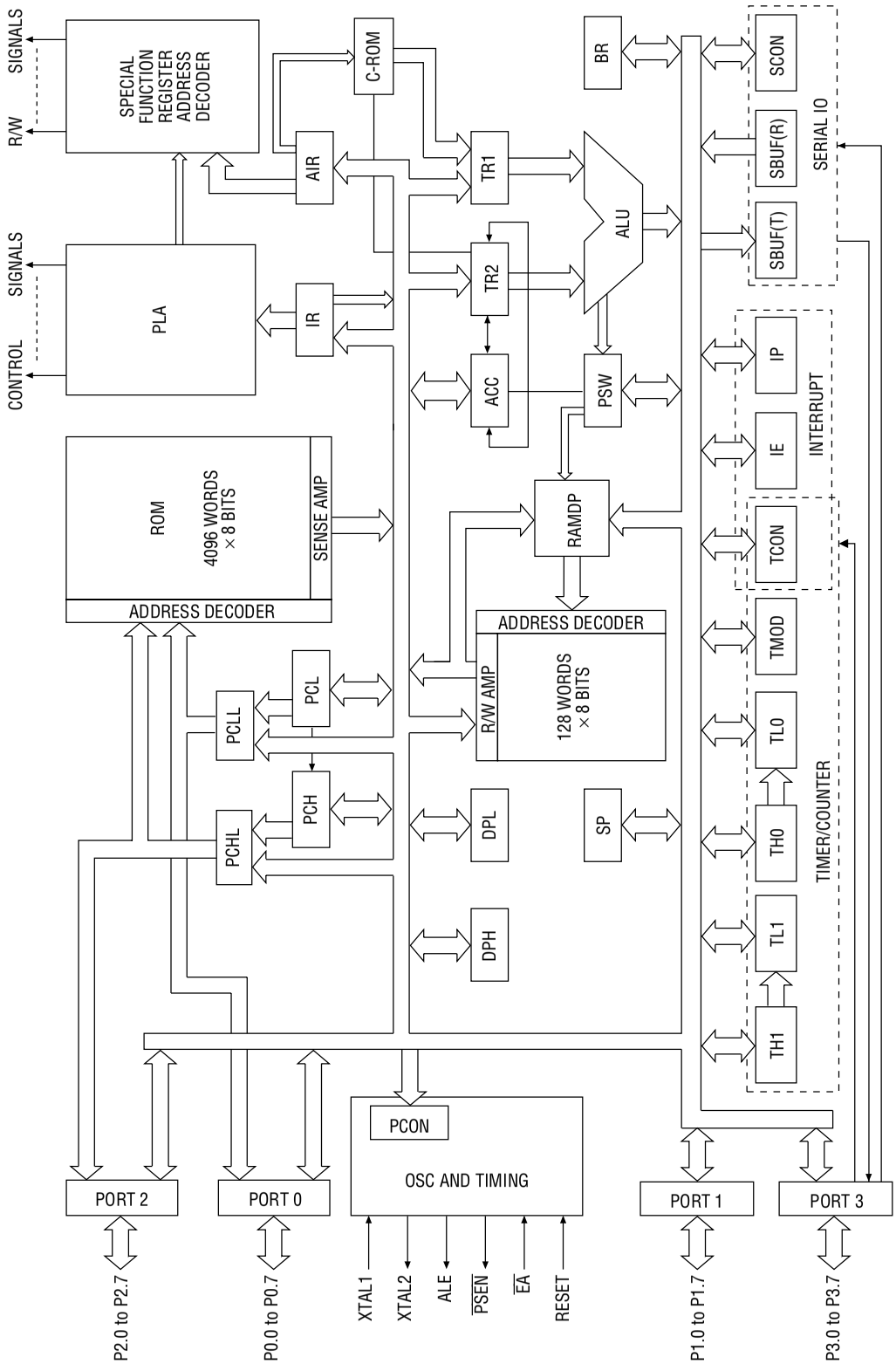
××× indicates the code number.

DIFFERENCES BETWEEN MSM80C31F/MSM80C51F AND MSM80C31/MSM80C51

- Operating frequency
  - 0.5 to 16 MHz MSM80C31F-1/MSM80C51F-1
  - 0.5 to 12 MHz MSM80C31/MSM80C51/MSM80C31F/MSM80C51F
- External clock input terminal
  - XTAL1 ..... MSM80C31F(-1)/MSM80C51F(-1)
  - XTAL2 ..... MSM80C31/MSM80C51
- Emulation mode
  Output impedance of ALE and $\overline{PSEN}$ pins becomes about 20 kΩ while CPU is being reset in MSM80C31F/MSM80C51F.

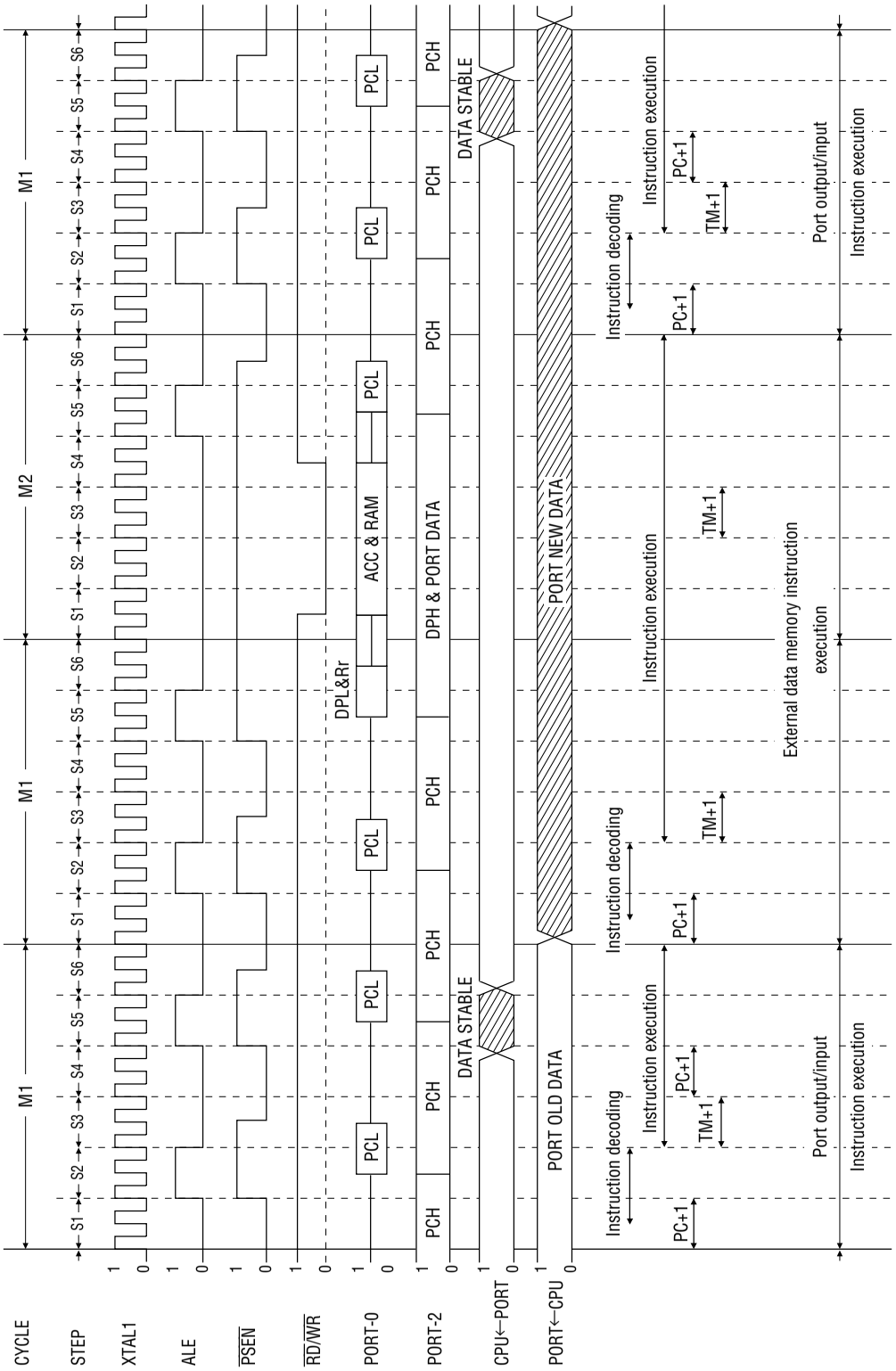
Any other functions and electrical characteristics of MSM80C31F/MSM80C51F except for above three differences are the same as those of MSM80C31/MSM80C51.

BLOCK DIAGRAM

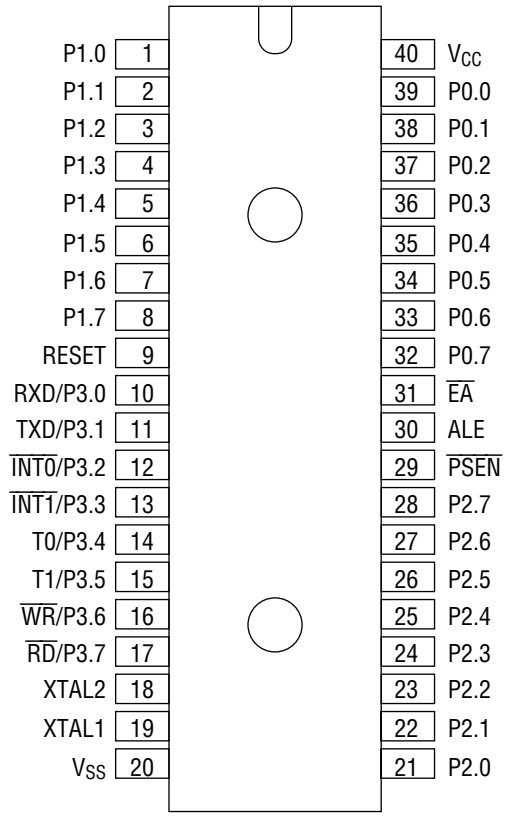


CLOCK WAVEFORMS

Basic Timing Chart

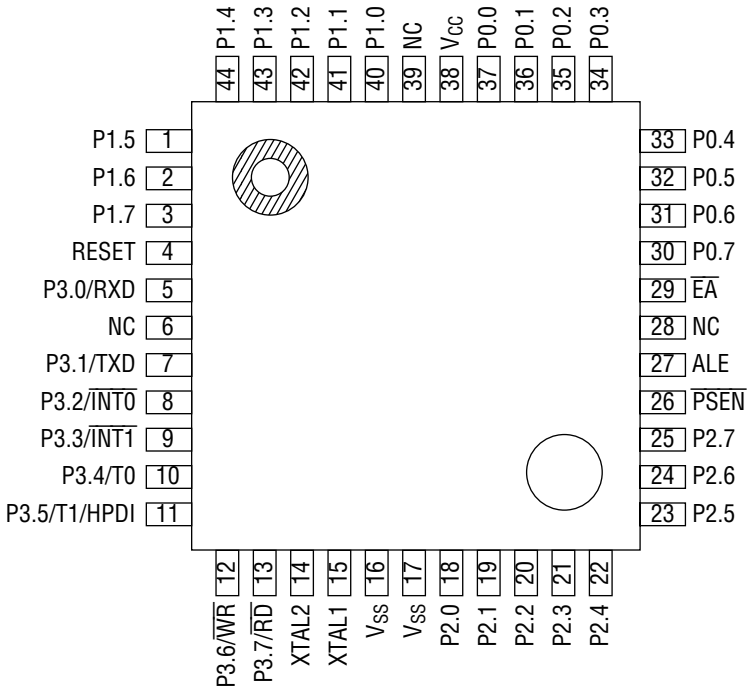


PIN CONFIGURATION (TOP VIEW)



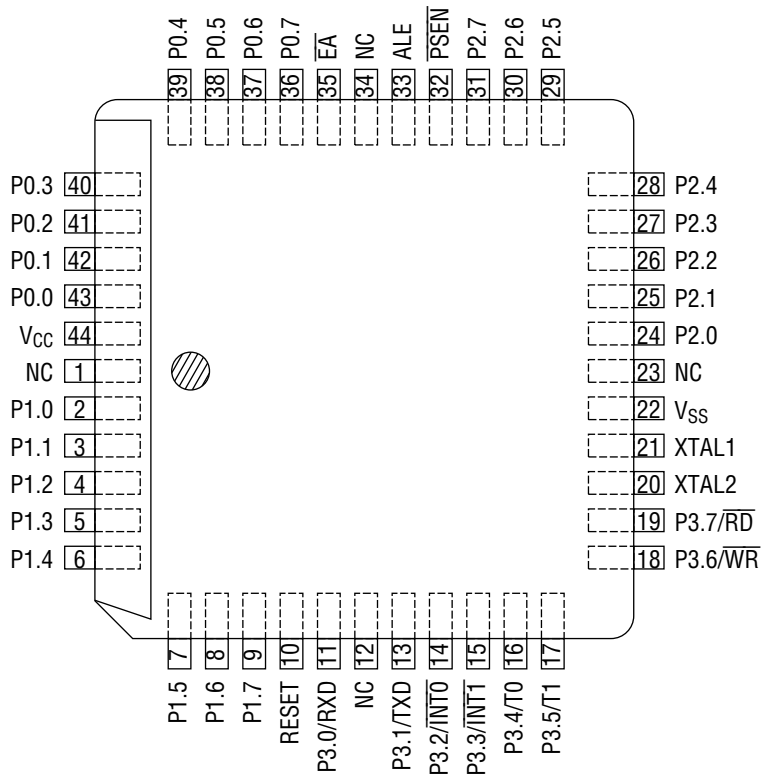
40-Pin Plastic DIP

PIN CONFIGURATION (TOP VIEW) (continued)



44-Pin Plastic QFP

PIN CONFIGURATION (TOP VIEW) (continued)

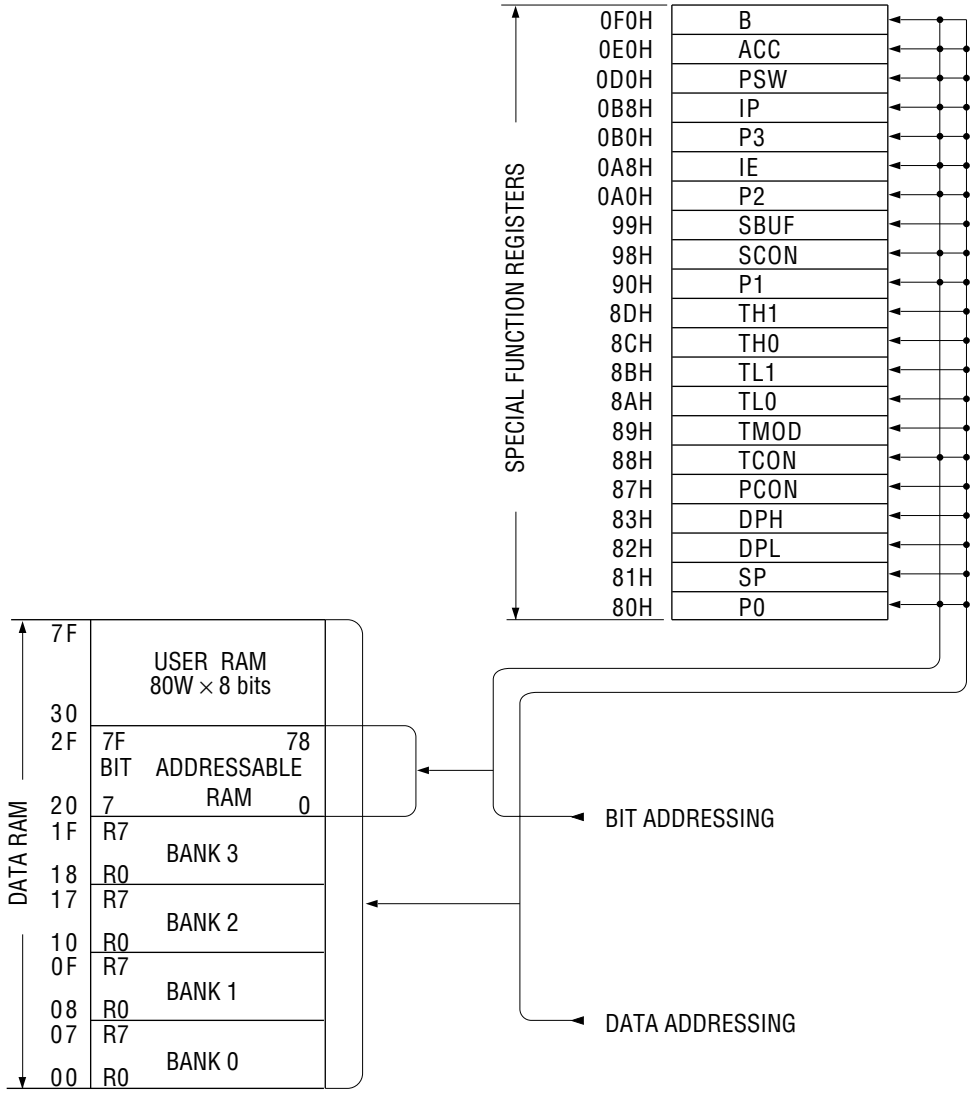


44-Pin Plastic QFJ (PLCC)

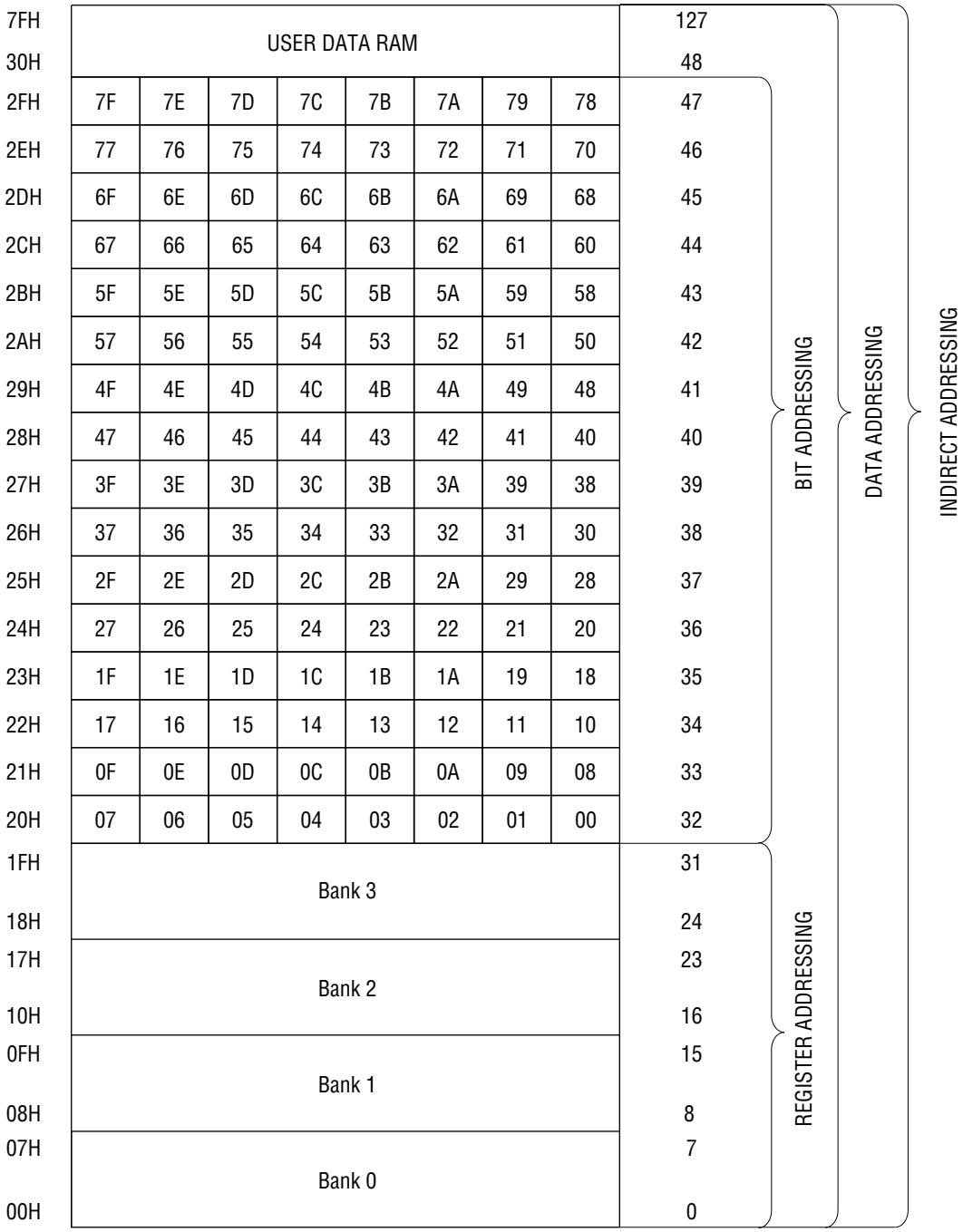
PIN DESCRIPTION

Symbol	Description
V_{SS}	Ground potential
V_{CC}	Supply voltage during Normal, Idle and Power Down operation
Port 0.0 - 0.7	Port 0 is an 8-bit open-drain bidirectional I/O port. It is also the mutiplexed low-order address and data bus during accesses to external memory.
Port 1.0 - 1.7	Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. It can drive CMOS inputs without external pull-ups.
Port 2.0 - 2.7	Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. It outputs the high-order address byte during accesses to external memory. It can drive CMOS inputs without external pull-ups.
Port 3.0 - 3.7	Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. It also provides various special features, as shown below: **Port Pin** **Alternate Function** P3.0 RXD (serial input port) P3.1 TXD (serial output port) P3.2 INT0 (external interrupt) P3.3 INT1 (external interrupt) P3.4 T0 (Timer 0 external input) P3.5 T1 (Timer 1 external input) P3.6 WR (external data memory write strobe) P3.7 RD (external data memory read strobe) Port 3 can drive CMOS inputs without external pull-ups.
RESET	Reset input pin. A reset is accomplished by holding the RESET pin high for at least 1µs. even if the oscillator has been stopped. The CPU responds by executing an internal reset. An internal pull-down resistor permits Power-On reset using only a capacitor connected to V_{CC}. This pin does not receive the power down voltage since the function has been transferred to the V_{CC} pin.
ALE	Address Latch Enable. This output latches for latching the low byte of the address during accesses to external memory. For this purpose, ALE is activated twice every machine cycle or at a constant rate of 1/6th the oscillator frequency, except during an external memory access at which time one ALE pulse is skipped. ALE can drive CMOS inputs without an external pull-up.
$\overline{PSEN}$	Program Store Enable output. This output is the read strobe to external program memory. For this purpose, $\overline{PSEN}$ is activated twice every machine cycle. (However, when executing out of external program memory, two activations of $\overline{PSEN}$ are skipped during each access to external data memory.) $\overline{PSEN}$ is not activated during fetches from internal program memory. It can drive CMOS inputs without an external pull-up.
$\overline{EA}$	External Access input pin. When $\overline{EA}$ is held high, the CPU executes out of internal program memory (unless the program counter exceeds 0FFFH). When $\overline{EA}$ is held low, the CPU executes only out of external program memory. $\overline{EA}$ must not be floated.
XTAL1	Crystal 1 pin. It is an input to the inverting amplifier which forms the internal oscillator.
XTAL2	Crystal 2 pin. It is an output of the inverting amplifier that forms the internal oscillator.

DATA MEMORY AND SPECIAL FUNCTION REGISTER LAYOUT DIAGRAM



DETAILED DIAGRAM OF DATA MEMORY (RAM)



DETAILED DIAGRAM OF SPECIAL FUNCITON REGISTERS

Data Address	(MSB) Bit Address (LSB)								Special Function Register Symbol
0F0H	F7	F6	F5	F4	F3	F2	F1	F0	B
0E0H	E7	E6	E5	E4	E3	E2	E1	E0	ACC
	CY	AC	F0	RS1	RS0	OV	F1	P	
0D0H	D7	D6	D5	D4	D3	D2	D1	D0	PSW
				PS	PT1	PX1	PT0	PX0	
0B8H	—	—	—	BC	BB	BA	B9	B8	IP
0B0H	B7	B6	B5	B4	B3	B2	B1	B0	P3
	EA			ES	ET1	EX1	ET0	EX0	
0A8H	AF	—	—	AC	AB	AA	A9	A8	IE
0A0H	A7	A6	A5	A4	A3	A2	A1	A0	P2
99H	Not Bit Addressable								SBUF
	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	
98H	9F	9E	9D	9C	9B	9A	99	98	SCON
90H	97	96	95	94	93	92	91	90	P1
8DH	Not Bit Addressable								TH1
8CH	Not Bit Addressable								TH0
8BH	Not Bit Addressable								TL1
8AH	Not Bit Addressable								TL0
89H	Not Bit Addressable								TMOD
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	
88H	8F	8E	8D	8C	8B	8A	89	88	TCON
87H	Not Bit Addressable								PCON
83H	Not Bit Addressable								DPH
82H	Not Bit Addressable								DPL
81H	Not Bit Addressable								SP
80H	87	86	85	84	83	82	81	80	P0

INSTRUCTION LIST

List of Instruction Symbols

A	:	Accumulator
AB	:	Register pair
AC	:	Auxiliary carry flag
B	:	Arithmetic operation register
C	:	Carry flag
DPTR	:	Data pointer
PC	:	Program counter
Rr	:	Register indicator (r = 0 to 7)
SP	:	Stack pointer
AND	:	Logical product
OR	:	Logical sum
XOR	:	Exclusive-OR
+	:	Addition
–	:	Subtraction
X	:	Multiplication
/	:	Division
(X)	:	Denotes the contents of X
((X))	:	Denotes the contents of address determined by the contents of X
#	:	Denotes the immediate data
@	:	Denotes the indirect address
=	:	Equality
≠	:	Non-equality
←	:	Substitution
→	:	Substitution
—	:	Negation
<	:	Smaller than
>	:	Larger than
bit address	:	RAM and the special function register bit specifier address (b_0 to b_7)
code address	:	Absolute address (A_0 to A_{15})
data	:	Immediate data (I_0 to I_7)
relative offset	:	Relative jump address offset value (R_0 to R_7)
direct address	:	RAM and the special function register byte specifier address (a_0 to a_7)

MSM80C31F/MSM80C51F Instruction Codes

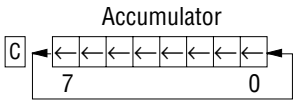
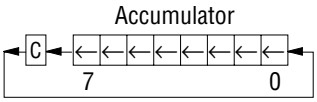
L / H	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111
0 0000	NOP	AJMP address 11 (Page 0)	LJMP address 16	RR A	INC A	INC direct	INC @R0	INC @R1
1 0001	JBC bit, rel	ACALL address 11 (Page 0)	LCALL adress 16	RRC A	DEC A	DEC direct	DEC @R0	DEC @R1
2 0010	JB bit, rel	AJMP address 11 (Page 1)	RET	RL A	ADD A, #data	ADD A, direct	ADD A, @R0	ADD A, @R1
3 0011	JNB bit, rel	ACALL address 11 (Page 1)	RETI	RLC A	ADDC A, #data	ADDC A, direct	ADDC A, @R0	ADDC A, @R1
4 0100	JC rel	AJMP address 11 (Page 2)	ORL direct, A	ORL direct, #data	ORL A, #data	ORL A, direct	ORL A, @R0	ORL A, @R1
5 0101	JNC rel	ACALL address 11 (Page 2)	ANL direct, A	ANL direct, #data	ANL A, #data	ANL A, direct	ANL A, @R0	ANL A, @R1
6 0110	JZ rel	AJMP address 11 (Page 3)	XRL direct, A	XRL direct, #data	XRL A, #data	XRL A, direct	XRL A, @R0	XRL A, @R1
7 0111	JNZ rel	ACALL address 11 (Page 3)	ORL C, bit	JMP @A+DPTR	MOV A, #data	MOV direct #data	MOV @R0, #data	MOV @R1, #data
8 1000	SJMP rel	AJMP address 11 (Page 4)	ANL C, bit	MOVC A, @A+PC	DIV AB	MOV direct1, direct2	MOV direct, @R0	MOV direct, @R1
9 1001	MOV DPTR, #data 16	ACALL address 11 (Page 4)	MOV bit, C	MOVC A, @A+DPTR	SUBB A, #data	SUBB A, direct	SUBB A, @R0	SUBB A, direct
A 1010	ORL C, /bit	AJMP address 11 (Page 5)	MOV C, bit	INC DPTR	MUL AB		MOV @R0, direct	MOV @R1, direct
B 1011	ANL C, /bit	ACALL address 11 (Page 5)	CPL bit	CPL C	CJNE A, #data rel	CJNE A, direct, rel	CJNE @R0 #data, rel	CJNE @R1, #data, rel
C 1100	PUSH direct	AJMP address 11 (Page 6)	CLR bit	CLR C	SWAP A	XCH A, direct	XCH A, @R0	XCH A, @R1
D 1101	POP direct	ACALL address 11 (Page 6)	SETB bit	SETB C	DA A	DJNZ direct, rel	XCHD A, @R0	XCHD A, @R1
E 1110	MOVX A, @DPTR	AJMP address 11 (Page 7)	MOVX A, @R0	MOVX A, @R1	CLR A	MOV A, direct	MOV A, @R0	MOV A, @R1
F 1111	MOVX @DPTR, A	ACALL address 11 (Page 7)	MOVX @R0, A	MOVX @R1, A	CPL A	MOV direct, A	MOV @R0, A	MOV @R1, A

2BYTES		3BYTES
	MNEMONIC	
2CYCLES		4CYCLES

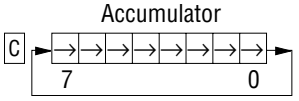
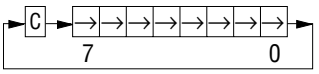
MSM80C31F/MSM80C51F Instruction Codes (continued)

H \ L	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111
0 0000	INC R0	INC R1	INC R2	INC R3	INC R4	INC R5	INC R6	INC R7
1 0001	DEC R0	DEC R1	DEC R2	DEC R3	DEC R4	DEC R5	DEC R6	DEC R7
2 0010	ADD A, R0	ADD A, R1	ADD A, R2	ADD A, R3	ADD A, R4	ADD A, R5	ADD A, R6	ADD A, R7
3 0011	ADDC A, R0	ADDC A, R1	ADDC A, R2	ADDC A, R3	ADDC A, R4	ADDC A, R5	ADDC A, R6	ADDC A, R7
4 0100	ORL A, R0	ORL A, R1	ORL A, R2	ORL A, R3	ORL A, R4	ORL A, R5	ORL A, R6	ORL A, R7
5 0101	ANL A, R0	ANL A, R1	ANL A, R2	ANL A, R3	ANL A, R4	ANL A, R5	ANL A, R6	ANL A, R7
6 0110	XRL A, R0	XRL A, R1	XRL A, R2	XRL A, R3	XRL A, R4	XRL A, R5	XRL A, R6	XRL A, R7
7 0111	MOV R0, #data	MOV R1, #data	MOV R2, #data	MOV R3, #data	MOV R4, #data	MOV R5, #data	MOV R6, #data	MOV R7, #data
8 1000	MOV direct, R0	MOV direct, R1	MOV direct, R2	MOV direct, R3	MOV direct, R4	MOV direct, R5	MOV direct, R6	MOV direct, R7
9 1001	SUBB A, R0	SUBB A, R1	SUBB A, R2	SUBB A, R3	SUBB A, R4	SUBB A, R5	SUBB A, R6	SUBB A, R7
A 1010	MOV R0, direct	MOV R1, direct	MOV R2, direct	MOV R3, direct	MOV R4, direct	MOV R5, direct	MOV R6, direct	MOV R7, direct
B 1011	CJNE R0, #data rel	CJNE R1, #data rel	CJNE R2, #data rel	CJNE R3, #data rel	CJNE R4, #data rel	CJNE R5, #data rel	CJNE R6, #data rel	CJNE R7, #data rel
C 1100	XCH A, R0	XCH A, R1	XCH A, R2	XCH A, R3	XCH A, R4	XCH A, R5	XCH A, R6	XCH A, R7
D 1101	DJNZ R0, rel	DJNZ R1, rel	DJNZ R2, rel	DJNZ R3, rel	DJNZ R4, rel	DJNE R5, rel	DJNE R6, rel	DJNE R7, rel
E 1110	MOV A, R0	MOV A, R1	MOV A, R2	MOV A, R3	MOV A, R4	MOV A, R5	MOV A, R6	MOV A, R7
F 1111	MOV R0, A	MOV R1, A	MOV R2, A	MOV R3, A	MOV R4, A	MOV R5, A	MOV R6, A	MOV R7, A

Instruction Set Details

Type	Mnemonic	Instruction code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Bytes	Cycles	Description
Airthmetic operation instructions	ADD A, Rr	0	0	1	0	1	r_2	r_1	r_0	1	1	(AC), (0V), (C), (A) ← (A)+(Rr)
	ADD A, direct	0	0	1	0	0	1	0	1	2	1	(AC), (0V), (C), (A) ← (A)+(direct address)
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
	ADD A, @Rr	0	0	1	0	0	1	1	r_0	1	1	(AC), (0V), (C), (A) ← (A)+((Rr))
	ADD A, #data	0	0	1	0	0	1	0	0	2	1	(AC), (0V), (C), (A) ← (A)+#data
		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0			
	ADDC A, Rr	0	0	1	1	1	r_2	r_1	r_0	1	1	(AC), (0V), (C), (A) ← (A)+(C)+(Rr)
	ADDC A, direct	0	0	1	1	0	1	0	1	2	1	(AC), (0V), (C), (A) ← (A)+(C)+(direct address)
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
	ADDC A, @Rr	0	0	1	1	0	1	1	r_0	1	1	(AC), (0V), (C), (A) ← (A)+(C)+((Rr))
	ADDC A, #data	0	0	1	1	0	1	0	0	2	1	(AC), (0V), (C), (A) ← (A)+(C)+#data
		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0			
	SUBB A, Rr	1	0	0	1	1	r_2	r_1	r_0	1	1	(AC), (0V), (C), (A) ← (A)–((C))+((Rr))
	SUBB A, direct	1	0	0	1	0	1	0	1	2	1	(AC), (0V), (C), (A) ← (A)–((C)+(direct address))
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
	SUBB A, @Rr	1	0	0	1	0	1	1	r_0	1	1	(AC), (0V), (C), (A) ← (A)–((C)+((Rr))
	SUBB A, #data	1	0	0	1	0	1	0	0	2	1	(AC), (0V), (C), (A) ← (A)–((C)+#data)
		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0			
	MUL AB	1	0	1	0	0	1	0	0	1	4	(AB) ← (A) x (B)
	DIV AB	1	0	0	0	0	1	0	0	1	4	(A)quotient, (B) remainder ← (A)/(B)
	DA A	1	1	0	1	0	1	0	0	1	1	When the contents of accumulator bits 0 thru 3 are greater than 9, or when auxiliary carry (AC) is 1, 6 is added to bits 0 thru 3. Bits 4 thru 7 are then examined, and when bits 4thru 7 follwoing compensation of lower bits 0 thru 3 is greater than 9, or when carry (C) is 1, 6 is added to bits 4 thru 7. As a result, the cary flag can be set, but cannot be cleared.
Accumulation operation instructions	CLR A	1	1	1	0	0	1	0	0	1	1	(A) ← 0
	CPL A	1	1	1	1	0	1	0	0	1	1	(A) ← $\overline{(A)}$
	PL A	0	0	1	0	0	0	1	1	1	1	
	PL C	0	0	1	1	0	0	1	1	1	1	

Instruction Set Details (continued)

Type	Mnemonic	Instruction code								Bytes	Cycles	Description
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			
Accumulation operation instructions	RR A	0	0	0	0	0	0	1	1	1	1	Accumulator 
	RRC A	0	0	0	1	0	0	1	1	1	1	Accumulator 
	SWAP A	1	1	0	0	0	1	0	0	1	1	$(A_{4\text{-}7}) \leftrightarrow (A_{0\text{-}3})$
Increment/decrement	INC A	0	0	0	0	0	1	0	0	1	1	(A) ← (A)+1
	INC Rr	0	0	0	0	1	r_2	r_1	r_0	1	1	(Rr) ← (Rr)+1
	INC direct	0	0	0	0	0	1	0	1	2	1	(direct address) ← (direct address)+1
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
	INC @Rr	0	0	0	0	0	1	1	r_0	1	1	((Rr)) ← ((Rr))+1
	INC DPTR	1	0	1	0	0	0	1	1	1	2	(DPTR) ← (DPTR)+1
	DEC A	0	0	0	1	0	1	0	0	1	1	(A) ← (A)–1
	DEC Rr	0	0	0	1	1	r_2	r_1	r_0	1	1	(Rr) ← (Rr)–1
	DEC direct	0	0	0	1	0	1	0	1	2	1	(direct address) ← (direct address)–1
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
	DEC @Rr	0	0	0	1	0	1	1	r_0	1	1	((Rr)) ← ((Rr))–1
Logical operation instructions	ANL A, Rr	0	1	0	1	1	r_2	r_1	r_0	1	1	(A) ← (A) AND (Rr)
	ANL A, direct	0	1	0	1	0	1	0	1	2	1	(A) ← (A) AND (direct address)
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
	ANL A, @Rr	0	1	0	1	0	1	1	r_0	1	1	(A) ← (A) AND ((Rr))
	ANL A, #data	0	1	0	1	0	1	0	0	2	1	(A) ← (A) AND #data
		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0			
	ANL direct, A	0	1	0	1	0	0	1	0	2	1	(direct address) ← (direct address) AND (A)
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
	ANL direct, #data	0	1	0	1	0	0	1	1	3	2	(direct address) ← (direct address) AND #data
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0			
	ORL A, Rr	0	1	0	0	1	r_2	r_1	r_0	1	1	(A) ← (A) OR (Rr)
	ORL A, direct	0	1	0	0	0	1	0	1	2	1	(A) ← (A) OR (direct address)
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
	ORL A, @Rr	0	1	0	0	0	1	1	r_0	1	1	(A) ← (A) OR ((Rr))
	ORL A, #data	0	1	0	0	0	1	0	0	2	1	(A) ← (A) OR #data
		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0			
	ORL direct, A	0	1	0	0	0	0	1	0	2	1	(direct address) ← (direct address) OR (A)
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			

Instruction Set Details (continued)

Type	Mnemonic	Instruction code								Bytes	Cycles	Description
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			
Logical operation instructions	ORL direct, #data	0	1	0	0	0	0	1	1	3	2	(direct address) ← (direct address) OR #data
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0			
	XRL A, Rr	0	1	1	0	1	r_2	r_1	r_0	1	1	(A) ← (A) XOR (Rr)
	XRL A, direct	0	1	1	0	0	1	0	1	2	1	(A) ← (A) XOR (direct address)
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
	XRL A, @Rr	0	1	1	0	0	1	1	r_0	1	1	(A) ← (A) XOR ((Rr))
	XRL A, #data	0	1	1	0	0	1	0	0	2	1	(A) ← (A) XOR #data
		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0			
	XRL direct, A	0	1	1	0	0	0	1	0	2	1	(direct address) ← (direct address) XOR (A)
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
	XRL direct, #data	0	1	1	0	0	0	1	1	3	2	(direct address) ← (direct address) XOR #data
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0			
Immediate data setting instructions	MOV A, #data	0	1	1	1	0	1	0	0	2	1	(A) ← #data
		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0			
	MOV Rr, #data	0	1	1	1	1	r_2	r_1	r_0	2	1	(Rr) ← #data
		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0			
	MOV direct, #data	0	1	1	1	0	1	0	1	3	2	(direct address) ← #data
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0			
	MOV @Rr, #data	0	1	1	1	0	1	1	r_0	2	1	(Rr)) ← #data
		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0			
	MOV DPTR, #data 16	1	0	0	1	0	0	0	0	3	2	(DPTR) ← #data 16
		I_{15}	I_{14}	I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8			
		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0			
Carry flag operation instructions	CLR C	1	1	0	0	0	0	1	1	1	1	(C) ← 0
	SETB C	1	1	0	1	0	0	1	1	1	1	(C) ← 1
	CPL C	1	0	1	1	0	0	1	1	1	1	(C) ← $\overline{(C)}$
	ANL C, bit	1	0	0	0	0	0	1	0	2	2	(C) ← (C) AND (bit address)
		b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0			
	ANL C,/bit	1	0	1	1	0	0	0	0	2	2	(C) ← (C) AND $\overline{\text{(bit address)}}$
		b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0			
	ORL C, bit	0	1	1	1	0	0	1	0	2	2	(C) ← (C) OR (bit address)
		b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0			
	ORL C,/bit	1	0	1	0	0	0	0	0	2	2	(C) ← (C) OR $\overline{\text{(bit address)}}$
		b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0			

Instruction Set Details (continued)

Type	Mnemonic	Instruction code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Bytes	Cycles	Description
Carry flag operation instructions	MOV C, bit	1	0	1	0	0	0	1	0	2	1	(C) ← (bit address)
		b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0			
	MOV bit, C	1	0	0	1	0	0	1	0	2	2	(bit address) ← (C)
		b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0			
Bit operation instructions	SETB bit	1	1	0	1	0	0	1	0	2	1	(bit address) ← 1
		b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0			
	CLR bit	1	1	0	0	0	0	1	0	2	1	(bit address) ← 0
		b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0			
	CPL bit	1	0	1	1	0	0	1	0	2	1	(bit address) ← $\overline{\text{(bit address)}}$
		b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0			
Data transfer instructions	MOV A, Rr	1	1	1	0	1	r_2	r_1	r_0	1	1	(A) ← (Rr)
	MOV A, direct	1	1	1	0	0	1	0	1	2	1	(A) ← (direct address)
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
	MOV A, @Rr	1	1	1	0	0	1	1	r_0	1	1	(A) ← ((Rr))
	MOV Rr, A	1	1	1	1	1	r_2	r_1	r_0	1	1	(Rr) ← (A)
	MOV Rr, direct	1	0	1	0	1	r_2	r_1	r_0	2	2	(Rr) ← (direct address)
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
	MOV direct, A	1	1	1	1	0	1	0	1	2	1	(direct address) ← (A)
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
	MOV direct, Rr	1	0	0	0	1	r_2	r_1	r_0	2	2	(direct address) ← (Rr)
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
	MOV direct 1, direct 2	1	0	0	0	0	1	1	r_0	3	2	(direct address 1) ← (direct address 2)
		a_7^2	a_6^2	a_5^2	a_4^2	a_3^2	a_2^2	a_1^2	a_0^2			
		a_7^1	a_6^1	a_5^1	a_4^1	a_3^1	a_2^1	a_1^1	a_0^1			
	MOV @Rr, A	1	1	1	1	0	1	1	r_0	1	1	((Rr)) ← (A)
	MOV @Rr, direct	1	0	1	0	0	1	1	r_0	2	2	((Rr)) ← (direct address)
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
Constant code instructions	MOVC A, @A+DPTR	1	0	0	1	0	0	1	1	1	2	(A) ← ((A)+(DPTR))
	MOVC A, @A+PC	1	0	0	0	0	0	1	1	1	2	(PC) ← (PC+1) (A) ← ((A)+(PC))
Data exchange instructions	XCH A, Rr	1	1	0	0	1	r_2	r_1	r_0	1	1	(A) ↔ (Rr)
	XCH A, direct	1	1	0	0	0	1	0	1	2	2	(A) ↔ (direct address)
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
	XCH A, @Rr	1	1	0	0	0	1	1	r_0	1	1	(A) ↔ ((Rr))
	XCHD A, @Rr	1	1	0	1	0	1	1	r_0	1	1	(A_{0-3}) ↔ ((Rr_{0-3}))

Instruction Set Details (continued)

Type	Mnemonic	Instruction code								Bytes	Cycles	Description
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			
Subroutine instructions	PUSH direct	1	1	0	0	0	0	0	0	2	2	(SP) ← (SP)+1 ((SP)) ← (direct address)
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
	POP direct	1	1	0	1	0	0	0	0	2	2	(direct address) ← ((SP)) (SP) ← (SP)–1
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
	ACALL addr 11	A_{10}	A_9	A_8	1	0	0	0	1	2	2	(PC) ← (PC)+2 (SP) ← (SP)+1 ((SP)) ← ($PC_{0\text{ - }7}$) (SP) ← (SP)+1 ((SP)) ← ($PC_{8\text{ - }15}$) ($PC_{0\text{ - }10}$) ← $A_{0\text{ - }10}$
		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0			
	LCALL addr 16	0	0	0	1	0	0	1	0	3	2	(PC) ← (PC)+3 (SP) ← (SP)+1 ((SP)) ← ($PC_{0\text{ - }7}$) (SP) ← (SP)+1 ((SP)) ← ($PC_{8\text{ - }15}$) ($PC_{0\text{ - }10}$) ← $A_{0\text{ - }10}$
		A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8			
		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0			
	RET	0	0	1	0	0	0	1	0	1	2	($PC_{8\text{ - }15}$) ← ((SP)) (SP) ← (SP)–1 ($PC_{0\text{ - }7}$) ← ((SP)) (SP) ← (SP)–1
	RETI	0	0	1	1	0	0	1	0	1	2	($PC_{8\text{ - }15}$) ← ((SP)) (SP) ← (SP)–1 ($PC_{0\text{ - }7}$) ← ((SP)) (SP) ← (SP)–1
Jump instructions	AJMP addr 11	A_{10}	A_9	A_8	0	0	0	0	1	2	2	(PC) ← (PC)+2 ($PC_{0\text{ - }10}$) ← $A_{0\text{ - }10}$
		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0			
	LJMP addr 16	0	0	0	0	0	0	1	0	3	2	($PC_{0\text{ - }15}$) ← $A_{0\text{ - }15}$
		A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8			
		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0			
	SJMP rel	1	0	0	0	0	0	0	0	2	2	(PC) ← (PC)+3 (SP) ← (SP)+1
		R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0			
	JMP @A+ DPTR	0	1	1	1	0	0	1	1	1	2	(PC) ← (A)+(DPTR)

Instruction Set Details (continued)

Type	Mnemonic	Instruction code								Bytes	Cycles	Description
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			
Branch instructions	CJNE A, direct, rel	1	0	1	1	0	1	0	1	3	2	(PC) ← (PC)+3 IF (A)≠(direct address) THEN (PC) ← (PC)+relative offset IF (A)<(direct address) THEN (C) ← 1 ELSE (C) ← 0
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
		R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0			
	CJNE A, #data, rel	1	0	1	1	0	1	0	0	3	2	(PC) ← (PC)+3 IF (A)≠ #data THEN (PC) ← (PC)+relative offset IF (A)< #data THEN (C) ← 1 ELSE (C) ← 0
		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0			
		R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0			
	CJNE Rr, #data, rel	1	0	1	1	1	r_2	r_1	r_0	3	2	(PC) ← (PC)+3 IF ((Rr))≠ #data THEN (PC) ← (PC)+relative offset IF (Rr))< #data THEN (C) ← 1 ELSE (C) ← 0
		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0			
		R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0			
	CJNE @Rr, #data, rel	1	0	1	1	0	1	1	r_0	3	2	(PC) ← (PC)+3 IF ((Rr))≠ #data THEN (PC) ← (PC)+relative offset IF ((Rr))< #data THEN (C) ← 1 ELSE (C) ← 0
		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0			
		R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0			
	DJNZ Rr, rel	1	1	0	1	1	r_2	r_1	r_0	2	2	(PC) ← (PC)+2 (Rr) ← (Rr)–1 IF (Rr)< 0 THEN (PC) ← (PC)+relative offset
		R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0			
	DJNZ direct, rel	1	1	0	1	0	1	0	1	3	2	(PC) ← (PC)+3 (direct address) ← (direct address)–1 IF (direct address)≠ 0 THEN (PC) ← (PC)+relative offset
		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
		R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0			

Instruction Set Details (continued)

Type	Mnemonic	Instruction code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Bytes	Cycles	Description
Branch instructions	JZ rel	0	1	1	0	0	0	0	0	2	2	(PC) ← (PC)+2 IF (A) = 0 THEN (PC) ← (PC)+relative offset
		R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0			
	JNZ rel	0	1	1	1	0	0	0	0	2	2	(PC) ← (PC)+2 IF (A) ≠ 0 THEN (PC) ← (PC)+relative offset
		R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0			
	JC rel	0	1	0	0	0	0	0	0	2	2	(PC) ← (PC)+2 IF (C) = 1 THEN (PC) ← (PC)+relative offset
		R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0			
	JNC rel	0	1	0	1	0	0	0	0	2	2	(PC) ← (PC)+2 IF (C) = 0 THEN (PC) ← (PC)+relative offset
		R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0			
	JB bit, rel	0	0	1	0	0	0	0	0	3	2	(PC) ← (PC)+3 IF (bit address) = 1 THEN (PC) ← (PC)+relative offset
		b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0			
		R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0			
	JNB bit, rel	0	0	1	1	0	0	0	0	3	2	(PC) ← (PC)+3 IF (bit address) = 0 THEN (PC) ← (PC)+relative offset
		b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0			
		R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0			
	JBC bit, rel	0	0	0	1	0	0	0	0	3	2	(PC) ← (PC)+3 IF (bit address) = 1 THEN (bit address) ← 0 (PC) ← (PC)+relative offset
		b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0			
		R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0			
External memory instructions	MOVX A, @Rr	1	1	1	0	0	0	0	r_0	1	2	(A) ← ((Rr)) EXTERNAL RAM
	MOVX A, @DPTR	1	1	1	0	0	0	0	0	1	2	(A) ← ((DPTR)) EXTERNAL RAM
	MOVX @Rr, A	1	1	1	1	0	0	1	r_0	1	2	(Rr) ← (A) EXTERNAL RAM
	MOVX @DPTR, A	1	1	1	1	0	0	0	0	1	2	((DPTP)) ← (A) EXTERNAL RAM
Other instructions	NOP	0	0	0	0	0	0	0	0	1	1	(PC) ← (PC)+1

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{CC}	Ta = 25°C	–0.5 to +7.0	V
Voltage from Any Pin to V_{SS}	V_I	Ta = 25°C	–0.5 to V_{CC} +7.0	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

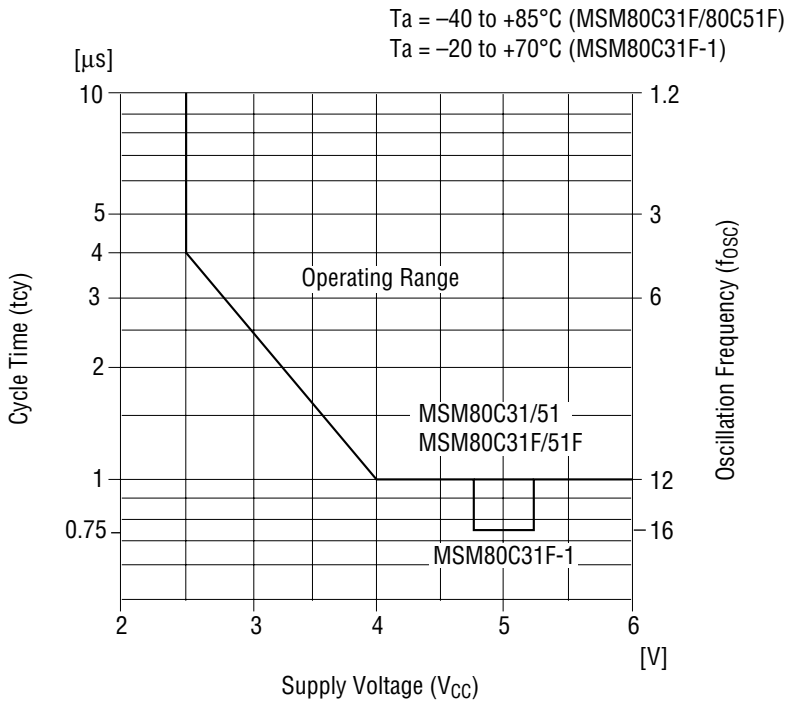
OPERATING RANGE

Parameter	Symbol	Condition	Range		Unit
Supply Voltage	V_{CC}	See figure below	2.5 to 6	*1	V
Memory Retention Voltage	V_{CC}	f_{OSC} = Oscillation stop	2 to 6		V
Oscillation Frequency	f_{OSC}	See figure below	DC to 16	*2	MHz
Ambient Temperature	Ta	MSM80C31F/51F	–40 to +85		°C
		MSM80C31F-1	–20 to +70		

*1 DC & AC characteristics in the range of 2.5 V ≤ V_{CC} < 4 V will be specified by DC & AC Characteristics 2.

*2 Specify MSM80C31F-1 when using MSM80C31F at 12 MHz to 16 MHz.

GUARANTEED OPERATING RANGE



ELECTRICAL CHARACTERISTICS

DC Characteristics 1

(MSM80C31F/51F V_{CC} = 5 V ±20%, V_{SS} = 0 V, Ta = –40°C to +85°C
MSM80C31F-1/51F-1 V_{CC} = 5 V ±5%, V_{SS} = 0 V, Ta = –20°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Low Input Voltage	V_{IL}	—	–0.5	—	0.2 V_{CC} – 0.1	V	1
High Input Voltage	V_{IH}	Except XTAL1, RESET and $\overline{EA}$	0.2 V_{CC} + 0.9	—	V_{CC} + 0.5	V	
High Input Voltage	V_{IH1}	XTAL1, RESET and $\overline{EA}$	0.7 V_{CC}	—	V_{CC} + 0.5	V	
Low Output Voltage (Port 1, 2 and 3)	V_{OL}	I_{OL} = 1.6 mA	—	—	0.45	V	
Low Output Voltage (Port 0, ALE and $\overline{PSEN}$)	V_{OL1}	I_{OL} = 3.2 mA	—	—	0.45	V	
High Output Voltage (Port 1, 2 and 3)	V_{OH}	I_{OH} = –60 µA V_{CC} = 5 V ±10%	2.4	—	—	V	
		I_{OH} = –30 µA	0.75 V_{CC}	—	—	V	
		I_{OH} = –10 µA	0.9 V_{CC}	—	—	V	
High Output Voltage (Port 0, ALE and $\overline{PSEN}$)	V_{OH1}	I_{OH} = –400 µA V_{CC} = 5 V ±10%	2.4	—	—	V	
		I_{OH} = –150 µA	0.75 V_{CC}	—	—	V	
		I_{OH} = –40 µA	0.9 V_{CC}	—	—	V	
Output Current at Low Input/ High Output Power Supply	I_{IL} / I_{OH}	V_I = 0.45 V / V_O = 0.45 V	–10	—	–200	µA	2
Output Current (Port 1, 2 and 3) at transition from H to L	I_{TL}	V_{IL} = 2.0 V	—	—	–500	µA	
Input Leakage Current (Floating Port 0 and $\overline{EA}$)	I_{LI}	V_{SS} < V_I < V_{CC}	—	—	±10	µA	3
RESET Pull-down Resistor	R_{RST}	—	20	40	125	kΩ	2
Input Pin Capacitor	C_{IO}	Ta = 25°C, f = 1 MHz 5 V (except XTAL1)	—	—	10	pF	—
Power Down Current	I_{PD}	V_{CC} = 2 V	—	1	50	µA	4

DC Characteristics 2

(V_{CC} = 2.5 to 4.0 V, V_{SS} = 0 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Low Input Voltage	V_{IL}	—	–0.5	—	$0.25V_{CC}$ – 0.1	V	1
High Input Voltage	V_{IH}	Except XTAL1, RESET and $\overline{EA}$	$0.25V_{CC}$ + 0.9	—	V_{CC} + 0.5	V	
High Input Voltage	V_{IH1}	XTAL1, RESET and $\overline{EA}$	$0.6V_{CC}$ + 0.6	—	V_{CC} + 0.5	V	
Low Output Voltage (Port 1, 2 and 3)	V_{OL}	I_{OL} = 10 µA	—	—	0.1	V	
Low Output Voltage (Port 0, ALE and $\overline{PSEN}$)	V_{OL1}	I_{OL} = 20 µA	—	—	0.1	V	
High Output Voltage (Port 1, 2 and 3)	V_{OH}	I_{OH} = –5 µA	0.75 V_{CC}	—	—	V	
High Output Voltage (Port 0, ALE and $\overline{PSEN}$)	V_{OH1}	I_{OH} = –20 µA	0.75 V_{CC}	—	—	V	
Output Current at Low Input/ High Output Power Supply	I_{IL} / I_{OH}	V_I = 0.1 V / V_O = 0.1 V	—	—	–100	µA	2
Output Current (Port 1, 2 and 3) at transition from H to L	I_{TL}	V_{IL} = 1.9 V	—	—	–300	µA	
Input Leakage Current (Floating Port 0 and $\overline{EA}$)	I_{LI}	$V_{SS} < V_I < V_{CC}$	—	—	±10	µA	3
RESET Pull-down Resistor	R_{RST}	—	20	40	125	kΩ	2
Input Pin Capacitor	C_{IO}	Ta = 25°C, f = 1 MHz 5 V (except XTAL1)	—	—	10	pF	—
Power Down Current	I_{PD}	—	—	1	10	µA	4

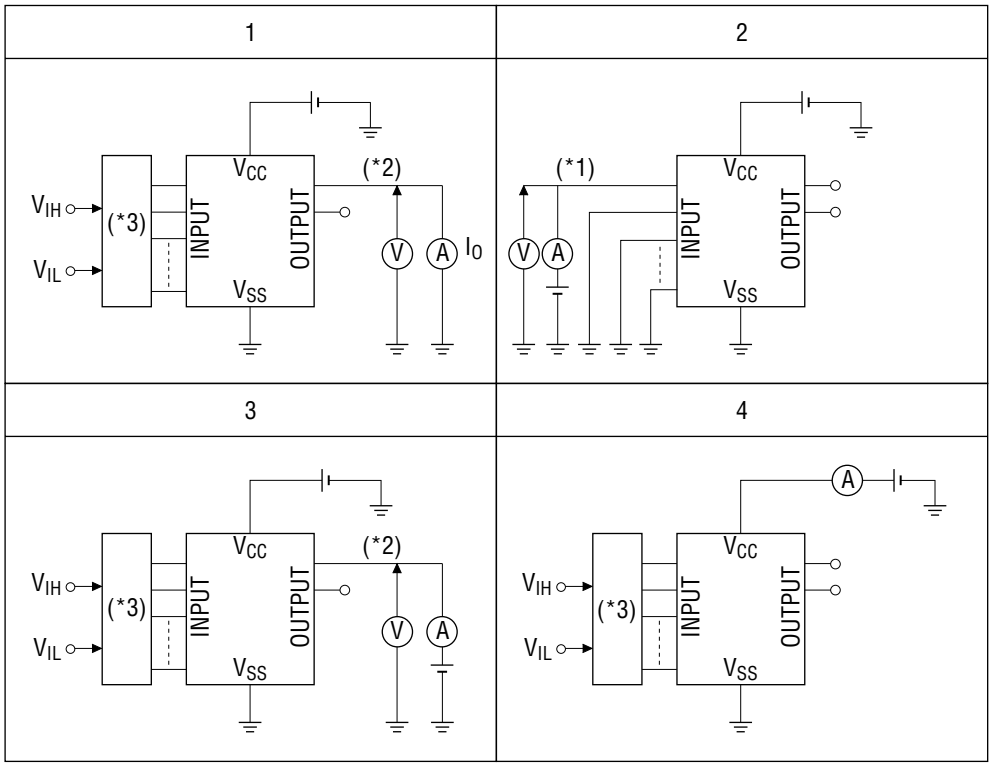
Maximum operating power supply I_{CC} [mA]

V_{CC}	2.5 V	3.0 V	4.0 V
Freq			
0.5 MHz	0.7	0.9	1.6
3.0 MHz	1.9	2.4	4.3
8 MHz	—	—	8.3
12 MHz	—	—	12.0

Maximum IDLE power supply I_{CC} [mA]

V_{CC}	2.5 V	3.0 V	4.0 V
Freq			
0.5 MHz	0.3	0.4	0.6
3.0 MHz	0.6	0.8	1.2
8 MHz	—	—	2.2
12 MHz	—	—	3.1

Measuring Circuit



*1 Repeated for specified input pin.
*2 Repeated for specified output pin.
*3 Logic input for specified condition.

External Program Memory Access AC Characteristics 1

(V_{CC} = 5 V ±20%, V_{SS} = 0 V, Ta = –40°C to +85°C; Load Capacitance for Port 0, ALE, and $\overline{PSEN}$ = 100 pF ; Load Capacitance for all other outputs = 80 pF)

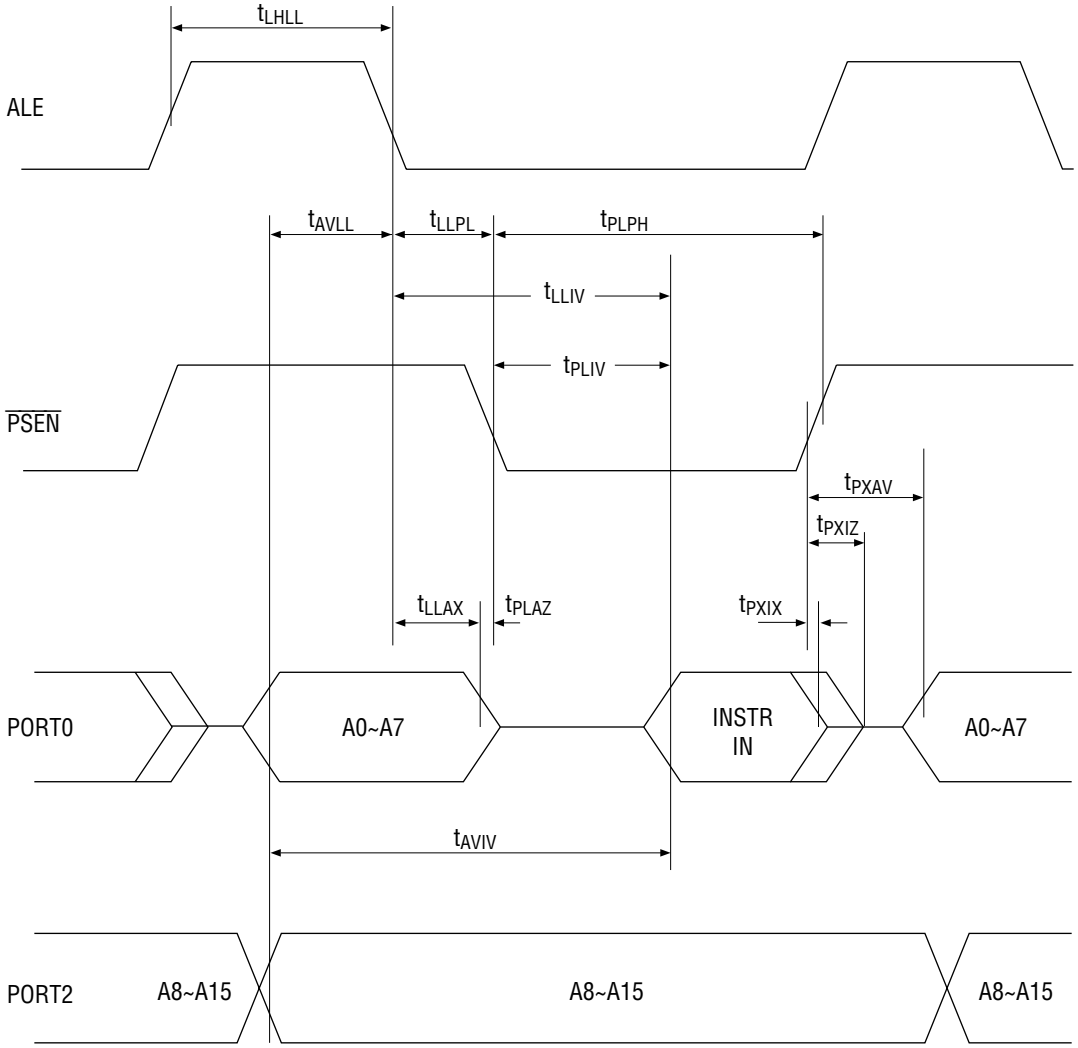
Parameter	Symbol	12 MHz Clock		Variable Clock See Guaranteed Operating Range		Unit
		Min.	Max.	Min.	Max.	
XTAL1, XTAL2 Oscillation Cycle	t_{CLCL}	—	—	83.3	—	ns
ALE Signal Width	t_{LHLL}	126	—	$2t_{CLCL}$ – 40	—	ns
Adderss Setup Time (to ALE Falling Edge)	t_{AVLL}	43	—	$1t_{CLCL}$ – 40	—	ns
Adderss Hold Time (from ALE Falling Edge)	t_{LLAX}	48	—	$1t_{CLCL}$ – 35	—	ns
Instruction Data Read Time (from ALE Falling Edge)	t_{LLIV}	—	233	—	$4t_{CLCL}$ – 100	ns
From ALE Falling Edge to $\overline{PSEN}$ Falling Edge	t_{LLPL}	58	—	$1t_{CLCL}$ – 25	—	ns
$\overline{PSEN}$ Signal Width	t_{PLPH}	215	—	$3t_{CLCL}$ – 35	—	ns
Instruction Data Read Time (from $\overline{PSEN}$ Falling Edge)	t_{PLIV}	—	145	—	$3t_{CLCL}$ – 105	ns
Instruction Data Hold Time (from $\overline{PSEN}$ Rising Edge)	t_{PXIX}	0	—	0	—	ns
Bus Floating Time after Instruction Data Read (from $\overline{PSEN}$ Rising Edge)	t_{PXIZ}	—	63	—	$1t_{CLCL}$ – 20	ns
Address Output Time from $\overline{PSEN}$ Rising Edge	t_{PXAV}	75	—	$1t_{CLCL}$ – 8	—	ns
Instruction Data Read Time (from Address Output)	t_{AVIV}	—	312	—	$5t_{CLCL}$ – 105	ns
Bus Floating Time (Address Float from $\overline{PSEN}$ Falling Edge)	t_{PLAZ}	—	0	—	0	ns

External Program Memory Access AC Characteristics 2

(V_{CC} = 2.5 to 4.0 V, V_{SS} = 0 V, Ta = –40°C to +85°C; Load Capacitance for Port 0, ALE, and $\overline{PSEN}$ = 100 pF ; Load Capacitance for all other outputs = 80 pF)

Parameter	Symbol	12 MHz Clock		Variable Clock See Guaranteed Operating Range		Unit
		Min.	Max.	Min.	Max.	
XTAL1, XTAL2 Oscillation Cycle	t_{CLCL}	—	—	83.3	—	ns
ALE Signal Width	t_{LHLL}	126	—	$2t_{CLCL}$ – 40	—	ns
Adderss Setup Time (to ALE Falling Edge)	t_{AVLL}	43	—	$1t_{CLCL}$ – 40	—	ns
Adderss Hold Time (from ALE Falling Edge)	t_{LLAX}	48	—	$1t_{CLCL}$ – 35	—	ns
Instruction Data Read Time (from ALE Falling Edge)	t_{LLIV}	—	233	—	$4t_{CLCL}$ – 100	ns
From ALE Falling Edge to $\overline{PSEN}$ Falling Edge	t_{LLPL}	58	—	$1t_{CLCL}$ – 25	—	ns
$\overline{PSEN}$ Signal Width	t_{PLPH}	215	—	$3t_{CLCL}$ – 35	—	ns
Instruction Data Read Time (from $\overline{PSEN}$ Falling Edge)	t_{PLIV}	—	145	—	$3t_{CLCL}$ – 105	ns
Instruction Data Hold Time (from $\overline{PSEN}$ Rising Edge)	t_{PXIX}	0	—	0	—	ns
Bus Floating Time after Instruction Data Read (from $\overline{PSEN}$ Rising Edge)	t_{PXIZ}	—	63	—	$1t_{CLCL}$ – 20	ns
Address Output Time from $\overline{PSEN}$ Rising Edge	t_{PXAV}	75	—	$1t_{CLCL}$ – 8	—	ns
Instruction Data Read Time (from Address Output)	t_{AVIV}	—	312	—	$5t_{CLCL}$ – 105	ns
Bus Floating Time (Address Float from $\overline{PSEN}$ Falling Edge)	t_{PLAZ}	—	0	—	0	ns

External Program Memory Read Cycle



External Data Memory Access AC Characteristics 1

(V_{CC} = 5 V ±20%, V_{SS} = 0 V, Ta = –40°C to +85°C; load capacitance for Port 0, ALE, and $\overline{PSEN}$ = 100 pF ; load capacitance for all other outputs = 80 pF)

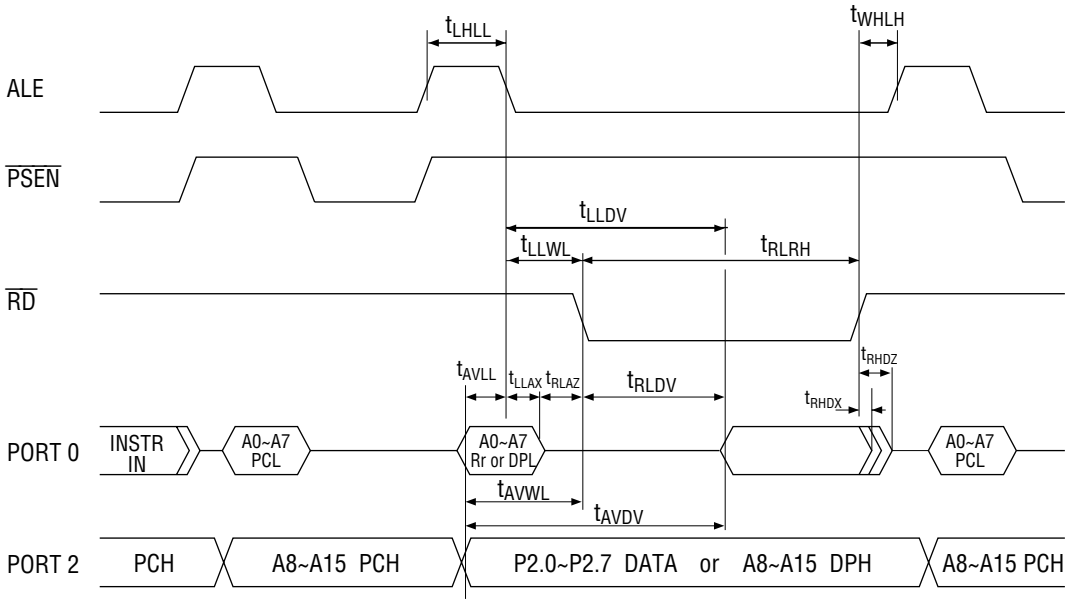
Parameter	Symbol	12 MHz Clock		Variable Clock See Guaranteed Operating Range		Unit
		Min.	Max.	Min.	Max.	
XTAL1, XTAL2 Oscillation Cycle	t_{CLCL}	—	—	62.5	—	ns
ALE Single Width	t_{LHLL}	126	—	$2t_{CLCL}$ – 40	—	ns
Adderss Setup Time (to ALE Falling Edge)	t_{AVLL}	43	—	$1t_{CLCL}$ – 40	—	ns
Adderss Hold Time (from ALE Falling Edge)	t_{LLAX}	48	—	$1t_{CLCL}$ – 35	—	ns
$\overline{RD}$ Single Width	t_{RLRH}	400	—	$6t_{CLCL}$ – 100	—	ns
$\overline{WR}$ Single Width	t_{WLWH}	400	—	$6t_{CLCL}$ – 100	—	ns
RAM Data Read Time (from $\overline{RD}$ Single Falling Edge)	t_{RLDV}	—	251	—	$5t_{CLCL}$ – 165	ns
RAM Data Read Hold Time (from $\overline{RD}$ Single Rising Edge)	t_{RHDX}	0	—	0	—	ns
Data Bus Floating Time (from $\overline{RD}$ Single Rising Edge)	t_{RHDZ}	—	96	—	$2t_{CLCL}$ – 70	ns
RAM Data Read Time (from $\overline{ALE}$ Single Falling Edge)	t_{LLDV}	—	516	—	$8t_{CLCL}$ – 150	ns
RAM Data Read Time (from Address Output)	t_{AVDV}	—	585	—	$9t_{CLCL}$ – 165	ns
$\overline{RD}$/$\overline{WR}$ Output Time from ALE Falling Edge	t_{LLWL}	200	300	$3t_{CLCL}$ – 50	$3t_{CLCL}$ + 50	ns
$\overline{RD}$/$\overline{WR}$ Output Time from Address Output	t_{AVWL}	203	—	$4t_{CLCL}$ – 130	—	ns
$\overline{RD}$ Output Time from Data Output	t_{QVWX}	23	—	$1t_{CLCL}$ – 60	—	ns
Time from Data Output to $\overline{WR}$ Rising Edge	t_{QVWH}	433	—	$7t_{CLCL}$ – 150	—	ns
Data Hold Time ($\overline{WR}$ Rising Edge)	t_{WHQX}	33	—	$1t_{CLCL}$ – 50	—	ns
Time from $\overline{RD}$ Output to Address Float	t_{RLAZ}	—	0	—	0	ns
Time from $\overline{RD}$/$\overline{WR}$ Rising Edge to ALE Rising Edge	t_{WHLH}	43	133	$1t_{CLCL}$ – 40	$1t_{CLCL}$ + 50	ns

External Data Memory Access AC Characteristics 2

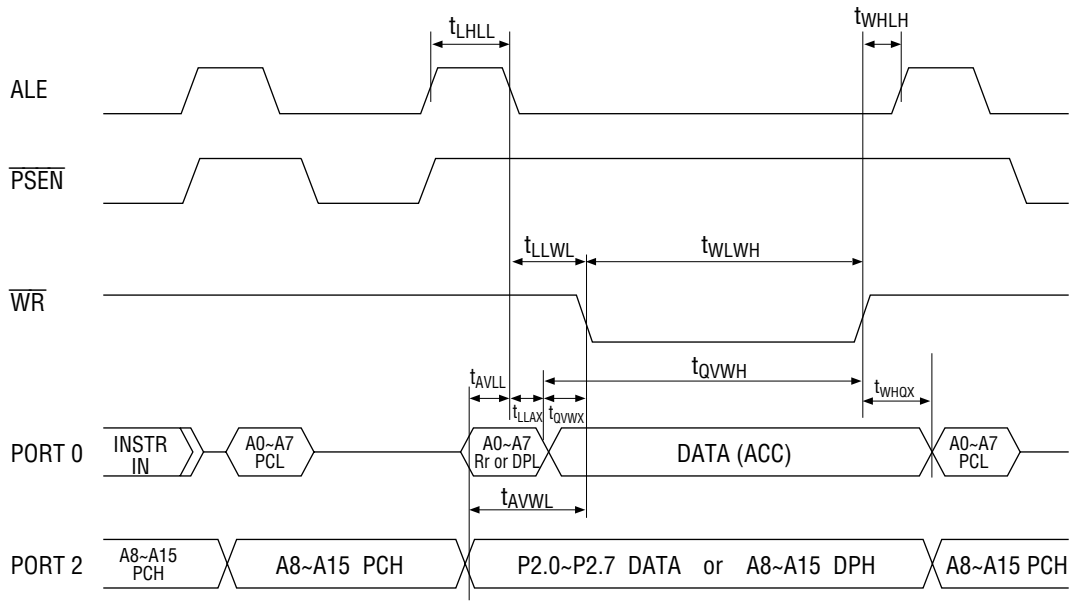
(V_{CC} = 2.5 to 4.0 V, V_{SS} = 0 V, Ta = –40°C to +85°C; load capacitance for Port 0, ALE, and $\overline{PSEN}$ = 100 pF ; load capacitance for all other outputs = 80 pF)

Parameter	Symbol	12 MHz Clock		Variable Clock See Guaranteed Operating Range		Unit
		Min.	Max.	Min.	Max.	
XTAL1, XTAL2 Oscillation Cycle	t_{CLCL}	—	—	62.5	—	ns
ALE Single Width	t_{LHLL}	126	—	$2t_{CLCL}$ – 40	—	ns
Adderss Setup Time (to ALE Falling Edge)	t_{AVLL}	43	—	$1t_{CLCL}$ – 40	—	ns
Adderss Hold Time (from ALE Falling Edge)	t_{LLAX}	48	—	$1t_{CLCL}$ – 35	—	ns
$\overline{RD}$ Single Width	t_{RLRH}	400	—	$6t_{CLCL}$ – 100	—	ns
$\overline{WR}$ Single Width	t_{WLWH}	400	—	$6t_{CLCL}$ – 100	—	ns
RAM Data Read Time (from $\overline{RD}$ Single Falling Edge)	t_{RLDV}	—	251	—	$5t_{CLCL}$ – 165	ns
RAM Data Read Hold Time (from $\overline{RD}$ Single Rising Edge)	t_{RHDX}	0	—	0	—	ns
Data Bus Floating Time (from $\overline{RD}$ Single Rising Edge)	t_{RHDZ}	—	96	—	$2t_{CLCL}$ – 70	ns
RAM Data Read Time (from $\overline{ALE}$ Single Falling Edge)	t_{LLDV}	—	516	—	$8t_{CLCL}$ – 150	ns
RAM Data Read Time (from Address Output)	t_{AVDV}	—	585	—	$9t_{CLCL}$ – 165	ns
$\overline{RD}$/$\overline{WR}$ Output Time from ALE Falling Edge	t_{LLWL}	150	300	$3t_{CLCL}$ – 100	$3t_{CLCL}$ + 50	ns
$\overline{RD}$/$\overline{WR}$ Output Time from Address Output	t_{AVWL}	203	—	$4t_{CLCL}$ – 130	—	ns
$\overline{RD}$ Output Time from Data Output	t_{QVWX}	23	—	$1t_{CLCL}$ – 60	—	ns
Time from Data Output to $\overline{WR}$ Rising Edge	t_{QVWH}	433	—	$7t_{CLCL}$ – 150	—	ns
Data Hold Time ($\overline{WR}$ Rising Edge)	t_{WHQX}	33	—	$1t_{CLCL}$ – 50	—	ns
Time from $\overline{RD}$ Output to Address Float	t_{RLAZ}	—	0	—	0	ns
Time from $\overline{RD}$/$\overline{WR}$ Rising Edge to ALE Rising Edge	t_{WHLH}	43	183	$1t_{CLCL}$ – 40	$1t_{CLCL}$ + 100	ns

External Data Memory Read Cycle



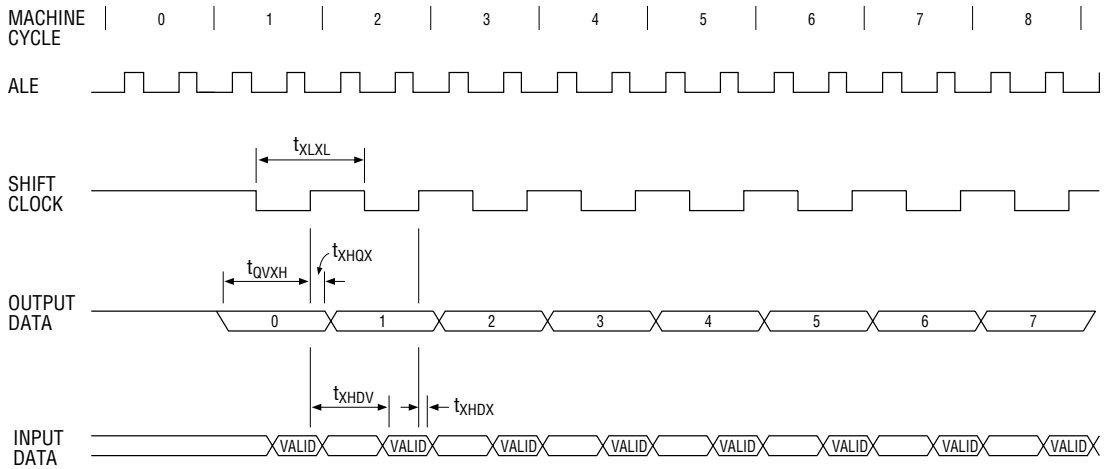
External Data Memory Write Cycle



Serial Port Timing (I/O Expansion Mode) AC Characteristics 1

(Ta = –40°C to +85°C ; V_{CC} = 5 V ±20% ; V_{SS} = 0 V)

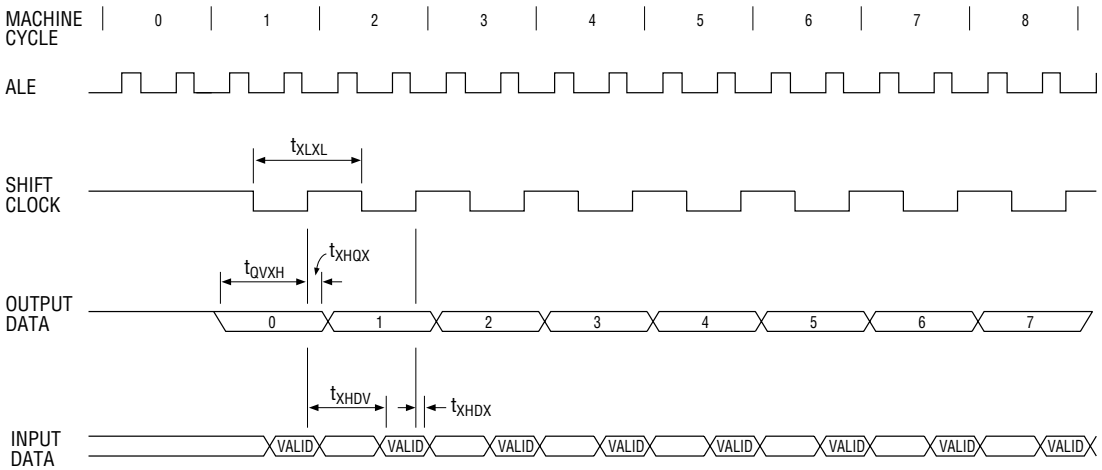
Parameter	Symbol	Min.	Max.	Unit
Serial port clock cycle time	t_{XLXL}	$12t_{CLCL}$	—	ns
Output data setup to clock rising edge	t_{QVXH}	$10t_{CLCL}$ – 133	—	ns
Output data hold after clock rising edge	t_{XHQX}	$2t_{CLCL}$ – 117	—	ns
Input data hold after clock rising edge	t_{XHDX}	0	—	ns
Clock rising edge to input data valid	t_{XHDV}	—	$10t_{CLCL}$ – 133	ns



Serial Port Timing (I/O Expansion Mode) AC Characteristics 2

(Ta = –40°C to +85°C ; V_{CC} =2.5 to 4.0 V ; V_{SS} = 0 V)

Parameter	Symbol	Min.	Max.	Unit
Serial port clock cycle time	t_{XLXL}	$12t_{CLCL}$	—	ns
Output data setup to clock rising edge	t_{QVXH}	$10t_{CLCL}$ – 133	—	ns
Output data hold after clock rising edge	t_{XHQX}	$2t_{CLCL}$ – 117	—	ns
Input data hold after clock rising edge	t_{XHDX}	0	—	ns
Clock rising edge to input data valid	t_{XHDV}	—	$10t_{CLCL}$ – 133	ns

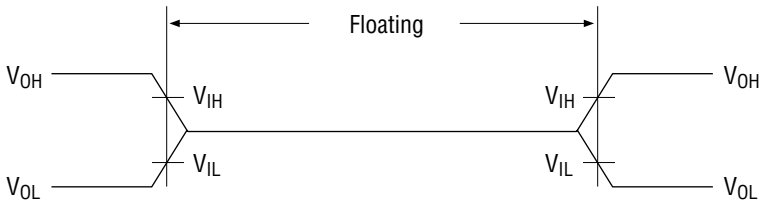


AC Characteristics Measuring Conditions

Input/output signal

* The input signals in AC test mode are either V_{OH} (logic "1") or V_{OL} (logic "0") input signals where logic "1" corresponds to a CPU output signal waveform measuring point in excess of V_{IH}, and logic "0" to a point below V_{IL}.

Floating

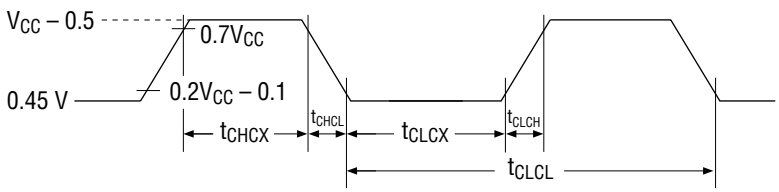


* The port 0 floating interval is measured from the time the port 0 pin voltage drops below V_{IH} after sinking to GND at 2.4 mA when switching to floating status from a "1" output, and from the time the port 0 pin voltage exceeds V_{IL} after connecting to a 400 µA source when switching to floating status from a "0" output.

XTAL1 External Clock Input Waveform Conditions

Parameter	Symbol	Variable Clock See Guaranteed Operating Range		
		Min.	Max.	Unit
External Clock Frequency	$1/t_{CLCL}$	DC	16	MHz
High Time	t_{CHCX}	20	—	ns
Low Time	t_{CLCX}	20	—	ns
Rise Time	t_{CLCH}	—	20	ns
Fall Time	t_{CHCL}	—	20	ns

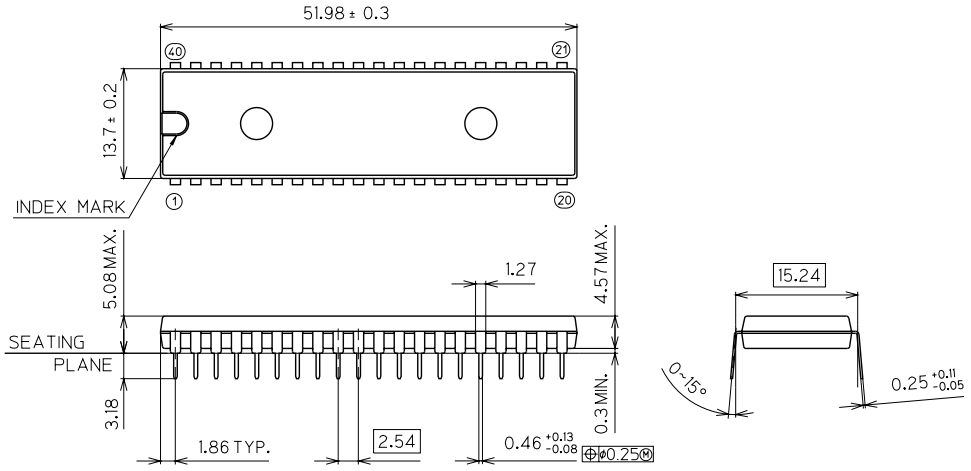
External clock waveform



PACKAGE DIMENSIONS

(Unit : mm)

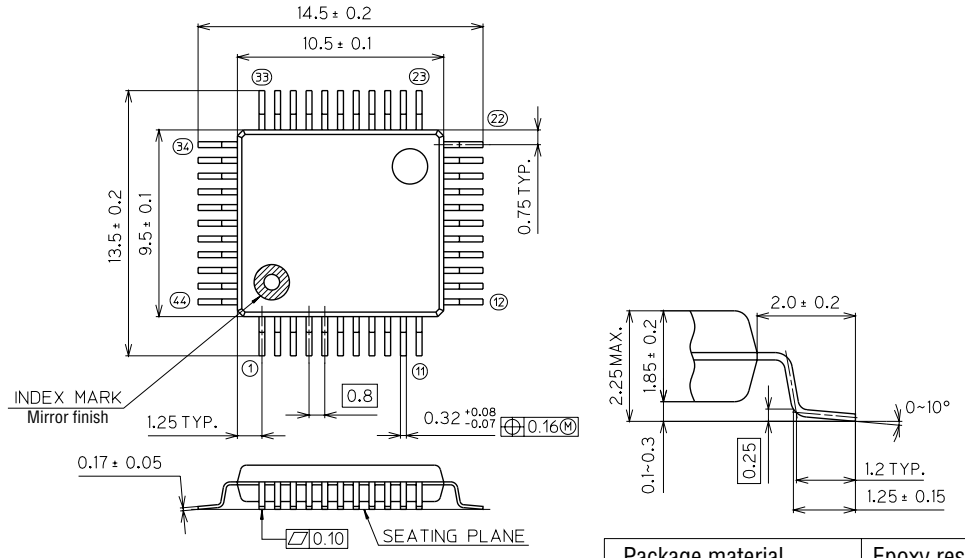
DIP40-P-600-2.54



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	6.10 TYP.

(Unit : mm)

QFP44-P-910-0.80-2K



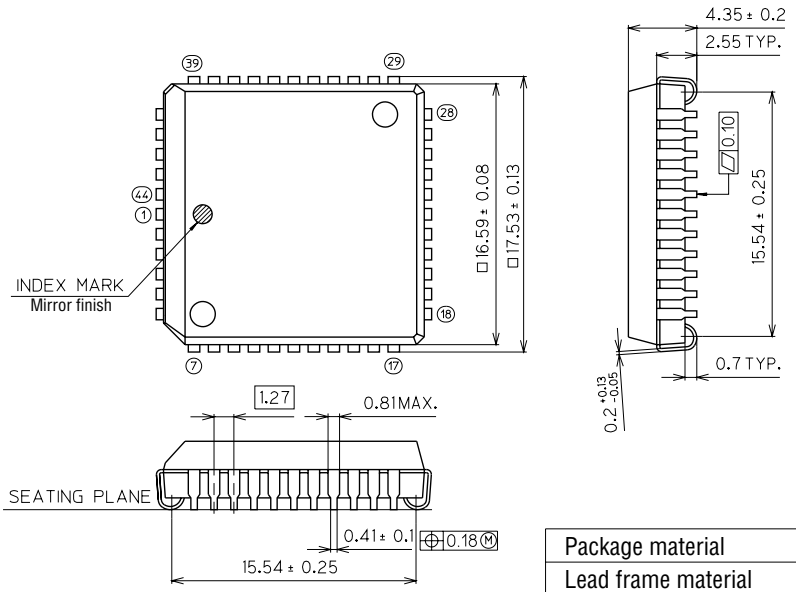
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.41 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFJ44-P-S650-1.27



Package material	Epoxy resin
Lead frame material	Cu alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	2.00 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

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