

T-4623-14

MSM832S/T/V/W 32K X 8 Monolithic CMOS SRAM

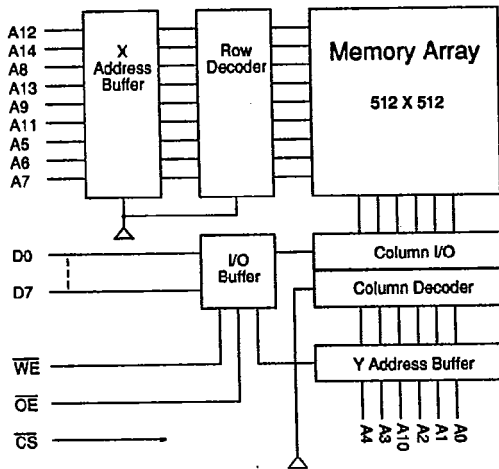
Issue 2.1 April 1989

32,768 x 8 CMOS High Speed Static RAM

Features

- Access Times of 85/100/120/150 ns
- Standard 28 pin DIL/32 pin LCC Footprint
- Low Power Standby 10 μW (typ)- L Version
- Low Power Operation 40 mW (typ)- L Version
- Completely Static Operation
- Battery Back-up Capability
- Directly TTL Compatible
- May be Processed to MIL-STD883C (suffix MB).

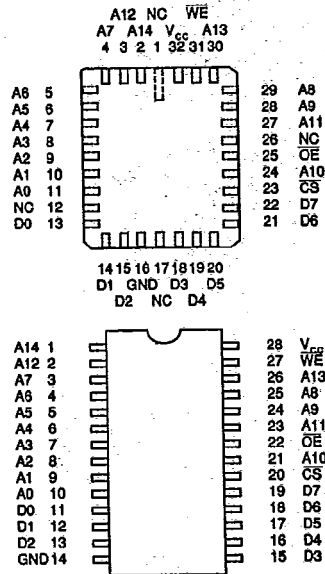
Block Diagram



PRELIMINARY INFORMATION

Pin Definitions

Package Types: 'S', 'T', 'V', 'W'



Pin Functions

- A0-A14 Address inputs
- D0-7 Data Input/Output
- CS Chip Select
- OE Output Enable
- WE Write Enable
- V_{cc} Power(+5V)



Package Details

Pin Count	Description	Package Type	Material	Pin Out
28	600 mil Dual-in-line (DIP)	S	Ceramic	JEDEC
28	300 mil Dual-in-line (DIP)	T	Ceramic	JEDEC
28	100 mil Vertical-in-line (VIL)	V	Ceramic	JEDEC
32	Leadless Chip Carrier (LCC)	W	Ceramic	JEDEC

Package dimensions and outlines are displayed on page 2-65,66.
 VIL is a trademark of Mosaic Semiconductor Inc., Patent Pending #287982

Absolute Maximum Ratings

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Voltage on any pin relative to V_{SS}	V_I	-0.5V to +7	V
Power Dissipation	P_t	1	W
Storage Temperature	T_{STG}	-55 to +150	°C

Note: V_I can be -3.5V pulse of less than 20ns.

Recommended Operating Conditions

		min	typ	max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V
Operating Temperature	T_a	0	-	70	°C
	T_{al}	-40	-	85	°C (832I)
	T_{am}	-55	-	125	°C (832M,832MB)

DC Electrical Characteristics

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_U	$V_{in}=0V$ to V_{CC}	-	-	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$, $V_{IO}=Gnd$ to V_{CC}	-	-	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{IO}=0mA$, I/P's static	-	8	15	mA
Average Power Supply Current	I_{CC1}	Min. Cycle, duty=100%, $I_{IO}=0mA$	-	50	70	mA
Standby Current (L Part)	I_{SIL}^* I_{SIL1}^*	$\overline{CS}=V_{IH}$, I/P's static $\overline{CS} \geq V_{CC}-0.2V$, I/P's < 0.2V or $\geq V_{CC}-0.2V$	-	0.5 .04	3 2	mA mA
Output Voltage	V_{OL} V_{OH}	$I_{OL}=2.1mA$ $I_{OH}=-1.0mA$	- 2.4	- -	100 0.4	μA V V

Typical values are at $V_{CC}=5.0V$, $T_a=25^\circ C$ and specified loading.
* V_{IL} min = -0.3V

Capacitance ($V_{CC}=5V \pm 10\%$, $T_a=25^\circ C$)

Parameter	Symbol	Test Condition	typ	max	Unit
Input Capacitance:	C_{in}	$V_{in} = 0V$	-	6	pF
I/O Capacitance:	C_{IO}	$V_{IO} = 0V$	-	8	pF

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

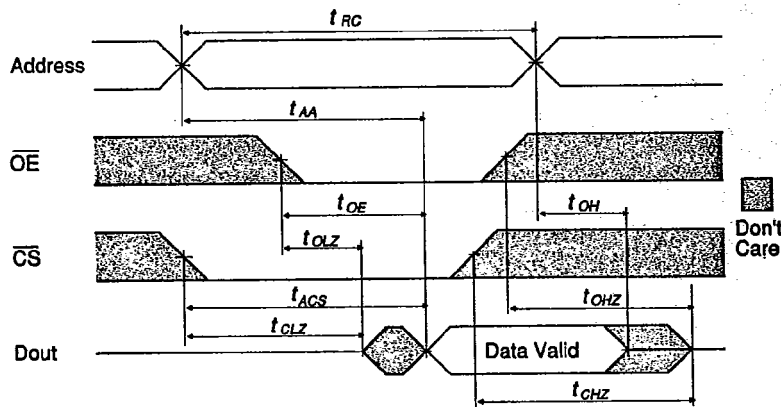
- * Input pulse levels: 0.8V to 2.4V
- * Input rise and fall times: 5ns
- * Input and Output timing reference levels: 1.5V
- * Output load: 1 TTL gate + 100pF
- * $V_{CC}=5V \pm 10\%$

Electrical Characteristics & Recommended AC Operating Conditions

Read Cycle

Parameter	Symbol	-85		-100		-120		-150		Unit
		min	max	min	max	min	max	min	max	
Read Cycle Time	t_{RC}	85	-	100	-	120	-	150	-	nS
Address Access Time	t_{AA}	-	85	-	100	-	120	-	150	nS
Chip Select Access Time	t_{ACS}	-	85	-	100	-	120	-	150	nS
Output Enable to Output Valid	t_{OE}	-	45	-	50	-	60	-	70	nS
Output Hold from Address Change	t_{OH}	5	-	10	-	10	-	10	-	nS
Chip Selection to Output in Low Z	t_{CLZ}	10	-	10	-	10	-	10	-	nS
Output Enable to Output in Low Z	t_{OLZ}	5	-	5	-	5	-	5	-	nS
Chip Deselection to Output in High Z	t_{CHZ}	0	30	0	35	0	40	0	50	nS
Output Disable to Output in High Z	t_{OHZ}	0	30	0	35	0	40	0	50	nS

Read Cycle Timing Waveform (1)



Notes:

1. \overline{WE} is High for Read Cycle.
2. Address valid prior to or coincident with \overline{CS} transition Low.

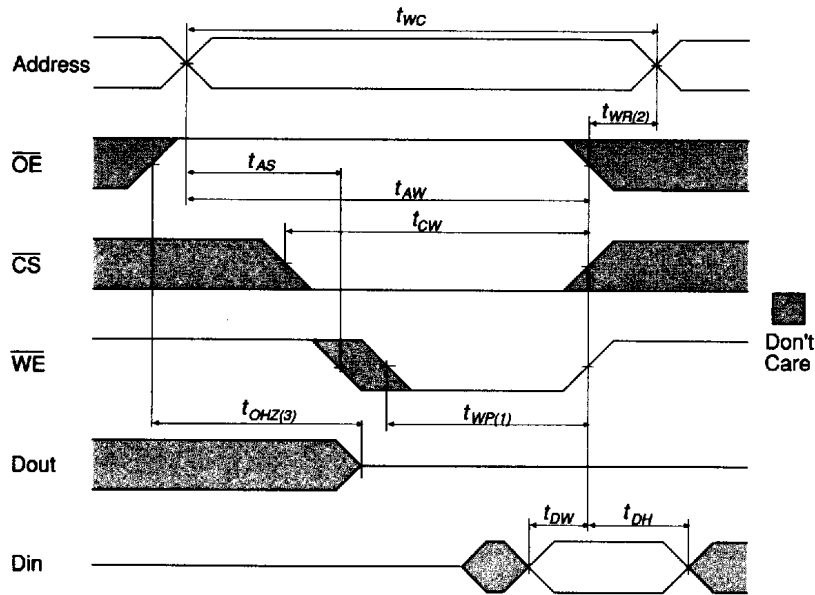


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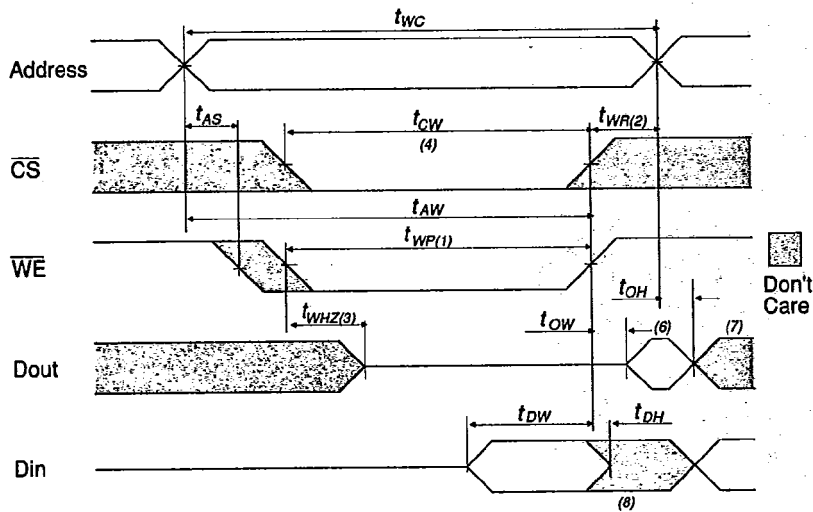
Write Cycle

Parameter	Symbol	-85		-100		-120		-150		Unit
		min	max	min	max	min	max	min	max	
Write Cycle Time	t_{WC}	85	-	100	-	120	-	150	-	nS
Chip Selection to End of Write	t_{CW}	75	-	80	-	85	-	100	-	nS
Address Valid to End of Write	t_{AW}	75	-	80	-	85	-	100	-	nS
Address Setup Time	t_{AS}	0	-	0	-	0	-	0	-	nS
Write Pulse Width	t_{WP}	60	-	60	-	70	-	90	-	nS
Write Recovery Time	t_{WR}	10	-	0	-	0	-	0	-	nS
Write to Output in High Z	t_{WHZ}	0	30	0	35	0	40	0	50	nS
Data to Write Time Overlap	t_{DW}	40	-	40	-	50	-	60	-	nS
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	0	-	nS
Output Disable to Output in High Z	t_{OHZ}	0	30	0	35	0	40	0	50	nS
Output Active from End of Write	t_{OW}	5	-	5	-	5	-	5	-	nS

Write Cycle No.1 Timing Waveform



Write Cycle No.2 Timing Waveform (5)



Notes:

1. A write occurs during the overlap (t_{WP}) of a low \overline{CS} and a low \overline{WE} .
2. t_{WR} is measured from the earlier of CS or WE going high to the end of write cycle.
3. During this period, I/O pins are in the output state. Input signals out of phase must not be applied.
4. If the \overline{CS} low transition occurs simultaneously with the \overline{WE} low transition or after the \overline{WE} low transition, outputs remain in a high impedance state.
5. \overline{OE} is continuously low. ($\overline{OE} = V_L$)
6. Dout is in the same phase as written data of this write cycle.
7. Dout is the read data of next address.
8. If \overline{CS} is low during this period, I/O pins are in the output state. Input signals out of phase must not be applied to I/O pins.

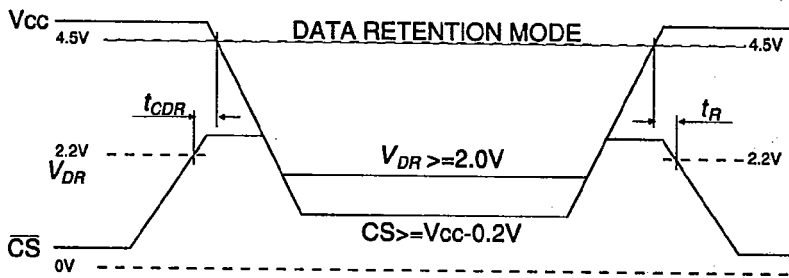
Low V_{cc} Data Retention Characteristics - L Version Only

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Parameter	Symbol	Test Condition	min	typ	max	Unit
V _{cc} for Data Retention	V _{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2.0	-	-	V
Data Retention Current	I _{CCDR1}	V _{CC} =3.0V, $\overline{CS} \geq 2.8V$ T _{op} =T _a	-	8	30	μA
	I _{CCDR2}	T _{op} =T _{al}	-	-	50	μA
	I _{CCDR3}	T _{op} =T _{am}	-	-	100	μA
Chip Deselect to Data Retention Time	t _{CDR}	See Retention Waveform	0	-	-	nS
Operation Recovery Time	t _R	See Retention Waveform	t _{RC} ⁽¹⁾	-	-	nS

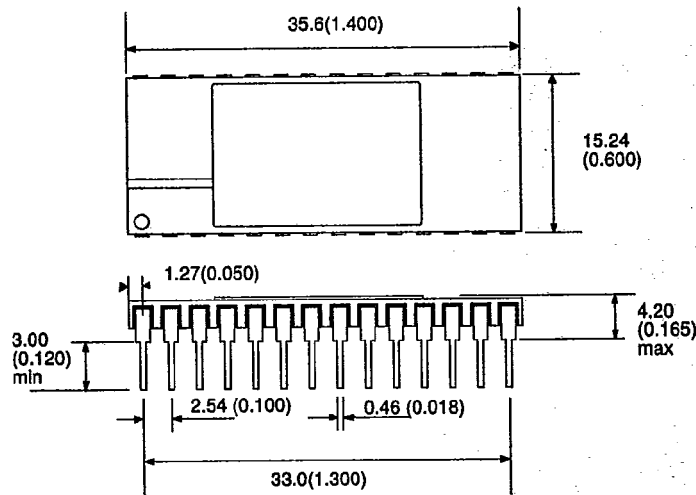
Notes 1. t_{RC}=Read Cycle Time

Low V_{cc} Data Retention Timing Diagram - L Version Only

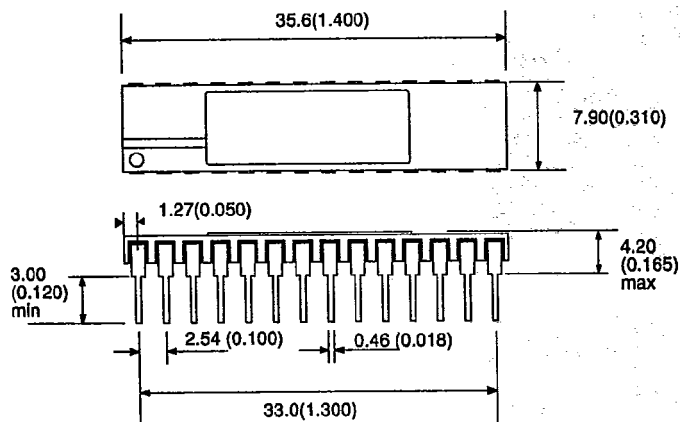


Package Details Dimensions in mm (inches) Tolerance on all dimensions $\pm 0.254(0.010)$.

28 Pin DIL ('S' Package)

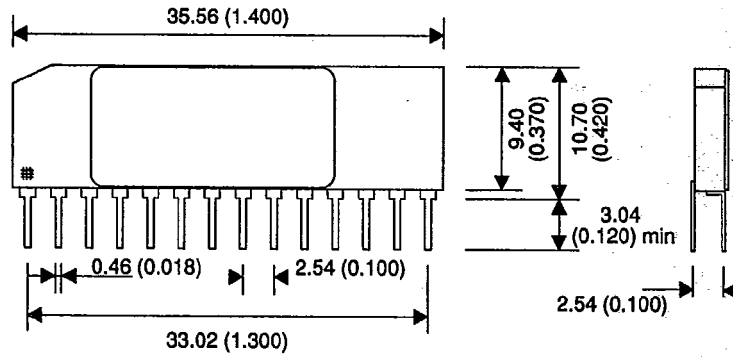


28 Pin DIP ('T' Package)

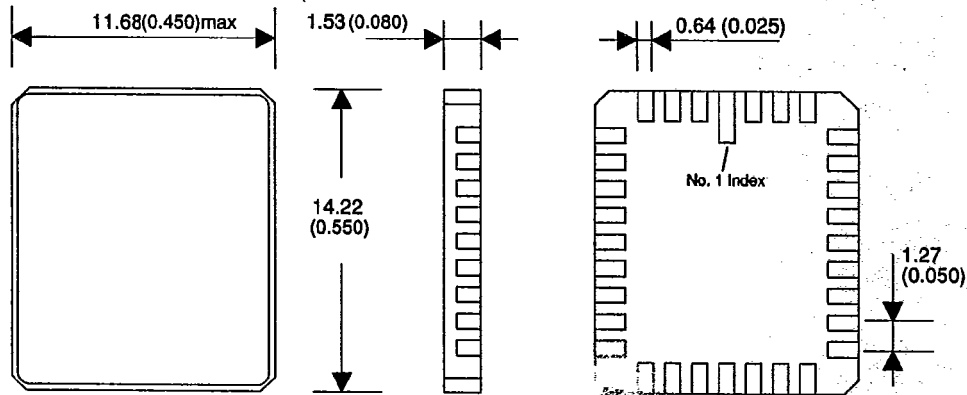


28 Pin Vertical in line ('V' Package)

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32 Pin LCC ('W' Package)



Military Screening Procedure

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Component Screening Flow for high reliability product is in accordance with Mil-883C method 5004 and is detailed below:

MB COMPONENT SCREENING FLOW

SCREEN	TEST METHOD	LEVEL
Visual and Mechanical		
Internal visual	2010 Condition B or manufacturers equivalent	100%
High-temperature storage	1008 Condition C (24hrs @ +150°C)	100%
Temperature cycle	1010 Condition C (10 Cycles, -65°C to +150°C)	100%
Constant acceleration	2001 Condition E (Y, only) (30,000g)	100%
Pre-Burn-in electrical	Per applicable device specifications at Ta=+25°C	100%
Burn-in	Method 1015, Condition D, Ta=+125°C, 160hrs min	100%
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ Ta=+25°C and power supply extremes b) @ temperature and power supply extremes	100% 100%
Functional	a) @ Ta=+25°C and power supply extremes b) @ temperature and power supply extremes	100% 100%
Switching (ac)	a) @ Ta=+25°C and power supply extremes b) @ temperature and power supply extremes	100% 100%
Percent Defective allowable (PDA)	Calculated at post-burn-in at Ta=+25°C	5%
Hermeticity	1014	
Fine	Condition A	100%
Gross	Condition C	100%
External Visual	2009 Per vendor or customer specification	100%



Ordering Information

MSM832WLMB-10

