

75V(D-S) N-Channel Enhancement Mode Power MOS FET

Features

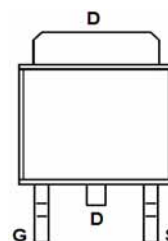
- $V_{DS}=75V$; $I_D=60A@V_{GS}=10V$;
 $R_{DS(ON)}<8.5m\Omega @V_{GS}=10V$
- Special process technology for high ESD capability
- Special designed for Convertors and power controls
- High density cell design for ultra low $R_{ds(on)}$
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation



Lead Free

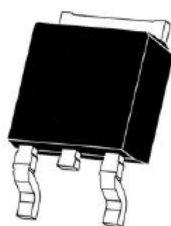
Application

- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply

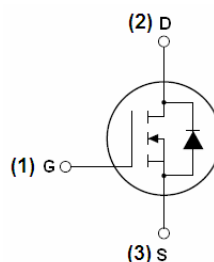


Marking and pin assignment

PIN Configuration



TO-252-2L top view



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MSN0860D	MSN0860D	TO-252-2L	-	-	-

Table 1. Absolute Maximum Ratings ($T_C=25^{\circ}C$)

Parameter	Symbol	Value	Unit
Drain-Source Voltage ($V_{GS}=0V$)	V_{DS}	75	V
Gate-Source Voltage ($V_{DS}=0V$)	V_{GS}	± 20	V
Drain Current (DC) at $T_C=25^{\circ}C$	$I_D(DC)$	60	A
Drain Current (DC) at $T_C=100^{\circ}C$	$I_D(DC)$	42	A
Drain Current-Continuous@ Current-Pulsed (Note 1)	$I_{DM}(pluse)$	310	A
Peak diode recovery voltage	dv/dt	30	V/ns
Maximum Power Dissipation($T_C=25^{\circ}C$)	P_D	140	W
Derating factor		0.95	W/ $^{\circ}C$
Single pulse avalanche energy (Note 2)	E_{AS}	300	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^{\circ}C$

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2.EAS condition: $T_J=25^{\circ}C, V_{DD}=37.5V, V_G=10V, L=0.5mH$

Table 2. Thermal Characteristic

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Maximum)	R_{thJC}	1.05	°C/W
Thermal Resistance, Junction-to-Ambient (Maximum)	R_{thJA}	50	°C/W

Table 3. Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

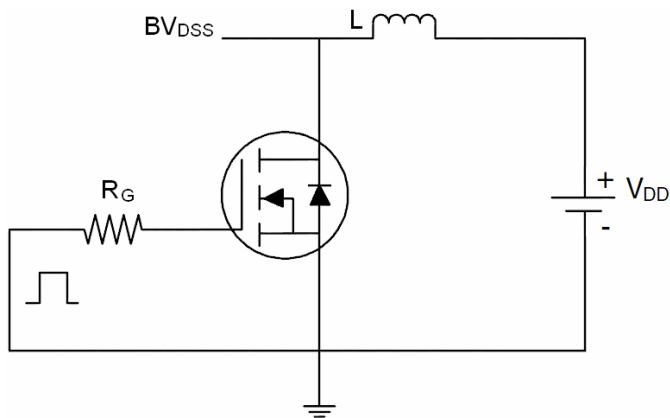
Parameter	Symbol	Condition	Min	Typ	Max	Unit
On/off states						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	75	84	-	V
Zero Gate Voltage Drain Current(Tc=25℃)	I _{DSS}	V _{DS} =75V,V _{GS} =0V	-	-	1	μA
Zero Gate Voltage Drain Current(Tc=125℃)	I _{DSS}	V _{DS} =75V,V _{GS} =0V	-	-	10	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	2	3	4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =30A	-	6.8	8.5	mΩ
Dynamic Characteristics						
Forward Transconductance	g _{FS}	V _{DS} =5V,I _D =30A		66	-	S
Input Capacitance	C _{iss}	V _{DS} =25V,V _{GS} =0V, F=1.0MHz		4400	-	PF
Output Capacitance	C _{oss}			340	-	PF
Reverse Transfer Capacitance	C _{rss}			260	-	PF
Total Gate Charge	Q _g	V _{DS} =30V,I _D =30A, V _{GS} =10V		100	-	nC
Gate-Source Charge	Q _{gs}			20	-	nC
Gate-Drain Charge	Q _{gd}			30	-	nC
Switching times						
Turn-on Delay Time	t _{d(on)}	V _{DD} =30V,I _D =2A,R _L =15Ω V _{GS} =10V,R _G =2.5Ω	-	17.8	-	nS
Turn-on Rise Time	t _r		-	11.8	-	nS
Turn-Off Delay Time	t _{d(off)}		-	56	-	nS
Turn-Off Fall Time	t _f		-	14.6	-	nS
Source- Drain Diode Characteristics						
Source-drain current(Body Diode)	I _{SD}		-	-	80	A
Pulsed Source-drain current(Body Diode)	I _{SDM}		-	-	320	A
Forward on voltage ^(Note 1)	V _{SD}	Tj=25℃,I _{SD} =30A,V _{GS} =0V	-	-	1.2	V
Reverse Recovery Time ^(Note 1)	t _{rr}	Tj=25℃,I _F =75A,di/dt=100A/μs	-	-	36	nS
Reverse Recovery Charge ^(Note 1)	Q _{rr}		-	-	56	nC
Forward Turn-on Time	t _{on}	Intrinsic turn-on time is negligible(turn-on is dominated by L _S +L _D)				

Notes

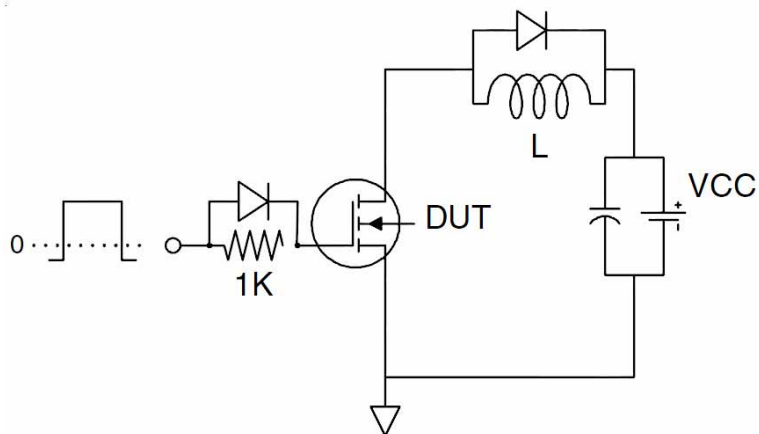
1. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 1.5\%$, $R_G=25\Omega$, Starting $T_J=25^{\circ}\text{C}$

Test Circuit

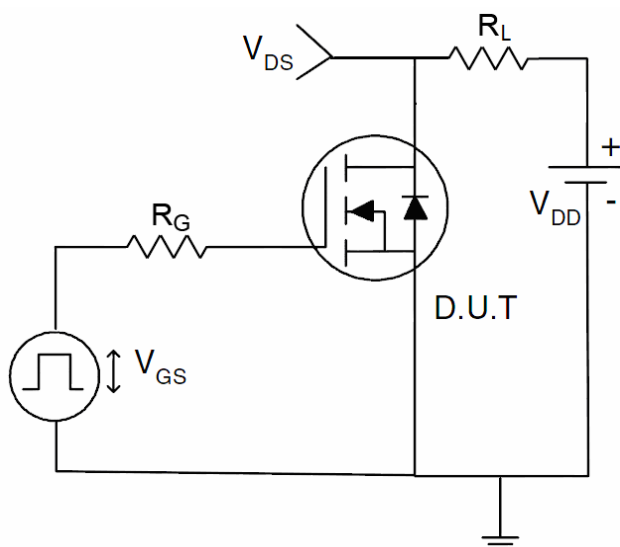
1) E_{AS} test circuit



2) Gate charge test circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (curves)

Figure1. Safe operating area

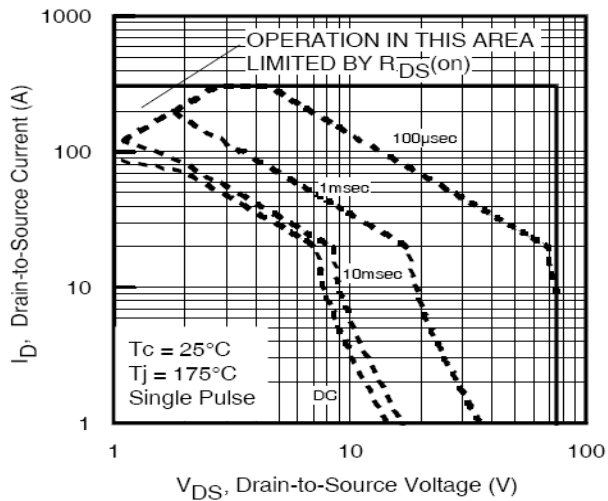


Figure2. Source-Drain Diode Forward Voltage

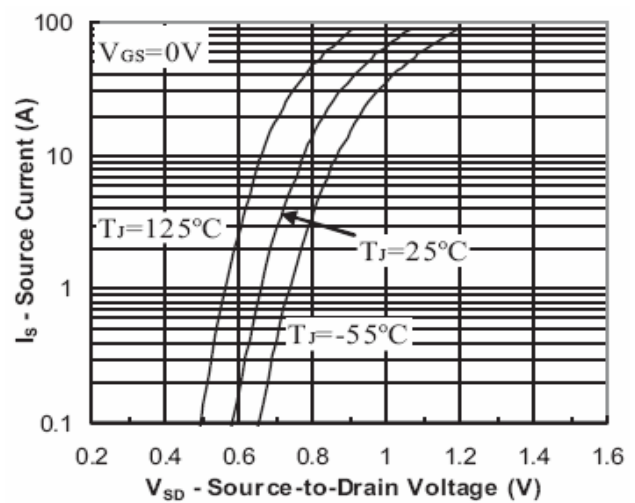


Figure3. Output characteristics

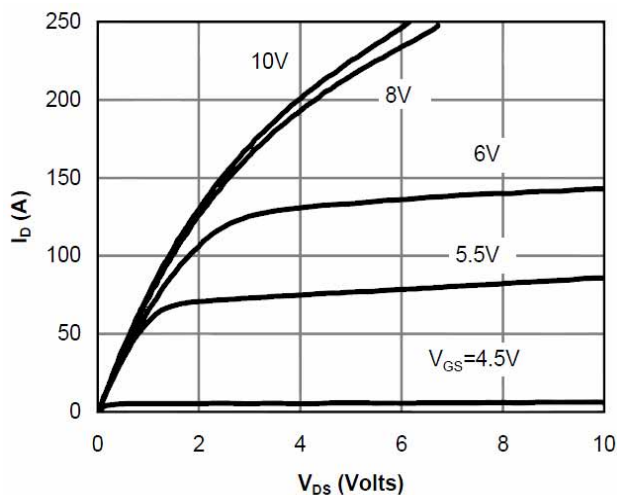


Figure4. Transfer characteristics

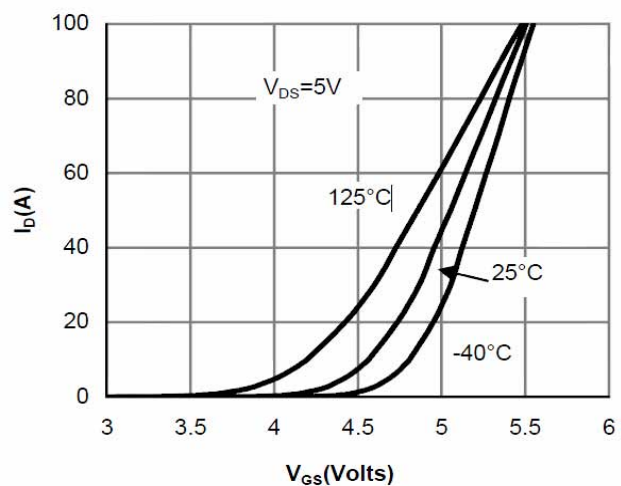


Figure5. Static drain-source on resistance

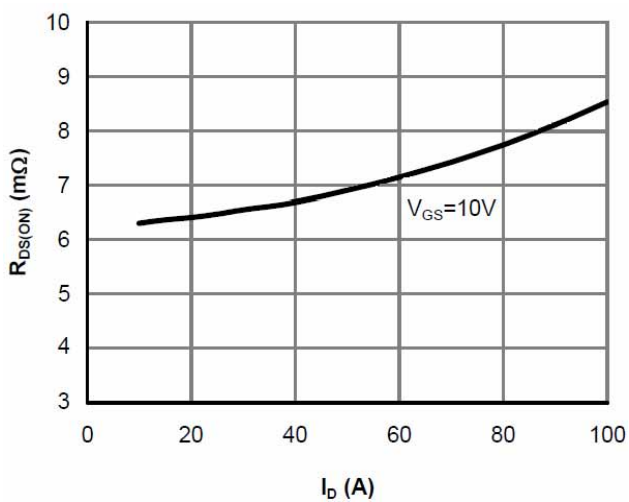


Figure6. $R_{DS(on)}$ vs Junction Temperature

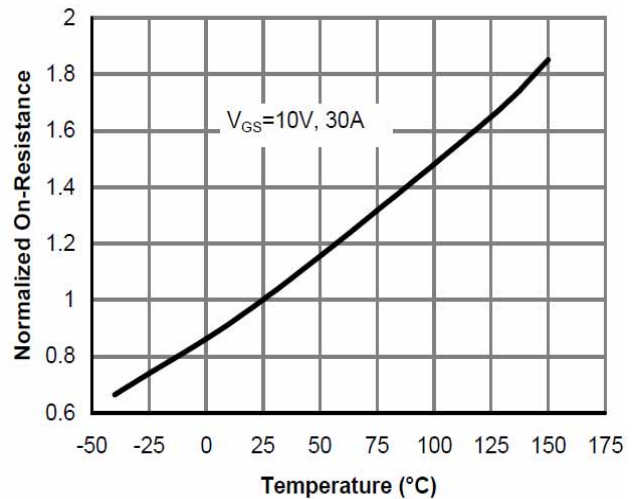


Figure7. BV_{DSS} vs Junction Temperature

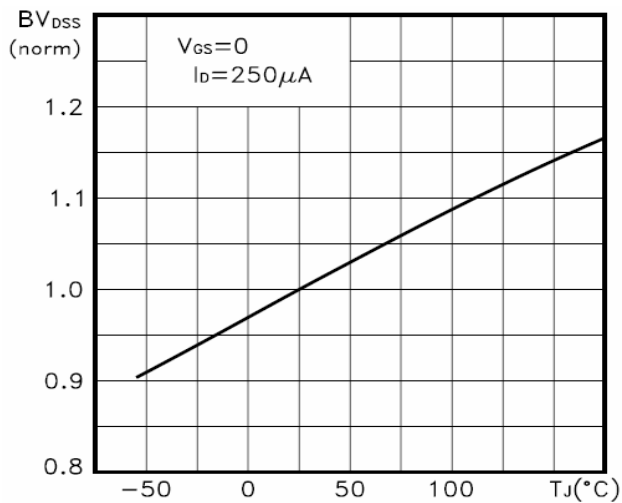


Figure8. $V_{GS(th)}$ vs Junction Temperature

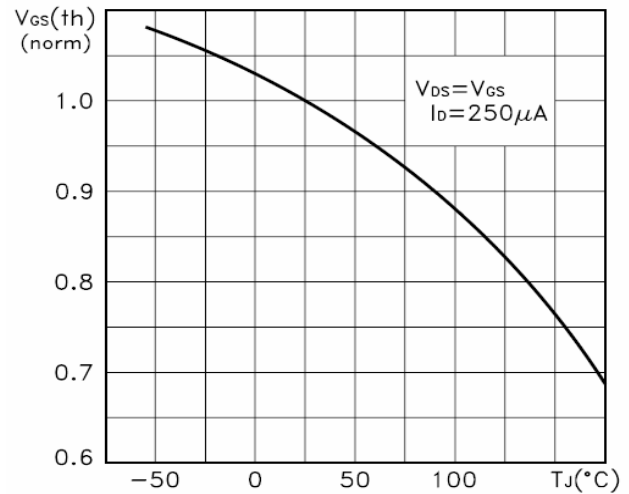


Figure9. Gate charge waveforms

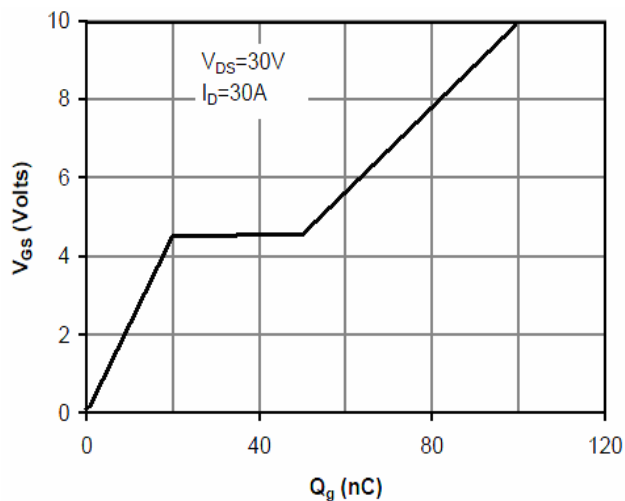


Figure10. Capacitance

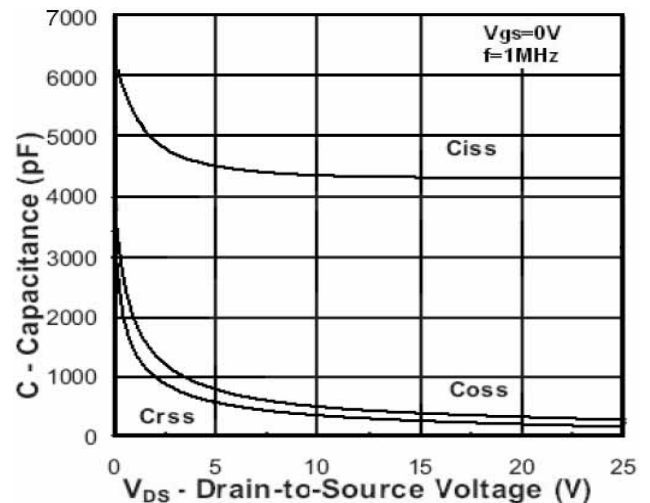
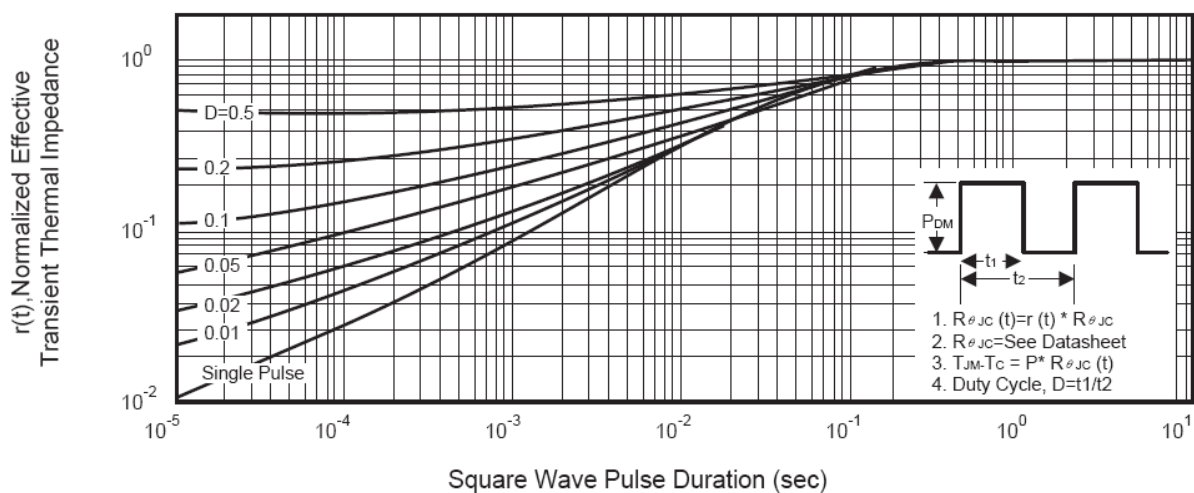
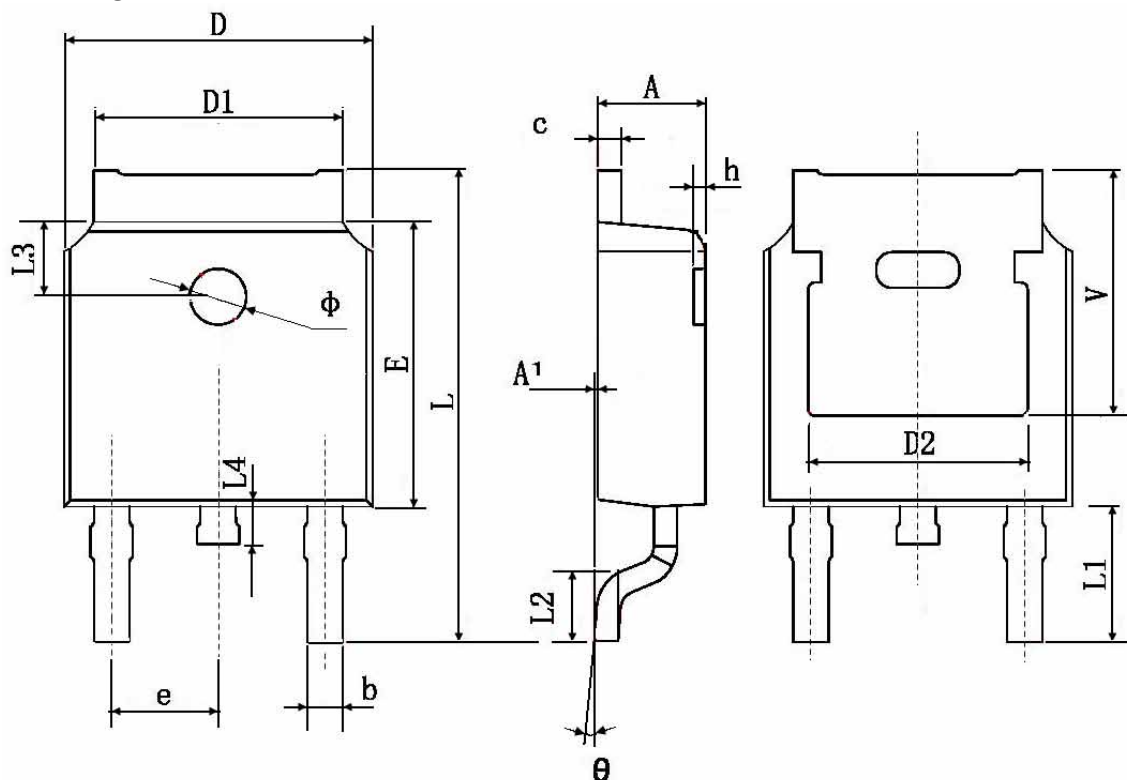


Figure11. Normalized Maximum Transient Thermal Impedance



TO-252 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	0.483 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	