

## 50V(D-S) N-Channel Enhancement Mode Power MOS FET

**General Features**

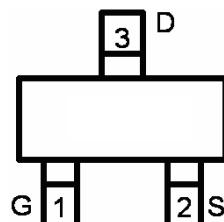
- $V_{DS} = 50V, I_D = 0.22A$
- $R_{DS(ON)} < 3\Omega @ V_{GS}=5V$
- $R_{DS(ON)} < 2\Omega @ V_{GS}=10V$
- Lead free product is acquired
- Surface mount package



Lead Free

**Application**

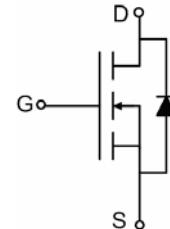
- Direct logic-level interface: TTL/CMOS
- Drivers: relays, solenoids, lamps, hammers , display, memories, transistors, etc.
- Battery operated systems
- Solid-state relays



Marking and pin assignment

**PIN Configuration**

SOT-23 top view



Schematic diagram

**Package Marking and Ordering Information**

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
	MSN138	SOT-23	Ø180mm	8 mm	3000 units

**Absolute Maximum Ratings ( $T_A=25^\circ C$  unless otherwise noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	50	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	0.22	A
Drain Current-Pulsed <sup>(Note 1)</sup>	$I_{DM}$	0.88	A
Maximum Power Dissipation	$P_D$	0.35	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	°C

**Thermal Characteristic**

Thermal Resistance, Junction-to-Ambient <sup>(Note 2)</sup>	$R_{\theta JA}$	350	°C/W
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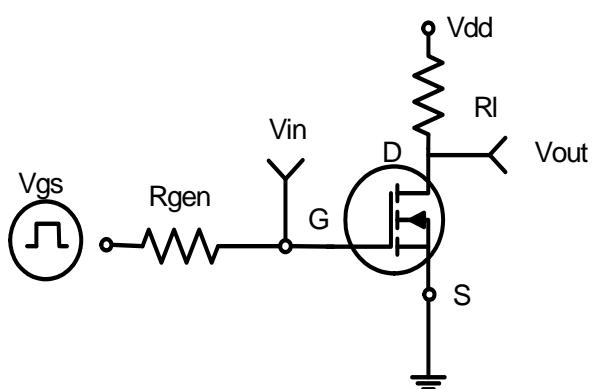
**Electrical Characteristics ( $T_A=25^\circ\text{C}$  unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$\text{BV}_{\text{DSS}}$	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	50	65	-	V
Zero Gate Voltage Drain Current	$I_{\text{DSS}}$	$V_{\text{DS}}=50\text{V}, V_{\text{GS}}=0\text{V}$	-	-	0.5	$\mu\text{A}$
Gate-Body Leakage Current	$I_{\text{GSS}}$	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	$\pm 100$	nA
<b>On Characteristics</b> <sup>(Note 3)</sup>						
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	0.8	1.2	1.6	V
Drain-Source On-State Resistance	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}}=5\text{V}, I_{\text{D}}=0.05\text{A}$	-	1.2	3	$\Omega$
		$V_{\text{GS}}=10\text{V}, I_{\text{D}}=0.5\text{A}$	-	1	2	$\Omega$
Forward Transconductance	$g_{\text{FS}}$	$V_{\text{DS}}=10\text{V}, I_{\text{D}}=0.2\text{A}$	0.12	-	-	S
<b>Dynamic Characteristics</b> <sup>(Note 4)</sup>						
Input Capacitance	$C_{\text{iss}}$	$V_{\text{DS}}=25\text{V}, V_{\text{GS}}=0\text{V}, F=1.0\text{MHz}$	-	27	-	PF
Output Capacitance	$C_{\text{oss}}$		-	12	-	PF
Reverse Transfer Capacitance	$C_{\text{rss}}$		-	6	-	PF
<b>Switching Characteristics</b> <sup>(Note 4)</sup>						
Turn-on Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}}=30\text{V}, I_{\text{D}}=0.22\text{A}$ $V_{\text{GS}}=10\text{V}, R_{\text{GEN}}=6\Omega$	-	2.5	-	nS
Turn-on Rise Time	$t_{\text{r}}$		-	6	-	nS
Turn-Off Delay Time	$t_{\text{d}(\text{off})}$		-	20	-	nS
Turn-Off Fall Time	$t_{\text{f}}$		-	7	-	nS
Total Gate Charge	$Q_{\text{g}}$	$V_{\text{DS}}=25\text{V}, I_{\text{D}}=0.3\text{A}, V_{\text{GS}}=10\text{V}$	-	1.7	2.4	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage <sup>(Note 3)</sup>	$V_{\text{SD}}$	$V_{\text{GS}}=0\text{V}, I_{\text{S}}=0.22\text{A}$	-	-	1.3	V
Diode Forward Current <sup>(Note 2)</sup>	$I_{\text{S}}$	-	-	-	0.22	A

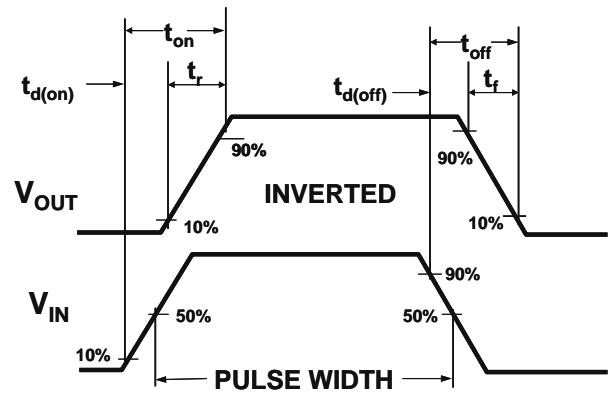
**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production

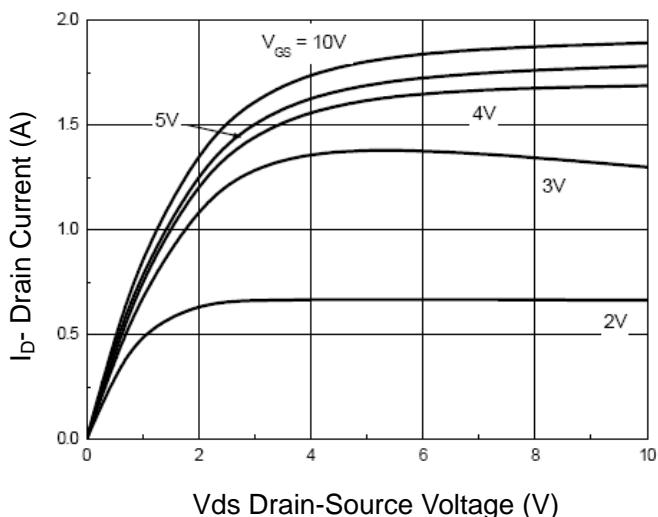
### Typical Electrical and Thermal Characteristics



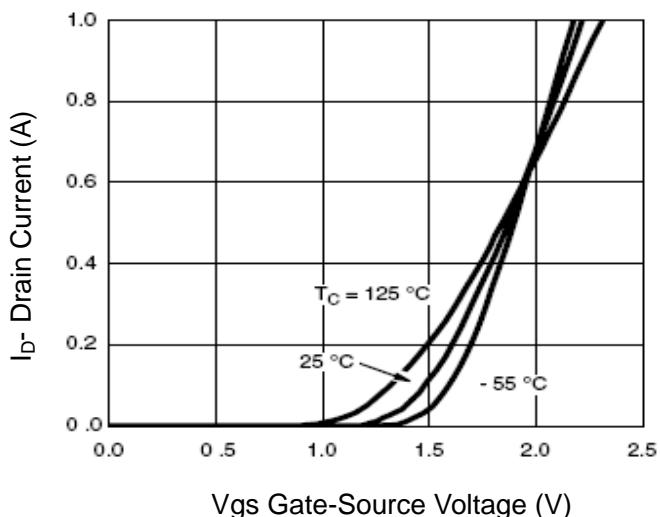
**Figure 1:Switching Test Circuit**



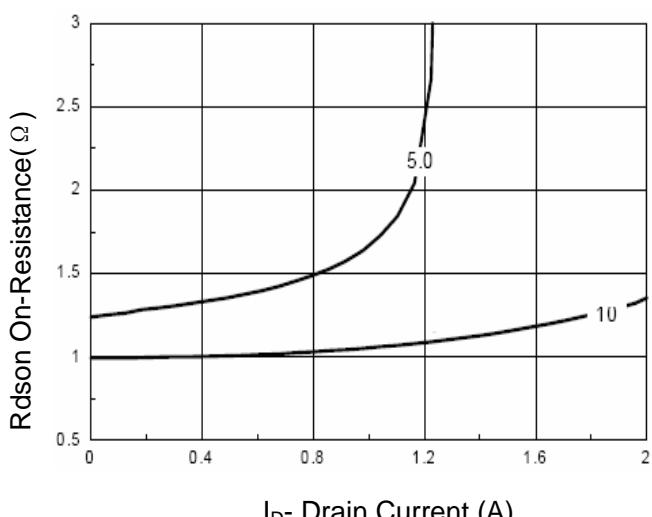
**Figure 2:Switching Waveforms**



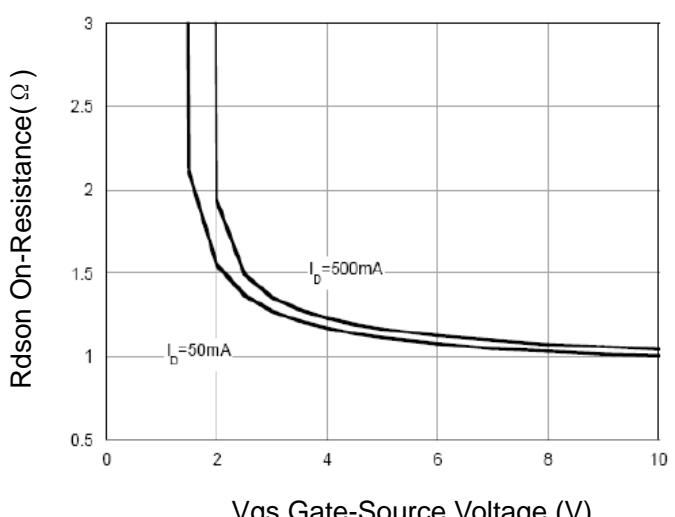
**Figure 3 Output Characteristics**



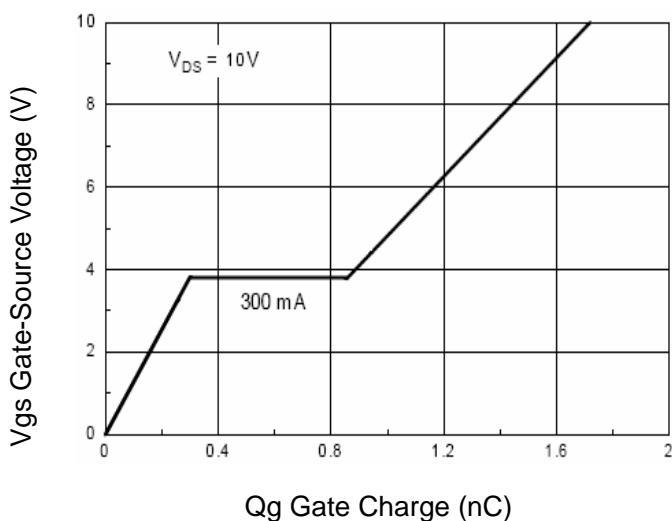
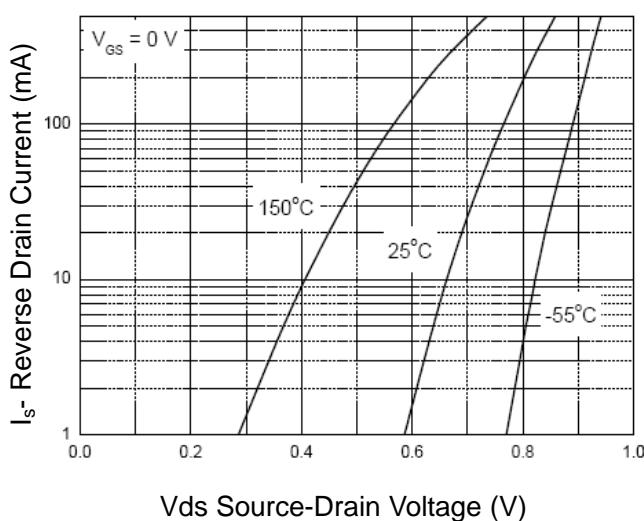
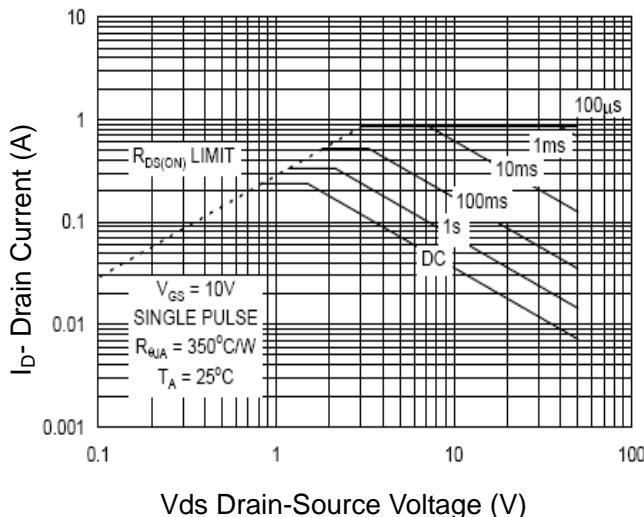
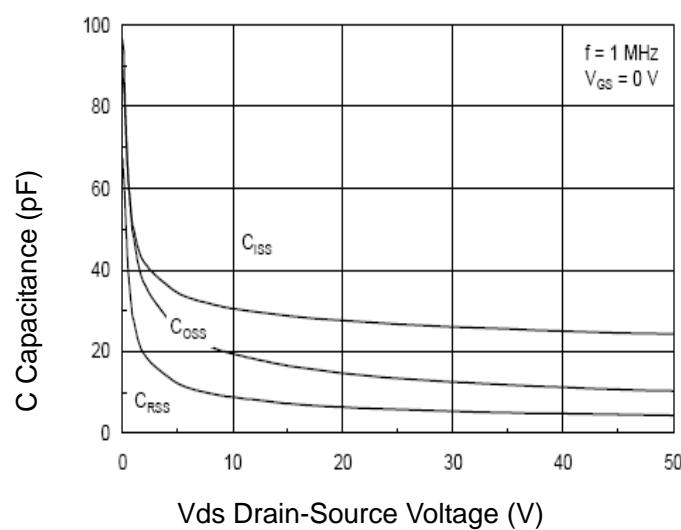
**Figure 4 Transfer Characteristics**

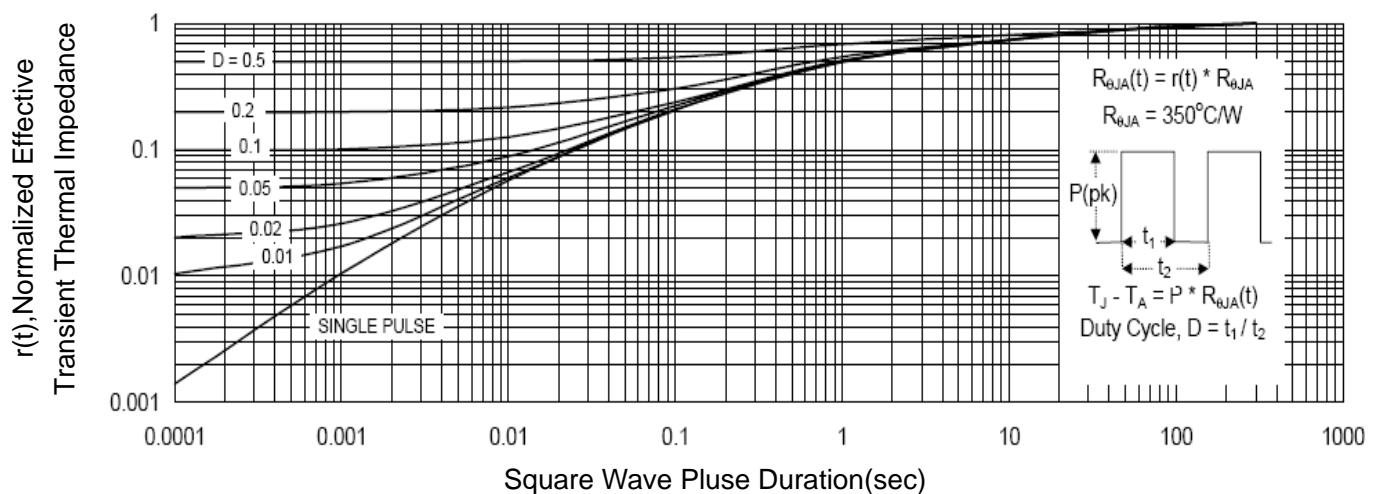


**Figure 5 Drain-Source On-Resistance**



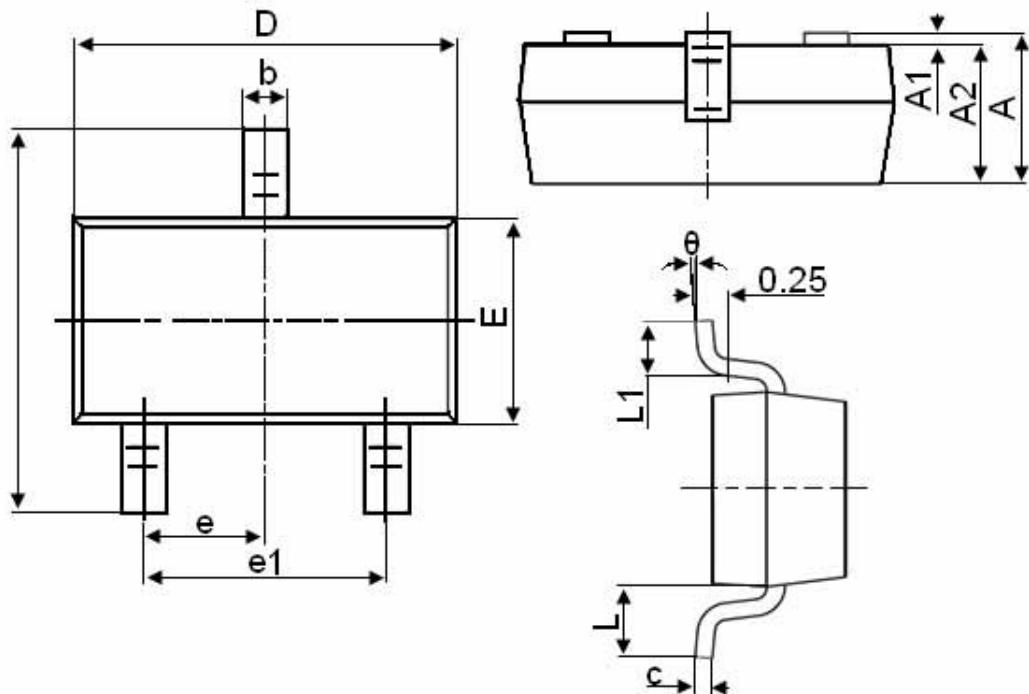
**Figure 6 Rdson vs Vgs**

**Figure 7 Gate Charge****Figure 8 Source-Drain Diode Forward****Figure 10 Safe Operation Area****Figure 11 Capacitance vs Vds**



**Figure 12 Normalized Maximum Transient Thermal Impedance**

## SOT-23 Package Information



Symbol	Dimensions in Millimeters	
	MIN.	MAX.
A	0.900	1.150
A1	0.000	0.100
A2	0.900	1.050
b	0.300	0.500
c	0.080	0.150
D	2.800	3.000
E	1.200	1.400
E1	2.250	2.550
e	0.950TYP	
e1	1.800	2.000
L	0.550REF	
L1	0.300	0.500
θ	0°	8°

## Notes

1. All dimensions are in millimeters.
2. Tolerance  $\pm 0.10\text{mm}$  (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.