700V(D-S) N-Channel Enhancement Mode Power MOS FET

General Features

- V_{DS} =700V,I_D =2A

    $R_{DS(ON)}$ <6.5 Ω @ V_{GS}=10V

- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
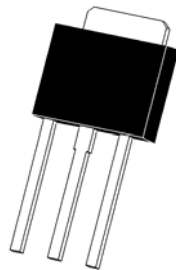- Special process technology for high ESD capability

Application

- Power switching application
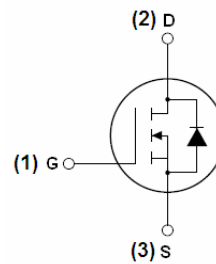- Hard switched and high frequency circuits
- Electronic ballast and transformer

Lead Free
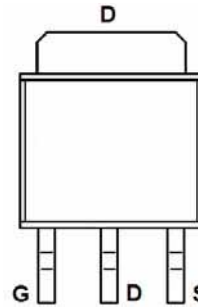
Marking and pin assignment

PIN Configuration

TO-251 top view

Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MSN7002Z	MSN7002Z	TO-251	-	-	-

Absolute Maximum Ratings (T$_C$=25℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	700	V
Gate-Source Voltage	V_{GS}	±30	V
Drain Current-Continuous	I_D	2	A
Drain Current-Continuous(T$_C$=100℃)	I_D (100℃)	1.25	A
Pulsed Drain Current	I_{DM}	8	A
Maximum Power Dissipation	P_D	28	W
Derating factor		0.20	W/℃
Single pulse avalanche energy [Note 5]	E_{AS}	120	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case[Note 2]	$R_{\theta JC}$	4.46	℃/W

Electrical Characteristics (T$_C$=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250µA	700	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=700V,V_{GS}=0V	-	-	25	µA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±30V,V_{DS}=0V	-	-	±100	nA
On Characteristics [(Note 3)]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250µA	2	-	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=1.0A	-	5.5	6.5	Ω
Forward Transconductance	g_{FS}	V_{DS}=40V,I_D=1.0A	-	1.5	-	S
Dynamic Characteristics [(Note4)]						
Input Capacitance	C_{Iss}	V_{DS}=25V,V_{GS}=0V, F=1.0MHz	-	290	-	PF
Output Capacitance	C_{oss}		-	31	-	PF
Reverse Transfer Capacitance	C_{rss}		-	9	-	PF
Switching Characteristics [(Note 4)]						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=300V,I_D=2A,R_L=25Ω V_{GS}=10V,R_G=2.5Ω	-	10	-	nS
Turn-on Rise Time	t_r		-	25	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	24	-	nS
Turn-Off Fall Time	t_f		-	26	-	nS
Total Gate Charge	Q_g	V_{DS}=560V,I_D=2A, V_{GS}=10V	-	14.5		nC
Gate-Source Charge	Q_{gs}		-	1.8		nC
Gate-Drain Charge	Q_{gd}		-	8.3		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage [(Note 3)]	V_{SD}	V_{GS}=0V,I_S=2.0A	-		1.4	V
Diode Forward Current [(Note 2)]	I_S		-	-	2.0	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF = 2.0A di/dt = 100A/µs[(Note3)]	-	380		nS
Reverse Recovery Charge	Q_{rr}		-	0.9		µC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.

2. Surface Mounted on FR4 Board, t ≤ 10 sec.

3. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2%.

4. Guaranteed by design, not subject to production

5. E_{AS} condition: j=25℃,V_{DD}=50V,V_G=10V,L=0.5mH,Rg=25Ω

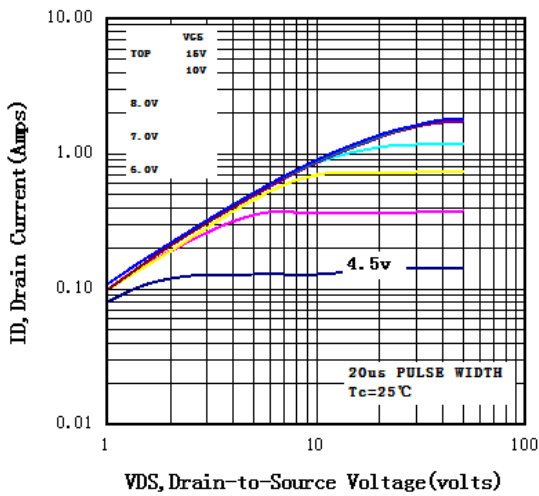## Typical Electrical and Thermal Characteristics (Curves)

Fig1 Typical Output Characteristics, Tc=25℃

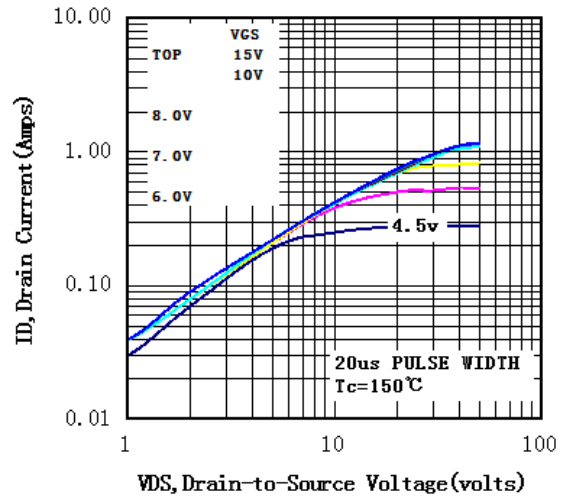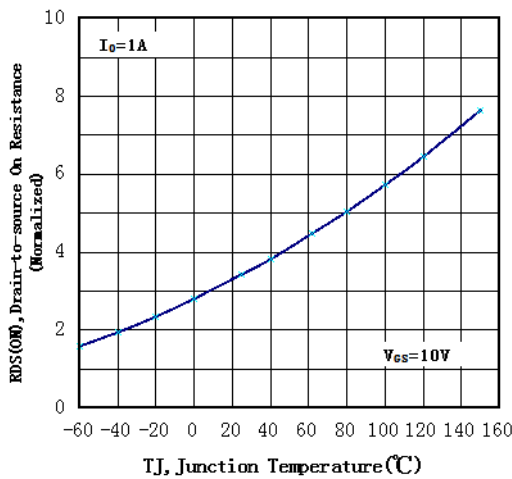
Fig2 Typical Output Characteristics, Tc=150℃

Fig3 Normalized Resistance Vs. Temperature
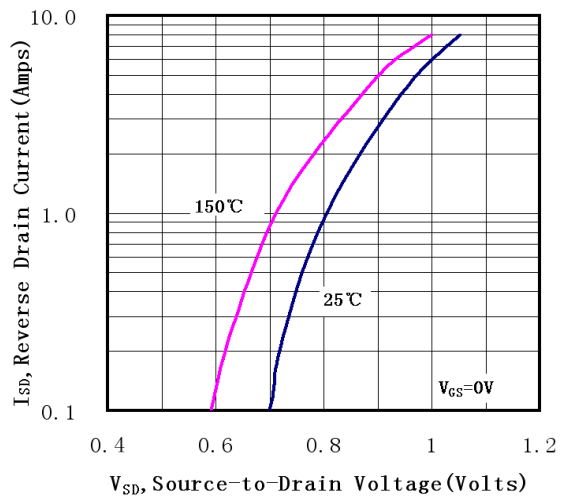

Fig4 Typical Source-Drain Diode Forward Voltage

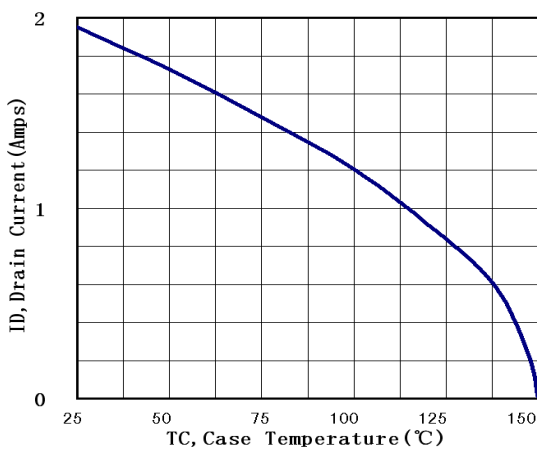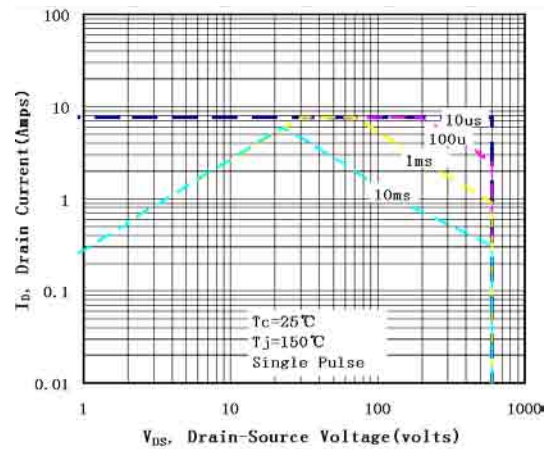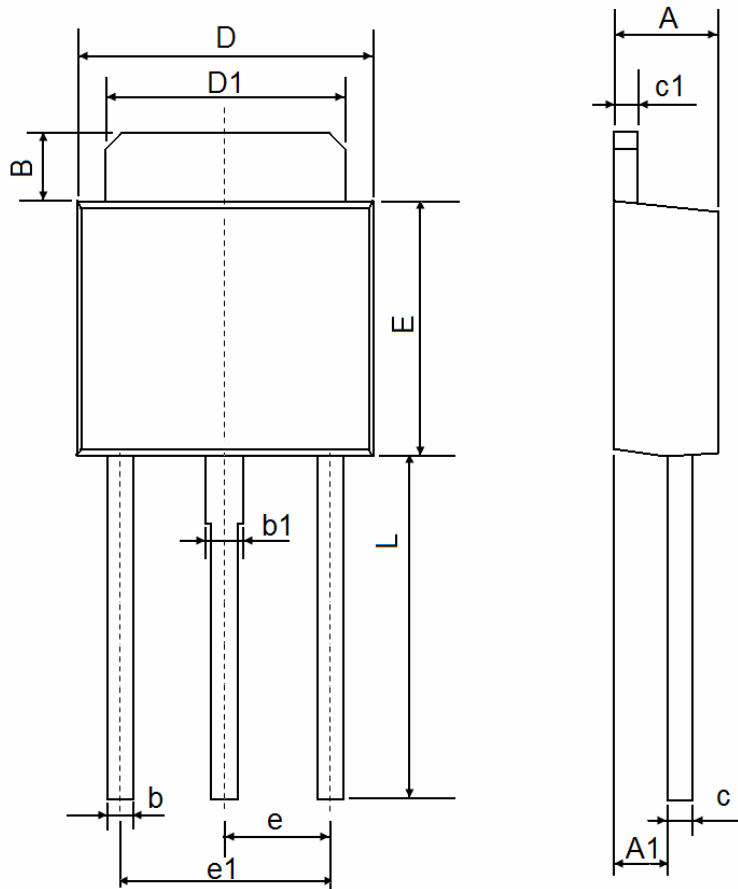Fig5 Maximum Drain Current Vs. Case Temperature

Fig6 Maximum Safe Operating Area

TO-251 Package Information

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	1.050	1.350	0.042	0.054
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300 TYP		0.091 TYP	
e1	4.500	4.700	0.177	0.185
L	7.500	7.900	0.295	0.311