

**-30V(D-S) P-Channel Enhancement Mode Power MOS FET**

**General Features**

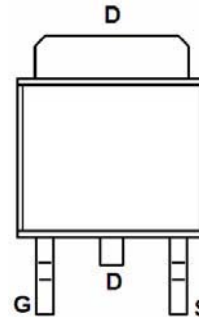
- $V_{DS} = -30V, I_D = -15A$   
 $R_{DS(ON)} < 54m\Omega @ V_{GS} = -10V$   
 $R_{DS(ON)} < 82m\Omega @ V_{GS} = -4.5V$
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation



**Lead Free**

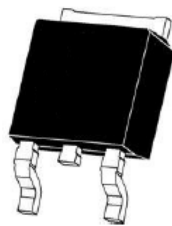
**Application**

- High side switch for full bridge converter
- DC/DC converter for LCD display
- Power Management in Portable Equipment and BPS

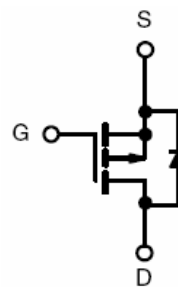


**Marking and pin assignment**

**PIN Configuration**



**TO-252-2L top view**



**Schematic diagram**

**Package Marking and Ordering Information**

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MSP0315D	MSP0315D	TO-252-2L	-	-	2500PCS

**Absolute Maximum Ratings ( $T_C = 25^\circ C$  unless otherwise noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	-15	A
Drain Current-Continuous( $T_C = 100^\circ C$ )	$I_D(100^\circ C)$	-10.5	A
Pulsed Drain Current	$I_{DM}$	-45	A
Maximum Power Dissipation	$P_D$	2.5	W
Derating factor		0.4	W/ $^\circ C$
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	40	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^\circ C$

**Thermal Characteristic**

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	2.5	°C/W
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**Electrical Characteristics ( $T_C=25^\circ\text{C}$  unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-30	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-24V, V_{GS}=0V$	-	-	-1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics <sup>(Note 3)</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0	-1.5	-2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-50A$	-	43	54	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=-5V, I_D=-1A$	-	5	-	S
<b>Dynamic Characteristics <sup>(Note 4)</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS}=-15V, V_{GS}=0V,$ $F=1.0MHz$	-	782	-	PF
Output Capacitance	$C_{oss}$		-	125	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	86	-	PF
<b>Switching Characteristics <sup>(Note 4)</sup></b>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-15V, I_D=-1A,$ $V_{GS}=-10V, R_{GEN}=3\Omega$	-	9	-	nS
Turn-on Rise Time	$t_r$		-	10	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	38	-	nS
Turn-Off Fall Time	$t_f$		-	23	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=-15V, I_D=-1A, V_{GS}=-10V$	-	11	-	nC
Gate-Source Charge	$Q_{gs}$		-	2.1	-	nC
Gate-Drain Charge	$Q_{gd}$		-	2.9	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage <sup>(Note 3)</sup>	$V_{SD}$	$V_{GS}=0V, I_S=-1.7A$	-	-	-1.2	V

**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5.  $E_{AS}$  condition:  $T_J=25^\circ C, V_{DD}=-15V, V_G=-10V, L=0.5mH, R_g=25\Omega, I_{AS}=-26A$

Test Circuit

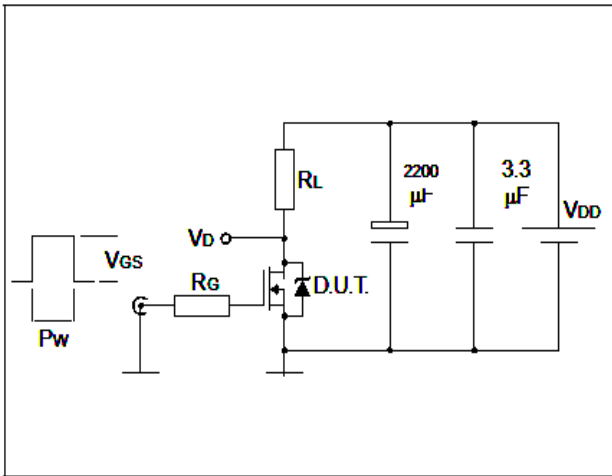


Figure 1. Switching times test circuit for Resistive load

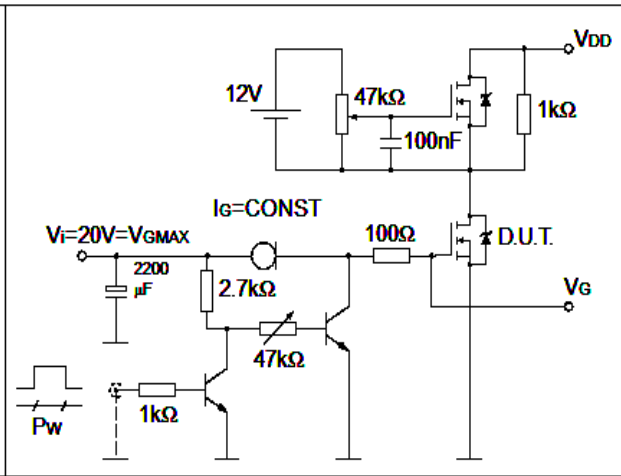


Figure 2. Gate charge test circuit

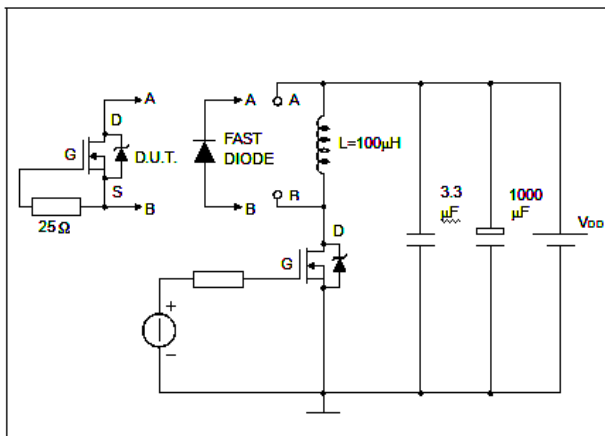


Figure 3. Test circuit for inductive load and diode recovery times

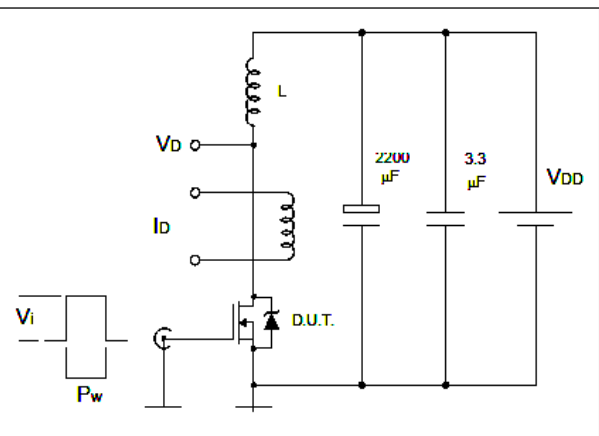


Figure 4. Unclamped Inductive load test circuit switching

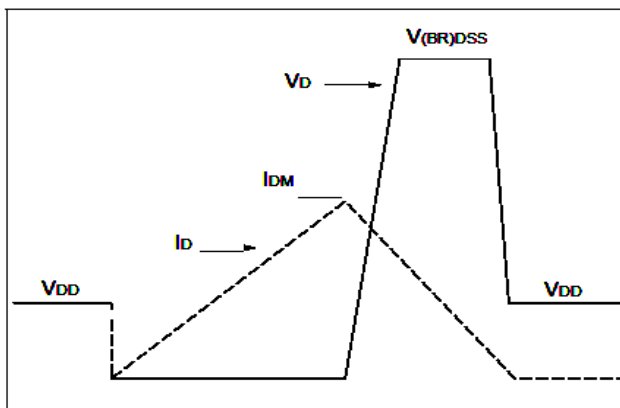


Figure 5. Unclamped inductive waveform

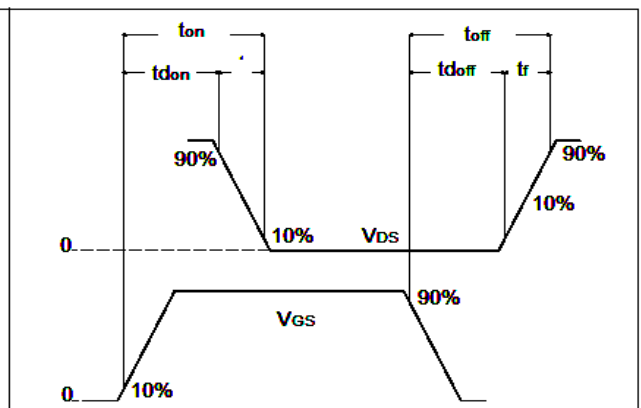


Figure 6. Switching time waveform

Typical Electrical and Thermal Characteristics (Curves)

Figure 1. Output Characteristics

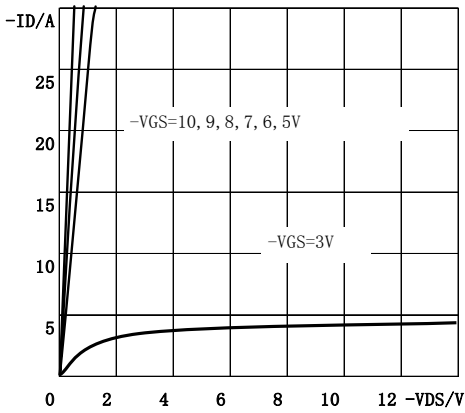


Figure 2. Transfer Characteristics

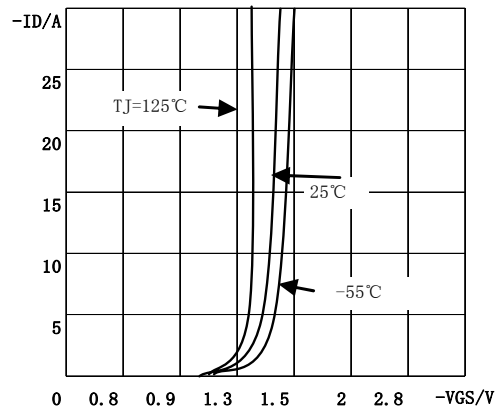


Figure 3. Capacitance variations

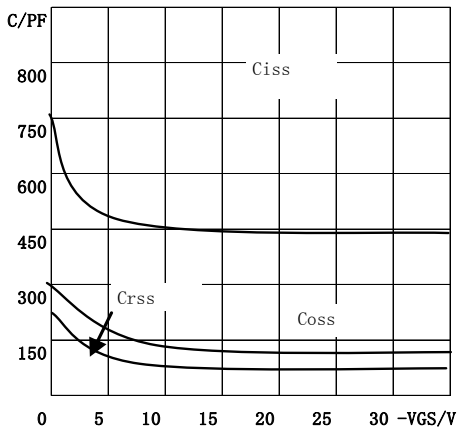


Figure 4. On-Resistance Variation with Temperature

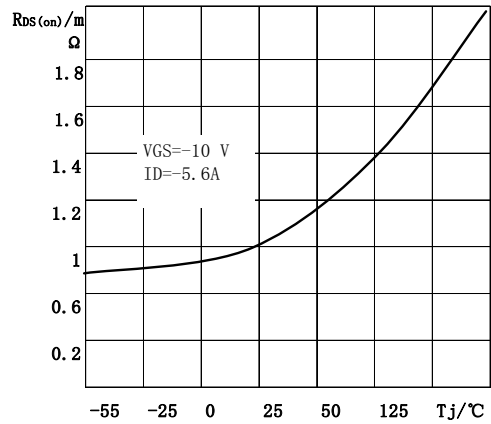


Figure 5. Gate Threshold Variation with Temperatures

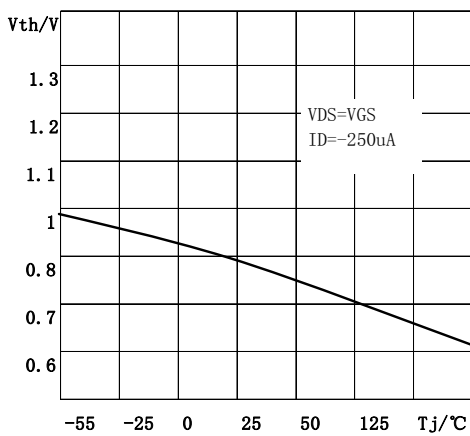


Figure 6. Breakdown Voltage Variation with temperatures

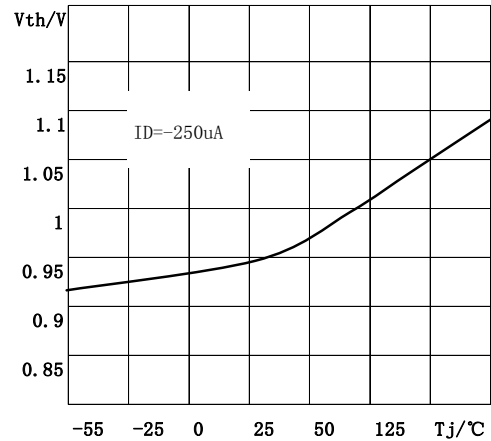


Figure7. Transconductance Variation With Drain Current

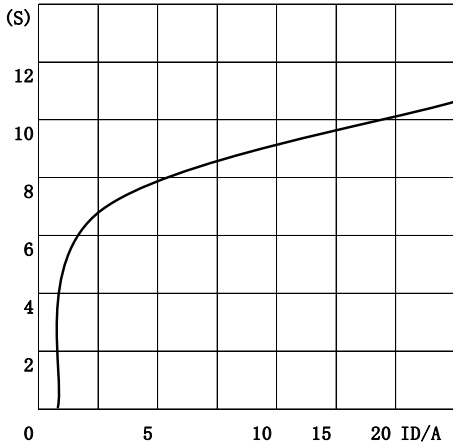


Figure8. Body Diode Forward Voltage Variation with Source Current

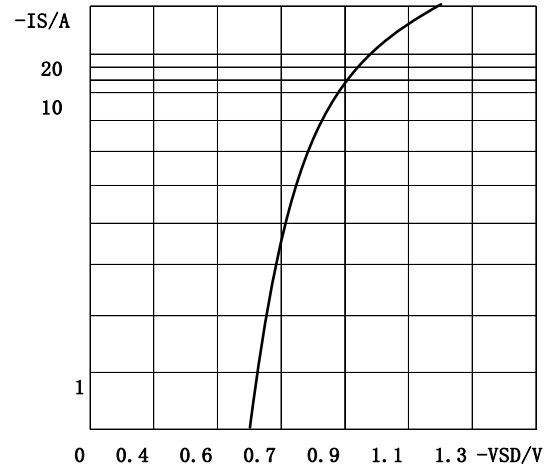


Figure9. Gate charge VS. Gate-source Voltage

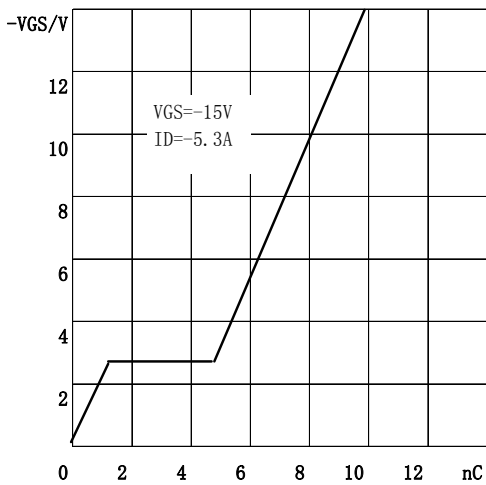
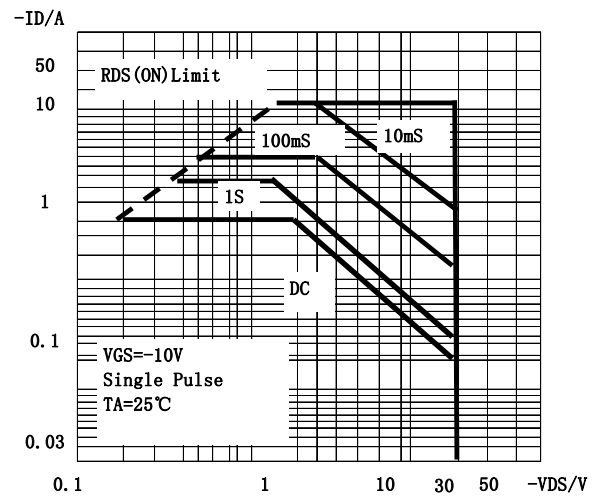
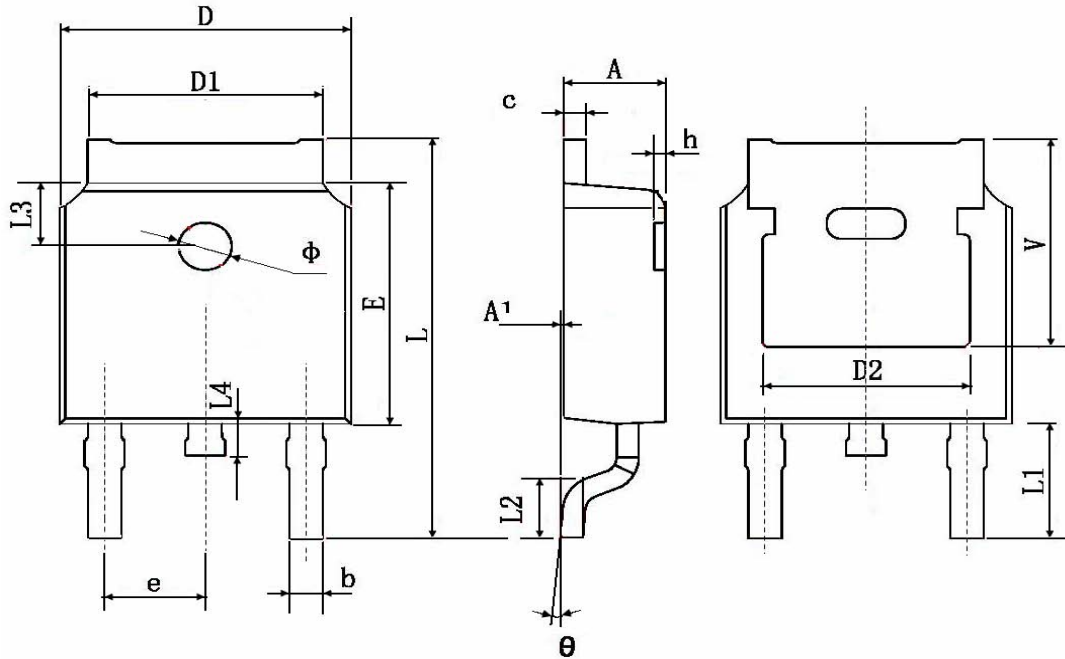


Figure10. Maximum Safe Operating Area



TO-252 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
$\Phi$	1.100	1.300	0.043	0.051
$\theta$	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	