Maplesemi

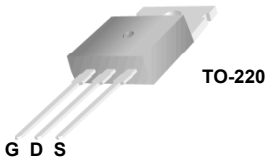
MSP120N08G
80V N-Channel MOSFET

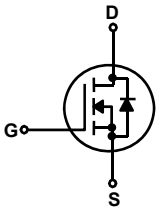
General Description

This Power MOSFET is produced using Maple semi's advanced technology.
which provides high performance in on-state resistance, fast switching performance and excellent quality.
MSP120N08G suitable device forSynchronous Rectification For Server and general purpose applications.

Features

- 120A, 80V, $R_{DS(TYP)}$ = 5.5mΩ@V_{GS} = 10 V
- Low gate charge (typical 59 nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability





Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	MSP120N08G	Units
V_{DSS}	Drain-Source Voltage	80	V
I_D	Drain Current - Continuous (T_C = 25℃)	120	A
	- Continuous (T_C = 100℃)	67	A
I_{DM}	Drain Current - Pulsed (Note 1)	420	A
V_{GSS}	Gate-Source Voltage	±20	V
EAS	Single Pulsed Avalanche Energy (Note 2)	144.5	mJ
I_{AR}	Avalanche Current (Note 1)	120	A
P_D	Power Dissipation (T_C = 25℃)	157	W
	- Derate above 25℃	1.26	W/℃
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	℃
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	℃

* Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	MSP120N08G	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.8	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	℃/W

Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 uA	80	--	--	V
$\triangle BV_{DSS}$ / $\triangle T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 uA, Referenced to 25℃	--	0.1	--	V/℃
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 64 V, V_{GS} = 0 V	--	--	1	uA
		V_{DS} = 64 V, T_C = 125℃	--	--	10	uA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 20 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 uA	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 60A	--	5.5	7.0	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 60 A (Note 3)	--	47	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 40 V, V_{GS} = 0 V, f = 1.0 MHz	--	3841	--	pF
C_{oss}	Output Capacitance		--	34	--	
C_{rss}	Reverse Transfer Capacitance		--	652	--	
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{Ds} = 40 V, I_D = 60 A, R_G = 3.0 Ω (Note3, 4)	--	15.6	--	ns
t_r	Turn-On Rise Time		--	32.7	--	
$t_{d(off)}$	Turn-Off Delay Time		--	24.2	--	
t_f	Turn-Off Fall Time		--	15.1	--	
Q_g	Total Gate Charge	V_{DS} = 40 V, I_D = 60 A, V_{GS} = 10 V (Note 3, 4)	--	59.4	--	nC
Q_{gs}	Gate-Source Charge		--	16.5	--	
Q_{gd}	Gate-Drain Charge		--	12.3	--	
Drain-Source Diode Characteristics and Maximum Ratings						
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 60 A	--	0.9	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 60 A, dI_F / dt = 100 A/us (Note 3)	--	64.3	--	ns
Q_{rr}	Reverse Recovery Charge		--	152.7	--	uC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. I_{AS} = 17A,L=1.0mH,V_{GS} = 10V, Starting T_J = 25°C
3. Pulse Test : Pulse width ≤ 300us, Duty cycle ≤ 2%
4. Essentially independent of operating temperature

Typical Characteristics

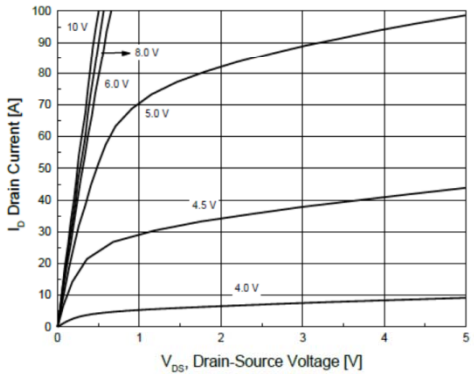


Figure 1. On-Region Characteristics

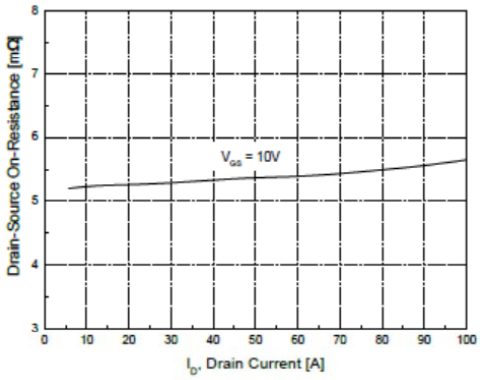


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

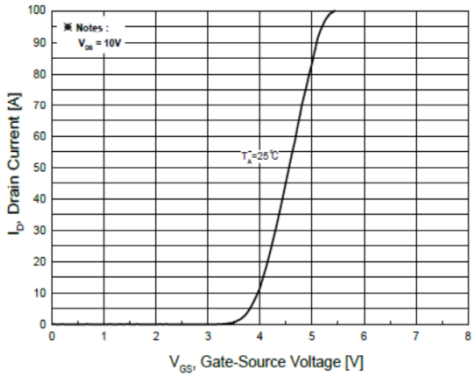


Figure 3. Transfer Characteristics

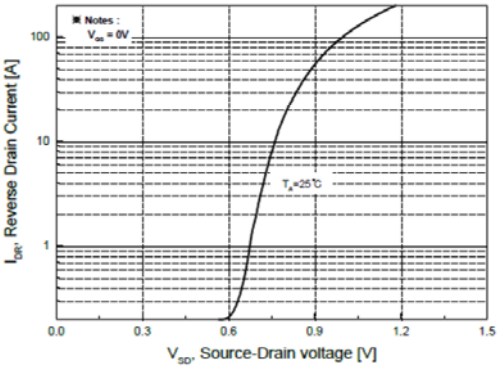


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

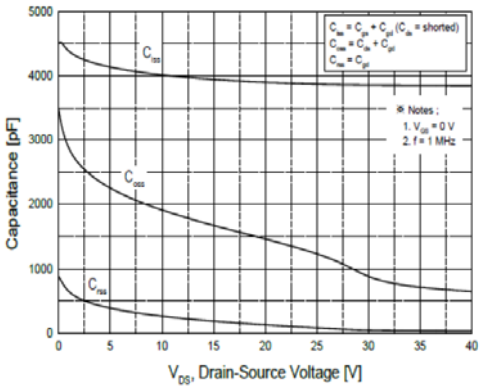


Figure 5. Capacitance Characteristics

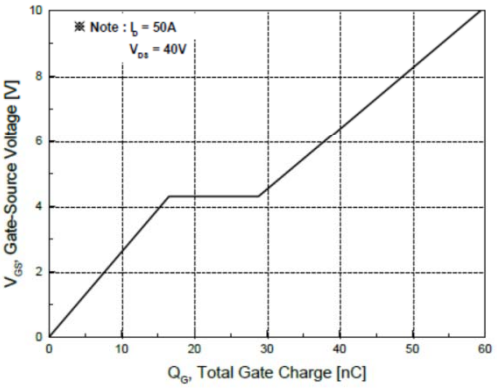


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

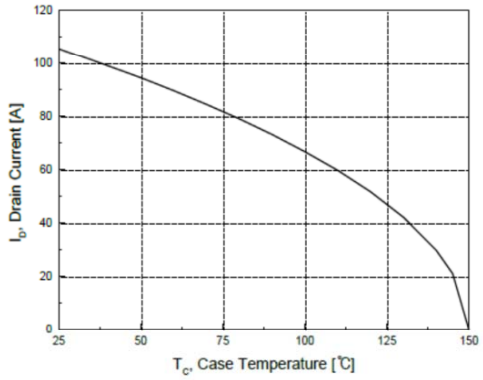


Figure 7. Maximum Drain Current VS Case Temperature

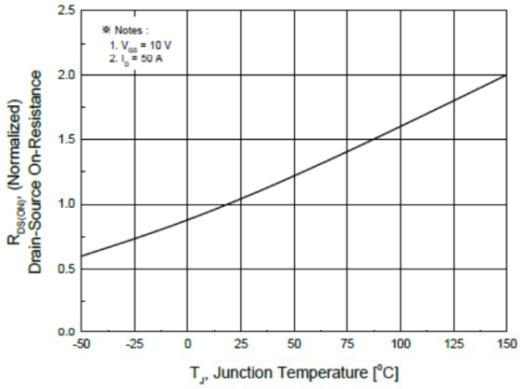


Figure 8. On-Resistance Variation vs Temperature

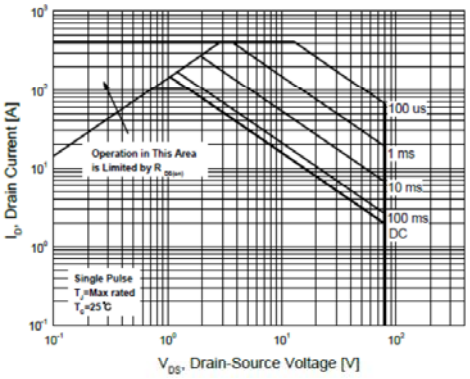


Figure 9. Maximum Safe Operating Area

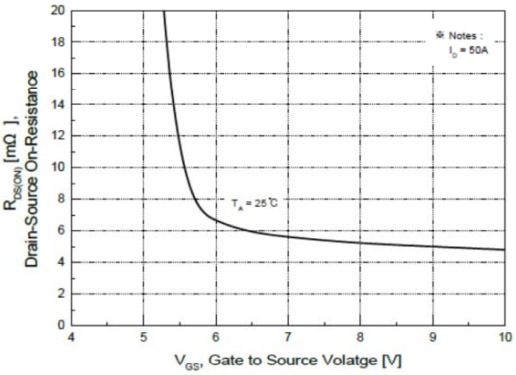


Figure 10.On-Resistance Variation with Gate to Source Voltage

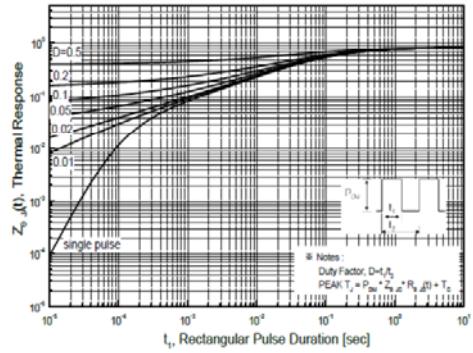
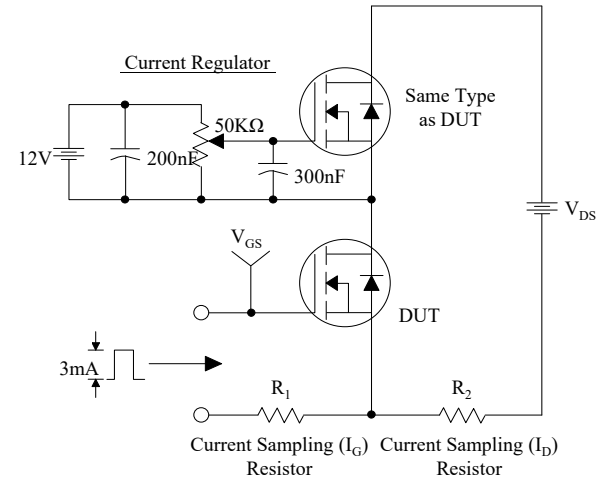
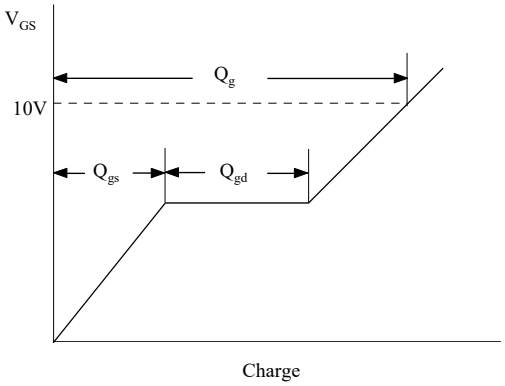


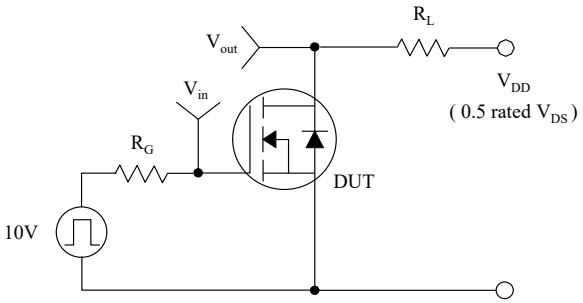
Figure 11.Transient Thermal Response Curve

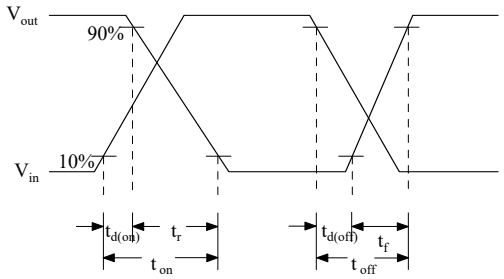
Gate Charge Test Circuit & Waveform



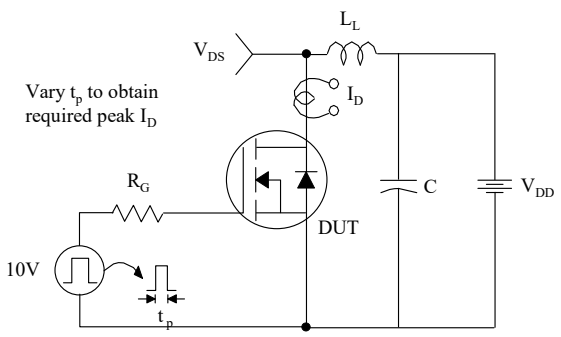


Resistive Switching Test Circuit & Waveforms

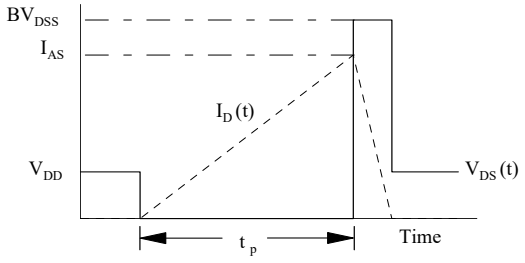




Unclamped Inductive Switching Test Circuit & Waveforms



$$E_{AS} = \frac{1}{2} L_L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



Peak Diode Recovery dv/dt Test Circuit & Waveforms