MORESEMI

MSP3401L

-30V(D-S) P-Channel Enhancement Mode Power MOS FET

General Features

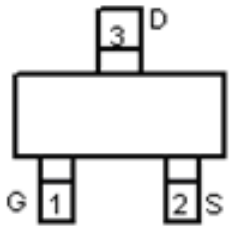
- V_{DS} = -30V,I_D = -4.2A
  $R_{DS(ON)}$ < 130mΩ @ V_{GS}=-2.5V
  $R_{DS(ON)}$ < 75mΩ @ V_{GS}=-4.5V
  $R_{DS(ON)}$ < 55mΩ @ V_{GS}=-10V
- High power and current handing capability
- Lead free product is acquired
- Surface mount package

RoHS Compliant

Lead Free

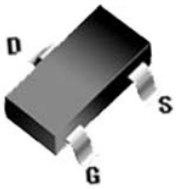
Application

- PWM applications
- Load switch
- Power management

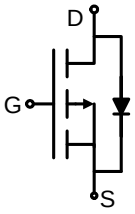


Marking and pin Assignment

PIN Configuration



SOT-23-3L top view



Schematic diagram

Package Marking And Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
	MSP3401L	SOT-23-3L	Ø180mm	8 mm	3000 units

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	±12	V
Drain Current-Continuous	I_D	-4.2	A
Drain Current-Pulsed (Note 1)	I_{DM}	-30	A
Maximum Power Dissipation	P_D	1.2	W
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Ambient (Note 2)	$R_{\theta JA}$	104	℃/W

Electrical Characteristics (TA=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=-250μA	-30		-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-24V,V_{GS}=0V	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±10V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-0.7	-1	-1.3	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-4.2A	-	47	55	mΩ
		V_{GS}=-4.5V, I_D=-4A	-	56	75	mΩ
		V_{GS}=-2.5V, I_D=-1A		72	130	mΩ
Forward Transconductance	g_{FS}	V_{DS}=-5V,I_D=-4.2A	-	10	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=-15V,V_{GS}=0V, F=1.0MHz	-	880	-	PF
Output Capacitance	C_{oss}		-	105	-	PF
Reverse Transfer Capacitance	C_{rss}		-	65	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=-15V,I_D=-4.2A V_{GS}=-10V,R_{GEN}=6Ω	-	7	-	nS
Turn-on Rise Time	t_r		-	3	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	30	-	nS
Turn-Off Fall Time	t_f		-	12	-	nS
Total Gate Charge	Q_g	V_{DS}=-15V,I_D=-4.2A,V_{GS}=-4.5V	-	8.5	-	nC
Gate-Source Charge	Q_{gs}		-	1.8	-	nC
Gate-Drain Charge	Q_{gd}		-	2.7	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=-4.2A	-	-	-1.2	V

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

Typical Electrical and Thermal Characteristics

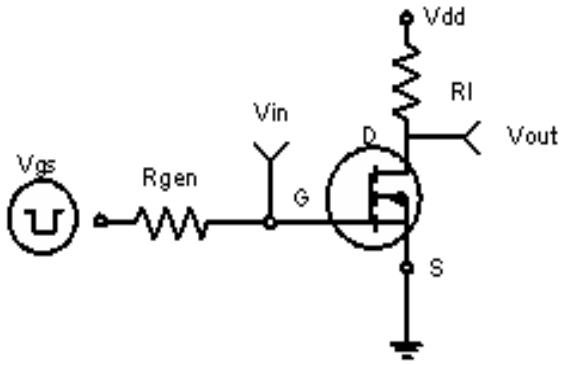


Figure 1:Switching Test Circuit

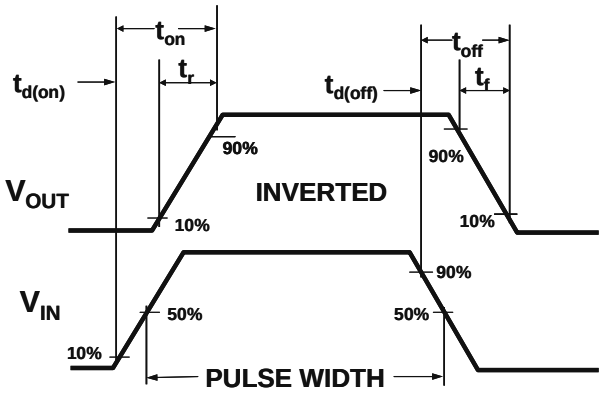
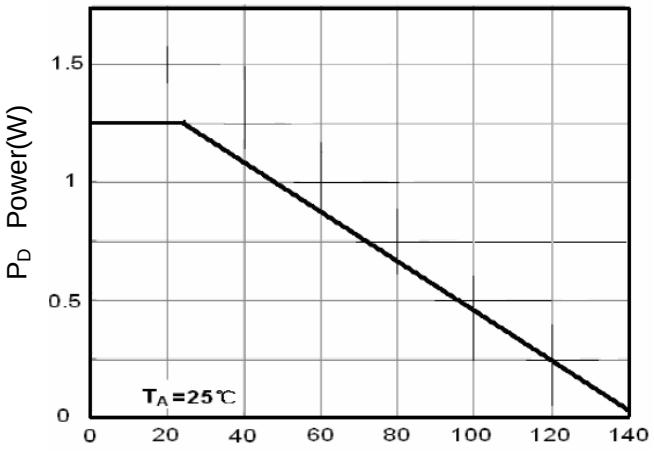
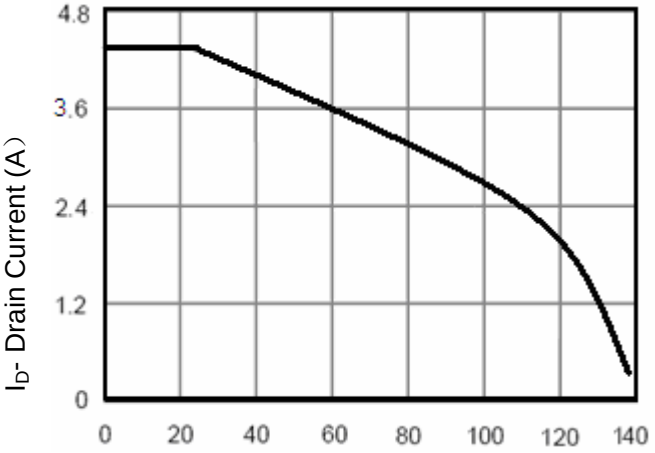


Figure 2:Switching Waveforms



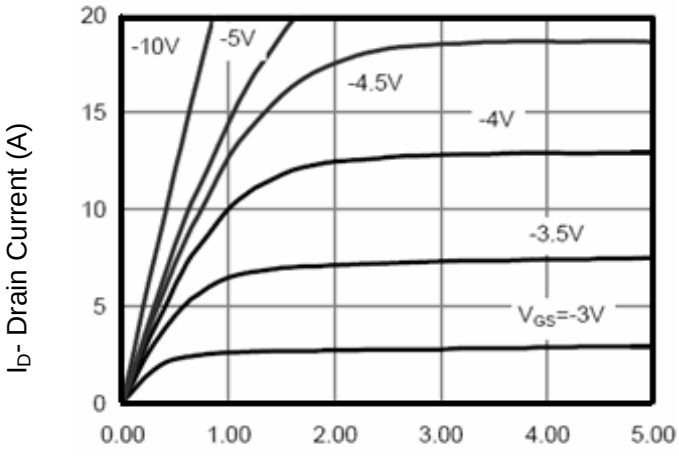
T_J-Junction Temperature(℃)

Figure 3 Power Dissipation



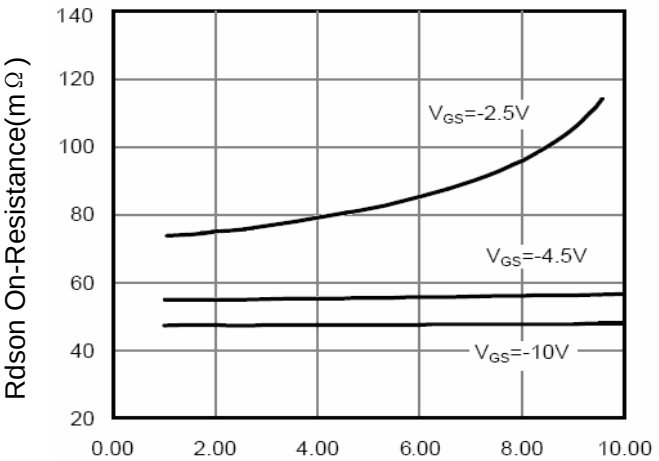
T_J-Junction Temperature(℃)

Figure 4 Drain Current



Vds Drain-Source Voltage (V)

Figure 5 Output Characteristics



I_D- Drain Current (A)

Figure 6 Drain-Source On-Resistance

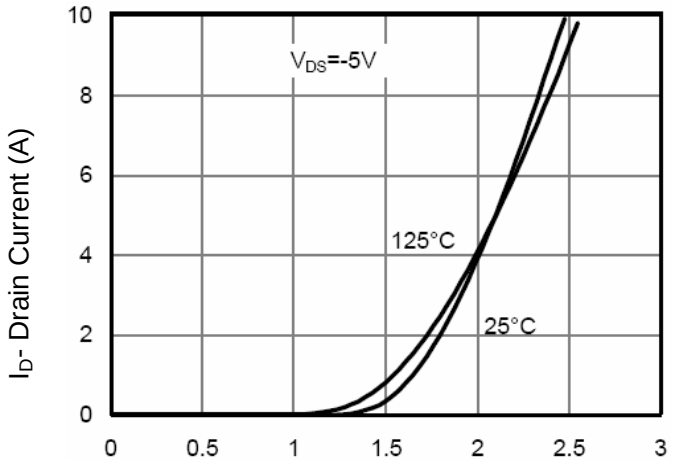


Figure 7 Transfer Characteristics

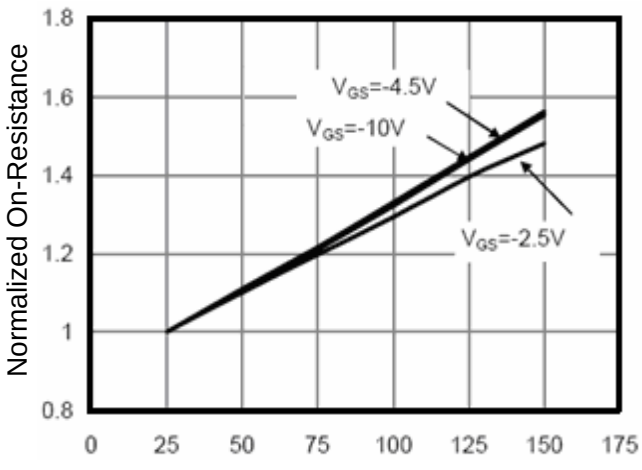


Figure 8 Drain-Source On-Resistance

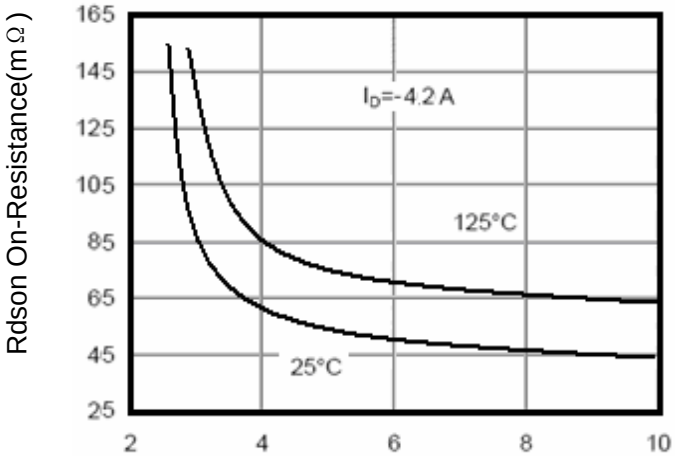


Figure 9 Rdson vs Vgs

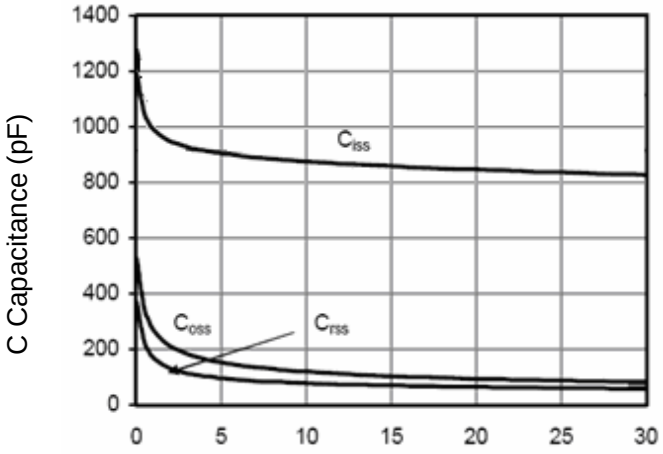


Figure 10 Capacitance vs Vds

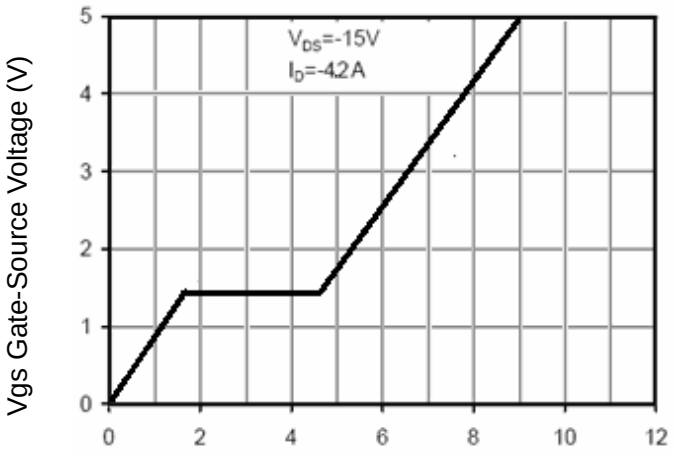


Figure 11 Gate Charge

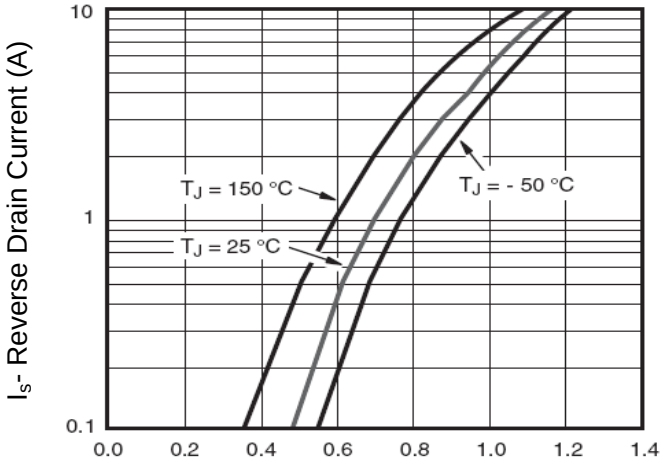


Figure 12 Source- Drain Diode Forward

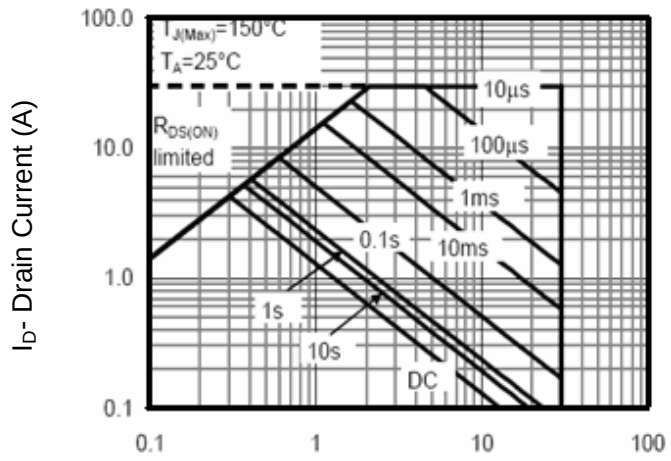


Figure 13 Safe Operation Area

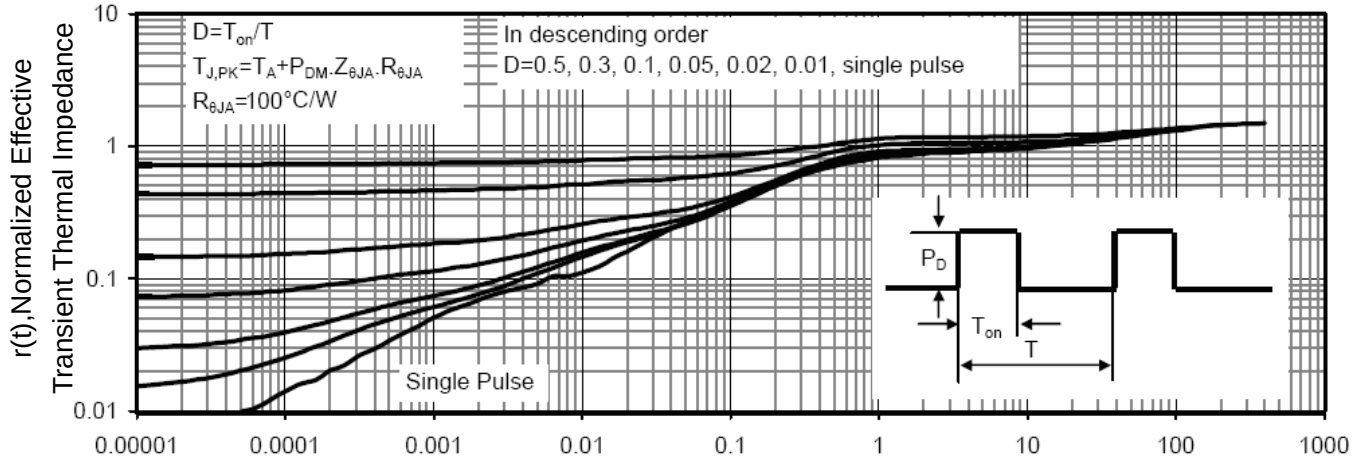
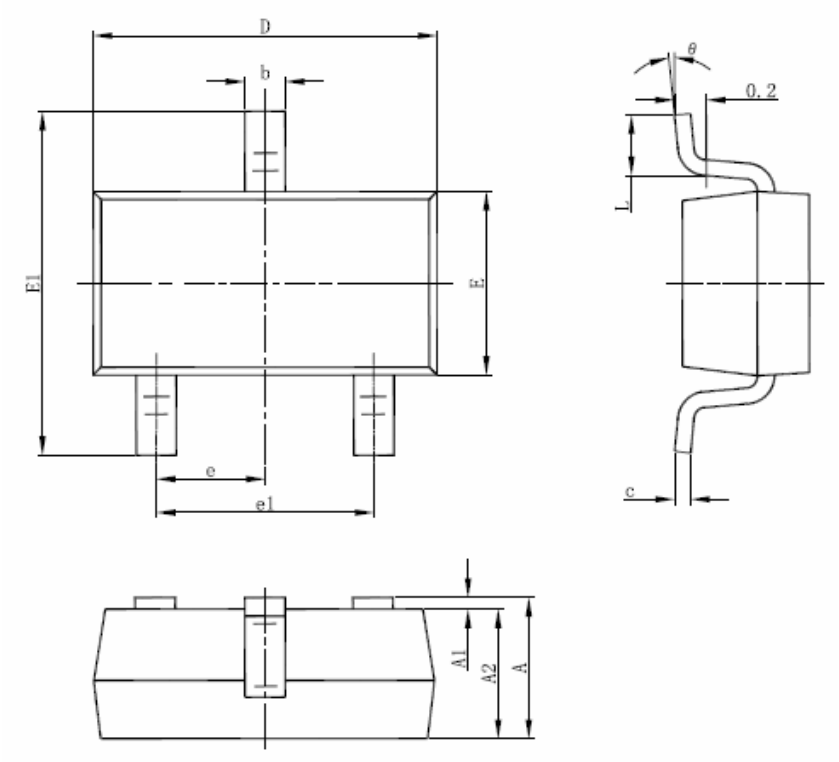


Figure 14 Normalized Maximum Transient Thermal Impedance

SOT-23-3L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Notes

1. All dimensions are in millimeters.
2. Tolerance ±0.10mm (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.