PRELIMINARY DATA SHEET

MSP 3405D, MSP 3415D Multistandard Sound Processors

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Multistandard Sound Processor

Release Notes: The hardware description in this document is valid for the MSP 34x5D version A2 and following versions. Revision bars indicate significant changes to the previous edition.

1. Introduction

The **MSP 34x5D** is designed as a single-chip Multistandard Sound Processor for applications in analog and digital TV sets, video recorders, and PC-cards. As derivative versions of the MSP 34x0D, the MSP 34x5D combines all demodulator features of the MSP 34x0D with less I/O and reduced audio baseband processing.

The IC is produced in submicron CMOS technology, combined with high-performance digital signal processing. The MSP 34x5D is available in the following packages: PLCC68, PSDIP64, PSDIP52, PQFP80, and PMQFP44.

Note: The MSP 34x5D version has reduced control registers and less functional pins. The remaining registers are software compatible to the MSP 3410D. The pinning is compatible to the MSP 3410D.

1.1. Common Features of MSP 34x5D

- Dolby Pro Logic together with DPL 351xA
- Analog sound IF input
- No external filters required
- Stereo baseband input via integrated A/D converters
- Two pairs of D/A converters
- Two carrier FM
- I^2S Interface for version B3 and later versions
- AVC: Automatic Volume Correction
- Bass, treble, volume, loudness, and spatial effects processing
- Full SCART in/out matrix without restrictions
- Improved FM-identification (as in MSPC)
- Demodulator short programming
- Autodetection for terrestrial TV-sound standards
- Improved carrier mute algorithm (as in MSPD)
- Improved AM-demodulation (as in MSPD)
- Digital control output pins D_CTR_OUT0/1
- Reduction of necessary controlling
- Less external components

1.2. Specific MSP 3415D Features

- All NICAM standards
- Precise bit-error rate indication
- Automatic switching from NICAM to FM/AM or vice versa
- Improved NICAM synchronization algorithm

1.3. Unsupported MSP 34x0D Functions

- Equalizer

1.4. MSP 34x0D Inputs and Outputs not included in the MSP 34x5D

- 2nd IF input
- 3rd and 4th SCART input
- 2nd SCART output
- 2nd SCART DA
- Headphone output
- Subwoofer output
- ADR interface

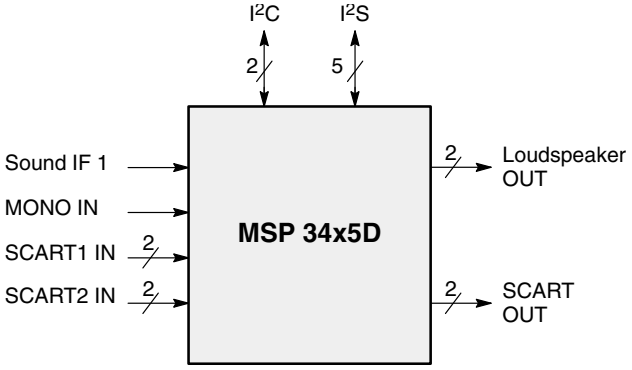


Fig. 1–1: Main I/O signals of the MSP 34x5D

2. Basic Features of the MSP 34x5D

2.1. Demodulator and NICAM Decoder Section

The MSP 3415D is designed to simultaneously perform digital demodulation and decoding of NICAM-coded TV stereo sound, as well as demodulation of FM or AM-mono TV sound. Alternatively, two carrier FM systems according to the German terrestrial specs can be processed with the MSP 34x5D.

The MSP 34x5D facilitates profitable multistandard capability, offering the following advantages:

- Automatic Gain Control (AGC) for analog input: input range: 0.10 – 3 Vpp
- integrated A/D converter for sound IF input
- all demodulation and filtering is performed on chip and is individually programmable
- easy realization of all digital NICAM standards (B/G, I, L and D/K, not for MSP 3405D)
- FM-demodulation of all terrestrial standards (including identification decoding)
- no external filter hardware is required
- only one crystal clock (18.432 MHz) is necessary
- high deviation FM-mono mode (max. deviation: approx. ±360 kHz)

2.2. DSP-Section (Audio Baseband Processing)

- two digital inputs and one digital output via I^2S bus for external signal processors like the DPL 351x.
- flexible selection of audio sources to be processed
- performance of terrestrial deemphasis systems (FM, NICAM)
- digitally performed FM-identification decoding and dematrixing
- digital baseband processing: volume, bass, treble, loudness, and spatial effects
- simple controlling of volume, bass, treble, loudness, and spatial effects

2.3. Analog Section

- two selectable analog pairs of audio baseband inputs (= two SCART inputs)
  input level: ≤2 V RMS,
  input impedance: ≥25 kΩ
- one selectable analog mono input (i.e. AM sound):
  input level: ≤2 V RMS,
  input impedance: ≥15 kΩ
- two high-quality A/D converters, S/N-Ratio: ≥85 dB
- 20 Hz to 20 kHz bandwidth for SCART-to-SCART-copy facilities
- loudspeaker: one pair of four-fold oversampled D/A-converters
  output level per channel: max. 1.4 VRMS
  output resistance: max. 5 kΩ
  S/N-ratio: ≥85 dB at maximum volume
  max. noise voltage in mute mode: ≤10 μV
  (BW: 20 Hz ...16 kHz)
- one pair of four-fold oversampled D/A converters supplying a pair of SCART-outputs.
  output level per channel: max. 2 V RMS,
  output resistance: max. 0.5 kΩ,
  S/N-Ratio: ≥85 dB (20 Hz...16 kHz)

3. Application Fields of the MSP 34x5D

In the following sections, a brief overview about the two main TV sound standards, NICAM 728 and German FM-Stereo, demonstrates the complex requirements of a multistandard audio IC.

3.1. NICAM plus FM/AM-Mono

According to the British, Scandinavian, Spanish, and French TV-standards, high-quality stereo sound is transmitted digitally. The systems allow two high-quality digital sound channels to be added to the already existing FM/AM-channel. The sound coding follows the format of the so-called Near Instantaneous Companding System (NICAM 728). Transmission is performed using Differential Quadrature Phase Shift Keying (DQPSK). Table 3–2 gives some specifications of the sound coding (NICAM); Table 3–3 offers an overview of the modulation parameters.

In the case of NICAM/FM (AM) mode, there are three different audio channels available: NICAM A, NICAM B, and FM/AM-mono. NICAM A and B may belong either to a stereo or to a dual language transmission. Information about operation mode and about the quality of the NICAM signal can be read by the CCU via the control bus. In the case of low quality (high bit error rate), the CCU may decide to switch to the analog FM/AM-mono sound. Alternatively, an automatic NICAM-FM/AM switching may be applied.

3.2. German 2-Carrier System (DUAL FM System)

Since September 1981, stereo and dual sound programs have been transmitted in Germany using the 2-carrier system. Sound transmission consists of the already existing first sound carrier and a second sound carrier additionally containing an identification signal. More details of this standard are given in Tables 3–1 and 3–4. For D/K and M-Korea, very similar systems are used.

Table 3–1: TV standards

TV-System	Position of Sound Carrier [MHz]	Sound Modulation	Color System	Country
B/G	5.5/5.7421875	FM-Stereo	PAL	Germany
B/G	5.5/5.85	FM-Mono/NICAM	PAL	Scandinavia,Spain
L	6.5/5.85	AM-Mono/NICAM	SECAM-L	France
I	6.0/6.552	FM-Mono/NICAM	PAL	UK
D/K	6.5 /6.2578125 D/K1 6.5/6.7421875 D/K2 6.5/5.85 D/K-NICAM	FM-Stereo FM-Mono/NICAM	SECAM-East	USSR Hungary
M M-Korea	4.5 4.5/4.724212	FM-Mono FM-Stereo	NTSC	USA Korea
Satellite Satellite	6.5 7.02/7.2	FM-Mono FM-Stereo	PAL PAL	Europe (ASTRA) Europe (ASTRA)

Table 3–2: Summary of NICAM 728 sound coding characteristics

Characteristics	Values
Audio sampling frequency	32 kHz
Number of channels	2
Initial resolution	14 bit/sample
Companding characteristics	near instantaneous, with compression to 10 bits/sample in 32-samples (1 ms) blocks
Coding for compressed samples	2's complement
Preemphasis	CCITT Recommendation J.17 (6.5 dB attenuation at 800 Hz)
Audio overload level	+12 dBm measured at the unity gain frequency of the preemphasis network (2 kHz)

Table 3–3: Summary of NICAM 728 sound modulation parameters

Specification	I	B/G	L		D/K	
Carrier frequency of digital sound	6.552 MHz	5.85 MHz	5.85 MHz		5.85 MHz	
Transmission rate	728 kBit/s					
Type of modulation	Differentially encoded quadrature phase shift keying (DQPSK)					
Spectrum shaping Roll-off factor	by means of Roll-off filters					
	1.0	0.4	0.4		0.4	
Carrier frequency of analog sound component	6.0 MHz FM mono	5.5 MHz FM mono	6.5 MHz AM mono		6.5 MHz FM mono	
			terrestrial	cable		
Power ratio between vision carrier and analog sound carrier	10 dB	13 dB	10 dB	16 dB	13 dB	
Power ratio between analog and modulated digital sound carrier	10 dB	7 dB	17 dB	11 dB	Hungary	Poland
					12 dB	7 dB

Table 3–4: Key parameters for B/G, D/K, and M 2-carrier sound system

Sound Carriers	**Carrier FM1**			**Carrier FM2**		
	B/G	D/K	M	B/G	D/K	M
Vision/sound power difference	13 dB			20 dB		
Sound bandwidth	40 Hz to 15 kHz					
Pre-emphasis	50 µs		75 µs	50 µs		75 µs
Frequency deviation	±50 kHz		±25 kHz	±50 kHz		±25 kHz
Sound Signal Components						
Mono transmission	mono			mono		
Stereo transmission	(L+R)/2		(L+R)/2	R		(L–R)/2
Dual sound transmission	language A			language B		
Identification of Transmission Mode on Carrier FM2						
Pilot carrier frequency in kHz				54.6875		55.0699
Type of modulation				AM		
Modulation depth				50%		
Modulation frequency				mono: unmodulated stereo: 117.5 Hz dual: 274.1 Hz		149.9 Hz 276.0 Hz

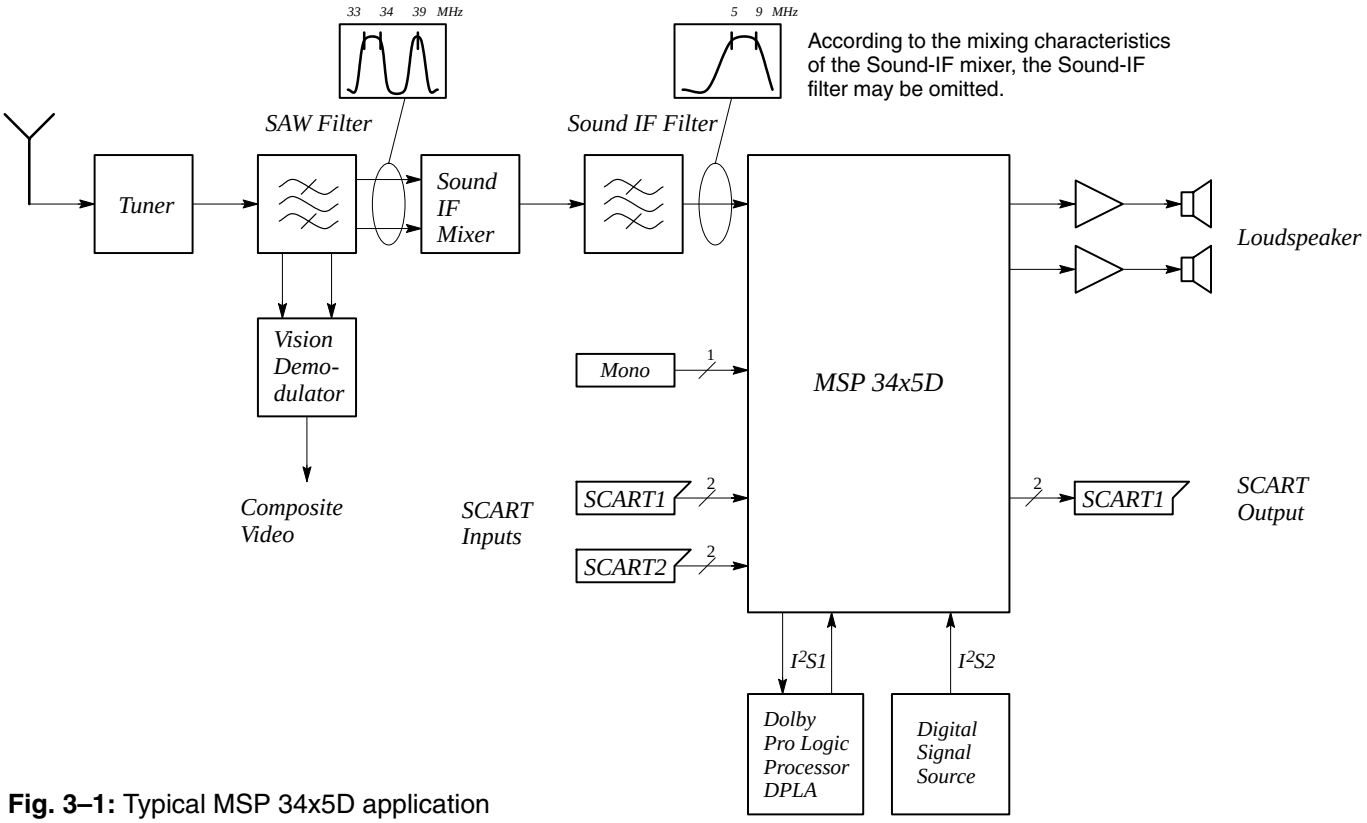


Fig. 3–1: Typical MSP 34x5D application

4. Architecture of the MSP 34x5D

Fig. 4–1 shows a simplified block diagram of the IC. Its architecture is split into three main functional blocks:

1. demodulator and NICAM decoder section
2. digital signal processing (DSP) section performing audio baseband processing
3. analog section containing two A/D-converters, four D/A-converters, and SCART switching facilities.

4.1. Demodulator and NICAM Decoder Section

4.1.1. Analog Sound IF – Input Section

The input pins ANA_IN1+ and ANA_IN– offer the possibility to connect sound IF (SIF) sources to the MSP 34x5D. The analog-to-digital conversion of the preselected sound IF signal is done by an A/D-converter, whose output can be used to control an analog automatic gain circuit (AGC), providing an optimal level for a wide range of input levels. It is possible to switch between automatic gain control and a fixed (setable) input gain. In the optimal case, the input range of the A/D converter is completely covered by the sound IF source. Some combinations of SAW filters and sound IF mixer ICs, however, show large picture components on their outputs. In this case, filtering is recommended. It was found, that the high pass filters formed by the coupling capacitors at pin ANA_IN1+ (as shown in the application diagram) are sufficient in most cases.

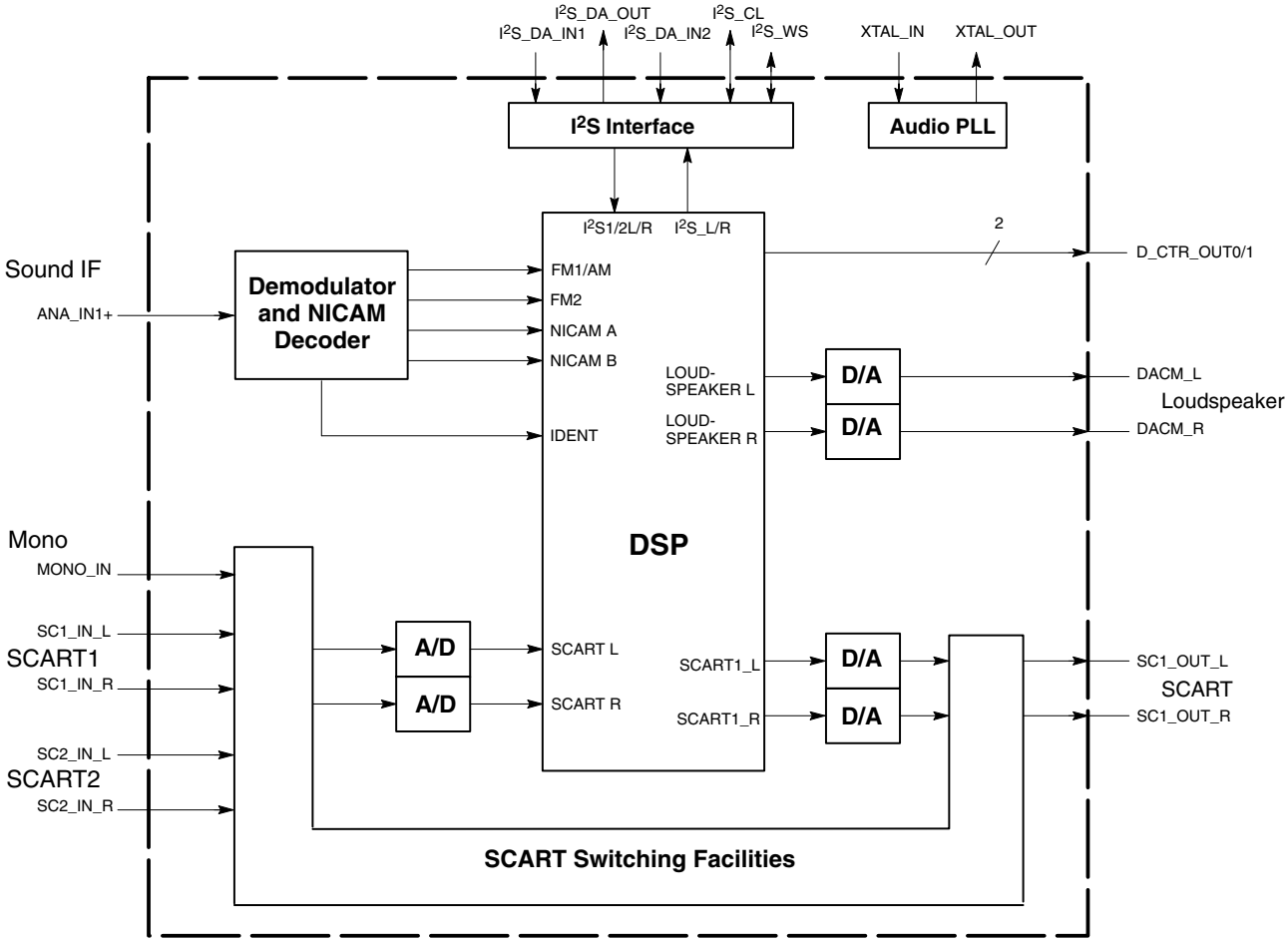


Fig. 4–1: Architecture of the MSP 34x5D

4.1.2. Quadrature Mixers

The digital input coming from the integrated A/D converter may contain audio information at a frequency range of theoretically 0 to 9 MHz corresponding to the selected standards. By means of two programmable quadrature mixers, two different audio sources; for example, NICAM and FM-mono, may be shifted into baseband position. In the following, the two main channels are provided to process either:

– NICAM (MSP-Ch1) and FM/AM mono (MSP-Ch2) simultaneously or, alternatively,

– FM2 (MSP-Ch1) and FM1 (MSP-Ch2).

NICAM is not possible with MSP 3405D.

Two programmable registers, to be divided up into low and high part, determine frequency of the oscillator, which corresponds to the frequency of the desired audio carrier. In section 6.2., format and values of the registers are listed.

4.1.3. Low-pass Filtering Block for Mixed Sound IF Signals

Data shaping and/or FM bandwidth limitation is performed by a linear phase Finite Impulse Response (FIR-filter). Just like the oscillators' frequency, the filter coefficients are programmable and are written into the IC by the CCU via the control bus. Thus, for example, different NICAM versions can easily be implemented. Two not necessarily different sets of coefficients are required, one for MSP-Ch1 (NICAM or FM2) and one for MSP-Ch2 (FM1 = FM-mono). In section 6.5.3., several coefficient sets are proposed.

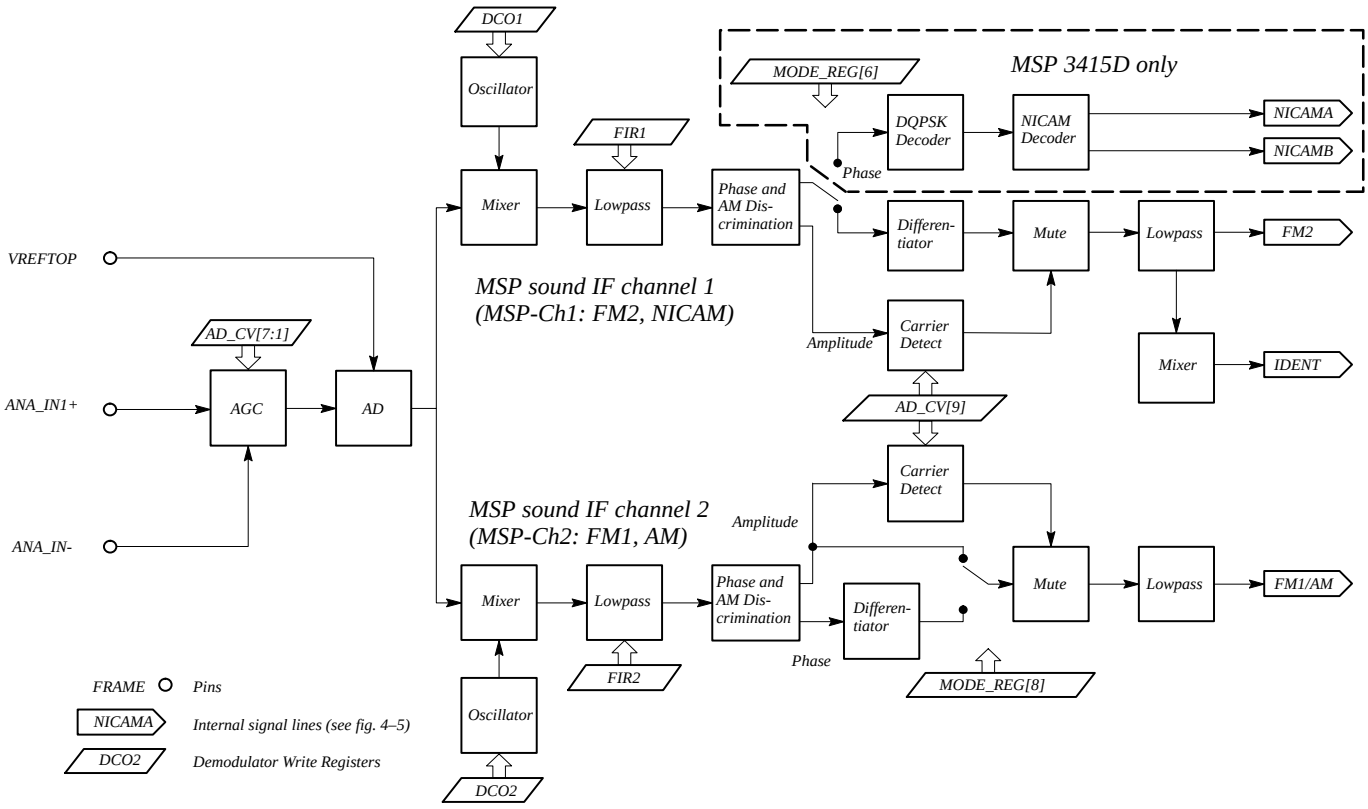


Fig. 4–2: Demodulator architecture of MSP 34x5D

4.1.4. Phase and AM Discrimination

The filtered sound IF signals are demodulated by means of the phase and amplitude discriminator block. On the output, the phase and amplitude is available for further processing. AM signals are derived from the amplitude information, whereas the phase information serves for FM and NICAM (DQPSK) demodulation.

4.1.5. Differentiators

FM demodulation is completed by differentiating the phase information output.

4.1.6. Low-pass Filter Block for Demodulated Signals

The demodulated FM and AM signals are further low-pass filtered and decimated to a final sampling frequency of 32 kHz. The usable bandwidth of the final baseband signals is about 15 kHz.

4.1.7. High Deviation FM Mode

By means of MODE_REG [9], the maximum FM-deviation can be extended to approximately ±360 kHz. Since this mode can be applied only for the MSP sound IF channel 2, the corresponding matrices in the baseband processing must be set to sound A. Apart from this, the coefficient sets 380 kHz FIR2 or 500 kHz FIR2 must be chosen for the FIR2. In relation to the normal FM-mode, the audio level of the high-deviation mode is reduced by 6 dB. The FM-prescaler should be adjusted accordingly. In high deviation FM-mode, neither FM-stereo nor FM-identification nor NICAM processing is possible simultaneously.

4.1.8. FM-Carrier-Mute Function in the Dual Carrier FM Mode

To prevent noise effects or FM identification problems in the absence of one of the two FM carriers, the MSP 3415 D offers a carrier detection feature, which must be activated by means of AD_CV[9]. If no FM carrier is available at the MSPD channel 1, the corresponding channel FM2 is muted. If no FM carrier is available at the MSPD channel 2, the corresponding channel FM1 is muted.

4.1.9. DQPSK-Decoder (MSP 3415D only)

In case of NICAM-mode, the phase samples are decoded according the DQPSK-coding scheme. The output of this block contains the original NICAM-bitstream.

4.1.10. NICAM-Decoder (MSP 3415D only)

Before any NICAM decoding can start, the MSP must lock to the NICAM frame structure by searching and synchronizing to the so-called Frame Alignment Words (FAW).

To reconstruct the original digital sound samples, the NICAM-bitstream has to be descrambled, deinterleaved, and rescaled. Also, bit error detection and correction (concealment) is performed in this NICAM specific block.

To facilitate the Central Control Unit CCU to switch the TV-set to the actual sound mode, control information on the NICAM mode and bit error rate are supplied by the the NICAM-Decoder. It can be read out via the I^2C-Bus.

An automatic switching facility (AUTO_FM) between NICAM and FM/AM reduces the amount of CCU-instructions in case of bad NICAM reception.

4.2. Analog Section

4.2.1. SCART Switching Facilities

The analog input and output sections include full matrix switching facilities, which are shown in Fig. 4–3.

The switches are controlled by the ACB bits defined in the audio processing interface (see section 7. Programming the DSP Section).

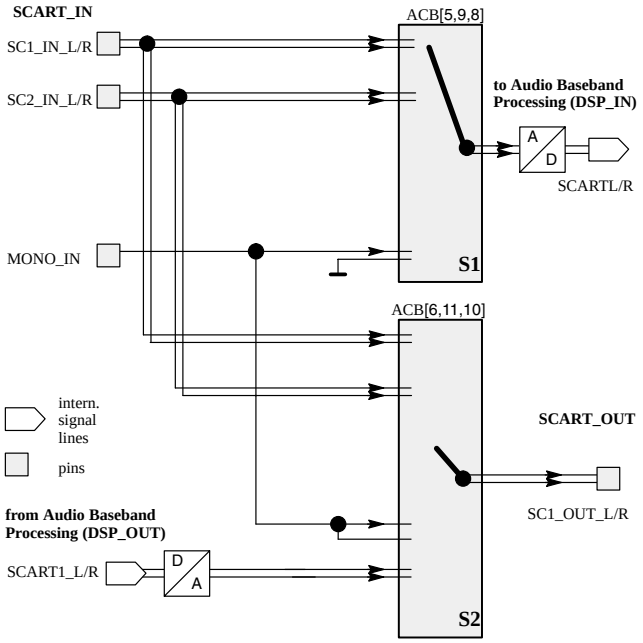


Fig. 4–3: SCART switching facilities (see 7.3.18.) Switching positions show the default configuration after power-on reset. Note: SCART_OUT is undefined after RESET!

4.2.2. Stand-by Mode

If the MSP 34x5D is switched off by first pulling STANDBYQ low, and then disconnecting the 5 V, but keeping the 8 V power supply (‘**Stand-by’-mode**), the switches S1 and S2 (see Fig. 4–3) maintain their position and function. This facilitates the copying from selected SCART-inputs to SCART-outputs in the TV-set’s stand-by mode.

In case of power-on start or starting from stand-by, the IC switches automatically to the default configuration, shown in Fig. 4–3. This action takes place after the first I^2C transmission into the DSP part. By transmitting the ACB register first, the individual default setting mode of the TV set can be defined.

4.3. DSP-Section (Audio Baseband Processing)

All audio baseband functions are performed by digital signal processing (DSP). The DSP functions are grouped into three processing parts: input preprocessing, channel source selection, and channel postprocessing (see Fig. 4–5 and section 7.).

The input preprocessing is intended to prepare the various signals of all input sources in order to form a standardized signal at the input to the channel selector. The signals can be adjusted in volume, are processed with the appropriate deemphasis, and are dematrixed if necessary.

Having prepared the signals that way, the channel selector makes it possible to distribute all possible source signals to the desired output channels.

All input and output signals can be processed simultaneously with the exception that FM2 cannot be processed at the same time as NICAM. FM-identification and adaptive deemphasis are not possible simultaneously (if adaptive deemphasis is active, the ID-level in stereo detection register is not valid).

4.3.1. Dual Carrier FM Stereo/Bilingual Detection

For the terrestrial dual FM carrier systems, audio information can be transmitted in three modes: mono, stereo, or bilingual. To obtain information about the current audio operation mode, the MSP 34x5D detects the so-called identification signal. Information is supplied via the Stereo Detection Register to an external CCU.

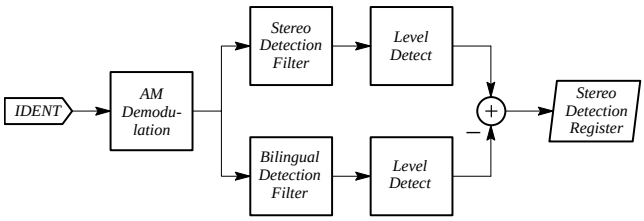


Fig. 4–4: Stereo/bilingual detection

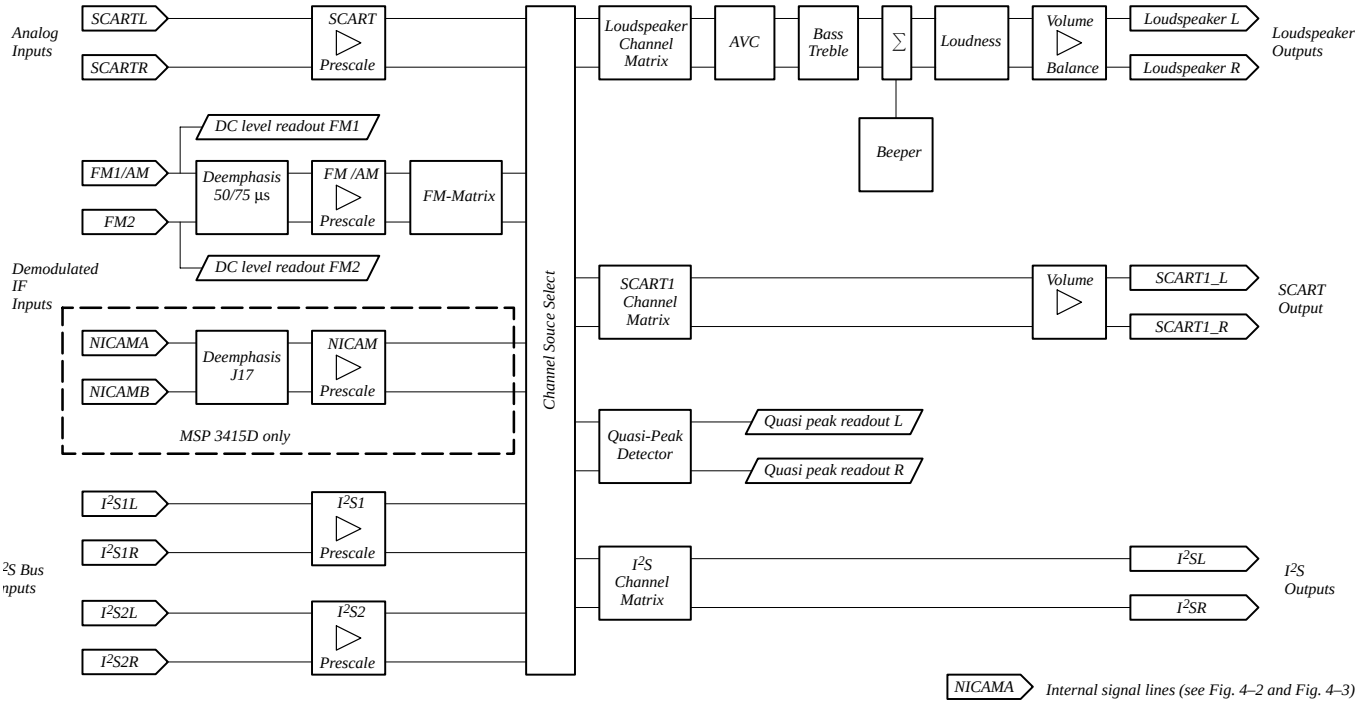


Fig. 4–5: Audio Baseband Processing (DSP-Firmware)

Table 4–1: Some examples for recommended channel assignments for demodulator and audio processing part

Mode	MSP Sound IF-Channel 1	MSP Sound IF-Channel 2	FM-Matrix	Channel-Select	Channel Matrix
B/G-Stereo	FM2 (5.74 MHz): R	FM1 (5.5 MHz): (L+R)/2	B/G Stereo	Speakers: FM	Stereo
B/G-Bilingual	FM2 (5.74 MHz): Sound B	FM1 (5.5 MHz): Sound A	No Matrix	Speakers: FM	Speakers: Sound A H. Phone: Sound B
NICAM-I-ST/ FM-mono	NICAM (6.552 MHz)	FM (6.0 MHz): mono	No Matrix	Speakers: NICAM	Speakers: Stereo H. Phone: Sound A
Sat-Mono	not used	FM (6.5 MHz): mono	No Matrix	Speakers: FM	Sound A
Sat-Stereo	7.2 MHz: R	7.02 MHz: L	No Matrix	Speakers: FM	Stereo
Sat-Bilingual	7.38 MHz: Sound C	7.02 MHz: Sound A	No Matrix	Speakers: FM	Speakers: Sound A H. Phone: Sound B=C
Sat-High Dev. Mode	don't care	6.552 MHz	No Matrix	Speakers: FM	Speakers: Sound A H. Phone: Sound A

4.4. Audio PLL and Crystal Specifications

The MSP 34x5D requires a 18.432 MHz (12 pF, parallel) crystal. The clock supply of the whole system depends on the MSP 34x5D operation mode:

1. FM-Stereo, FM-Mono:
   The system clock runs free on the crystal's 18.432 MHz.
2. NICAM:
   An integrated clock PLL uses the 364 kHz baud-rate, accomplished in the NICAM demodulator block, to lock the system clock to the bit rate, respectively, 32 kHz sampling rate of the NICAM transmitter. As a result, the whole audio system is supplied with a controlled 18.432 MHz clock.

Remark on using the crystal:
External capacitors at each crystal pin to ground are required (see General Crystal Recommendations on page 60).

4.5. Digital Control Output Pins

The static level of two output pins of the MSP 34x5D (D_CTR_OUT0/1) is switchable between HIGH and LOW by means of the I²C-bus. This enables the controlling of external hardware controlled switches or other devices via I²C-bus (see section 7.3.18.).

4.6. I²S Bus Interface

By means of this standardized interface, additional feature processors can be connected to the MSP 34x0D. Two possible formats are supported: The standard mode (MODE_REG[4]=0) selects the SONY format, where the I2S_WS signal changes at the word boundaries. The PHILIPS format, which is characterized by a change of the I2S_WS signal one I2S_CL period before the word boundaries, is selected by setting MODE_REG[4]=1.

The MSP 34x5D normally serves as the master on the I²S interface. Here, the clock and word strobe lines are driven by the MSP. By setting MODE_REG[3]=1, the MSP 34x5D is switched to a slave mode. Now, these lines are input to the MSP and the master clock is synchronized to 576 times the I2S_WS rate (32 kHz). NICAM operation is not possible in this mode.

The I²S bus interface consists of five pins:

1. I2S_DA_IN1, I2S_DA_IN2:
   For input, four channels (two channels per line, 2*16 bits) per sampling cycle (32 kHz) are transmitted.
2. I2S_DA_OUT:
   For output, two channels (2*16 bits) per sampling cycle (32 kHz) are transmitted.
3. I2S_CL:
   Gives the timing for the transmission of I²S serial data (1.024 MHz).
4. I2S_WS:
   The I2S_WS word strobe line defines the left and right sample.

A precise I²S timing diagram is shown in Fig. 4–6.

(Data: MSB first)

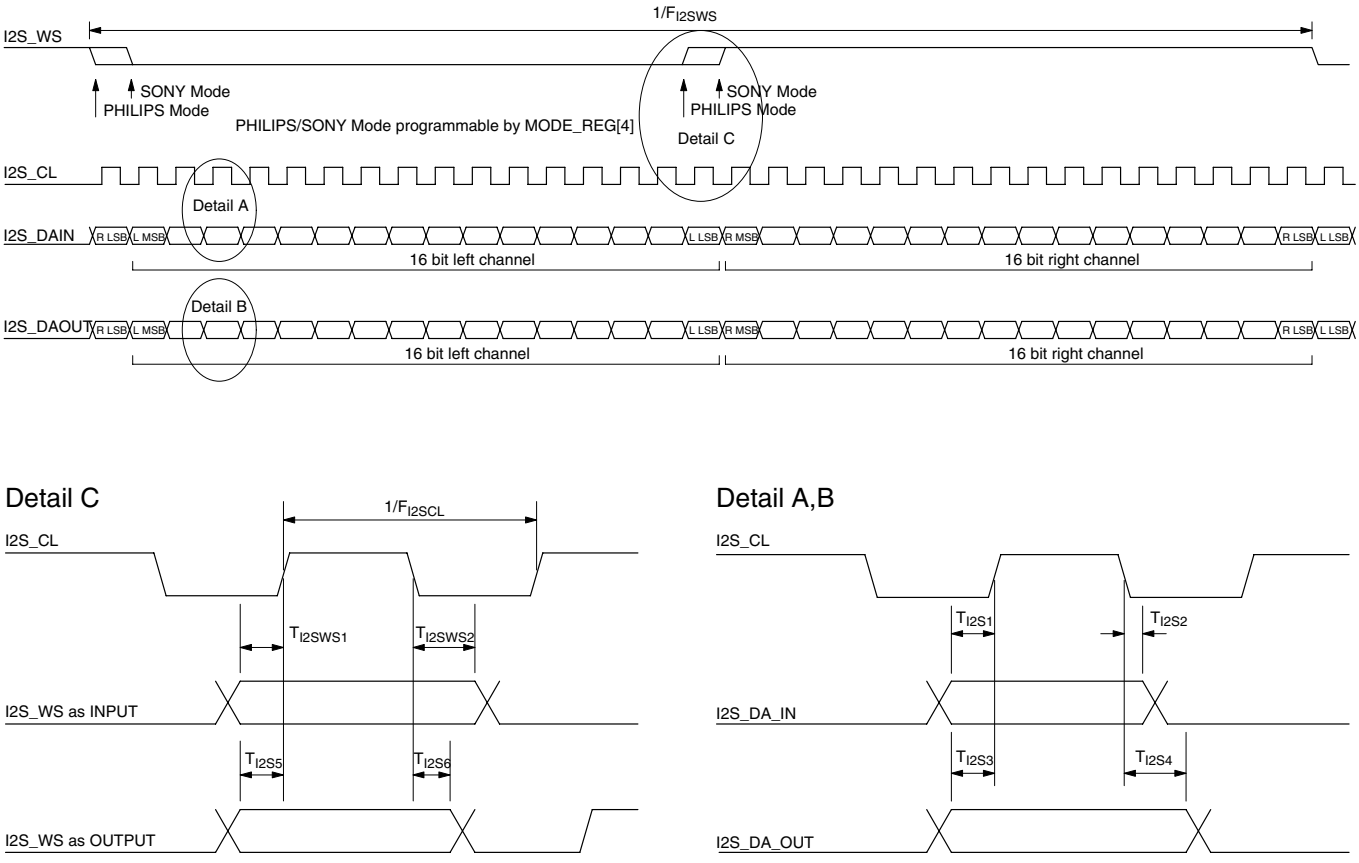


Fig. 4–6: I²S bus timing diagram

5. I²C Bus Interface: Device and Subaddresses

As a slave receiver, the MSP 34x5D can be controlled via I²C bus. Access to internal memory locations is achieved by subaddressing. The demodulator and the DSP processor parts have two separate subaddressing register banks.

In order to allow for more MSP 34x5D ICs to be connected to the control bus, an ADR_SEL pin has been implemented. With ADR_SEL pulled to high, low, or left open, the MSP 34x5D responds to changed device addresses. Thus, three identical devices can be selected.

By means of the RESET bit in the CONTROL register, all devices with the same device address are reset.

The IC is selected by asserting a special device address in the address part of an I²C transmission. A device address pair is defined as a write address (80, 84, or 88_{hex}) and a read address (81, 85, or 89_{hex}) (see Table 5–1). Writing is done by sending the device write address, followed by the subaddress byte, two address bytes, and two data bytes. Reading is done by sending the device write address, followed by the subaddress byte and two address bytes. Without sending a stop condition, reading of the addressed data is completed by sending the device read address (81, 85, or 89_{hex}) and reading two bytes of data (see Fig. 5–1: “I²C Bus Protocol” and section 5.2. “Proposal for MSP 34x5D I²C Telegrams”).

Due to the internal architecture of the MSP 34x5D the IC cannot react immediately to an I²C request. The typical response time is about 0.3 ms for the DSP processor part and 1 ms for the demodulator part if NICAM processing is active. If the receiver (MSP) can’t receive another complete byte of data until it has performed some other function; for example, servicing an internal interrupt, it can hold the clock line I²C_CL LOW to force the transmitter into a wait state. The positions within a transmission where this may happen are indicated by ’Wait’ in section 5.1. The maximum Wait-period of the MSP during normal operation mode is less than 1 ms.

I²C bus error caused by MSP hardware problems:
In case of any internal error, the MSPs wait-period is extended to 1.8 ms. Afterwards, the MSP does not acknowledge (NAK) the device address. The data line will be left HIGH by the MSP and the clock line will be released. The master can then generate a STOP condition to abort the transfer.

By means of NAK, the master is able to recognize the error state and to reset the IC via I²C bus. While transmitting the reset protocol (see section 5.2.4. on page 18) to ‘CONTROL’, the master must ignore the not acknowledge bits (NAK) of the MSP.

A general timing diagram of the I²C bus is shown in Fig. 5–2 on page 18.

Table 5–1: I²C Bus Device Addresses

ADR_SEL	Low		High		Left Open	
Mode	**Write**	**Read**	**Write**	**Read**	**Write**	**Read**
MSP device address	80_{hex}	81_{hex}	84_{hex}	85_{hex}	88_{hex}	89_{hex}

Table 5–2: I²C Bus Subaddresses

Name	Binary Value	Hex Value	Mode	Function
CONTROL	0000 0000	00	W	software reset
TEST	0000 0001	01	W	only for internal use
WR_DEM	0001 0000	10	W	write address demodulator
RD_DEM	0001 0001	11	W	read address demodulator
WR_DSP	0001 0010	12	W	write address DSP
RD_DSP	0001 0011	13	W	read address DSP

Table 5–3: Control Register (Subaddress: 00_{hex})

Name	Subaddress	MSB	14	13..1	LSB
CONTROL	00 hex	1 : RESET 0 : normal	0	0	0

5.1. Protocol Description

Write to DSP or Demodulator

S	write device address	Wait	ACK	sub-addr	ACK	addr-byte high	ACK	addr-byte low	ACK	data-byte high	ACK	data-byte low	ACK	P

Read from DSP or Demodulator

S	write device address	Wait	ACK	sub-addr	ACK	addr-byte high	ACK	addr-byte low	ACK	S	read device address	Wait	ACK	data-byte high	ACK	data-byte low	NAK	P

Write to Control or Test Registers

S	write device address	Wait	ACK	sub-addr	ACK	data-byte high	ACK	data-byte low	ACK	P

Note: S = I^2C-Bus Start Condition from master
P = I^2C-Bus Stop Condition from master
ACK = Acknowledge-Bit: LOW on I2C_DA from slave (=MSP, gray) or master (=CCU, hatched)
NAK = Not Acknowledge-Bit: HIGH on I2C_DA from master (=CCU, hatched) to indicate 'End of Read' or from MSP indicating internal error state
Wait = I^2C-Clock line held low by the slave (=MSP) while interrupt is serviced (<1.8 ms)

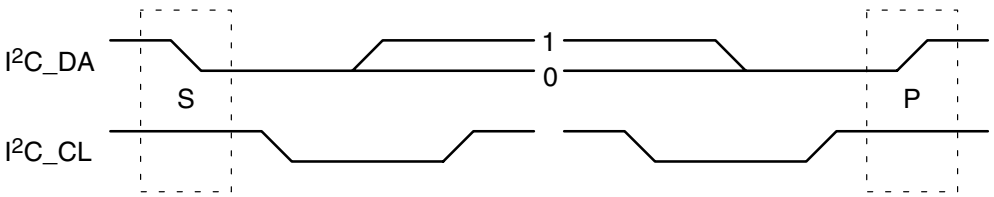


Fig. 5–1: I^2C bus protocol (MSB first; data must be stable while clock is high)

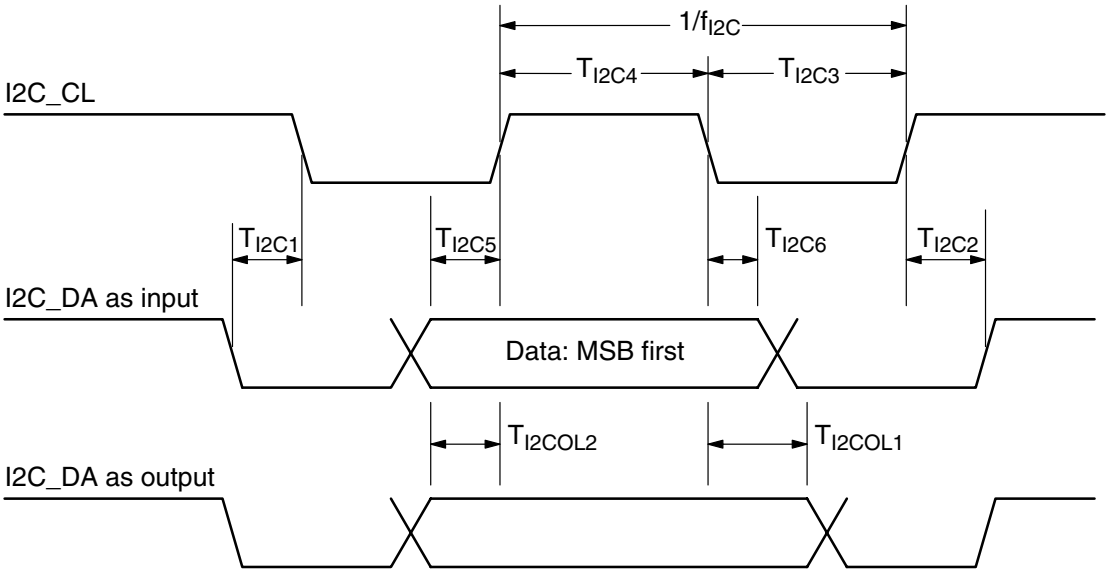


Fig. 5–2: I²C bus timing diagram

5.2. Proposal for MSP 34x5D I²C Telegrams

5.2.1. Symbols

daw	write device address
dar	read device address
<	Start Condition
>	Stop Condition
aa	Address Byte
dd	Data Byte

5.2.2. Write Telegrams

<daw 00 d0 00>	write to CONTROL register
<daw 10 aa aa dd dd>	write data into demodulator
<daw 12 aa aa dd dd>	write data into DSP

5.2.3. Read Telegrams

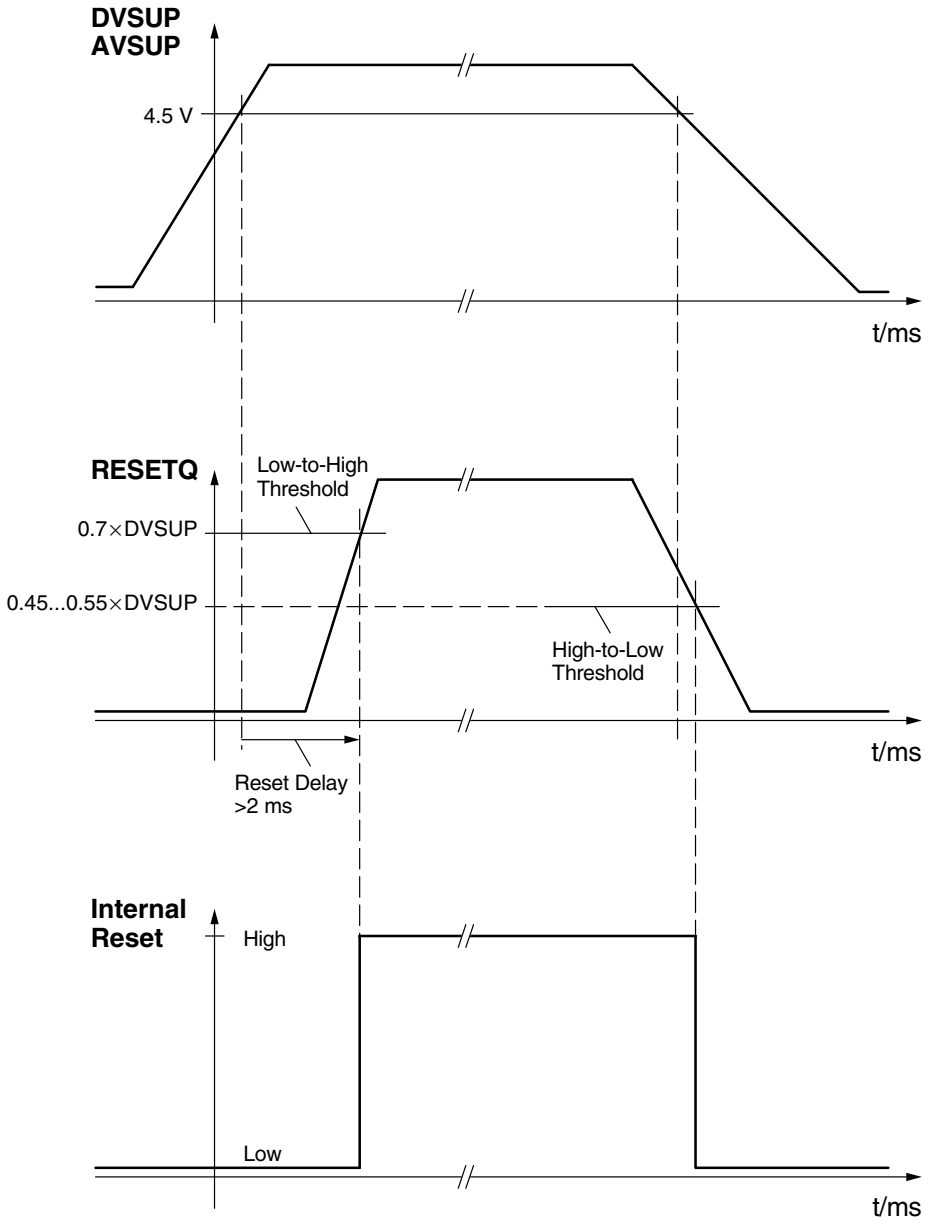
<daw 11 aa aa <dar dd dd>	read data from demodulator
<daw 13 aa aa <dar dd dd>	read data from DSP

5.2.4. Examples

<80 00 80 00>	RESET MSP statically
<80 00 00 00>	clear RESET
<80 12 00 08 01 20>	set loudspeaker channel source to NICAM and Matrix to STEREO

5.3. Start-Up Sequence: Power-Up and I²C-Controlling

After power-on or RESET (see Fig. 5–3), the IC is in an inactive state. The CCU has to transmit the required coefficient set for a given operation via the I²C bus. Initialization should start with the demodulator part. If required for any reason, the audio processing part can be loaded before the demodulator part.



Power-up reset: threshold and timing
Note: 0.7×DVSUP means 3.5 Volt with DVSUP = 5.0 Volt

Fig. 5–3: Power-up sequence

Note: The reset should not reach high level before the oscillator has started. This requires a reset delay of >2 ms

6. Programming the Demodulator Section

6.1. Short-Programming and General Programming of the Demodulator Part

The Demodulator Part of the MSP 34x5D can be programmed in **two different modes**:

1. Demodulator Short-Programming facilitates a comfortable way to set up the demodulator for many terrestrial TV-sound standards with one single I^2C-Bus transmission. The coding is listed in section 6.4.1.. If a parameter doesn't coincide with the individual programming concept, it simply can be overwritten by using the General Programming mode. Some bits of the registers AD_CV (see section 6.5.1.) and MODE_REG (see section 6.5.2.) are not affected by the short-programming. They must be transmitted once if their reset status does not fit. The Demodulator Short-Programming is not compatible to MSP 3410B and MSP 3400C.

Autodetection for terrestrial TV standards (as part of the below Demodulator Short-Programming) provides the most comfortable way to set up the MSPD-demodulator. This feature facilitates within 0.5 s the detection and set-up of the actual TV-sound standard. Since the detected standard is readable by the control processor, the autodetection feature is mainly recommended for the primary set-up of a TV-set: after having determined once the corresponding TV-channels, their sound standards can be stored and later on programmed by the Demodulator Short-Programming (see sections 6.4.1. and 6.6.1.).

2. General Programming ensures the software compatibility to other MSPs. It offers a very flexible way to apply all of the MSP 34x5D demodulator facilities. All registers except 0020_{hex} have to be written with values corresponding to the individual requirements. For satellite applications, with their many variations, this mode must be selected.

All transmissions on the control bus are 16 bits wide. However, data for the demodulator part have only 8 or 12 significant bits. These data have to be inserted LSB-bound and filled with zero bits into the 16-bit transmission word. Table 4–1 explains how to assign FM carriers to the MSP-Sound IF channels and the corresponding matrix modes in the audio processing part.

6.2. Demodulator Write Registers: Table and Addresses

Table 6–1: Demodulator Write Registers; Subaddress: 10_{hex}; these registers are not readable!

Demodulator Write Registers	Address (hex)	Function
Demodulator Short-Programming	0020	Write into this register to apply Demodulator Short Programming (see section 6.4.1.). If the internal setting coincidences with the individual requirements no more of the remaining Demodulator Write Registers have to be transferred.
AUTO_FM/AM	0021	Only for NICAM (MSP 3415D): Automatic switching between NICAM and FM/AM in case of bad NICAM reception (see section 6.4.2.)
Write Registers necessary for **General Programming Mode** only		
AD_CV	00BB	input selection, configuration of AGC, Mute Function and selection of A/D-converter, FM-Carrier-Mute on/off
MODE_REG	0083	mode register
FIR1 FIR2	0001 0005	filter coefficients channel 1 (6 · 8 bit) filter coefficients channel 2 (6 · 8 bit), + 3 · 8 bit offset (total 72 bit)
DCO1_LO DCO1_HI DCO2_LO DCO2_HI	0093 009B 00A3 00AB	increment channel 1 Low Part increment channel 1 High Part increment channel 2 Low Part increment channel 2 High Part
PLL_CAPS	001F	switchable PLL capacitors to tune open-loop frequency; to use only if NICAM of MODE_REG = 0 normally not of interest for the customer

6.3. Demodulator Read Registers: Table and Addresses

Table 6–2: Demodulator Read Registers; Subaddress: 11_{hex}; these registers are not writeable!

Demodulator Read Registers	Address (hex)	Function
Result of Autodetection	007E	see Table 6–13
C_AD_BITS	0023	NICAM-Sync bit, NICAM-C-Bits, and three LSBs of additional data bits
ADD_BITS	0038	NICAM: bit [10:3] of additional data bits
CIB_BITS	003E	NICAM: CIB1 and CIB2 control bits
ERROR_RATE	0057	NICAM error rate, updated with 182 ms
CONC_CT	0058	only to be used in MSPB compatibility mode
FAWCT_IST	0025	only to be used in MSPB compatibility mode
PLL_CAPS	021F	Not for customer use.
AGC_GAIN	021E	Not for customer use.

Note: All NICAM relevant registers are “0” for MSP 3405D.

6.4. Demodulator Write Registers for Short-Programming: Functions and Values

In the following, the functions of some registers are explained and their (default) values are defined:

6.4.1. Demodulator Short-Programming

Table 6–3: MSP 34x5D Demodulator Short-Programming

Demodulator Short-Programming 0020$_{hex}$							
TV-Sound Standard		**Internal Setting**					
Description	**Code (hex)**	**AD_CV[2)]** (see Table 6–5)	**MODE_REG[2)]** (see Table 6–8)	**DCO1 (MHz)**	**DCO2 (MHz)**	**FIR1/2 Coefficients**	**Identification Mode**
Autodetection	0001	Detects and sets one of the standards listed below, if available. Results are to be read out of the demodulator read register ”Result of Autodetection” (Section 6.6.1.)					
M Dual-FM	0002	AD_CV-FM	M1	4.72421	4.5	see Table 6–11: Terrestrial TV-Standards	Reset, then Standard M
B/G Dual-FM	0003	AD_CV-FM	M1	5.74218	5.5		Reset, then Standard B/G
D/K1 Dual-FM	0004	AD_CV-FM	M1	6.25781	6.5		
D/K2 Dual-FM	0005	AD_CV-FM	M1	6.74218	6.5		
	0006/ 0007	reserved for future Dual FM Standards					**AUTO_FM/AM**
NICAM-Modes for MSP 3415D only; MSP 3405D responds with FM/AM Mono							
B/G-NICAM-FM	0008	AD_CV-FM	M2	5.85	5.5	see Table 6–11: Terrestrial TV-Standards	1)
L-NICAM-AM	0009	AD_CV-AM	M3	5.85	6.5		
I-NICAM-FM	000A	AD_CV-FM	M2	6.552	6.0		
D/K-NICAM-FM	000B	AD_CV-FM	M2	5.85	6.5		
	>000B	reserved for future NICAM Standards					

1) corresponds to the actual setting of AUTO_FM (Address = 0021$_{hex}$)

2) Bits of AD_CV or MODE_REG, which are not affected by the short-programming, must be transmitted separately if their reset status does not fit.

Note: All parameters in the DSP section (Audio Baseband Processing), except the identification mode register, are not affected by the Demodulator Short-Programming . They still have to be defined by the control processor.

6.4.2. AUTO_FM/AM: Automatic Switching between NICAM and FM/AM-Mono (MSP 3415D only)

In case of bad NICAM transmission or loss of the NICAM-carrier, the MSPD offers a comfortable mode to switch back to the FM/AM-mono signal. If automatic switching is active, the MSP internally evaluates the ERROR_RATE. All output channels which are assigned to the NICAM-source are switched back to the FM/AM-mono source without any further CCU instruction, if the NICAM-carrier fails or the ERROR_RATE exceeds the definable threshold.

Note, that the channel matrix of the corresponding output-channels must be set according to the NICAM-mode and need not be changed in the FM/AM-fall-back case. An appropriate hysteresis algorithm avoids oscillating effects. Bit 11 of the register C_AD_BITS (Address: 0023_{hex}) informs about the actual NICAM-FM/AM-Status (see section 6.6.2.).

There are two possibilities to define the threshold deciding for NICAM or FM/AM-mono (see Table 6–4):

1. default value of the MSPD (internal threshold=700, i.e. switch to FM/AM if ERROR_RATE > 700)

2. definable by the customer (recommendable range: threshold = 50....2000, i. e. Bits [10:1] = 25...1000).

Note:
The auto_fm feature is only active if the NICAM-bit of MODE_REG is set.

Table 6–4: Coding of automatic NICAM-FM/AM switching; reset status: mode 0

Mode	Auto_fm [11....0] Addr. = 0021_{hex}	Selected Sound at the NICAM Channel Select	Threshold	Comment
0. default	Bit [0] = 0 Bits [11...1] = 0	always NICAM	none	Compatible to MSP 3410B, i.e. automatic switching is disabled
1.	Bit [0] = 1 Bit [11:1] = 0	NICAM or FM/AM, depending on ERROR_RATE	700 dec	automatic switching with **internal** threshold
2.	Bit [0] = 1 Bit [10:1] = 25...1000 int = threshold/2 Bit [11] = 0	NICAM or FM/AM, depending on ERROR_RATE	set by customer	automatic switching with **external** threshold
3.	Bit [11] = [0] = 1 Bit [10...1] = 0	always FM/AM	none	Forced FM-mono mode, i.e. automatic switching is disabled

6.5. Demodulator Write Registers for the General Programming Mode: Functions and Values

6.5.1. Register 'AD_CV'

Table 6–5: AD_CV Register; reset status: all bits are "0"

AD_CV 00BB$_{hex}$			Set by Short-Programming	
Bit	**Meaning**	**Settings**	**AD_CV-FM**	**AD_CV-AM**
AD_CV [0]	not used	must be set to 0	0	0
AD_CV [6:1]	Reference level in case of Automatic Gain Control = on (see Table 6–6). Constant gain factor when Automatic Gain Control = off (see Table 6–7).		101000	100011
AD_CV [7]	Determination of Automatic Gain or Constant Gain	0 = constant gain 1 = automatic gain	1	1
AD_CV [8]	not used	must be set to 0	not affected	not affected
AD_CV [9]	MSP-Carrier-Mute Function (Must be switched off in High Deviation Mode)	0 = off: no mute 1 = on: mute as described in section 4.1.8. on page 12	1	0
AD_CV [15–10]	not used	must be set to 0	0	0

Table 6–6: Reference values for active AGC (AD_CV[7] = 1)

Application	**Input Signal Contains**	**AD_CV [6:1] Ref. Value**	**AD_CV [6:1] in integer**	**Range of Input Signal at pin ANA_IN1+ and ANA_IN2+**
Terrestrial TV				
FM-Stereo	2 FM Carriers	101000	40	0.10 – 3 V_{pp} [1)]
FM/NICAM	1 FM and 1 NICAM Carrier	101000	40	0.10 – 3 V_{pp} [1)]
AM/NICAM	1 AM and 1 NICAM carrier	100011	35	0.10 – 1.4 V_{pp} recommended: 0.10 – 0.8V_{pp}
NICAM only	1 NICAM Carrier only	010100	20	0.05 – 1.0 V_{pp}
SAT	1 or more FM Carriers	100011	35	0.10 – 3 V_{pp} [1)]

[1)] For signals above 1.4 Vpp, the minimum gain of 3 dB is switched, and overflow of the A/D converter may result. Due to the robustness of the internal processing, the IC works up to and even more than 3 Vpp, if norm conditions of FM/NICAM or FM1/FM2 ratio are supposed. In this overflow case, a loss of FM-S/N-ratio of about 10 dB may appear.

Table 6–7: AD_CV parameters for constant input gain (AD_CV[7]=0)

Step	AD_CV [6:1] Constant Gain	Gain (dB)	Input Level at pin ANA_IN1+
0	000000	3.00	maximum input level: 3 V_{pp} (FM) or 1 V_{pp} (NICAM)[1)]
1	000001	3.85	
2	000010	4.70	
3	000011	5.55	
4	000100	6.40	
5	000101	7.25	
6	000110	8.10	
7	000111	8.95	
8	001000	9.80	
9	001001	10.65	
10	001010	11.50	
11	001011	12.35	
12	001100	13.20	
13	001101	14.05	
14	001110	14.90	
15	001111	15.75	
16	010000	16.60	
17	010001	17.45	
18	010010	18.30	
19	010011	19.15	
20	010100	20.00	maximum input level: 0.14 V_{pp}

1) For signals above 1.4 Vpp, the minimum gain of 3 dB is switched, and overflow of the A/D converter may result. Due to the robustness of the internal processing, the IC works up to and even more than 3 Vpp, if norm conditions of FM/NICAM or FM1/FM2 ratio are supposed. In this overflow case, a loss of FM-S/N-ratio of about 10 dB may appear.

6.5.2. Register ‘MODE_REG’

The register ‘MODE_REG’ contains the control bits determining the operation mode of the MSP 34x5D; Table 6–8 explains all bit positions.

Table 6–8: Control word ‘MODE_REG’; reset status: all bits are “0”

MODE_REG 0083$_{hex}$				Set by Short-Programming		
Bit	**Function**	**Comment**	**Definition**	**M1**	**M2**	**M3**
[0]	not used		0 : strongly recommended	0	0	0
[1]	DCTR_TRI	Digital Control Outputs active / tri-state	0 : active 1 : tri-state	X	X	X
[2]	I2S_TRI	I2S Outputs (I2S_CL, I2S_WS, I2S_DA_OUT) active / tri-state	0 : active 1 : tri-state	X	X	X
[3]	I^2S Mode[1)]	Master / Slave Mode of the I^2S Bus	0 : Master 1 : Slave	X	X	X
[4]	I2S_WS Mode	WS due to the Sony or Philips format	0 : Sony 1 : Philips	X	X	X
[5]	not used		1 : recommended	X	X	X
[6]	NICAM [1)]	Mode of MSP-Ch1 MSP 3405D: always FM	0 : FM 1 : Nicam	0	1	1
[7]	not used		0 : strongly recommended	0	0	0
[8]	FM AM	Mode of MSP-Ch2	0 : FM 1 : AM	0	0	1
[9]	HDEV	High Deviation Mode (channel matrix must be sound A)	0 : normal 1 : high deviation mode	0	0	0
[11:10]	not used		0 : strongly recommended	0	0	0
[12]	MSP-Ch1 Gain	see Table 6–11	0 : Gain = 6 dB 1 : Gain = 0 dB	0	0	0
[13]	FIR1-Filter Coeff. Set	see Table 6–11	0 : use FIR1 1 : use FIR2	1	0	0
[14]	not used		0 : strongly recommended	0	0	0
[15]	AM-Gain	Gain for AM Demodulation	0 : 0 dB (default. of MSPB) 1 : 12 dB (recommended)	1	1	1
[1)] In case of NICAM operation, I^2S slave mode is not possible. In case of I^2S slave mode, no synchronization to NICAM is allowed.				X: not affected by short-programming		

Table 6–9: Channel modes ‘MODE_REG [6, 8, 9]‘

NICAM bit[6]	FM AM bit[8]	HDEV bit[9]	MSP-Ch1	MSP-Ch2
1	0	0	NICAM (undefined sound for MSP 3405D)	FM1
1	1	0		AM
0	0	0	FM2	FM1
0	0	1	–	High Deviation FM

6.5.3. FIR-Parameter

The following data values (see Table 6–10) are to be transferred **8 bits at a time embedded LSB-bound in a 16-bit word**.

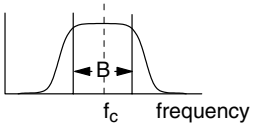
The loading sequences must be obeyed. To change a coefficient set, the complete block FIR1 or FIR2 must be transmitted.

Note: For compatibility with MSP 3410B, IMREG1 and IMREG2 have to be transmitted. The value for IMREG1 and IMREG2 is 004. Due to the partitioning to 8-bit units, the values 04_{hex}, 40_{hex}, and 00_{hex} arise.

Table 6–10: Loading sequence for FIR-coefficients

FIR1 0001_{hex} (MSP-Ch1: NICAM/FM2)			
No.	**Symbol Name**	**Bits**	**Value**
1	NICAM/FM2_Coeff. (5)	8	see Table 6–11
2	NICAM/FM2_Coeff. (4)	8	
3	NICAM/FM2_Coeff. (3)	8	
4	NICAM/FM2_Coeff. (2)	8	
5	NICAM/FM2_Coeff. (1)	8	
6	NICAM/FM2_Coeff. (0)	8	
FIR2 0005_{hex} (MSP-Ch2: FM1/AM)			
No.	**Symbol Name**	**Bits**	**Value**
1	IMREG1	8	04_{hex}
2	IMREG1 / IMREG2	8	40_{hex}
3	IMREG2	8	00_{hex}
4	FM/AM_Coef (5)	8	see Table 6–11
5	FM/AM_Coef (4)	8	
6	FM/AM_Coef (3)	8	
7	FM/AM_Coef (2)	8	
8	FM/AM_Coef (1)	8	
9	FM/AM_Coef (0)	8	

Table 6–11: 8-bit FIR-coefficients (decimal integer) for MSP 34x5D; reset status: all coefficients are “0”

Coefficients for FIR1 0001_{hex} and FIR2 0005_{hex}														
	Terrestrial TV-Standards							**FM - Satellite** FIR filter corresponds to a bandpass with a bandwidth of B = 130 to 500 kHz 						
	B/G-, D/K-NICAM-FM		**I-NICAM-FM**		**L-NICAM-AM**		**B/G-,D/K-, M-Dual FM**	**130 kHz**	**180 kHz**	**200 kHz**	**280 kHz**	**380 kHz**	**500 kHz**	**Auto-search**
Coef(i)	**FIR1**	**FIR2**	**FIR1**	**FIR2**	**FIR1**	**FIR2**	**FIR2**	**FIR2**	**FIR2**	**FIR2**	**FIR2**	**FIR2**	**FIR2**	**FIR2**
0	–2	3	2	3	–2	–4	3	73	9	3	–8	–1	–1	–1
1	–8	18	4	18	–8	–12	18	53	18	18	–8	–9	–1	–1
2	–10	27	–6	27	–10	–9	27	64	28	27	4	–16	–8	–8
3	10	48	–4	48	10	23	48	119	47	48	36	5	2	2
4	50	66	40	66	50	79	66	101	55	66	78	65	59	59
5	86	72	94	72	86	126	72	127	64	72	107	123	126	126
MODE-REG[12]	0		0		0		0	1	1	1	1	1	1	0
MODE-REG[13]	0		0		0		1	1	1	1	1	1	1	0
For compatibility, except for the FIR2-AM and the autosearch sets, the FIR-filter programming as used for the MSP 3410B is also possible.														

6.5.4. DCO-Registers

For a chosen TV standard, a corresponding set of 24-bit registers determining the mixing frequencies of the quadrature mixers, has to be written into the IC. In Table 6–12, some examples of DCO registers are listed. It is necessary to divide them up into low part and high part. The formula for the calculation of the registers for any chosen IF-Frequency is as follows:

$INCR_{dec} = int (f / fs \cdot 2^{24})$

with: int = integer function
f = IF-frequency in MHz
f_S = sampling frequency (18.432 MHz)

Conversion of INCR into hex-format and separation of the 12-bit low and high parts lead to the required register values (DCO1_HI or _LO for MSP-Ch1, DCO2_HI or LO for MSP-Ch2).

6.6. Demodulator Read Registers: Functions and Values

All registers except C_AD_BITs are 8 bit wide. They can be read out of the RAM of the MSP 34x5D.

All transmissions take place in 16-bit words. The valid 8 bit data are the 8 LSBs of the received data word.

To enable appropriate switching of the channel select matrix of the baseband processing part, the NICAM or FM-identification parameters must be read and evaluated by the CCU. The FM-identification registers are described in section 7.2. To handle the NICAM-sound and to observe the NICAM-quality, at least the registers C_AD_BITS and ERROR_RATE must be read and evaluated by the CCU. Additional data bits and CIB bits, if supplied by the NICAM transmitter, can be obtained by reading the registers ADD_BITS and CIB_BITS.

Observing the presence and quality of NICAM can be delegated to the MSP 34x5D, if the automatic switching feature (AUTO_FM, section 6.4.2.) is applied.

Table 6–12: DCO registers for the MSP 34x5D; reset status: DCO_HI/LO = ”0000”

DCO1_LO 0093_{hex}, DCO1_HI $009B_{hex}$; DCO2_LO $00A3_{hex}$, DCO2_HI $00AB_{hex}$					
Freq. [MHz]	**DCO_HI$_{hex}$**	**DCO_LO$_{hex}$**	**Freq. [MHz]**	**DCO_HI$_{hex}$**	**DCO_LO$_{hex}$**
4.5	03E8	000			
5.04 5.5 5.58 5.7421875	0460 04C6 04D8 04FC	0000 038E 0000 00AA	5.76 5.85 5.94	0500 0514 0528	0000 0000 0000
6.0 6.2 6.5 6.552	0535 0561 05A4 05B0	0555 0C71 071C 0000	6.6 6.65 6.8	05BA 05C5 05E7	0AAA 0C71 01C7
7.02	0618	0000	7.2	0640	0000
7.38	0668	0000	7.56	0690	0000

6.6.1. Autodetect of Terrestrial TV-Audio Standards

By means of autodetect, the MSP 34x5D offers a simple and fast (<0.5 s) facility to detect the actual TV-audio standard. The algorithm checks for the FM-mono and NICAM carriers of all common TV-Sound Standards. The following notes must be considered when applying the autodetect feature:

1. Since there is no way to distinguish between AM and FM-carrier, a carrier detected at 6.5 MHz is interpreted as an AM-carrier. If video detection results in SECAM-East, the MSPD result "9" of autodetect must be reinterpreted as "B_{hex}" in case of CAD_BITS[0] = 1, or as "4" or "5" by using the demodulator short programming mode. A simple decision can be made between the two D/K FM-stereo standards by setting D/K1 and D/K2 using the short programming mode and checking the identification of both versions (see Table 6–13).
2. During active autodetect, I^2C-transfers are not recommended except for reading the autodetect result. Under no circumstances should the following parameters: Prescale FM/AM, FM Matrix, Deemphasis FM, Quasi-Peak Detector Source, and Quasi-Peak Detector Matrix be written. Results exceeding $07FF_{hex}$ indicate an active autodetect.
3. The results are to be understood as static information, i.e. no evaluation of FM or NICAM identification concerning the dynamic mode (stereo, bilingual, or mono) are done.
4. Before switching to autodetect, the audio processing part should be muted. Do not forget to demute after having received the result.

Table 6–13: Result of Autodetection

<table>
<tr><th colspan="4">Result of Autodetect 007E$_{hex}$</th></tr>
<tr><th>Code
(Data) hex</th><th colspan="3">Detected TV-Sound Standard
Note: After detection the detected standard is set automatically according to Table 6–3.</th></tr>
<tr><td>>07FF</td><td colspan="3">autodetect still active</td></tr>
<tr><td>0000</td><td colspan="3">no TV Sound Standard was detected; select sound standard manually</td></tr>
<tr><td>0002</td><td colspan="3">M Dual-FM, even if only FM1 is available</td></tr>
<tr><td>0003</td><td colspan="3">B/G Dual-FM, even if only FM1 is available</td></tr>
<tr><td>0008</td><td colspan="3">B/G-FM-NICAM, only if NICAM is available (MSP 3415D only)</td></tr>
<tr><td rowspan="5">0009</td><td colspan="3">L_AM-NICAM, whenever a 6.5 MHz carrier is detected, even if NICAM is not available.
If also D/K might be possible a decision has to be made according to the video-mode:</td></tr>
<tr><td rowspan="4">Video = SECAM_L → no more activities necessary</td><td colspan="2">Video = SECAM_EAST</td></tr>
<tr><td>CAD_BITS[0] = 0</td><td>CAD_BITS[0] = 1</td></tr>
<tr><td colspan="2">To be set by means of the
short programming mode:</td></tr>
<tr><td>D/K1 or D/K2
see section 6.6.1.</td><td>D/K-NICAM
(standard 000B$_{hex}$)</td></tr>
<tr><td>000A</td><td colspan="3">I-FM-NICAM, even if NICAM is not available</td></tr>
<tr><td colspan="4">Note: Similar as for the Demodulator Short-Programming, the Autodetection does not affect most of the parameters of the DSP section (Audio Baseband Processing): The following exceptions are to be considered:
– identification mode: Autodetection resets and sets the corresponding identification mode.
– Prescale FM/AM and FM matrix and Deemphasis FM are undefined after Autodetection.</td></tr>
</table>

6.6.2. C_AD_BITS (MSP 3415D only)

NICAM operation mode control bits and A[2...0] of the additional data bits.

Format:

MSB				C_AD_BITS 0023_{hex}					LSB
11	...	7	6	5	4	3	2	1	0
Auto _FM	...	A[2]	A[1]	A[0]	C4	C3	C2	C1	S

Important: “S” = Bit [0] indicates correct NICAM-synchronization (S=1). If S = 0, the MSP 34x5D has not yet synchronized correctly to frame and sequence, or has lost synchronization. The remaining read registers are therefore not valid. The MSP 34x5D mutes the NICAM output automatically and tries to synchronize again as long as MODE_REG[6] is set.

The operation mode is coded by C4-C1 as shown in Table 6–14.

Table 6–14: NICAM operation modes as defined by the EBU NICAM 728 specification

C4	C3	C2	C1	Operation Mode
0	0	0	0	Stereo sound (NICAMA/B), independent mono sound (FM1)
0	0	0	1	Two independent mono signals (NICAMA, FM1)
0	0	1	0	Three independent mono channels (NICAMA, NICAMB, FM1)
0	0	1	1	Data transmission only; no audio
1	0	0	0	Stereo sound (NICAMA/B), FM1 carries same channel
1	0	0	1	One mono signal (NICAMA). FM1 carries same channel as NICAMA
1	0	1	0	Two independent mono channels (NICAMA, NICAMB). FM1 carries same channel as NICAMA
1	0	1	1	Data transmission only; no audio
x	1	x	x	Unimplemented sound coding option (not yet defined by EBU NICAM 728 specification)
AUTO_FM: monitor bit for the AUTO_FM Status: 0: NICAM source is NICAM 1: NICAM source is FM				

6.6.3. ADD_BITS [10...3] (MSP 3415D only)

Contains the remaining 8 of the 11 additional data bits. The additional data bits are not yet defined by the NICAM 728 system.

Format:

MSB			ADD_BITS 0038_{hex}				LSB
7	6	5	4	3	2	1	0
A[10]	A[9]	A[8]	A[7]	A[6]	A[5]	A[4]	A[3]

6.6.4. CIB_BITS (MSP 3415D only)

Cib bits 1 and 2 (see NICAM 728 specifications)

Format:

MSB			CIB_BITS $003E_{hex}$				LSB
7	6	5	4	3	2	1	0
x	x	x	x	x	x	CIB1	CIB2

6.6.5. ERROR_RATE (MSP 3415D only)

Average error rate of the NICAM reception in a time interval of 182 ms, which should be close to 0.. The initial and maximum value of ERROR_RATE is 2047. This value is also active, if the NICAM bit of MODE_REG is not set. Since the value is achieved by filtering, a certain transition time (appr. 0.5 sec) is unavoidable. Acceptable audio may have error_rates up to a value of 700int. Individual evaluation of this value by the CCU and an appropriate threshold may define the fallback mode from NICAM to FM/AM-mono in case of poor NICAM reception.

The bit error rate per second (BER) can be calculated by means of the following formula:

$BER = ERROR\_RATE * 12.3*10^{-6} /s$

If the automatic switching feature (AUTO_FM; section 6.4.2. on page 23) is applied, reading of ERROR_RATE can be omitted.

ERROR_RATE	0057_{hex}
Error free	0000_{hex}
maximum error rate	$07FF_{hex}$

6.6.6. CONC_CT (for compatibility with MSP 3410B)

This register contains the actual number of bit errors of the previous 728-bit data frame. Evaluation of CONC_CT is no longer recommended.

6.6.7. FAWCT_IST (for compatibility with MSP3410B)

For compatibility with MSP 3410B this value equals 12 as long as NICAM quality is sufficient. It decreases to 0 if NICAM reception gets poor. Evaluation of FAWCT_IST is no longer recommended.

6.6.8. PLL_CAPS

It is possible to read out the actual setting of the PLL_CAPS. In standard applications, this register is not of interest for the customer.

PLL_CAPS	**0021F$_{hex}$**	
minimum frequency	0111 1111	$7F_{hex}$
nominal frequency	0101 0110 RESET	56_{hex}
maximum frequency	0000 0000	00_{hex}

6.6.9. AGC_GAIN

It is possible to read out the actual setting of AGC_GAIN in Automatic Gain Mode. In standard applications, this register is not of interest for the customer.

AGC_GAIN	**0021E$_{hex}$**	
max. amplification (20 dB)	0001 0100	14_{hex}
min. amplification (3 dB)	0000 0000	00_{hex}

6.7. Sequences to Transmit Parameters and to Start Processing

After having been switched on, the MSP has to be initialized by transmitting the parameters according to the LOAD_SEQ_1/2 of Table 6–15. The data are immediately active after transmission into the MSP. It is no longer necessary to transmit LOAD_REG_1/2 or LOAD_REG_1 as it was for MSP 3410B. Nevertheless, transmission of LOAD_REG_1/2 or LOAD_REG_1 does no harm.

For NICAM operation, the following steps listed in 'NICAM_WAIT, _READ and _Check' in Table 6–15 must be taken.

For FM-stereo operation, the evaluation of the identification signal must be performed. For a positive identification check, the MSP 34x5D sound channels have to be switched corresponding to the detected operation mode.

Table 6–15: Sequences to initialize and start the MSP 34x5D

<table>
<tr><td colspan="2">LOAD_SEQ_1/2: General Initialization</td></tr>
<tr><td>General Programming Mode</td><td>Demodulator Short Programming</td></tr>
<tr><td>Write into MSP 34x5D:

1. AD_CV
2. FIR1
3. FIR2
4. MODE_REG
5. DCO1_LO
6. DCO1_HI
7. DCO2_LO
8. DCO2_HI</td><td>Write into MSP 34x5D:

For example: Addr: 0020_{hex}, Data 0008_{hex}
Alternatively, for terrestrial reception, the autodetect feature can be applied.</td></tr>
<tr><td colspan="2">AUDIO PROCESSING INIT</td></tr>
<tr><td colspan="2">Initialization of Audio Baseband Processing section, which may be customer dependant (see section 7.).</td></tr>
<tr><td colspan="2">NICAM_WAIT: Automatic Start of the NICAM-Decoder if Bit[6] of MODE_REG is set to 1</td></tr>
<tr><td colspan="2">1. Wait at least 0.25 s</td></tr>
<tr><td colspan="2">NICAM_CHECK: Read NICAM specific information and check for presence, operation mode, and quality of NICAM signal.
DO NOT read and DO NOT evaluate Stereo Detection register.</td></tr>
<tr><td colspan="2">Read out of MSP 34x5D (For MSP 3405D, all NICAM read registers contain “0”):

1. C_AD_BITS
2. CONC_CT or ERROR_RATE; if AUTO_FM is active, reading of CONC_CT or ERROR_RATE can be omitted.

Evaluation of C_AD_BITS and CONC_CT or ERROR_RATE in the CCU (see section 6.6.).
If necessary, switch the corresponding sound channels within the audio baseband processing section.</td></tr>
<tr><td colspan="2">FM_WAIT: Automatic start of the FM-identification process if Bit[6] of MODE_REG is set to 0.</td></tr>
<tr><td colspan="2">1. Ident Reset
2. Wait at least 0.5 s</td></tr>
<tr><td colspan="2">FM_IDENT_CHECK: Read Stereo Detection register and check for operation mode of dual carrier FM.
DO NOT read and DO NOT evaluate NICAM specific information.</td></tr>
<tr><td colspan="2">Read out of MSP 34x5D:

1. Stereo Detection register (DSP register 0018_{hex}, high part)

Evaluation of the Stereo Detection register (see section 7.5.1.)
If necessary, switch the corresponding sound channels within the audio baseband processing section.</td></tr>
<tr><td colspan="2">LOAD_SEQ_1: Reinitialization of Channel 1 without affecting Channel 2</td></tr>
<tr><td>Write into MSP 34x5D:

1. FIR1 (6 · 8 bit)
2. MODE_REG (12 bit)
3. DCO1_LO (12 bit)
4. DCO1_HI</td><td>Write into MSP 34x5D:

For example: Addr: 0020_{hex}, Data: 0003_{hex}</td></tr>
<tr><td colspan="2">PAUSE: Duration of “Pause” determines the repetition rate of the NICAM or the FM_IDENT-check.</td></tr>
</table>

6.8. Software Proposals for Multistandard TV-Sets

To familiarize the reader with the programming scheme of the MSP 34x5D demodulator part, three examples in the shape of flow diagrams are shown in the following sections.

6.8.1. Multistandard Including System B/G or I (NICAM/FM-Mono only) or SECAM L (NICAM/AM-Mono only)

Fig. 6–1 shows a flow diagram for the CCU software, applied for the MSP 34x5D in a TV set, which facilitates NICAM and FM/AM-mono sound. For the instructions, please refer to Table 6–15.

If the program is changed, resulting in another program within the same TV-sound system, no parameters of the MSP 34x5D need be modified. To facilitate the check for NICAM, the CCU has only to continue at the 'NICAM_WAIT' instruction. During the NICAM-identification process, the MSP 34x5D must be switched to the FM-mono sound.

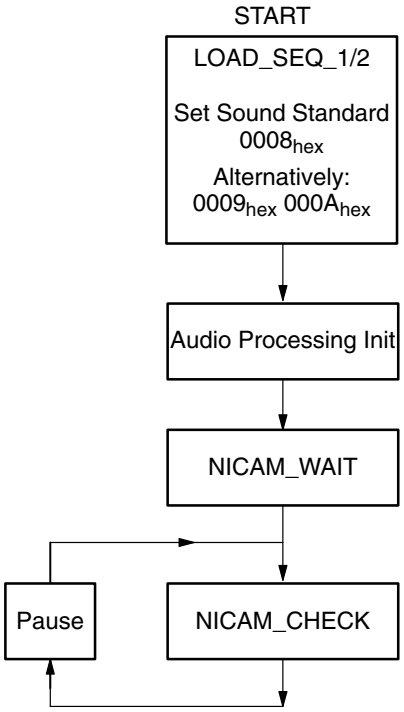


Fig. 6–1: CCU software flow diagram for NICAM/FM or AM mono with Demodulator Short Programming

6.8.2. Multistandard Including System B/G with NICAM/FM-Mono and German DUAL FM

Fig. 6–3 shows a flow diagram for the CCU software, applied for the MSP 34x5D in a TV set, which supports all standards according to System B/G. For the instructions used in the diagram, please refer to Table 6–15.

After having switched on the TV-set and having initialized the MSP 34x5D (LOAD_SEQ_1/2), FM-mono sound is available.

Fig. 6–3 shows that to check for any stereo or bilingual audio information, the sound standards 0008_{hex} (B/G-NICAM) and 0003_{hex} must simply be set alternately. If successful, the MSP 3415D must switch to the desired audio mode.

6.8.3. Satellite Mode

Fig. 6–2 shows the simple flow diagram to be used for the MSP 34x5D in a satellite receiver. For FM-mono operation, the corresponding FM carrier should preferably be processed at the MSP-channel 2.

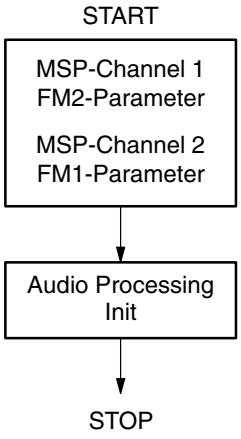


Fig. 6–2: CCU software flow diagram: SAT-mode

6.8.4. Automatic Search Function for FM-Carrier Detection

The AM demodulation ability of the MSP 34x5D offers the possibility to calculate the "field strength" of the momentarily selected FM carrier, which can be read out by the CCU. In SAT receivers, this feature can be used to make automatic FM carrier search possible.

Therefore, the MSPD has to be switched to AM-mode (MODE_REG[8]), FM-Prescale must be set to $7F_{hex} = +127_{dec}$, and the FM DC notch must be switched off. The sound-IF frequency range must now be "scanned" in the MSPD-channel 2 by means of the programmable quadrature mixer with an appropriate incremental frequency (i.e. 10 kHz).

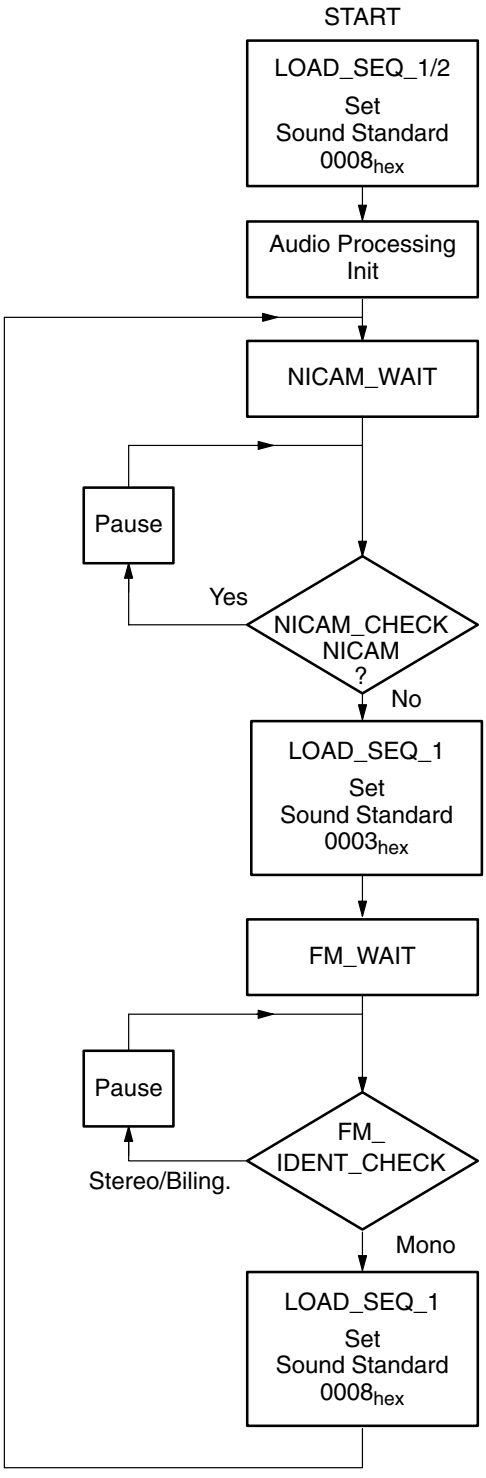


Fig. 6–3: CCU software flow diagram: standard B/G with NICAM or FM stereo with Demodulator Short Programming Mode

After each incrementation, a field strength value is available at the quasi-peak detector output (quasi-peak detector source must be set to FM), which must be examined for relative maxima by the CCU. This results in either continuing search or switching the MSP 34x5D back to FM demodulation mode.

During the search process, the FIR2 must be loaded with the coefficient set “AUTOSEARCH”, which enables small bandwidth, resulting in appropriate field strength characteristics. The absolute field strength value (can be read out of “quasi peak detector output FM1”) also gives information on whether a main FM carrier or a subcarrier was detected, and as a practical consequence, the FM bandwidth (FIR1/2) and the deemphasis (50 µs or adaptive) can be switched automatically.

Due to the fact that a constant demodulation frequency offset of a few kHz, leads to a DC-level in the demodulated signal, further fine tuning of the found carrier can be achieved by evaluating the “DC Level Readout FM1”. Therefore, the FM DC Notch must be switched on, and the demodulator part must be switched back to FM-demodulation mode.

For a detailed description of the automatic search function, please refer to the corresponding MSP 3400C Windows software.

Note: The automatic search is still possible by evaluating only the DC Level Readout FM1 (DC Notch On) as it is described with the MSP 3410B, but the above mentioned method is faster. If this DC Level method is applied with the MSP 34x5D, it is recommended to set MODE_REG[15] to 1 (AM-Gain= 12 dB) and to use the new Autosearch FIR2 coefficient set as given in Table 6–11.

7. Programming the DSP Section (Audio Baseband Processing)

7.1. DSP Write Registers: Table and Addresses

Table 7–1: DSP Write Registers; Subaddress: 12_{hex}; if necessary these registers are readable as well.

DSP Write Register	Address	High/ Low	Adjustable Range, Operational Modes	Reset Mode
Volume loudspeaker channel	0000_{hex}	H	[+12 dB ... –114 dB, MUTE]	MUTE
Volume / Mode loudspeaker channel		L	1/8 dB Steps, Reduce Volume / Tone Control	00_{hex}
Balance loudspeaker channel [L/R]	0001_{hex}	H	[0..100 / 100 % and vv][–127..0 / 0 dB and vv]	100%/100%
Balance Mode loudspeaker		L	[Linear mode / logarithmic mode]	linear mode
Bass loudspeaker channel	0002_{hex}	H	[+12 dB ... –12 dB]	0 dB
Treble loudspeaker channel	0003_{hex}	H	[+12 dB ... –12 dB]	0 dB
Loudness loudspeaker channel	0004_{hex}	H	[0 dB ... +17 dB]	0 dB
Loudness Filter Characteristic		L	[NORMAL, SUPER_BASS]	NORMAL
Spatial effect strength loudspeaker ch.	0005_{hex}	H	[–100%...OFF...+100%]	OFF
Spatial effect mode/customize		L	[SBE, SBE+PSE]	SBE+PSE
Volume SCART1 channel	0007_{hex}	H	[00_{hex} ... $7F_{hex}$],[+12 dB ... –114 dB, MUTE]	00_{hex}
Volume / Mode SCART1 channel		L	[Linear mode / logarithmic mode]	linear mode
Loudspeaker channel source	0008_{hex}	H	[FM/AM, NICAM, SCART, I^2S1, I^2S2]	FM/AM
Loudspeaker channel matrix		L	[SOUNDA, SOUNDB, STEREO, MONO]	SOUNDA
SCART1 channel source	$000A_{hex}$	H	[FM/AM, NICAM, SCART, I^2S1, I^2S2]	FM/AM
SCART1 channel matrix		L	[SOUNDA, SOUNDB, STEREO, MONO]	SOUNDA
I^2S channel source	$000B_{hex}$	H	[FM/AM, NICAM, SCART, I^2S1, I^2S2]	FM/AM
I^2S channel matrix		L	[SOUNDA, SOUNDB, STEREO, MONO]	SOUNDA
Quasi-peak detector source	$000C_{hex}$	H	[FM/AM, NICAM, SCART, I^2S1, I^2S2]	FM/AM
Quasi-peak detector matrix		L	[SOUNDA, SOUNDB, STEREO, MONO]	SOUNDA
Prescale SCART	$000D_{hex}$	H	[00_{hex} ... $7F_{hex}$]	00_{hex}
Prescale FM/AM	$000E_{hex}$	H	[00_{hex} ... $7F_{hex}$]	00_{hex}
FM matrix		L	[NO_MAT, GSTEREO, KSTEREO]	NO_MAT
Deemphasis FM	$000F_{hex}$	H	[OFF, 50 µs, 75 µs, J17]	50 µs
Adaptive Deemphasis FM		L	[OFF, WP1]	OFF
Prescale NICAM (MSP 3415D only)	0010_{hex}	H	[00_{hex} ... $7F_{hex}$]	00_{hex}
Prescale I^2S2	0012_{hex}	H	[00_{hex} ... $7F_{hex}$]	10_{hex}
ACB Register (SCART Switching Facilities)	0013_{hex}	H/L	Bits [15..0]	00_{hex}
Beeper	0014_{hex}	H/L	[00_{hex} ... $7F_{hex}$]/[00_{hex} ... $7F_{hex}$]	0/0
Identification Mode	0015_{hex}	L	[B/G, M]	B/G
Prescale I^2S1	0016_{hex}	H	[00_{hex} ... $7F_{hex}$]	10_{hex}
FM DC Notch	0017_{hex}	L	[ON, OFF]	ON
Automatic Volume Correction	0029_{hex}	H	[off, on, decay time]	OFF

7.2. DSP Read Registers: Table and Addresses

Table 7–2: DSP Read Registers; Subaddress: 13_{hex}; these registers are not writable

DSP Read Register	Address	High/Low	Output Range	
Stereo detection register	0018_{hex}	H	$[80_{hex}$ ... $7F_{hex}]$	8 bit two's complement
Quasi peak readout left	0019_{hex}	H & L	$[00_{hex}$ ... $7FFF_{hex}]$	16 bit two's complement
Quasi peak readout right	$001A_{hex}$	H & L	$[00_{hex}$ ... $7FFF_{hex}]$	16 bit two's complement
DC level readout FM1/Ch2-L	$001B_{hex}$	H & L	$[8000_{hex}$ ... $7FFF_{hex}]$	16 bit two's complement
DC level readout FM2/Ch1-R	$001C_{hex}$	H & L	$[8000_{hex}$ ... $7FFF_{hex}]$	16 bit two's complement
MSP hardware version code	$001E_{hex}$	H	$[00_{hex}$ ... $FF_{hex}]$	
MSP major revision code	$001E_{hex}$	L	$[00_{hex}$ ... $FF_{hex}]$	
MSP product code	$001F_{hex}$	H	$[05_{hex}$, $0F_{hex}]$	
MSP ROM version code	$001F_{hex}$	L	$[00_{hex}$ ... $FF_{hex}]$	

7.3. DSP Write Registers: Functions and Values

Write registers are 16 bit wide, whereby the MSB is denoted bit [15]. Transmissions via I^2C bus have to take place in 16-bit words. Some of the defined 16-bit words are divided into low [7..0] and high [15..8] byte, or in an other manner, thus holding two different control entities. All write registers are readable. Unused parts of the 16-bit registers must be zero. Addresses not given in this table must not be written at any time!

7.3.1. Volume Loudspeaker Channel

Volume Loudspeaker	**0000_{hex}** **[15..4]**	
+12 dB	0111 1111 0000	$7F0_{hex}$
+11.875 dB	0111 1110 1110	$7EE_{hex}$
+0.125 dB	0111 0011 0010	732_{hex}
0 dB	0111 0011 0000	730_{hex}
–0.125 dB	0111 0010 1110	$72E_{hex}$
–113.875 dB	0000 0001 0010	012_{hex}
–114 dB	0000 0001 0000	010_{hex}
Mute	0000 0000 0000 RESET	000_{hex}
Fast Mute	1111 1111 1110	FFE_{hex}

The highest given positive 8-bit number ($7F_{hex}$) yields in a maximum possible gain of 12 dB. Decreasing the volume register by 1 LSB decreases the volume by 1 dB. Volume settings lower than the given minimum mute the output. With large scale input signals, positive volume settings may lead to signal clipping.

The MSP 34x5D loudspeaker volume function is divided up in a digital and an analog section.

With Fast Mute, volume is reduced to mute position by digital volume only. Analog volume is not changed. This reduces any audible DC plops. Going back from Fast Mute should be done to the volume step before Fast Mute was activated.

The Fast Mute facility is activated by the I^2C command. After 75 ms (typically), the signal is completely ramped down.

Clipping Mode Loudspeaker	**0000_{hex}**	**[3..0]**
Reduce Volume	0000 RESET	0_{hex}
Reduce Tone Control	0001	1_{hex}
Compromise Mode	0010	2_{hex}

If the clipping mode is set to “Reduce Volume”, the following clipping procedure is used: To prevent severe clipping effects with bass or treble boosts, the internal volume is automatically limited to a level where, in combination with either bass or treble setting, the amplification does not exceed 12 dB.

If the clipping mode is “Reduce Tone Control”, the bass or treble value is reduced if amplification exceeds 12 dB.

If the clipping mode is “Compromise Mode”, the bass or treble value and volume are reduced half and half if amplification exceeds 12 dB.

Example:	**Vol.: +6 dB**	**Bass: +9 dB**	**Treble: +5 dB**
Red. Volume	3	9	5
Red. Tone Con.	6	6	5
Compromise	4.5	7.5	5

7.3.2. Balance Loudspeaker Channel

Positive balance settings reduce the left channel without affecting the right channel; negative settings reduce the right channel leaving the left channel unaffected. In linear mode, a step by 1 LSB decreases or increases the balance by about 0.8% (exact figure: 100/127). In logarithmic mode, a step by 1 LSB decreases or increases the balance by 1 dB.

Balance Mode Loudspeaker	**0001_{hex}**	**[3..0]**
linear	0000 RESET	0_{hex}
logarithmic	0001	1_{hex}

Linear Mode		
Balance Loudspeaker Channel [L/R]	**0001_{hex}**	**H**
Left muted, Right 100%	0111 1111	$7F_{hex}$
Left 0.8%, Right 100%	0111 1110	$7E_{hex}$
Left 99.2%, Right 100%	0000 0001	01_{hex}
Left 100%, Right 100%	0000 0000 RESET	00_{hex}
Left 100%, Right 99.2%	1111 1111	FF_{hex}
Left 100%, Right 0.8%	1000 0010	82_{hex}
Left 100%, Right muted	1000 0001	81_{hex}

Logarithmic Mode		
Balance Loudspeaker Channel [L/R]	**0001_{hex}**	**H**
Left –127 dB, Right 0 dB	0111 1111	$7F_{hex}$
Left –126 dB, Right 0 dB	0111 1110	$7E_{hex}$
Left –1 dB, Right 0 dB	0000 0001	01_{hex}
Left 0 dB, Right 0 dB	0000 0000 RESET	00_{hex}
Left 0 dB, Right –1 dB	1111 1111	FF_{hex}
Left 0 dB, Right –127 dB	1000 0001	81_{hex}
Left 0 dB, Right –128 dB	1000 0000	80_{hex}

7.3.3. Bass Loudspeaker Channel

Bass Loudspeaker	**0002_{hex}**	**H**
+20 dB	0111 1111	$7F_{hex}$
+18 dB	0111 1000	78_{hex}
+16 dB	0111 0000	70_{hex}
+14 dB	0110 1000	68_{hex}
+12 dB	0110 0000	60_{hex}
+11 dB	0101 1000	58_{hex}
+1 dB	0000 1000	08_{hex}
+1/8 dB	0000 0001	01_{hex}
0 dB	0000 0000 RESET	00_{hex}
–1/8 dB	1111 1111	FF_{hex}
–1 dB	1111 1000	$F8_{hex}$
–11 dB	1010 1000	$A8_{hex}$
–12 dB	1010 0000	$A0_{hex}$

With positive bass settings, internal overflow may occur even with overall volume less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set bass to a value that, in conjunction with volume, would result in an overall positive gain.

7.3.4. Treble Loudspeaker Channel

Treble Loudspeaker	0003_{hex}	H
+15 dB	0111 1000	78_{hex}
+14 dB	0111 0000	70_{hex}
+1 dB	0000 1000	08_{hex}
+1/8 dB	0000 0001	01_{hex}
0 dB	0000 0000 RESET	00_{hex}
–1/8 dB	1111 1111	FF_{hex}
–1 dB	1111 1000	$F8_{hex}$
–11 dB	1010 1000	$A8_{hex}$
–12 dB	1010 0000	$A0_{hex}$

With positive treble settings, internal overflow may occur even with overall volume less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set treble to a value that, in conjunction with volume, would result in an overall positive gain.

7.3.5. Loudness Loudspeaker Channel

Loudness Loudspeaker	0004_{hex}	H
+17 dB	0100 0100	44_{hex}
+16 dB	0100 0000	40_{hex}
+1 dB	0000 0100	04_{hex}
0 dB	0000 0000 RESET	00_{hex}

Mode Loudness Loudspeaker	0004_{hex}	L
Normal (constant volume at 1 kHz)	0000 0000 RESET	00_{hex}
Super Bass (constant volume at 2 kHz)	0000 0100	04_{hex}

Loudness increases the volume of low and high frequency signals, while keeping the amplitude of the 1 kHz reference frequency constant. The intended loudness has to be set according to the actual volume setting. Because loudness introduces gain, it is not recommended to set loudness to a value that, in conjunction with volume, would result in an overall positive gain.

By means of 'Mode Loudness', the corner frequency for bass amplification can be set to two different values. In Super Bass mode, the corner frequency is shifted up. The point of constant volume is shifted from 1 kHz to 2 kHz.

7.3.6. Spatial Effects Loudspeaker Channel

Spatial Effect Strength Loudspeaker	0005_{hex}	H
Enlargement 100%	0111 1111	$7F_{hex}$
Enlargement 50%	0011 1111	$3F_{hex}$
Enlargement 1.5%	0000 0001	01_{hex}
Effect off	0000 0000 RESET	00_{hex}
Reduction 1.5%	1111 1111	FF_{hex}
Reduction 50%	1100 0000	$C0_{hex}$
Reduction 100%	1000 0000	80_{hex}

Spatial Effect Mode Loudspeaker	0005_{hex}	[7:4]
Stereo Basewidth Enlargement (SBE) and Pseudo Stereo Effect (PSE). (Mode A)	0000 RESET 0000	0_{hex} 0_{hex}
Stereo Basewidth Enlargement (SBE) only. (Mode B)	0010	2_{hex}

Spatial Effect Customize Coefficient Loudspeaker	0005_{hex}	[3:0]
max high pass gain	0000 RESET	0_{hex}
2/3 high pass gain	0010	2_{hex}
1/3 high pass gain	0100	4_{hex}
min high pass gain	0110	6_{hex}
automatic	1000	8_{hex}

There are several spatial effect modes available:

Mode A (low byte = 00_{hex}) is compatible to the formerly used spatial effect. Here, the kind of spatial effect depends on the source mode. If the incoming signal is in mono mode, Pseudo Stereo Effect is active; for stereo signals, Pseudo Stereo Effect and Stereo Basewidth Enlargement is effective. The strength of the effect is controllable by the upper byte. A negative value reduces the stereo image. A rather strong spatial effect is recommended for small TV sets where loudspeaker spacing is rather close. For large screen TV sets, a more moderate spatial effect is recommended. In mode A, even in case of stereo input signals, Pseudo Stereo Effect is active, which reduces the center image.

In Mode B, only Stereo Basewidth Enlargement is effective. For mono input signals, the Pseudo Stereo Effect has to be switched on.

It is worth mentioning, that all spatial effects affect amplitude and phase response. With the lower 4 bits, the frequency response can be customized. A value of 0000_{bin} yields a flat response for center signals (L = R) but a high pass function of L or R only signals. A value of 0110_{bin} has a flat response for L or R only signals but a lowpass function for center signals. By using 1000_{bin}, the frequency response is automatically adapted to the sound material by choosing an optimal high pass gain.

7.3.7. Volume SCART1

Volume Mode SCART1	**0007_{hex}**	**[3..0]**
linear	0000 RESET	0_{hex}
logarithmic	0001	1_{hex}

Linear Mode		
Volume SCART1	**0007_{hex}**	**H**
OFF	0000 0000 RESET	00_{hex}
0 dB gain (digital full scale (FS) to 2 V_{RMS} output)	0100 0000	40_{hex}
+6 dB gain (–6 dBFS to 2 V_{RMS} output)	0111 1111	$7F_{hex}$

Logarithmic Mode		
Volume SCART1	**0007_{hex}**	**[15..4]**
+12 dB	0111 1111 0000	$7F0_{hex}$
+11.875 dB	0111 1110 1110	$7EE_{hex}$
+0.125 dB	0111 0011 0010	732_{hex}
0 dB	0111 0011 0000	730_{hex}
–0.125 dB	0111 0010 1110	$72E_{hex}$
–113.875 dB	0000 0001 0010	012_{hex}
–114 dB	0000 0001 0000	010_{hex}
Mute	0000 0000 0000 RESET	000_{hex}

7.3.8. Channel Source Modes

Loudspeaker Source	**0008_{hex}**	**H**
SCART1 Source	**$000A_{hex}$**	**H**
I^2S Source	**$000B_{hex}$**	**H**
Quasi-Peak Detector Source	**$000C_{hex}$**	**H**
FM/AM	0000 0000 RESET	00_{hex}
NICAM (MSP 3415D only)	0000 0001	01_{hex}
SCART	0000 0010	02_{hex}
I^2S1	0000 0101	05_{hex}
I^2S2	0000 0110	06_{hex}

7.3.9. Channel Matrix Modes

Loudspeaker Matrix	**0008_{hex}**	**L**
SCART1 Matrix	**$000A_{hex}$**	**L**
I^2S Matrix	**$000B_{hex}$**	**L**
Quasi-Peak Detector Matrix	**$000C_{hex}$**	**L**
SOUNDA / LEFT / MSP-IF-CHANNEL2	0000 0000 RESET	00_{hex}
SOUNDB / RIGHT / MSP-IF-CHANNEL1	0001 0000	10_{hex}
STEREO	0010 0000	20_{hex}
MONO	0011 0000	30_{hex}

7.3.10. SCART Prescale

Volume Prescale SCART	$000D_{hex}$ H	
OFF	0000 0000 RESET	00_{hex}
0 dB gain (2 V_{RMS} input to digital full scale)	0001 1001	19_{hex}
+14 dB gain (400 mV_{RMS} input to digital full scale)	0111 1111	$7F_{hex}$

Comments for the FM/AM-Prescaling:

For the **High Deviation Mode,** the FM prescaling values can be used in the range from 13_{hex} to 30_{hex}. Please consider the internal reduction of 6 dB for this mode. The FIR-bandwidth should be selected to 500 kHz.

1) Given deviations will result in internal digital full scale signals. Appropriate clipping headroom has to be set by the customer. This can be done by decreasing the listed values by a specific factor.

2) In the mentioned SIF-level range, the AM-output level remains stable and independent of the actual SIF-level. In this case, only the AM degree of audio signals above 40 Hz determines the AM-output level.

7.3.11. FM/AM Prescale

Volume Prescale FM (Normal FM Mode)	$000E_{hex}$ H	
OFF	0000 0000 RESET	00_{hex}
Maximum Volume (28 kHz deviation 1) recommended FIR-bandwidth: 130 kHz)	0111 1111	$7F_{hex}$
Deviation 50 kHz1) recommended FIR-bandwidth: 200 kHz	0100 1000	48_{hex}
Deviation 75 kHz1) recommended FIR-bandwidth: 200 or 280 kHz	0011 0000	30_{hex}
Deviation 150 kHz1) recommended FIR-bandwidth: 380 kHz	0001 1000	18_{hex}
Maximum deviation 192 kHz1) recommended FIR-bandwidth: 380 kHz	0001 0011	13_{hex}
Prescale for adaptive deemphasis WP1 recommended FIR-bandwidth: 130 kHz	0001 0000	10_{hex}
Volume Prescale FM (High Dev.- Mode)	**$000E_{hex}$**	**H**
OFF	0000 0000 RESET	00_{hex}
Deviation 150 kHz1) recommended FIR-bandwidth: 380 kHz	0011 0000	30_{hex}
Maximum deviation 384 kHz1) recommended FIR-bandwidth: 500 kHz	0001 0100	14_{hex}
Volume Prescale AM	**$000E_{hex}$**	**H**
OFF	0000 0000 RESET	00_{hex}
SIF input level: 0.1 Vpp – 0.8 Vpp 1) 2) 0.8 Vpp – 1.4 Vpp 1)	0111 1100	$7C_{hex}$ $<7C_{hex}$
Note: For AM, the bit MODE_REG[15] must be 1.		

7.3.12. FM Matrix Modes

FM Matrix	$000E_{hex}$	L
NO MATRIX	0000 0000 RESET	00_{hex}
GSTEREO	0000 0001	01_{hex}
KSTEREO	0000 0010	02_{hex}

NO_MATRIX is used for terrestrial mono or satellite stereo sound. GSTEREO dematrixes [(L+R)/2, R] to [L, R] and is used for German dual carrier stereo system (Standard B/G). KSTEREO dematrixes [(L+R)/2, (L–R)/2] to [L, R] and is used for the Korean dual carrier stereo system (Standard M).

7.3.13. FM Fixed Deemphasis

Deemphasis FM	$000F_{hex}$	H
50 µs	0000 0000 RESET	00_{hex}
75 µs	0000 0001	01_{hex}
J17	0000 0100	04_{hex}
OFF	0011 1111	$3F_{hex}$

7.3.14. FM Adaptive Deemphasis

FM Adaptive Deemphasis WP1	$000F_{hex}$	L
OFF	0000 0000 RESET	00_{hex}
WP1	0011 1111	$3F_{hex}$

7.3.15. NICAM Prescale (MSP 3415D only)

Volume Prescale NICAM	0010_{hex}	H
OFF	0000 0000 RESET	00_{hex}
0 dB gain	0010 0000	20_{hex}
+12 dB gain	0111 1111	$7F_{hex}$

7.3.16. NICAM Deemphasis (MSP 3415D only)

A J17 Deemphasis is always applied to the NICAM signal. It is not switchable.

7.3.17. I^2S1 and I^2S2 Prescale

Prescale I^2S1	0016_{hex}	H
Prescale I^2S2	**0012_{hex}**	**H**
OFF	0000 0000	00_{hex}
0 dB gain	0001 0000 RESET	10_{hex}
+18 dB gain	0111 1111	$7F_{hex}$

7.3.18. ACB Register (see Fig. 4–3); [15:14] = 0 !

Definition of Digital Control Output Pins

ACB Register	0013_{hex} [15..14]
D_CTR_OUT0	
low (RESET)	x0
high	x1
D_CTR_OUT1	
low (RESET)	0x
high	1x

Definition of SCART Switching Facilities

ACB Register	0013_{hex} [13..0]
DSP IN	
Selection of Source:	
* SC1_IN_L/R	xx xx00 xx00 0000
MONO_IN	xx xx01 xx00 0000
SC2_IN_L/R	xx xx10 xx00 0000
Mute	xx xx11 xx10 0000
SC1_OUT_L/R	
Selection of Source:	
SC2_IN_L/R	xx 01xx x0x0 0000
MONO_IN	xx 10xx x0x0 0000
SCART1 via D/A	xx 11xx x0x0 0000
SC1_IN_L/R	xx 01xx x1x0 0000
Mute	xx 11xx x1x0 0000

***** = RESET position, which becomes active at the time of the first write transmission on the control bus to the audio processing part (DSP). By writing to the ACB register first, the RESET state can be redefined.
Note: After RESET, SC1_OUT_L/R is undefined!

Note: If “MONO_IN” is selected at the DSP_IN selection, the channel matrix mode of the corresponding output channel(s) must be set to “sound A”.

7.3.19. Beeper

Beeper Volume	0014_{hex}	H
OFF	0000 0000 RESET	00_{hex}
Maximum Volume (full digital scale FDS)	0111 1111	$7F_{hex}$
Beeper Frequency	**0014_{hex}**	**L**
16 Hz (lowest)	0000 0001	01_{hex}
1 kHz	0100 0000	40_{hex}
4 kHz (highest)	1111 1111	FF_{hex}

A squarewave beeper can be added to the loudspeaker channel. The addition point is just before volume adjustment.

7.3.20. Identification Mode

Identification Mode	0015_{hex}	L
Standard B/G (German Stereo)	0000 0000 RESET	00_{hex}
Standard M (Korean Stereo)	0000 0001	01_{hex}
Reset of Ident-Filter	0011 1111	$3F_{hex}$

To shorten the response time of the identification algorithm after a program change between two FM-stereo capable programs, the reset of the ident-filter can be applied.

Sequence:

1. Program change
2. Reset ident-filter
3. Set identification mode back to standard B/G
4. Wait approx. 0.5 sec.
5. Read stereo detection register

7.3.21. FM DC Notch

The DC compensation filter (FM DC Notch) for FM input can be switched off. This is used to speed up the automatic search function (see section 6.8.4.). In normal FM-mode, the FM DC Notch should be switched on.

FM DC Notch	0017_{hex}	L
ON	0000 0000 Reset	00_{hex}
OFF	0011 1111	$3F_{hex}$

7.3.22. Automatic Volume Correction (AVC)

AVC	on/off	0029_{hex}	[15:12]
AVC	off and Reset of int. variables	0000 RESET	0_{hex}
AVC	on	1000	8_{hex}
AVC	**Decay Time**	**0029_{hex}**	**[11:8]**
8 sec	(long)	1000	8_{hex}
4 sec	(middle)	0100	4_{hex}
2 sec	(short)	0010	2_{hex}
20 ms	(very short)[1)]	0001	1_{hex}

[1)] intended for quick adaptation to the average volume level after channel change

Different sound sources (e.g. terrestrial channels, SAT channels, or SCART) fairly often do not have the same volume level. Advertisements during movies usually have a higher volume level than the movie itself. This results in annoying volume changes. The AVC solves this problem by equalizing the volume level.

To prevent clipping, the AVC's gain decreases quickly in dynamic boost conditions. To suppress oscillation effects, the gain increases rather slowly for low-level inputs. The decay time is programmable by the AVC register bits [11:8].

For input signals ranging from –24 dBr to 0 dBr, the AVC maintains a fixed output level of –18 dBr. Fig. 7–1 shows the AVC output level versus its input level. For prescale and volume registers set to 0 dB, a level of 0 dBr corresponds to full scale input/output. This is

– SCART in-, output 0 dBr = 2.0 V_{rms}

– Loudspeaker and Aux output 0 dBr = 1.4 Vrms

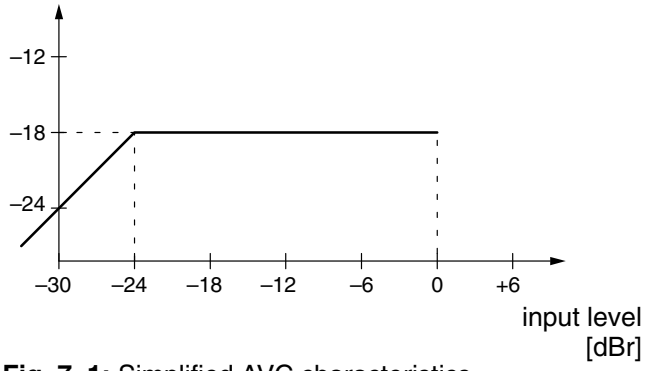


Fig. 7–1: Simplified AVC characteristics

To reset the internal variables, the AVC should be switched off and on during any channel or source change. For standard applications, the recommended decay time is 4 sec.

Note: AVC should not be used in any Dolby Pro Logic mode.

7.4. Exclusions for the Audio Baseband Features

In general, all functions can be switched independently of the others. One exception exists:

1. NICAM cannot be processed simultaneously with the FM2 channel (MSP 3415D only).
2. FM adaptive deemphasis WPI cannot be processed simultaneously with the FM-identification.

7.5. DSP Read Registers: Functions and Values

All readable registers are 16-bit wide. Transmissions via I^2C bus have to take place in 16-bit words. Single data entries are 8 bit. Some of the defined 16-bit words are divided into low and high byte, thus holding two different control entities.

These registers are not writeable.

7.5.1. Stereo Detection Register

Stereo Detection Register	**0018_{hex} H**
Stereo/Bilingual Mode	Reading ID-level (two's complement)
MONO	near zero
STEREO	positive value (ideal reception: $7F_{hex}$)
BILINGUAL	negative value (ideal reception: 80_{hex})

If FM Adaptive Deemphasis WP1 is active, the ID-level in Stereo Detection Register is not valid.

A control processor evaluating the content of the Stereo Detection Register (ID-level), should use the threshold recommendations, shown in Fig. 7–2 for switching to Stereo/Bilingual and back to Mono mode.

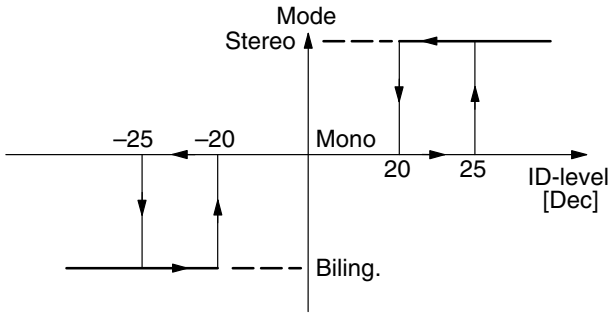


Fig. 7–2: Recommended thresholds for Stereo/ Mono/Bilingual switching

7.5.2. Quasi-Peak Detector

Quasi-Peak Readout Left	**0019_{hex} H+L**
Quasi-Peak Readout Right	**$001A_{hex}$ H+L**
Quasi peak readout	$[0_{hex}$ ... $7FFF_{hex}]$ values are 16 bit two's complement

The quasi peak readout register can be used to read out the quasi peak level of any input source, in order to adjust all inputs to the same normal listening level. The refresh rate is 32 kHz. The feature is based on a filter time constant:

attack-time: 1.3 ms
decay-time: 37 ms

7.5.3. DC Level Register

DC Level Readout FM1 (MSP-Ch2)	$001B_{hex}$ H+L
DC Level Readout FM2 (MSP-Ch1)	**$001C_{hex}$ H+L**
DC Level	[8000_{hex} ... $7FFF_{hex}$] values are 16 bit two's complement

The DC level register measures the DC component of the incoming FM signals (FM1 and FM2). This can be used for seek functions in satellite receivers and for IF FM frequencies fine tuning. A too low demodulation frequency (DCO) results in a positive DC-Level and vice versa. For further processing, the DC content of the demodulated FM signals is suppressed. The time constant τ, defining the transition time of the DC Level Register, is approximately 28 ms.

7.5.4. MSP Hardware Version Code

Hardware Version	$001E_{hex}$ H
Hardware Version	[00_{hex} ... FF_{hex}]
MSP 34x5D – **A**2	01_{hex}
MSP 34x5D – **B**3	02_{hex}

A change in the hardware version code defines hardware optimizations that may have influence on the chip's behavior. The readout of this register is identical to the hardware version code in the chip's imprint.

7.5.5. MSP Major Revision Code

Major Revision	$001E_{hex}$ L
MSP 34x5**D**	04_{hex}

The MSP 34x5D is the fourth generation of ICs in the MSP family.

7.5.6. MSP Product Code

Product	$001F_{hex}$ H
MSP 34**05**D	05_{hex}
MSP 34**15**D	$0F_{hex}$

By means of the MSP-Product Code, the control processor is able to decide whether or not NICAM-controlling should be accomplished.

7.5.7. MSP ROM Version Code

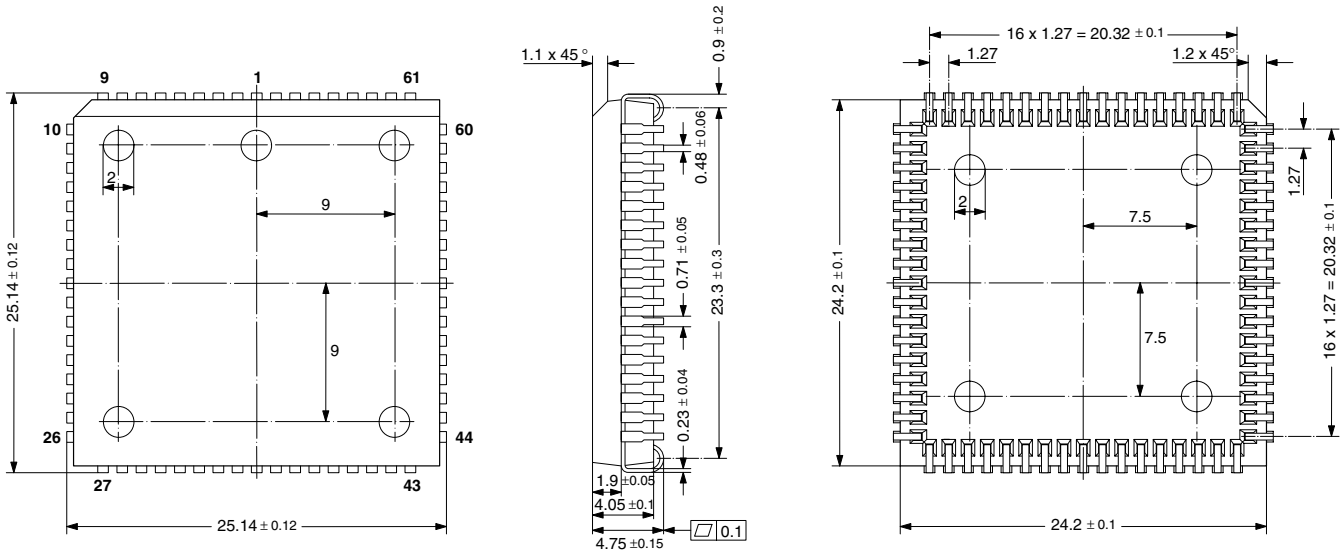
ROM Version	$001F_{hex}$ L
Major software revision	[00_{hex} ... FF_{hex}]
MSP 34x5D – A**2**	22_{hex}
MSP 34x5D – B**3**	23_{hex}

A change in the ROM version code defines internal software optimizations, that may have influence on the chip's behavior, e.g. new features may have been included. While a software change is intended to create no compatibility problems, customers that want to use the new functions can identify new MSP 34x5D versions according to this number.

To avoid compatibility problems with the MSPB series, an offset of 20_{hex} is added to the ROM version code of the chip's imprint.

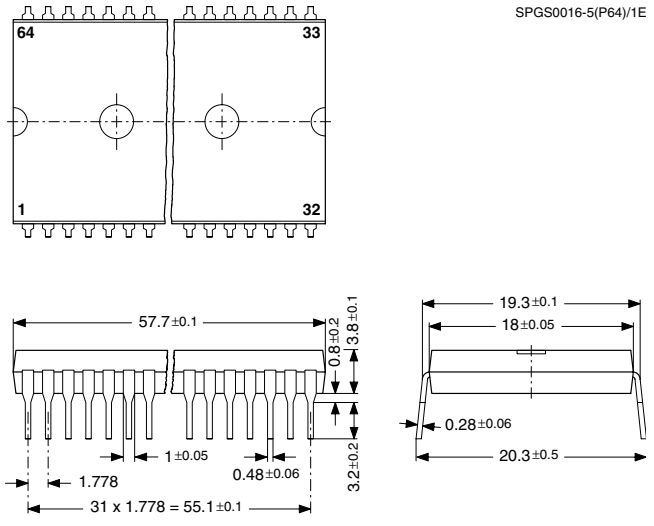
8. Specifications

8.1. Outline Dimensions



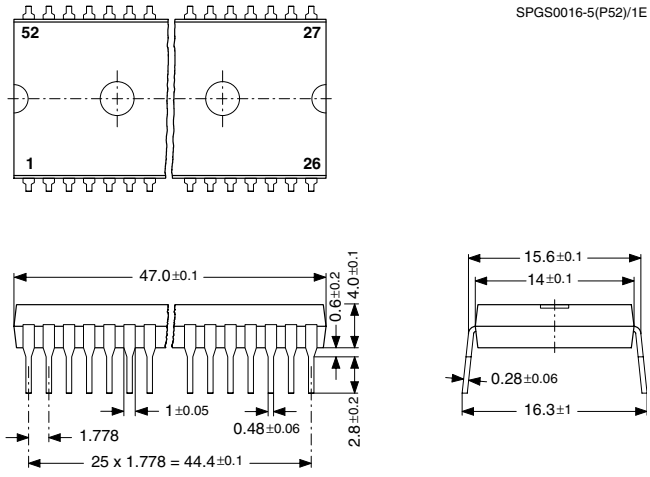
SPGS0027-2(P68)/1E

Fig. 8–1:
68-Pin Plastic Leaded Chip Carrier Package
(PLCC68)
Weight approximately 4.8 g
Dimensions in mm



SPGS0016-5(P64)/1E

Fig. 8–2:
64-Pin Plastic Shrink Dual Inline Package
(PSDIP64)
Weight approximately 9.0 g
Dimensions in mm



SPGS0016-5(P52)/1E

Fig. 8–3:
52-Pin Plastic Shrink Dual In Line Package
(PSDIP52)
Weight approximately 5.5 g
Dimensions in mm

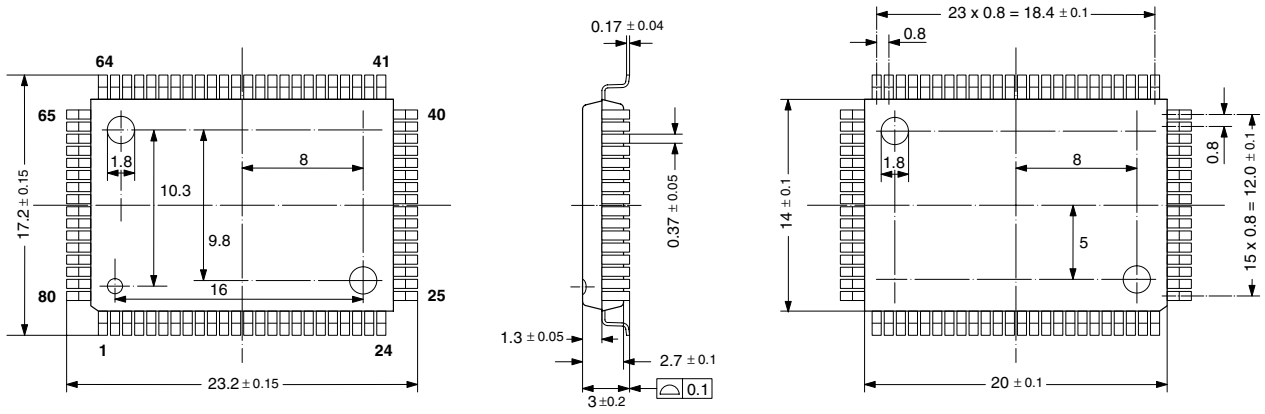


Fig. 8–4:
80-Pin Plastic Quad Flat Package
(PQFP80)
Weight approximately 1.61 g
Dimensions in mm

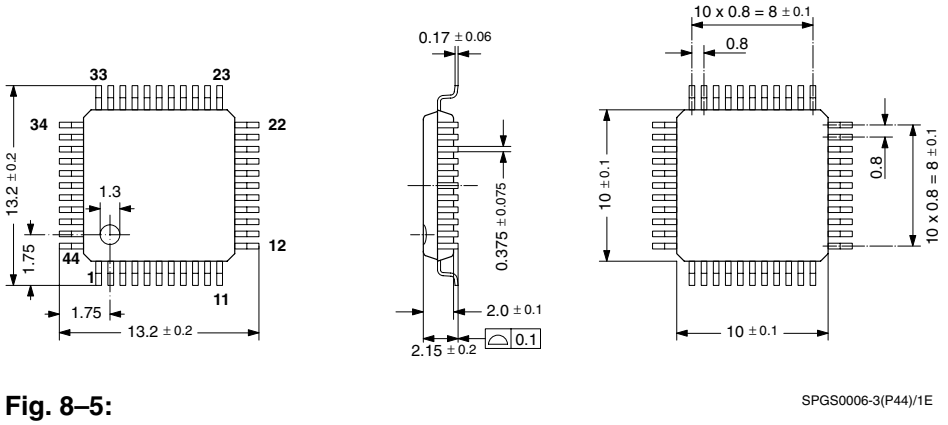


Fig. 8–5:
44-Pin Plastic Metric Quad Flat Package
(PMQFP44)
Weight approx. 0.4 g
Dimensions in mm

8.2. Pin Connections and Short Descriptions

NC = not connected (**leave vacant** for future compatibility reasons)
TP = Test Pin (**leave vacant**; pin is used for production test only)
LV = leave vacant
X = obligatory; connect as described in application circuit diagram

Pin No.					Pin Name	Type	Connection (if not used)	Short Description
PLCC 68-pin	PSDIP 64-pin	PSDIP 52-pin	PQFP 80-pin	PMQFP 44-pin				
1	16	14	9	–	TP	OUT	LV	Test pin
2	–	–	–	–	NC		LV	Not connected
3	15	13	8	–	TP	OUT	LV	Test pin
4	14	12	7	17	I2S_DA_IN1	IN	LV	I^2S1 data input
5	13	11	6	16	I2S_DA_OUT	OUT	LV	I^2S data output
6	12	10	5	15	I2S_WS	IN/OUT	LV	I^2S word strobe
7	11	9	4	14	I2S_CL	IN/OUT	LV	I^2S clock
8	10	8	3	13	I2C_DA	IN/OUT	X	I^2C data
9	9	7	2	12	I2C_CL	IN/OUT	X	I^2C clock
10	8	–	1	–	NC		LV	Not connected
11	7	6	80	11	STANDBYQ	IN	X	Standby (low-active)
12	6	5	79	10	ADR_SEL	IN	X	I^2C Bus address select
13	5	4	78	9	D_CTR_OUT0	OUT	LV	Digital control output 0
14	4	3	77	8	D_CTR_OUT1	OUT	LV	Digital control output 1
15	3	–	76	–	NC		LV	Not connected
16	2	–	75	–	NC		LV	Not connected
17	–	–	–	–	NC		LV	Not connected
18	1	2	74 [1)]	–	NC		LV	Not connected
19	64	1	73	7	TP		LV	Test pin
20	63	52	72	6	XTAL_OUT	OUT	X	Crystal oscillator
21	62	51	71	5	XTAL_IN	IN	X	Crystal oscillator
22	61	50	70	4	TESTEN	IN	X	Test pin
23	60	49	69	–	NC		LV	Not connected
24	59	48	68	3	ANA_IN–	IN	LV	IF common
25	58	47	67	2	ANA_IN1+	IN	LV	IF input 1
26	57	46	66	1	AVSUP		X	Analog power supply +5 V
–	–	–	65	–	AVSUP		X	Analog power supply +5 V
–	–	–	64	–	NC		LV	Not connected
–	–	–	63	–	NC		LV	Not connected

Pin No.					Pin Name	Type	Connection (if not used)	Short Description
PLCC 68-pin	PSDIP 64-pin	PSDIP 52-pin	PQFP 80-pin	PMQFP 44-pin				
27	56	45	62	44	AVSS		X	Analog ground
–	–	–	61	–	AVSS		X	Analog ground
28	55	44	60	43	MONO_IN	IN	LV	Mono input
–	–	–	59	–	NC		LV	Not connected
29	54	43	58	42	VREFTOP		X	Reference voltage IF A/D converter
30	53	42	57	41	SC1_IN_R	IN	LV	Scart 1 input, right
31	52	41	56	40	SC1_IN_L	IN	LV	Scart 1 input, left
32	51	–	55	39	ASG1		AHVSS	Analog shield ground 1
33	50	40	54	38	SC2_IN_R	IN	LV	Scart 2 input, right
34	49	39	53	37	SC2_IN_L	IN	LV	Scart 2 input, left
35	48	–	52 [1)]	–	NC		LV or AHVSS	Not connected
36	47	38	51	–	NC		LV	Not connected
37	46	37	50	–	NC		LV	Not connected
38	45	–	49	–	NC		LV	Not connected
39	44	–	48	–	NC		LV	Not connected
40	43	–	47	–	NC		LV	Not connected
41	–	–	46	–	NC		LV	Not connected
42	42	36	45	36	AGNDC		X	Analog reference voltage high voltage part
43	41	35	44	35	AHVSS		X	Analog ground
–	–	–	43	–	AHVSS		X	Analog ground
–	–	–	42	–	NC		LV	Not connected
–	–	–	41	–	NC		LV	Not connected
44	40	34	40	34	CAPL_M		X	Volume capacitor MAIN
45	39	33	39	33	AHVSUP		X	Analog power supply +8 V
46	38	32	38	32	NC		LV	Not connected
47	37	31	37	31	SC1_OUT_L	OUT	LV	Scart 1 output, left
48	36	30	36	30	SC1_OUT_R	OUT	LV	Scart 1 output, right
49	35	29	35	29	VREF1		X	Reference ground 1 high voltage part
50	34	28	34	28	NC		LV	Not connected
51	33	27	33	–	NC		LV	Not connected
52	–	–	32	–	NC		LV	Not connected

Pin No. PLCC 68-pin	PSDIP 64-pin	PSDIP 52-pin	PQFP 80-pin	PMQFP 44-pin	Pin Name	Type	Connection (if not used)	Short Description
53	32	–	31	–	NC		LV	Not connected
54	31	26	30	–	NC		LV	Not connected
55	30	–	29	–	NC		LV	Not connected
56	29	25	28	27	DACM_L	OUT	LV	Loudspeaker out, left
57	28	24	27	26	DACM_R	OUT	LV	Loudspeaker out, right
58	27	23	26	25	VREF2		X	Reference ground 2 high voltage part
59	26	22	25	24	NC		LV	Not connected
60	25	21	24	23	NC		LV	Not connected
–	–	–	23	–	NC		LV	Not connected
–	–	–	22	–	NC		LV	Not connected
61	24	20	21	22	RESETQ	IN	X	Power-on-reset
62	23	–	20	–	NC		LV	Not connected
63	22	–	19	–	NC		LV	Not connected
64	21	19	18	–	NC		LV	Not connected
65	20	18	17	21	I2S_DA_IN2	IN	LV	I^2S2 data input
66	19	17	16	–	DVSS		X	Digital ground
–	–	–	15	–	DVSS		X	Digital ground
–	–	–	14	20	DVSS		X	Digital ground
67	18	16	13	19	DVSUP		X	Digital power supply +5 V
–	–	–	12	–	DVSUP		X	Digital power supply +5 V
–	–	–	11	–	DVSUP		X	Digital power supply +5 V
68	17	15	10	18	TP_CO	OUT	LV	Test pin (Use this pin to define the capacitor size at crystal oscillator.)

1) **Note:** For PQFP80 package ONLY and for A2 version ONLY, the following pin-allocation is valid:
Pin 74 = TP, Pin 52 = ASG2

8.3. Pin Configurations

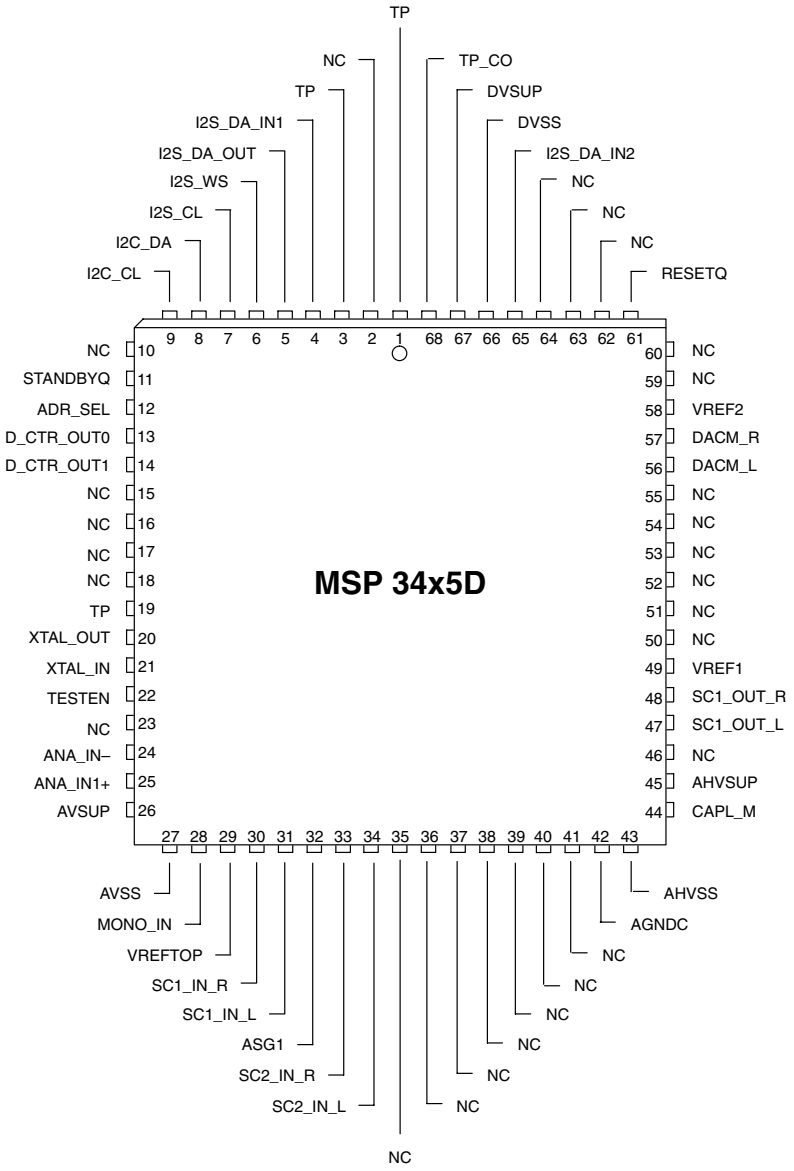


Fig. 8–6: 68-pin PLCC package

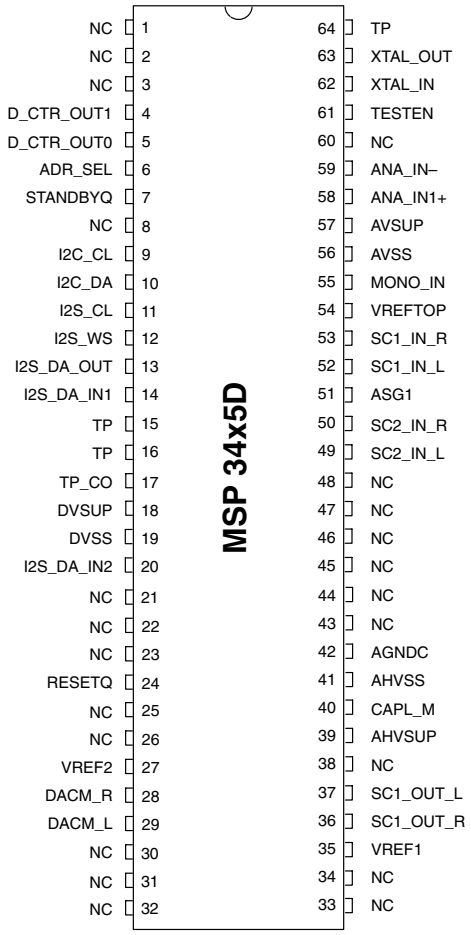


Fig. 8–7: 64-pin PSDIP package

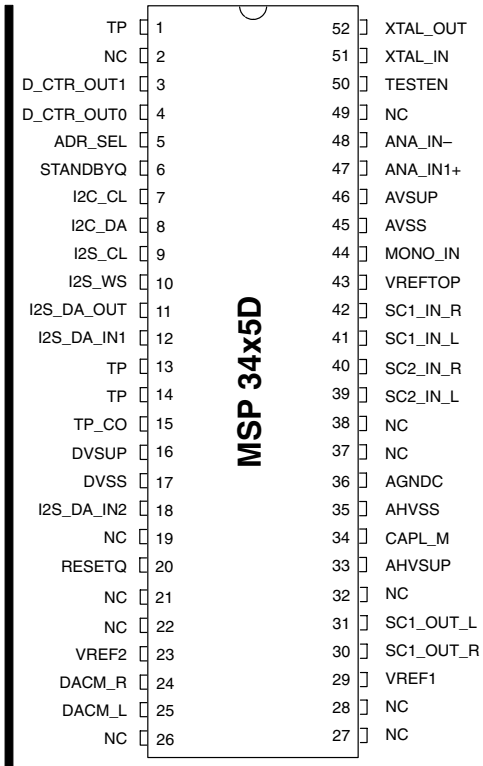


Fig. 8–8: 52-pin PSDIP package

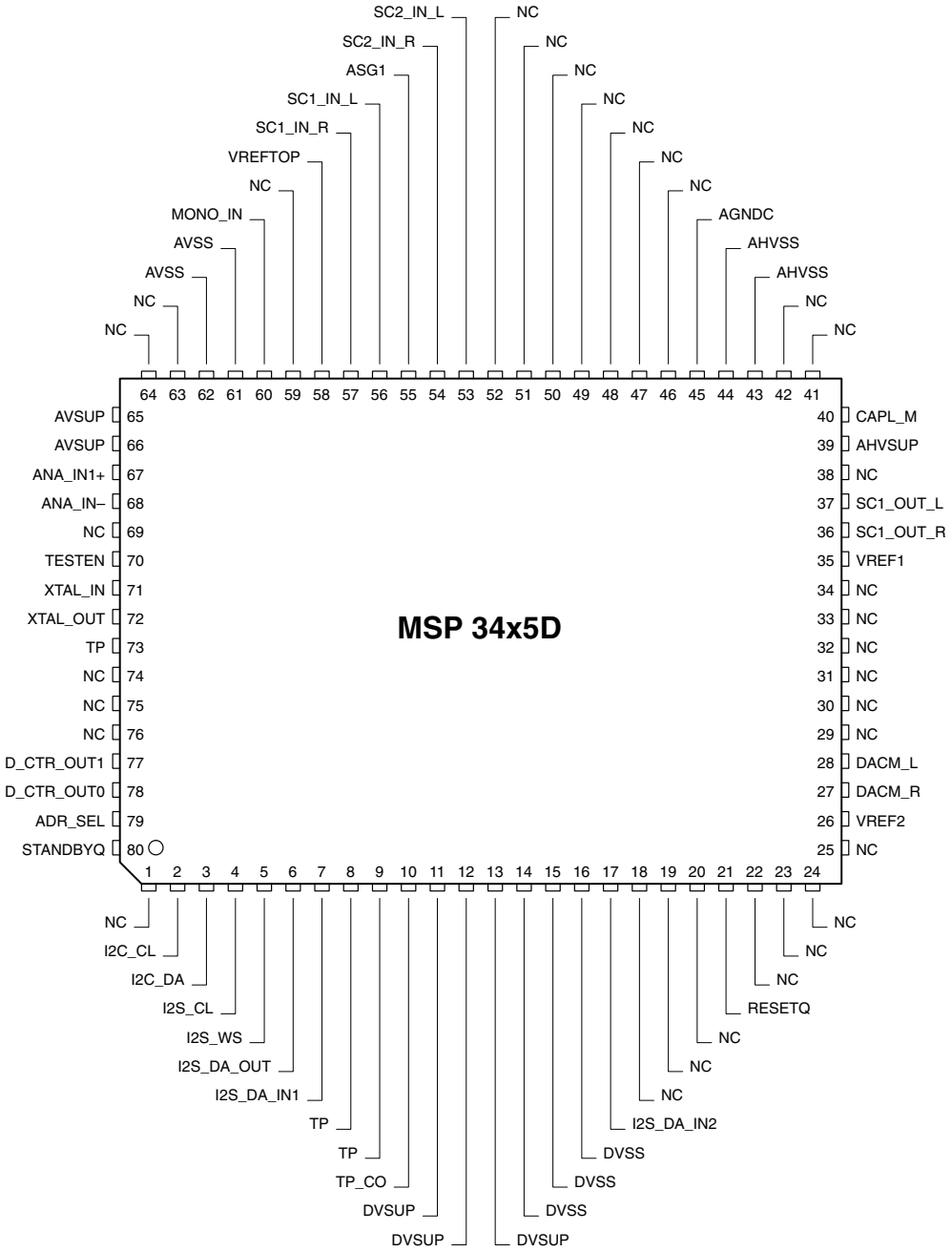


Fig. 8–9: 80-pin PQFP package

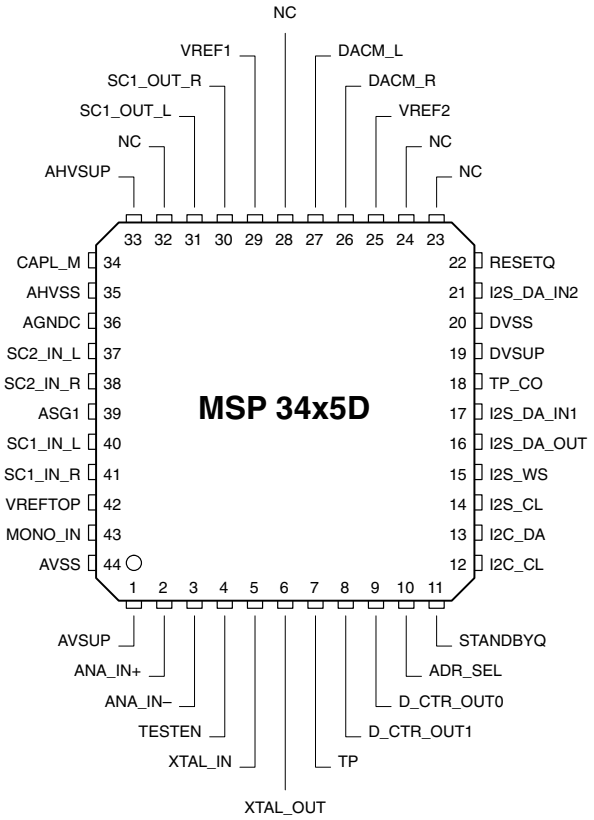


Fig. 8–10: 44-pin PMQFP package

8.4. Pin Circuits (pin numbers refer to PLCC68 package)

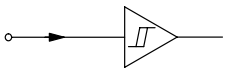


Fig. 8–11: Input Pins 4, 11, 12, 61, and 65 (I2S_DA_IN1, STANDBYQ, ADR_SEL, RESETQ, and I2S_DA_IN2)

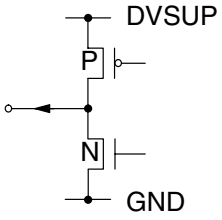


Fig. 8–12: Output pins 5, 13, 14, and 68 (I2S_DA_OUT, D_CTR_OUT0/1, TP_CO)

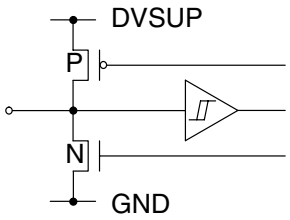


Fig. 8–13: Input/Output pins 6 and 7 (I2S_WS, I2S_CL)

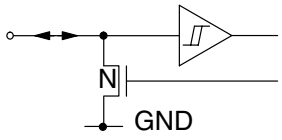


Fig. 8–14: Input/Output Pins 8 and 9 (I2C_DA, I2C_CL)

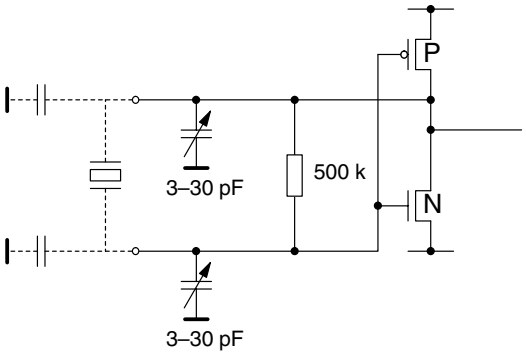


Fig. 8–15: Input/Output Pins 20 and 21 (XTAL_OUT/IN)

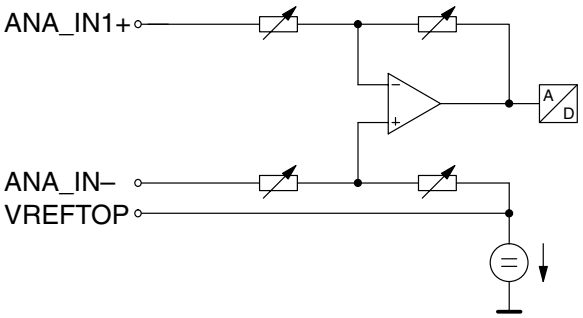


Fig. 8–16: Input Pins 24, 25, and 29 (ANA_IN–, ANA_IN1+, VREFTOP)

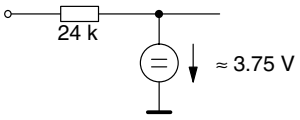


Fig. 8–17: Input Pin 28 (MONO_IN)

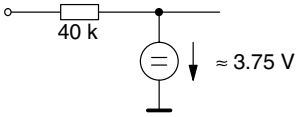


Fig. 8–18: Input Pins 30, 31, 33, and 34 (SC1–2_IN_L/R)

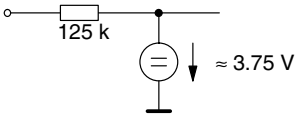


Fig. 8–19: Pin 42 (AGNDC)

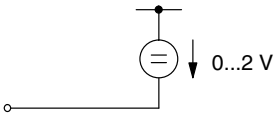


Fig. 8–20: Capacitor Pin 44 (CAPL_M)

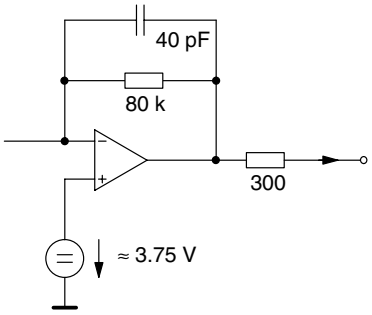


Fig. 8–21: Output Pins 47, 48 (SC1_OUT_L/R)

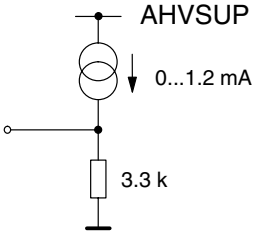


Fig. 8–22: Output Pins 56, 57 (DACM_L/R)

8.5. Electrical Characteristics

8.5.1. Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	70[1)]	°C
T_S	Storage Temperature	–	–40	125	°C
V_{SUP1}	First Supply Voltage	AHVSUP	–0.3	9.0	V
V_{SUP2}	Second Supply Voltage	DVSUP	–0.3	6.0	V
V_{SUP3}	Third Supply Voltage	AVSUP	–0.3	6.0	V
dV_{SUP23}	Voltage between AVSUP and DVSUP	AVSUP, DVSUP	–0.5	0.5	V
P_{TOT}	Package Power Dissipation PLCC68 without Heat Spreader PSDIP64 without Heat Spreader PSDIP52 without Heat Spreader PMQFP44 without Heat Spreader	AHVSUP, DVSUP, AVSUP		 1200 1300 1200 910[1)]	mW
V_{Idig}	Input Voltage, all Digital Inputs		–0.3	V_{SUP2}+0.3	V
I_{Idig}	Input Current, all Digital Pins	–	–20	+20	mA[2)]
V_{Iana}	Input Voltage, all Analog Inputs	SCn_IN_s,[3)] MONO_IN	–0.3	V_{SUP1}+0.3	V
I_{Iana}	Input Current, all Analog Inputs	SCn_IN_s,[3)] MONO_IN	–5	+5	mA[2)]
I_{Oana}	Output Current, all SCART Outputs	SC1_OUT_s	[4)], [5)]	[4)], [5)]	
I_{Oana}	Output Current, all Analog Outputs except SCART Outputs	DACM_s[3)]	[4)]	[4)]	
I_{Cana}	Output Current, other pins connected to capacitors	CAPL_M AGNDC	[4)]	[4)]	

1) For PMQFP44 package, max. ambient operating temperature is 65 °C.
2) positive value means current flowing into the circuit
3) “n” means “1” or “2”, “s” means “L” or “R”
4) The Analog Outputs are short circuit proof with respect to First Supply Voltage and Ground.
5) Total chip power dissipation must not exceed absolute maximum rating.

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

8.5.2. Recommended Operating Conditions

(at T_A = 0 to 70 °C)

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
V_{SUP1}	First Supply Voltage	AHVSUP	7.6	8.0	8.7[1)]	V
V_{SUP2}	Second Supply Voltage	DVSUP	4.75	5.0	5.25	V
V_{SUP3}	Third Supply Voltage	AVSUP	4.75	5.0	5.25	V
V_{RLH}	RESET Input Low-to-High Transition Voltage	RESETQ	0.7		0.8	DVSUP
V_{RHL}	RESET Input High-to-Low Transition Voltage *(see also Fig. 5–3 on page 19)*		0.45		0.55	DVSUP
V_{DIGIL}	Digital Input Low Voltage	ADR_SEL			0.2	V_{SUP2}
V_{DIGIH}	Digital Input High Voltage		0.8			V_{SUP2}
V_{DIGIL}	Digital Input Low Voltage	STANDBYQ			0.2	V_{SUP2}
V_{DIGIH}	Digital Input High Voltage MSP 34x5D version A1, A2 MSP 34x5D version B3 and later		 0.8 0.5			 V_{SUP2} V_{SUP2}
t_{STBYQ1}	STANDBYQ Setup Time before Turn-off of Second Supply Voltage	STANDBYQ, DVSUP	1			µs
I^2C-Bus Recommendations						
V_{I2CIL}	I^2C-Bus Input Low Voltage	I2C_CL, I2C_DA			0.3	V_{SUP2}
V_{I2CIH}	I^2C-Bus Input High Voltage		0.6			V_{SUP2}
t_{I2C1}	I^2C Start Condition Setup Time		120			ns
t_{I2C2}	I^2C Stop Condition Setup Time		120			ns
t_{I2C5}	I^2C-Data Setup Time before Rising Edge of Clock		55			ns
t_{I2C6}	I^2C-Data Hold Time after Falling Edge of Clock		55			ns
t_{I2C3}	I^2C-Clock Low Pulse Time	I2C_CL	500			ns
t_{I2C4}	I^2C-Clock High Pulse Time		500			ns
f_{I2C}	I^2C-Bus Frequency				1.0	MHz

[1)] For MSP 34x5D-A1 and -A2 versions in PMQFP44 package, only 8.4 V is allowed.

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
I²S-Bus Recommendations						
V_{I2SIH}	I²S-Data Input Low Voltage MSP 34x5D version A1, A2 MSP 34x5D version B3 and later	I2S_DA_IN1/2			 0.25 0.2	 V_{SUP2} V_{SUP2}
V_{I2SIL}	I²S-Data Input High Voltage MSP 34x5D version A1, A2 MSP 34x5D version B3 and later		 0.75 0.5			 V_{SUP2} V_{SUP2}
t_{I2S1}	I²S-Data Input Setup Time before Rising Edge of Clock	I2S_DA_IN1/2 I2S_CL	20			ns
t_{I2S2}	I²S-Data Input Hold Time after falling Edge of Clock		0			ns
f_{I2SCL}	I²S-Clock Input Frequency when MSP in I²S-Slave Mode	I2S_CL		1.024		MHz
R_{I2SCL}	I²S-Clock Input Ratio when MSP in I²S-Slave Mode		0.9		1.1	
f_{I2SWS}	I²S-Word Strobe Input Frequency when MSP in I²S-Slave Mode	I2S_WS		32.0		kHz
V_{I2SIDL}	I²S-Input Low Voltage when MSP in I²S-Slave Mode MSP 34x5D version A1, A2 MSP 34x5D version B3 and later	I2S_CL I2S_WS			 0.25 0.2	 V_{SUP2} V_{SUP2}
V_{I2SIDH}	I²S-Input High Voltage when MSP in I²S-Slave Mode MSP 34x5D version A1, A2 MSP 34x5D version B3 and later		 0.75 0.5			 V_{SUP2} V_{SUP2}
t_{I2SWS1}	I²S-Word Strobe Input Setup Time before Rising Edge of Clock when MSP in I²S-Slave Mode		60			ns
t_{I2SWS2}	I²S-Word Strobe Input Hold Time after falling Edge of Clock when MSP in I²S-Slave Mode		0			ns

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
General Crystal Recommendations						
f_P	Crystal Parallel Resonance Frequency at 12 pF Load Capacitance			18.432		MHz
R_R	Crystal Series Resistance			8	25	Ω
C_0	Crystal Shunt (Parallel) Capacitance			6.2	7.0	pF
C_L	External Load Capacitance[1)]	XTAL_IN, XTAL_OUT	PSDIP PLCC 3.3 P(M)QFP 3.3		1.5	pF pF pF
Crystal Recommendations for Master-Slave Applications						
f_{TOL}	Accuracy of Adjustment		–20		+20	ppm
D_{TEM}	Frequency Variation vs Temp.		–20		+20	ppm
C_1	Motional (Dynamic) Capacitance		19	24		fF
f_{CL}	Required Open Loop Clock Frequency (T_{amb} = 25 °C)	XTAL_IN, XTAL_OUT	18.431		18.433	MHz
Crystal Recommendations for FM / NICAM Applications (No Master-Slave Mode possible)						
f_{TOL}	Accuracy of Adjustment		–30		+30	ppm
D_{TEM}	Frequency Variation vs Temp.		–30		+30	ppm
C_1	Motional (Dynamic) Capacitance		15			fF
f_{CL}	Required Open Loop Clock Frequency (T_{amb} = 25 °C)	XTAL_IN, XTAL_OUT	18.4305		18.4335	MHz
Crystal Recommendations for FM Applications (No Master-Slave Mode possible)						
f_{TOL}	Accuracy of Adjustment		–100		+100	ppm
D_{TEM}	Frequency Variation versus Temperature		–50		+50	ppm
Amplitude Recommendation for Operation with External Clock Input (C_{load} after reset = 22 pF)						
V_{XCA}	External Clock Amplitude	XTAL_IN	0.7			V_{pp}

1) External capacitors at each crystal pin to ground are required. They are necessary to tune the open-loop frequency of the internal PLL and to stabilize the frequency in closed-loop operation.
Due to different layouts, the accurate capacitor size should be determined with the customer PCB. The suggested values (1.5...3.3 pF) are figures based on experience and should serve as “start value”.

To define the capacitor size, reset the MSP without transmitting any further I^2C telegrams. Set MODE_REG 0083_{hex} Bit [14]=1. Measure the frequency at pin TP_CO (see pin description in table on page 51). Change the capacitor size until the free running frequency at pin TP_CO matches 6.144000 MHz (=18.432000 MHz / 3) as closely as possible. The higher the capacity, the lower the resulting clock frequency.

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
Analog Input and Output Recommendations						
C_{AGNDC}	AGNDC-Filter-Capacitor	AGNDC	–20%	3.3		µF
	Ceramic Capacitor in Parallel		–20%	100		nF
C_{inSC}	DC-Decoupling Capacitor in front of SCART Inputs	SCn_IN_s[1)]	–20%	330	+20%	nF
V_{inSC}	SCART Input Level				2.0	V_{RMS}
V_{inMONO}	Input Level, Mono Input	MONO_IN			2.0	V_{RMS}
R_{LSC}	SCART Load Resistance	SC1_OUT_s[1)]	10			kΩ
C_{LSC}	SCART Load Capacitance				6.0	nF
C_{VMA}	Main Volume Capacitor	CAPL_M		10		µF
C_{FMA}	Main Filter Capacitor	DACM_s[1)]	–10%	1	+10%	nF
Recommendations for Analog Sound IF Input Signal						
$C_{VREFTOP}$	VREFTOP-Filter-Capacitor	VREFTOP	–20%	10		µF
	Ceramic Capacitor in Parallel		–20%	100		nF
F_{IF_FM}	Analog Input Frequency Range	ANA_IN1+, ANA_IN–	0		9	MHz
V_{IF_FM}	Analog Input Range FM/NICAM		0.1	0.8	3	Vpp
V_{IF_AM}	Analog Input Range AM/NICAM		0.1	0.45	0.8	Vpp
R_{FMNI}	Ratio: NICAM Carrier/FM Carrier (unmodulated carriers) BG: I:		 –20 –23	 –7 –10	 0 0	 dB dB
R_{AMNI}	Ratio: NICAM Carrier/AM Carrier (unmodulated carriers)		–25	–11	0	dB dB
R_{FM}	Ratio: FM-Main/FM-Sub Satellite			7		dB
$R_{FM1/FM2}$	Ratio: FM1/FM2 German FM-System			7		dB
R_{FC}	Ratio: Main FM Carrier/ Color Carrier		15	–	–	dB
R_{FV}	Ratio: Main FM Carrier/ Luma Components		15	–	–	dB
PR_{IF}	Passband Ripple		–	–	±2	dB
SUP_{HF}	Suppression of Spectrum Above 9.0 MHz		15		–	dB
FM_{MAX}	Maximum FM-Deviation (apprx.) normal mode high deviation mode				 ±180 ±360	kHz

1) "n" means "1" or "2", "s" means "L" or "R"

8.5.3. Characteristics

at T_A = 0 to 70 °C, f_{CLOCK} = 18.432 MHz, V_{SUP1} = 7.6 to 8.7 V, V_{SUP2} = 4.75 to 5.25 V for min./max. values
at T_A = 60 °C, f_{CLOCK} = 18.432 MHz, V_{SUP1} = 8 V, V_{SUP2} = 5 V for typical values, T_J = Junction Temperature
MAIN (M) = Loudspeaker Channel

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
f_{CLOCK}	Clock Input Frequency	XTAL_IN		18.432		MHz	
D_{CLOCK}	Clock High to Low Ratio		45		55	%	
t_{JITTER}	Clock Jitter (Verification not provided in production test)				50	ps	
V_{xtalDC}	DC-Voltage Oscillator			2.5		V	
$t_{Startup}$	Oscillator Startup Time at VDD Slew-rate of 1 V/1 µs	XTAL_IN, XTAL_OUT		0.4	2	ms	
I_{SUP1A}	First Supply Current (active) Analog Volume for Main and Aux at 0 dB Analog Volume for Main and Aux at –30 dB	AHVSUP	 9.6 6.3	 17.1 11.2	 24.6 16.1	 mA mA	
I_{SUP1S}	First Supply Current (standby mode) at T_j = 27 °C		3.5	5.6	7.7	mA	STANDBYQ = low
I_{SUP2A}	Second Supply Current (active) MSP 34x5D version A1, A2 MSP 34x5D version B3 and later	DVSUP	 86 50	 95 70	 102 85	 mA mA	
I_{SUP3A}	Third Supply Current (active) MSP 34x5D version A1, A2 MSP 34x5D version B3 and later	AVSUP	 15 20	 25 35	 35 45	 mA mA	
Digital Contol Outputs							
V_{DCTROL}	Digital Output Low Voltage	D_CTR_OUT0 D_CTR_OUT1			0.4	V	I_{DCTR} = 1 mA
V_{DCTROH}	Digital Output High Voltage		4.0			V	I_{DCTR} = –1 mA
I^2C-Bus							
V_{I2COL}	I^2C-Data Output Low Voltage	I2C_DA			0.4	V	I_{I2COL} = 3 mA
I_{I2COH}	I^2C-Data Output High Current				1.0	µA	V_{I2COH} = 5 V
t_{I2COL1}	I^2C-Data Output Hold Time after Falling Edge of Clock	I2C_DA, I2C_CL	15			ns	
t_{I2COL2}	I^2C-Data Output Setup Time before Rising Edge of Clock		100			ns	f_{I2C} = 1 MHz

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
I²S-Bus							
V_{I2SOL}	I²S Output Low Voltage	I2S_WS I2S_CL I2S_DA_OUT			0.4	V	I_{I2SOL} = 1 mA
V_{I2SOH}	I²S Output High Voltage		4.0			V	I_{I2SOH} = –1 mA
f_{I2SWS}	I²S Word Strobe Output Frequency	I2S_WS		32.0		kHz	NICAM-PLL closed
f_{I2SCL}	I²S Clock Output Frequency	I2S_CL		1024		kHz	
$t_{I2S1/I2S2}$	I²S Clock High/Low Ratio		0.9	1	1.1		
t_{I2S3}	I²S Data Setup Time before Rising Edge of Clock	I2S_CL I2S_DA_OUT	200			ns	C_L = 30 pF
t_{I2S4}	I²S Data Hold Time after Falling Edge of Clock				180	ns	
t_{I2S5}	I²S Word Strobe Setup Time before Rising Edge of Clock	I2S_CL I2S_WS	200			ns	
t_{I2S6}	I²S Word Strobe Hold Time after Falling Edge of Clock				180	ns	
Analog Ground							
V_{AGNDC0}	AGNDC Open Circuit Voltage	AGNDC	3.67	3.77	3.87	V	$R_{load} \geq 10\ M\Omega$
R_{outAGN}	AGNDC Output Resistance		70	125	180	kΩ	3 V ≤ V_{AGNDC} ≤ 4 V
Analog Input Resistance							
R_{inSC}	SCART Input Resistance from T_A = 0 to 70 °C	SCn_IN_s[1)]	25	40	58	kΩ	f_{signal} = 1 kHz, I = 0.05 mA
R_{inMONO}	MONO Input Resistance from T_A = 0 to 70 °C	MONO_IN	15	24	35	kΩ	f_{signal} = 1 kHz, I = 0.1 mA
Audio Analog-to-Digital-Converter							
V_{AICL}	Effective Analog Input Clipping Level for Analog-to-Digital-Conversion	SCn_IN_s[1)], MONO_IN	2.00		2.25	V_{RMS}	f_{signal} = 1 kHz
SCART Outputs							
R_{outSC}	SCART Output Resistance at T_j = 27 °C from T_A = 0 to 70 °C	SC1_OUT_s[1)]	200 200	330	460 500	Ω Ω	f_{signal} = 1 kHz, I = 0.1 mA
dV_{OUTSC}	Deviation of DC-Level at SCART Output from AGNDC Voltage		–70		+70	mV	
A_{SCtoSC}	Gain from Analog Input to SCART Output	SCn_IN_s[1)] MONO_IN → SC1_OUT_s[1)]	–1.0		+0.5	dB	f_{signal} = 1 kHz
$f_{rSCtoSC}$	Frequency Response from Analog Input to SCART Output, Bandwidth: 0 to 20000 Hz		–0.5		+0.5	dB	with resp. to 1 kHz
V_{outSC}	Effective Signal Level at SCART-Output during full-scale Digital Input Signal from DSP	SC1_OUT_s[1)]	1.8	1.9	2.0	V_{RMS}	f_{signal} = 1 kHz

1) "n" means "1", or "2"; "s" means "L" or "R"

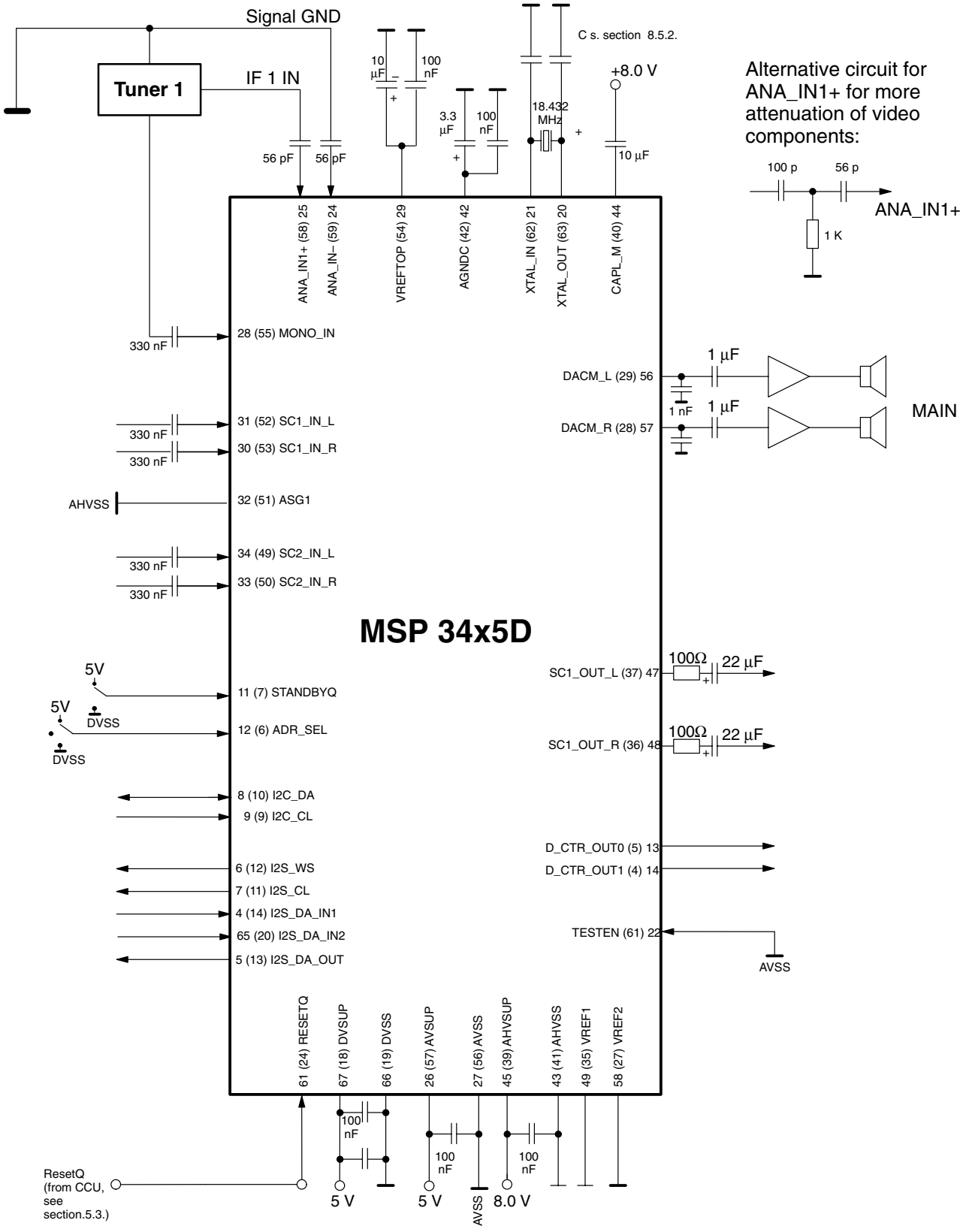
Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Main Outputs							
R_{outMA}	Main Output Resistance at T_j = 27 °C from T_A = 0 to 70 °C	DACM_s[1])	 2.1 2.1	3.3	 4.6 5.0	 kΩ kΩ	f_{signal} = 1 kHz, I = 0.1 mA
$V_{outDCMA}$	DC-Level at Main-Output for Analog Volume at 0 dB for Analog Volume at –30 dB		1.8	2.04 61	2.28	V mV	
V_{outMA}	Effective Signal Level at Main-Output during full-scale Digital Input Signal from DSP for Analog Volume at 0 dB		1.23	1.37	1.51	V_{RMS}	f_{signal} = 1 kHz
Analog Performance							
SNR	Signal-to-Noise Ratio						
	from Analog Input to SCART Output	MONO_IN, SCn_IN_s[1]) → SC1_OUT_s[1])	93	96		dB	Input Level = –20 dB, f_{sig} = 1 kHz, equally weighted 20 Hz...20 kHz
THD	Total Harmonic Distortion						
	from Analog Input to SCART Output	MONO_IN, SCn_IN_s[1]) → SC1_OUT_s[1])		0.01	0.03	%	Input Level = –3 dBr, f_{sig} = 1 kHz, equally weighted 20 Hz...20 kHz
XTALK	Crosstalk Attenuation						
	between left and right channel within SCART Input/Output pair (L→R, R→L) SCn_IN → SC1_OUT[1])		 80			 dB	Input Level = –3 dB, f_{sig} = 1 kHz, unused analog inputs connected to ground by Z < 1 kΩ equally weighted 20 Hz...20 kHz
PSRR: rejection of noise on AHVSUP at 1 kHz							
PSRR	AGNDC	AGNDC		80		dB	
	From Analog Input to SCART Output	MONO_IN, SCn_IN_s[1]) SC1_OUT_s[1])		70		dB	
S/N_{FM}	FM Input to Main/SCART Output	DACM_s[1]), SC1_OUT_s[1])	73			dB	1 FM-carrier 5.5 MHz, 50 µs, 1 kHz, 40 kHz deviation; RMS, unweighted 0 to 15 kHz (for S/N); full input range, FM-Prescale = 46h, Vol = 0 dB → Output Level 1 Vrms at DACM_s; SPM = 3
THD_{FM}	Total Harmonic Distortion and Noise of FM demodulated signal on Main/SCART Outputs	DACM_s[1]), SC1_OUT_s[1])			0.1	%	
S/N_{NICAM}	Signal-to-Noise Ratio of NICAM Baseband Signal on Main/SCART Outputs	DACM_s[1]), SC1_OUT_s[1])	72			dB	NICAM: –6 dB, 1 kHz, RMS unweighted 0 to 15 kHz, NICAM_Prescale = 7Fh, Vol = 9 dB → Output level 1 V_{RMS} at DACM_s; SPM = 8

1) "n" means "1" or "2"; "s" means "L" or "R"
SPM: Short Programming Mode

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
THD_{NICAM}	Total Harmonic Distortion and Noise of NICAM Baseband Signal on Main/SCART Outputs	DACM_s[1]), SC1_OUT_s[1])			0.1	%	2.12 kHz, modulator input level = 0 dBref SPM = 8
BER_{NI}	NICAM: Bit Error Rate	–			1	10^{-7}	FM and NICAM, norm conditions
S/N_{AM}	Signal-to-Noise Ratio of AM Baseband Signal on Main/SCART Outputs	DACM_s[1]), SC1_OUT_s[1])	48			dB	SIF input range: 0.1–0.8 Vpp; AM= 70%, 1 kHz, RMS unweighted (S/N); 0 to 15 kHz, FM/AM-Prescale = $3C_{hex}$, Vol = 0 dB → Output level: 0.5 V_{RMS} at DACM_s AM + NICAM, norm conditions; SPM = 9
THD_{AM}	Total Harmonic Distortion and Noise of AM Demodulated Signal on Main/SCART Outputs	DACM_s[1]), SC1_OUT_s[1])			0.3	%	
R_{IFIN}	Input Impedance	ANA_IN1+, ANA_IN–	1.5 10.5	2 14.1	2.5 17.6	kΩ kΩ	Gain AGC = 20 dB Gain AGC = 3 dB
$DC_{VREFTOP}$	DC Voltage at VREFTOP	VREFTOP	2.56	2.66	2.76	V	
DC_{ANA_IN}	DC Voltage on IF inputs	ANA_IN1+, ANA_IN–	1.3	1.5	1.7	V	
$XTALK_{IF}$	Crosstalk Attenuation	ANA_IN1+, ANA_IN–	40			dB	f_{signal} = 1 MHz Input Level = –2 dBr
BW_{IF}	3 dB Bandwidth		10			MHz	
AGC	AGC Step Width			0.85		dB	
dV_{FMOUT}	Tolerance of Output Voltage of FM Demodulated Signal	DACM_s[1]), SC1_OUT_s[1])	–1.5		+1.5	dB	1 FM-carrier, 50 µs, 1 kHz 40 kHz deviation; RMS
$dV_{NICAMOUT}$	Tolerance of Output Voltage of NICAM Baseband Signal	DACM_s[1]), SC1_OUT_s[1])	–1.5		+1.5	dB	2.12 kHz, modulator input level = 0 dBref
fR_{FM}	FM Frequency Response on Main/SCART Outputs, Bandwidth 20 to 15000 Hz	DACM_s[1]), SC1_OUT_s[1])	–1.0		+1.0	dB	1 FM-carrier 5.5 MHz, 50 µs, modulator input level = –14.6 dBref; RMS
fR_{NICAM}	NICAM Frequency Response on Main/SCART Outputs, Bandwidth 20 to 15000 Hz	DACM_s[1]), SC1_OUT_s[1])	–1.0		+1.0	dB	Modulator input level = –12 dB dBref; RMS
SEP_{FM}	FM Channel Separation (Stereo)	DACM_s[1]), SC1_OUT_s[1])	50			dB	2 FM-carriers 5.5/5.74 MHz, 50 µs, 1 kHz, 40 kHz deviation; RMS
SEP_{NICAM}	NICAM Channel Separation (Stereo)	DACM_s[1]), SC1_OUT_s[1])	80			dB	
$XTALK_{FM}$	FM Crosstalk Attenuation (Dual)	DACM_s[1]), SC1_OUT_s[1])	80			dB	2 FM-carriers 5.5/5.74 MHz, 50 µs, 1 kHz, 40 kHz deviation; RMS
$XTALK_{NICAM}$	NICAM Crosstalk Attenuation (Dual)	DACM_s[1]), SC1_OUT_s[1])	80			dB	

1) "n" means "1" or "2"; "s" means "L" or "R"
SPM: Short Programming Mode

9. Application Circuit



Note: Pin numbers refer to the PLCC68 package, numbers in brackets refer to the PSDIP64 package.

10. Appendix A: MSP 34x5D Version History

A1

First hardware release MSP 3415D

A2

Second hardware release MSP 3405D and MSP 3415D

B3

– I^2S Bus supported with version B3 and later versions

– digital input specification changed with version B3 and later versions (see section ...)

– max. analog high supply voltage AHVSUP 8.7 V

11. Data Sheet History

1. Preliminary Data Sheet: “MSP 34x5D Multistandard Sound Processors”, Aug. 5, 1998, 6251-475-1PD. First release of the preliminary data sheet.

2. Preliminary Data Sheet: “MSP 34x5D Multistandard Sound Processors”, Oct. 14, 1999, 6251-475-2PD. Second release of the preliminary data sheet. Major changes:

– specification for version B3 added (see Appendix A: Version History)

– specification for I^2S interface added

– section 8.1.: Outline Dimensions for all packages changed

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Preliminary Data Sheet Supplement

Subject:	Compatibility Differences
Data Sheet Concerned:	All MSP 34xxD Data Sheets: 6251-482-2PD, 6251-475-2PD, 6251-486-2PD
Supplement:	No. 3/ 6251-526-3PDS
Edition:	Oct. 11, 2000

MSP 34xxD Family Compatibility Differences:

The MSP-family (MSP 3410D, MSP 3400D, MSP 3415D, MSP 3405D, MSP 3417D, MSP 3407D) is currently available in different technologies (0.8 µ, 0.5 µ, and 0.45 µ).

The specific differences of the various implementations are listed in the attached table.

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Compatibility Differences between 0.5/0.45µ and 0.8µ MSPD Devices

MSP-Type		MSP 3410D / MSP 3400D			MSP 3415D / MSP 3405D			MSP 3417D / MSP 3407D		
Version Code		**B4**	**C5**		**A2**	**B3**		**A1**	**B2**	
Technology		**0.8µ**	**0.5µ**	**0.45µ**	**0.8µ**	**0.5µ**	**0.45µ**	**0.8µ**	**0.5µ**	**0.45µ**
Mask Iteration Code		**67, 6B, 6G**	**8C and 94**	**G1, G4 H1, H3**	**6C, 6D**	**8D**	**G2, G5 H2, H4**	**6E, 6F**	**8F**	**G3, G6, H5**
Feature	**Documented in**									
Datasheet Reference		MSP 3400D, MSP 3410D Edit. May 1999			MSP 3405D, MSP 3415D Edit Oct. 1999			MSP 3407D, MSP 3417D Edit Jan. 2000		
General Hardware										
Power Consumption	Datasheet	910 mW	640 mW	600 mW	910 mW	640 mW	600 mW	910 mW	640 mW	600 mW
Total Electromagnetic Radiation (EMR)		-	less due to less Power Consumption		-	less due to less Power Consumption		-	less due to less Power Consumption	
V_{AGNDC0} typical	Datasheet	3.73 V	3.77 V		3.73 V	3.77 V		3.73 V	3.77 V	
$DC_{VREFTOP}$ typical	Datasheet	2.6 V	2.66 V		2.6 V	2.66 V		2.6 V	2.66 V	
Maximum V_{sup1}	Datasheet	8.4 V	8.7 V		8.4 V	8.7 V		8.4 V	8.7 V	
Digital Input Pin characteristics (I2S_IN1/2, I2S_WS/CL, StANDBYQ)	Datasheet	-	modified specifications (see datasheet)		-	modified specifications (see datasheet)		-	modified specifications (see datasheet)	
Demodulator										
Carrier Mute		-	slightly slower, but more stable: 64ms mute, 500 ms demute		-	slightly slower, but more stable: 64ms mute, 500 ms demute		-	slightly slower, but more stable: 64ms mute, 500 ms demute	
AM-Frequency Response		-	more flat		-	more flat		-	more flat	
Automatic Standard Detection		-	faster, more stable and with mute-function		-	faster, more stable and with mute-function		-	faster, more stable and with mute-function	
Baseband Processing										
J17-Deemphasis for **FM**-Input channels	Datasheet Supplement	available	not available (75µs instead of J17)		available	not available (75µs instead of J17)		available	not available (75µs instead of J17)	
I^2S-Bus	Datasheet	available			not available	available		not available		
Frequency response of 50/75µs Deemphasis		-	more flat		-	more flat		-	more flat	
DC_Level (DSP-Reg.: $1B_{hex}/1C_{hex}$)		-	Level increased by appr. 15% 1*)		-	Level increased by appr. 15% 1*)		-	Level increased by appr. 15% 1*)	

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MSP-Type		MSP 3410D / MSP 3400D			MSP 3415D / MSP 3405D			MSP 3417D / MSP 3407D		
Version Code		B4	C5		A2	B3		A1	B2	
Technology		0.8µ	0.5µ	0.45µ	0.8µ	0.5µ	0.45µ	0.8µ	0.5µ	0.45µ
Mask Iteration Code		67, 6B, 6G	8C and 94	G1, G4 H1, H3	6C, 6D	8D	G2, G5 H2, H4	6E, 6F	8F	G3, G6, H5
Feature	Documented in									
D/A-Outputs										
S/N-ratio		-	improved		-	improved		-	improved	
Pinning										
SCART2_Out pin	Datasheet	connected			not connected			connected	not connected	
DAC-Headphone pins	Datasheet	connected			not connected			connected	not connected	
Audio_Clock_Out	Datasheet	connected			connected	not connected (s. Datasheet P.51)		not connected		
The following pins refer to PQFP80:										
Pin 52	Datasheet	ASG2	ASG2	ASG2	ASG2	not connected (s. Datasheet P.51)		MSP 34x7D not available in 80-PQFP		
Pin 32	Datasheet	ASG3	not connected (s. Datasheet P.59)		ASG3	not connected (s. Datasheet P.51)		MSP 34x7D not available in 80-PQFP		
Pin 14	Datasheet	not connected	DVSS	DVSS	not connected	DVSS	DVSS	MSP 34x7D not available in 80-PQFP		
Pin 16	Datasheet	DVSS	not connected	not connected	DVSS	not connected	not connected	MSP 34x7D not available in 80-PQFP		

*1) In spite of increased DC-level controller-algorithms for automatic Sat-Carrier detection should run properly