SPSS023C – DECEMBER 1999 – REVISED FEBRUARY 2001

- **Advanced, Integrated Speech Synthesizer for High-Quality Sound.**
- **Operates up to 12.32 MHz (Performs up to 12 MIPS)**
- **Single-Chip Solution for up to 6.8 Minutes of Speech**
- **External ROM Interface for up to 18.8 Hours of Speech**
- **Supports High-Quality Synthesis Algorithms Such as MELP, CELP, LPC, ADPCM, and Polyphonic Music**
- **Simultaneous Speech Plus Music Capability**
- **Very Low-Power Operation, Ideal for Hand-Held Devices.**
- **Low-Voltage Operation, Sustainable by Three Batteries**
- **Reduced Power Stand-By Modes, Less Than 10 µA in Deep-Sleep Mode**
- **Contains 64K Byte Words Onboard ROM (2K Words Reserved)**
- **640-Word RAM**
- **64 I/O Pins Consisting of**
  - **40 General-Purpose Bit Configurable I/O**
  - **8 Inputs With Programmable Pullup Resistor and Dedicated Interrupt (Key-Scan)**
  - **16 Dedicated Output Pins**
- **Direct Speaker Driver, 32 Ω (PDM)**
- **One-bit Comparator With Edge-Detection Interrupt Service**
- **Resistor-Trimmed Oscillator or 32.768 kHz Crystal Reference Oscillator**
- **Serial Scan Port for In-Circuit Emulation and Diagnostics**
- **The MSP50C614 Is Sold in Die Form, or 100-pin PJM Package**
- **An Emulator Device Is Available in a Ceramic Package for Development**

description

The MSP50C614 is a low-cost, mixed-signal processor that combines a speech synthesizer, general-purpose I/O, onboard ROM, and direct speaker-drive in a single package. The computational unit utilizes a powerful new DSP which gives the MSP50C614 unprecedented speed and computational flexibility compared with previous devices of its type. The MSP50C614 supports a variety of speech and audio coding algorithms, providing a range of options with respect to speech duration and sound quality.

The device consists of a micro-DSP core, embedded program, and data memory, and a self-contained clock generation system. General-purpose periphery is comprised of 64 bits of partially configurable I/O.

The core processor is a general-purpose 16-bit microcontroller with DSP capability. The basic core block includes computational unit (CU), data address unit, program address unit, two timers, eight level interrupt processor, and several system and control registers. The core processor gives the MSP50C614 break-point capability in emulation.

The processor is Harvard type for efficient DSP algorithm execution. It requires separate program and data memory blocks to permit simultaneous access. It is configured in 32K 17-bit words.

The total ROM space is divided into two areas: 1) The lower 2K words are reserved by Texas Instruments for the purposes of a built-in self-test 2) The upper 30K is for user program/data.

The data memory is internal static RAM. The RAM is configured in 640 17-bit words. Both memories are designed to consume minimum power at a given system clock and algorithm acquisition frequency.

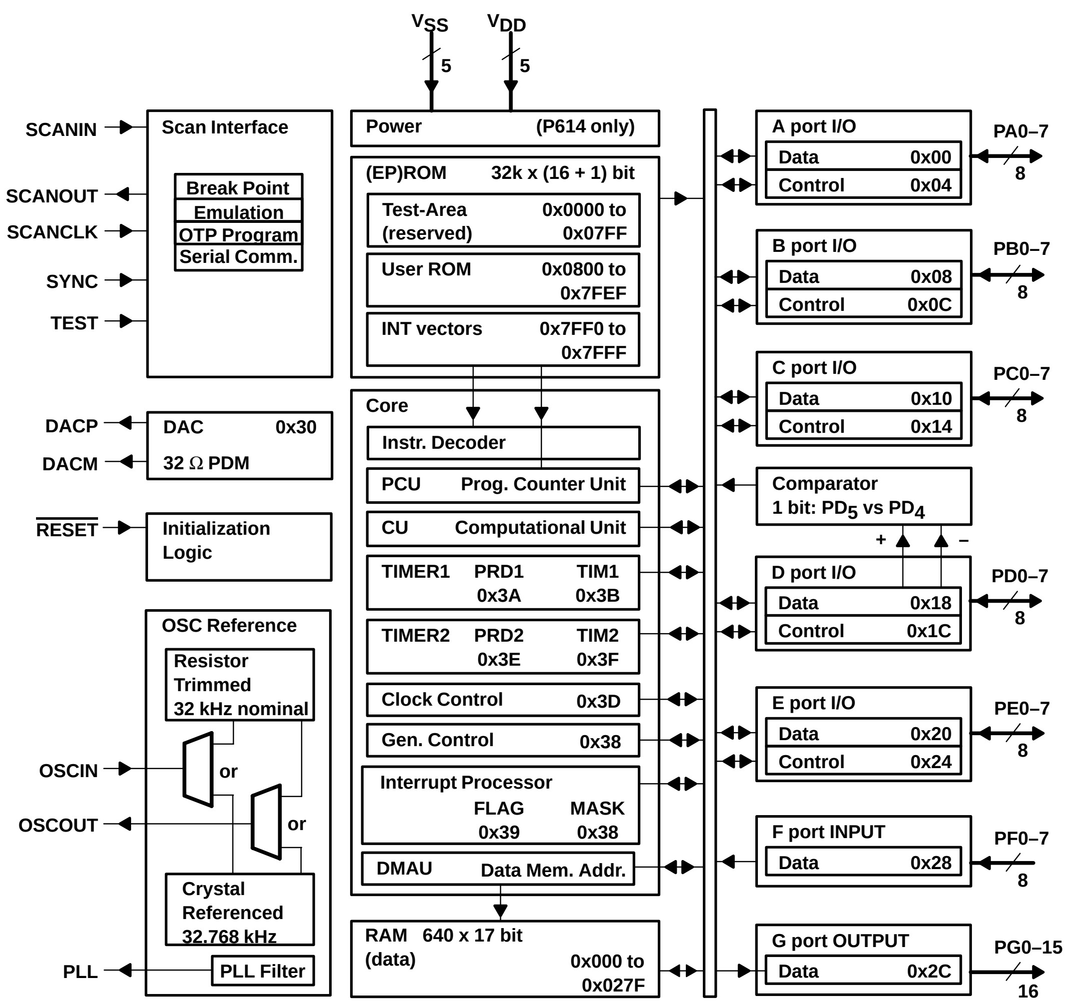
description (continued)

A flexible clock generation system enables the software to control the clock over a wide frequency range. The implementation uses a phase-locked loop (PLL) circuit that drives the processor clock at a selectable frequency between the minimum and maximum achievable. Selectable frequencies for the processor clock are spaced apart in 65.536 kHz steps. The PLL clock-reference is also selectable; either a resistor-trimmed oscillator or a crystal-referenced oscillator may be used. Internal and external clock sources are controlled separately to provide different levels of power management.

The periphery consists of five 8-bit wide general-purpose I/O ports, one 8-bit wide dedicated input port, and one 16-bit wide dedicated output port. The bidirectional I/O can be configured under software control as either high-impedance inputs or as totem-pole outputs. They are controlled via addressable I/O registers. The input-only port has a programmable pullup option (70-kΩ minimum resistance) and a dedicated service interrupt. These features make the input port especially useful as a key-scan interface.

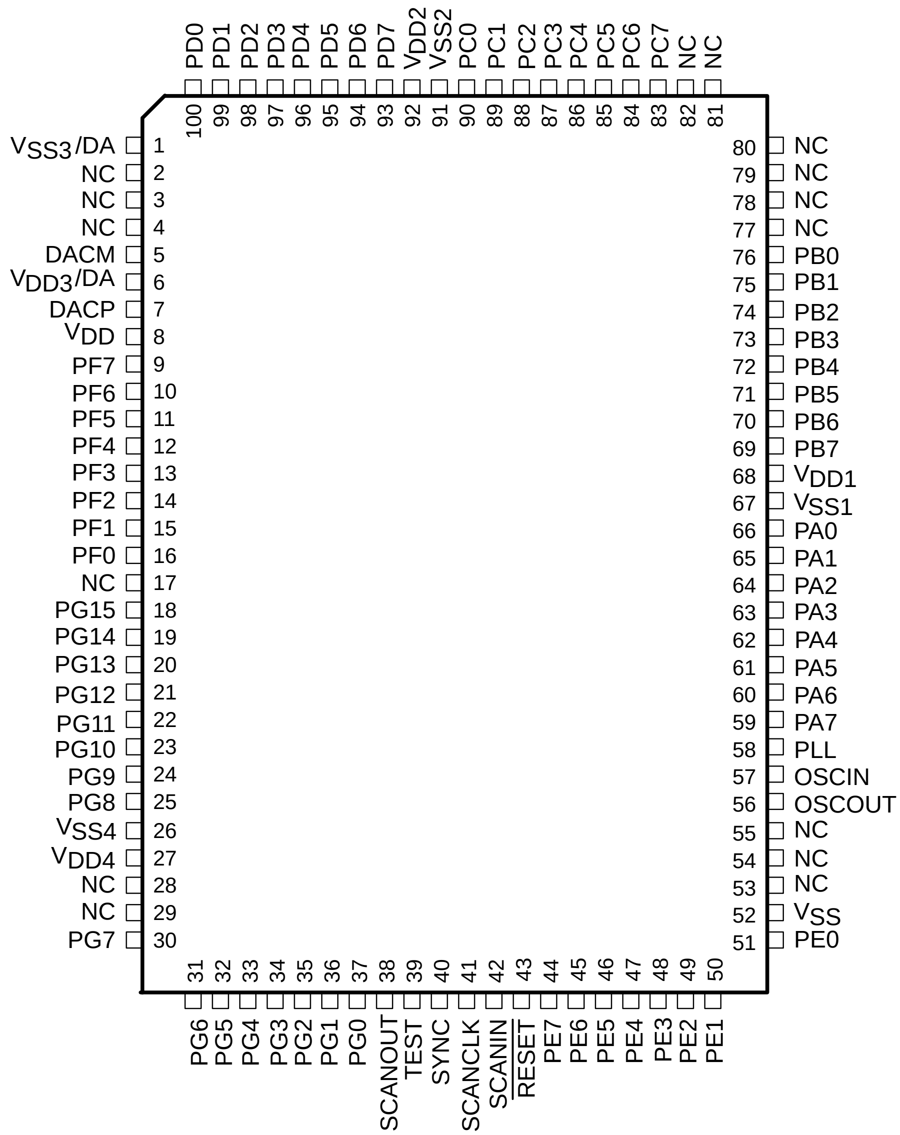
A simple one-bit comparator is also included in the periphery. The comparator is enabled by a control register, and its pin access is shared with two pins in one of the general-purpose I/O ports. Rounding out the MSP50C614 periphery is a built-in pulse-density-modulated DAC (digital-to-analog converter) with direct speaker-drive capability. The functional block diagram gives an overview of the MSP50C614 functionality.

functional block diagram



pin assignments

PJM PACKAGE
(TOP VIEW)



NC – No internal connection

Terminal Functions

NAME	PIN NO.	PAD NO.	I/O	DESCRIPTION
PA0 – PA7	66 – 59	75 – 68	I/O	Port A general-purpose I/O (1 Byte)
PB0 – PB7	76 – 69	85 – 78	I/O	Port B general-purpose I/O (1 Byte)
PC0 – PC7	90 – 83	8 – 1	I/O	Port C general-purpose I/O (1 Byte)
PD0 – PD7	100 – 93	18 – 11	I/O	Port D general-purpose I/O (1 Byte)
PE0 – PE7	51 – 44	63 – 56	I/O	Port E general-purpose I/O (1 Byte)
PF0 – PF7	16 – 9	31 – 24	I	Port F key-scan input (1 Byte)
PG0 – PG7	37 – 30	49 – 42	O	Port G dedicated output (2 Bytes)
PG8 – PG15	25 – 18	39 – 32		
Pins PD4 and PD5 may be dedicated to the comparator function, if the comparator enable bit is set. Refer to Section 3.3, *Comparator*, for details.				
Scan Port Control Signals				
SCANIN	42	54	I	Scan port data input
SCANOUT	38	50	O	Scan port data output
SCANCLK	41	53	I	Scan port clock
SYNC	40	52	I	Scan port synchronization
TEST	39	51	I	MSP50C614: test modes
The scan port pins must be bonded out on any MSP50C614 production board. Consult the *Important Note regarding Scan Port Bond Out*, see Chapter 7 in the MSP50C614 User's Guide (SPSU014).				
Reference Oscillator Signals				
OSCOUT	56	65	O	Resistor/crystal reference out
OSCIN	57	66	I	Resistor/crystal reference in
PLL	58	67	O	Phase-lock-loop filter
Digital-to-Analog Sound Output				
DACP	7	22	O	Digital-to-analog plus output (+)
DACM	5	20	O	Digital-to-analog minus output (–)
Initialization				
$\overline{RESET}$	43	55	I	Initialization
Power Signals				
V_{SS}	1[†], 26, 52, 67, 91	9, 19[†], 40, 64, 76		Ground
V_{DD}	6[†], 8, 27, 68, 92	10, 21[†], 23, 41, 77		Processor power (+)

† The V_{SS} and V_{DD} connections service the DAC circuitry. Their pins tend to sustain a higher current draw. A dedicated decoupling capacitor across these pins is therefore required.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . –0.3 to 7 V
Supply current, I_{DD} (see Note 2) . . . . 35 mA
Input voltage range, V_I (see Note 1) . . . . –0.3 to V_{DD} + 0.3 V
Output voltage range, V_O (see Note 1) . . . . –0.3 to V_{DD} + 0.3 V
Storage temperature range, T_A . . . . –30°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Unless otherwise noted, all voltages are measured with respect to V_{SS} .
2. The total supply current includes the current out of all the I/O pins as well as the operating current of the device.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage (with respect to V_{SS}), V_{DD}		3	5.2	V
CPU clock rate (as programmed), $f_{(CPU)}$		64	12,320	kHz
Load resistance between DAC_P and DAC_M, $R_{(DAC)}$		32		Ω
Operating free-air temperature, T_A	Device functionality	0	70	°C

timing requirements

		MIN	MAX	UNIT
$t_{(RESET)}$	Reset low pulse width, while V_{DD} is within specified limits	100		ns
$t1_{(WIDTH)}$	Pulse width required prior to a negative transition at pin...PD3, PD5, or PF0...PF7‡	2		$1/F_{CPU}$
$t2_{(WIDTH)}$	Pulse width required prior to a positive transition at pin...PD2 or PD4†	2		$1/F_{CPU}$

‡ While these pins are being used as interrupt inputs.

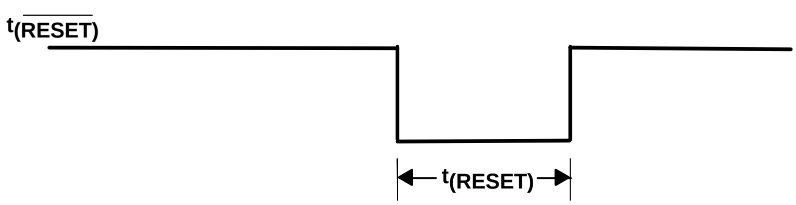


Figure 1. Initialization Timing Diagram

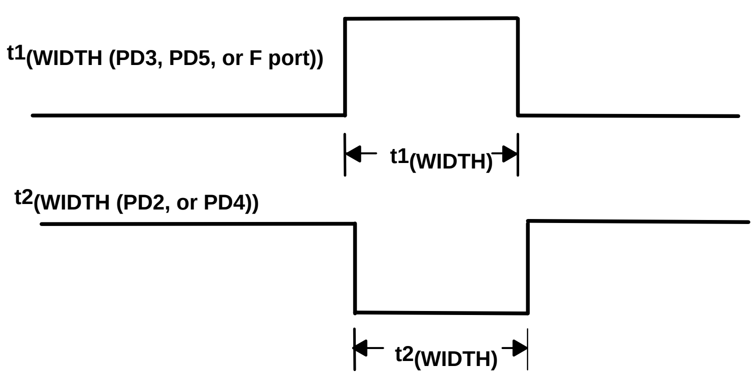


Figure 2. MSP50C614 External Interrupt Pin Pulse Width Requirements $t1_{WIDTH}$ and $t2_{WIDTH}$

dc electrical characteristics, T_A = 0 to 70°C

PARAMETER		TEST CONDITIONS		MIN	TYP§	MAX	UNIT
$\overline{RESET}$	Threshold changes	V_{DD} = 3 V	Positive going threshold		2.4		V
			Negative going threshold		1.8		
			Hysteresis		0.6		
		V_{DD} = 5.2 V	Positive going threshold		3.3		V
			Negative going threshold		2.9		
			Hysteresis		0.4		
V_{IH}	High-level input voltage	V_{DD} = 3 V		2		3	V
		V_{DD} = 4.5 V		3		4.5	
		V_{DD} = 5.2 V		3.5		5.2	
V_{IL}	Low-level input voltage	V_{DD} = 3 V		0		1	V
		V_{DD} = 4.5 V		0		1.5	
		V_{DD} = 5.2 V		0		1.7	
I_{OH}¶	High-level output current per pin of I/O port	V_{DD} = 4.5 V	V_{OH} = 4 V			–2	mA
I_{OL}¶	Low-level output current per pin of I/O port		V_{OL} = 0.5 V			5	mA
$I_{OH (DAC)}$	High-level output DAC current		V_{OH} = 4 V			–10	mA
$I_{OL (DAC)}$	Low-level output DAC current		V_{OL} = 0.5 V			20	mA
I_{lkg}	Input leakage current	Excludes OSC_{IN}				1	µA
$I_{(STANDBY)}$	Standby current	RESET is low			0.05	10	µA
I_{DD}†	Operating current	V_{DD} = 4.5 V,	F_{CLOCK} = 12.32 MHz		15		mA
$I_{(SLEEP-deep)}$	Supply current	V_{DD} = 4.5 V,	DAC off, ARM set, OSC disabled		0.05	10	µA
$I_{(SLEEP-mid)}$		V_{DD} = 4.5 V,	DAC off, ARM set, OSC enabled		40	60	
$I_{(SLEEP-light)}$		V_{DD} = 4.5 V,	DAC off, ARM clear, OSC enabled		60	100	
V_{IO}	Input offset voltage	V_{DD} = 4.5 V,	V_{ref} = 1 to 4.25 V		25	50	mV
$R_{(PULLUP)}$	F port pullup resistance	V_{DD} = 5 V		70	150		kΩ
$\Delta f_{(RTO-trim)}$	Trim deviation	R_{RTO} = 470 kΩ, V_{DD} = 4.5 V, T_A = 25°C, f_{RTO} = 8.192 MHz (PLL setting = 7 Ch)‡			±1%	±3%	
$\Delta f_{(RTO-volt)}$	Voltage deviation	R_{RTO} = 470 kΩ, V_{DD} = 3.5 to 5.2 V, T_A = 25°C, f_{RTO} = 8.192 MHz (PLL setting = 7 Ch)‡				±1.5%	
$\Delta f_{(RTO-temp)}$	Temperature deviation	R_{RTO} = 470 kΩ, V_{DD} = 4.5 V, T_A = 0 to 70°C, f_{RTO} = 8.192 MHz (PLL setting = 7 Ch)‡			±0.03		%/°C
$\Delta f_{(RTO-res)}$	Resistance deviation	V_{DD} = 4.5 V, T_A = 25°C, $R_{(OSC)}$ = 470 kΩ at ±1%, f_{RTO} = 8.192 MHz (PLL setting = 7 Ch)‡			±1%		

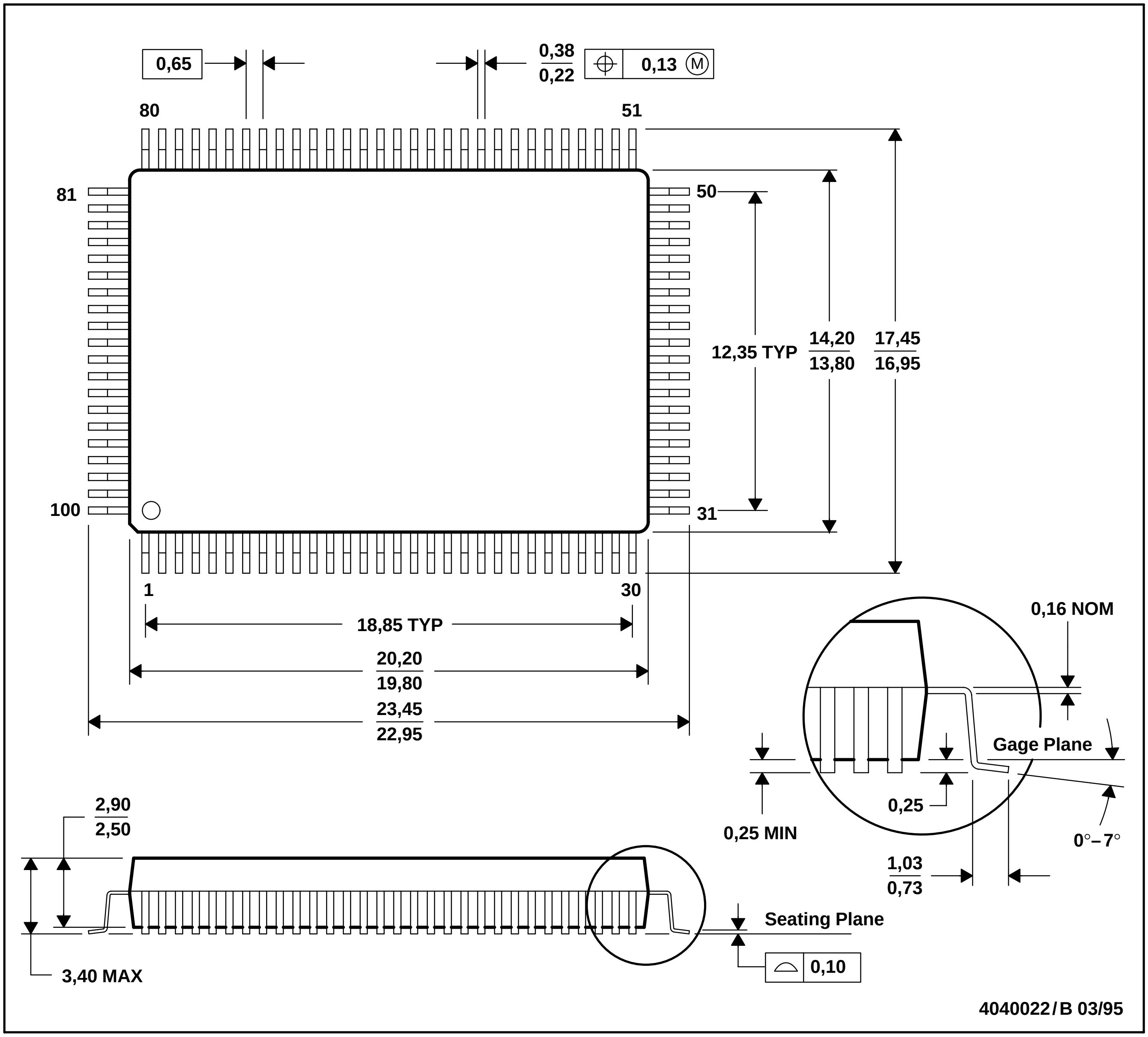
† Operating current assumes all inputs are tied to either V_{SS} or V_{DD} with no input currents due to programmed pullup resistors. The DAC output and other outputs are open circuited.
‡ The best trim value is selected at nominal temperature and voltage but the deviation due to the trim error is ignored.
§ Typical voltage and current measurement taken at 25°C
¶ Cannot exceed 15 mA total per internal V_{DD} pin. Port A, B share 1 internal V_{DD} pin; Port C, D share 1 internal V_{DD}.

external component absolute values

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$R_{(RTO)}$	RTO external resistance	T_A = 25°C,	1% tolerance		470	kΩ
$C_{(PLL)}$	PLL external capacitance	T_A = 25°C,	10% tolerance		3300	pF

MECHANICAL DATA

PJM (R-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-022

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