FEATURES

- LCD TV controller with PC & multimedia display functions
- Input supports up to UXGA & 1080P
- Supports up to SXGA panels
- Integrated two-port triple-ADC/PLL
- Integrated DVI/HDCP/HDMI compliant receiver
- YUV422 digital video input ports
- Dual high-quality scaling engines
- Dual 3-D video de-interlacers
- Full function PIP/POP
- MStarACE picture/color processing engine
- Embedded On-screen display controller (OSD) engine
- Digital audio I/O & sync processor
- Built-in dual-link LVDS transmitter
- 5 Volt tolerant inputs
- Low EMI and power saving features
- Supports PWM & GPO controls
- 208-pin PQFP package

Analog RGB/YPbPr Input Ports

- Dual analog ports support up to 165Mhz
- Supports PC RGB input up to UXGA@60Hz
- Supports HDTV RGB/YPbPr/YCbCr up to 1080P
- On-chip high-performance PLLs
- Supports Composite Sync and SOG (Sync-on-Green) separator
- Automatic color calibration

DVI/HDCP/HDMI Compliant Input Port

- Operates up to 165 MHz (up to UXGA @60Hz)
- Single link on-chip DVI 1.0 compliant receiver
- High-bandwidth Digital Content Protection (HDCP) 1.1 compliant receiver
- High Definition Multimedia Interface (HDMI) 1.0 compliant receiver with I2S and S/PDIF digital audio outputs
- Long-cable tolerant robust receiving

Video Input Port

- Two 4:2:2 ITU656 8-bit digital video input ports
- One 4:2:2 ITU601 16-bit digital video input port
- Supports 16-bit YUV 4:2:2 interlaced/ progressive video input up to 1080i/720P

Auto-Configuration/Auto-Detection

- Auto input signal format (SOG, Composite, Separated HSYNC, VSYNC, and DE), and input mode (all PC & TV modes) detection
- Auto-tuning function including phasing, positioning, offset, gain, and jitter detection
- Sync Detection for H/V Sync

Dual High-Performance Scaling Engines

- Fully programmable shrink/zoom capabilities
- Nonlinear video scaling supports various modes including Panorama

Video Processing & Conversion

- Dual 3-D motion adaptive video de-interlacers with upgraded edge-oriented adaptive algorithm for smooth low-angle edges
- Automatic 3:2 pull-down & 2:2 pull-down detection and recovery
- PIP/POP with programmable size and location, supports multi-video applications
- Video-over-graphic overlay
- MStar 2nd Generation Advanced Color Engine (MStarACE-2) automatic picture enhancement gives:
  - Brilliant and fresh color
  - Intensified contract and details
  - Vivid skin tone
  - Sharp edge
  - Enhanced depth of field perception
  - Accurate and independent color control
- Independent picture control for main and sub windows
- sRGB compliance allows end-user to experience the same colors as viewed on CRTs and other displays
- Programmable 10-bit RGB gamma CLUT
- 3-D video noise reduction

On-Screen OSD Controller

- 16/128 color palette
- 256/512 1-bit/pixel font
- 128/256/512 4-bit/pixel font
- Supports texture function
- Supports 4K attribute/code
- Horizontal and vertical stretch of OSD menus

- Ÿ Supports button function
- Ÿ Pattern generator for production test
- Ÿ Supports OSD MUX and alpha blending capability
- Ÿ Supports blinking and scrolling for closed caption applications

n Digital Audio Interface

- Ÿ I^2S digital audio input
- Ÿ I^2S digital audio output
- Ÿ S/PDIF digital audio output
- Ÿ HDMI audio channel processing capability
- Ÿ Programmable delay for audio/video synchronization

n LVDS Panel Interface

- Ÿ Supports dual link up to 135MHz dot clock for SXGA
- Ÿ Supports 2 data output formats: Thine & TI data mappings
- Ÿ Compatible with TIA/EIA
- Ÿ With 6/8 bits options
- Ÿ Reduced swing for LVDS for low EMI
- Ÿ Supports flexible spread spectrum frequency with 360Hz~11.8MHz and up to 25% modulation

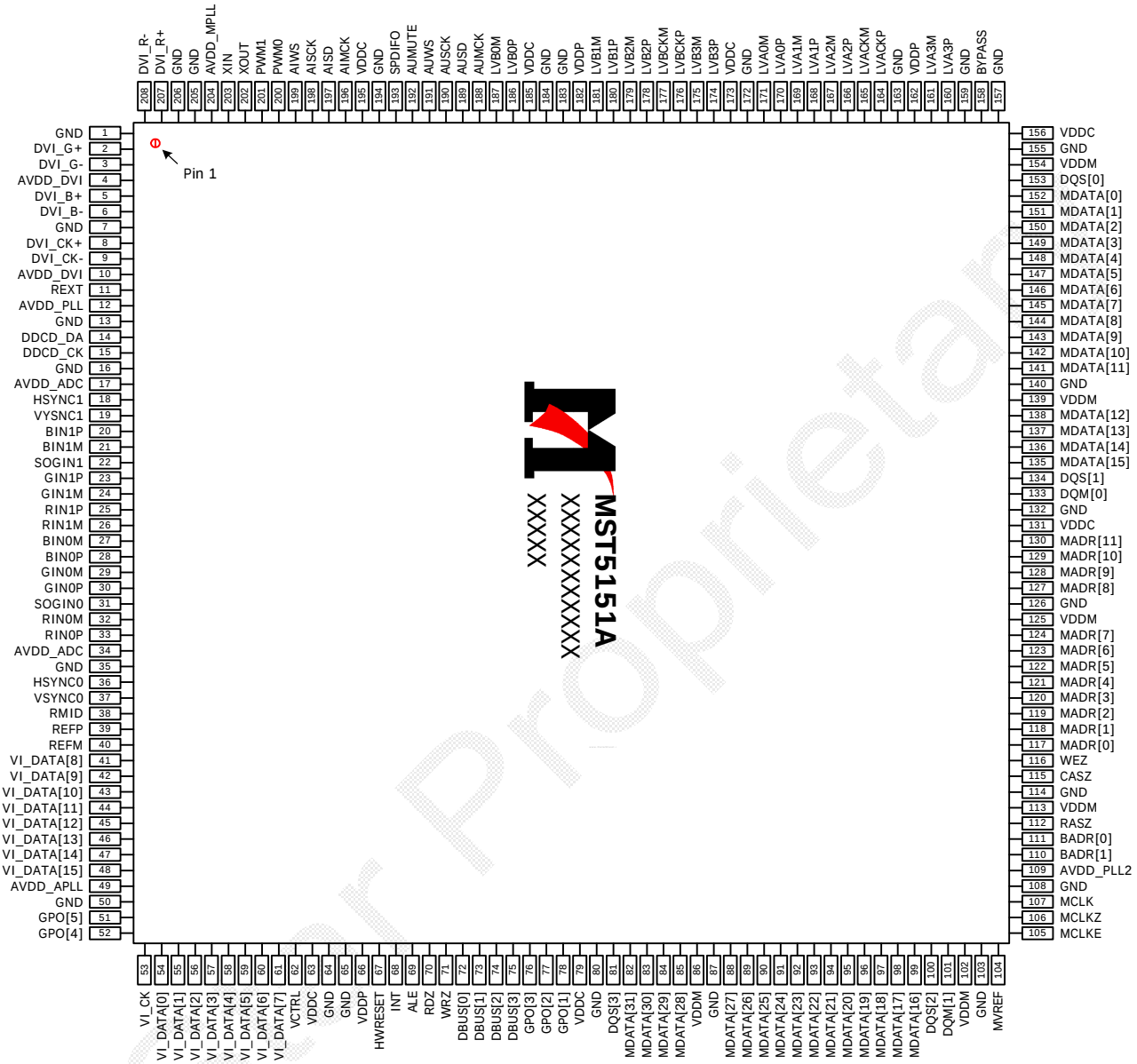
n External Connection/Component

- Ÿ Supports 4-wire double-data-rate direct MCU bus
- Ÿ 32-bit data bus for external frame buffer (SDR or DDR SDRAM)
- Ÿ All system clocks synthesized from a single external clock

GENERAL DESCRIPTION

The MST5151A is a high performance and fully integrated graphics processing IC solution for multi-function LCD monitor/TV with resolutions up to SXGA. It is configured with an integrated triple-ADC/PLL, an integrated DVI/HDCP/HDMI receiver, two video de-interlacers, two high quality scaling engines, an on-screen display controller, and a built-in output clock generator. By use of external frame buffer, PIP/POP is provided for multimedia applications. It supports de-interlaced full-screen video, video-on-graphic overlay, split screen, frame rate conversion, and aspect ratio conversion for various video sources. To further reduce system costs, the MST5151A also integrates intelligent power management control capability for green-mode requirements and spread-spectrum support for EMI management.

PIN DIAGRAM (MST5151A)



PIN DESCRIPTION

MCU Interface

Pin Name	Pin Type	Function	Pin
HWRESET	Schmitt Trigger Input w/ 5V-tolerant	Hardware Reset, active high	67
DBUS[3:0]	I/O w/ 5V-tolerant	MCU 4-bit DDR Direct bus; 4mA driving strength	75-72
ALE	I w/ 5V-tolerant	MCU Bus ALE, active high	69
RDZ	I w/ 5V-tolerant	MCU Bus RDZ, active high	70
WRZ	I w/ 5V-tolerant	MCU Bus WDZ, active high	71
INT	Output	MCU Bus Interrupt; 4mA driving strength	68

Analog Interface

Pin Name	Pin Type	Function	Pin
RMID		Mid-Scale Voltage Bypass	38
REFP		Internal ADC Top De-coupling Pin	39
REFM		Internal ADC Bottom De-coupling Pin	40
REXT	Analog Input	External Resister 390 ohm to AVDD_DVI	11
HSYNC0	Schmitt Trigger Input w/ 5V-tolerant	Analog HSYNC Input from Channel 0	36
VSYNC0	Schmitt Trigger Input w/ 5V-tolerant	Analog VSYNC Input from Channel 0	37
BIN0M	Analog Input	Reference Ground for Analog Blue Input from Channel 0	27
BIN0P	Analog Input	Analog Blue Input from Channel 0	28
GIN0M	Analog Input	Reference Ground for Analog Green Input from Channel 0	29
GIN0P	Analog Input	Analog Green Input from Channel 0	30
SOGIN0	Analog Input	Sync On Green Input from Channel 0	31
RIN0M	Analog Input	Reference Ground for Analog Red Input from Channel 0	32
RIN0P	Analog Input	Analog Red Input from Channel 0	33
HSYNC1	Schmitt Trigger Input w/ 5V-tolerant	Analog HSYNC Input from Channel 1	18
VSYNC1	Schmitt Trigger Input w/ 5V-tolerant	Analog VSYNC Input from Channel 1	19
BIN1P	Analog Input	Analog Blue Input from Channel 1	20
BIN1M	Analog Input	Reference Ground for Analog Blue Input from Channel 1	21
SOGIN1	Analog Input	Sync On Green Input from Channel 1	22
GIN1P	Analog Input	Analog Green Input from Channel 1	23

Pin Name	Pin Type	Function	Pin
GIN1M	Analog Input	Reference Ground for Analog Green Input from Channel 1	24
RIN1P	Analog Input	Analog Red Input from Channel 1	25
RIN1M	Analog Input	Reference Ground for Analog Red Input from Channel 1	26

DVI Interface

Pin Name	Pin Type	Function	Pin
DVI_R+	Input	DVI Input Channel Red +	207
DVI_R-	Input	DVI Input Channel Red -	208
DVI_G+	Input	DVI Input Channel Green +	2
DVI_G-	Input	DVI Input Channel Green -	3
DVI_B+	Input	DVI Input Channel Blue +	5
DVI_B-	Input	DVI Input Channel Blue -	60
DVI_CK+	Input	DVI Input Clock +	8
DVI_CK-	Input	DVI Input Clock -	9

Video Interface

Pin Name	Pin Type	Function	Pin
VI_CK	Input w/ 5V-tolerant	Digital Video Input Clock	66
VI_DATA[15:0]	Input w/ 5V-tolerant	Digital Video Input Data[15:0]	48-41, 61-54

Digital Audio Interface

Pin Name	Pin Type	Function	Pin
AUMCK	Output	Audio Master Clock Output	188
AUSD	Output	Audio Serial Data Output; 4mA driving strength	189
AUSCK	Output	Audio Serial Clock Output; 4mA driving strength	190
AUWS	Output	Word Select Output; 4mA driving strength	191
AUMUTE	Output	Audio Output Mute Control	192
SPDIFO	Output	S/PDIF Audio Output; 4mA driving strength	193
AIMCK	Input	Audio Master Clock Input	196
AISD	Input	Audio Serial Data Input	197
AISCK	Input	Audio Serial Clock Input	198
AIWS	Input	Word Select Input	199

LVDS Interface

Pin Name	Pin Type	Function	Pin
LVA0M	Output	A-Link Negative LVDS Differential Data Output	171
LVA0P	Output	A-Link Positive LVDS Differential Data Output	170
LVA1M	Output	A-Link Negative LVDS Differential Data Output	169
LVA1P	Output	A-Link Positive LVDS Differential Data Output	168
LVA2M	Output	A-Link Negative LVDS Differential Data Output	167
LVA2P	Output	A-Link Positive LVDS Differential Data Output	166
LVA3M	Output	A-Link Negative LVDS Differential Data Output	161
LVA3P	Output	A-Link Positive LVDS Differential Data Output	160
LVACKM	Output	A-Link Negative LVDS Differential Data Output	165
LVACKP	Output	A-Link Positive LVDS Differential Data Output	164
LVB0M	Output	B-Link Negative LVDS Differential Data Output	187
LVB0P	Output	B-Link Positive LVDS Differential Data Output	186
LVB1M	Output	B-Link Negative LVDS Differential Data Output	181
LVB1P	Output	B-Link Positive LVDS Differential Data Output	180
LVB2M	Output	B-Link Negative LVDS Differential Data Output	179
LVB2P	Output	B-Link Positive LVDS Differential Data Output	178
LVB3M	Output	B-Link Negative LVDS Differential Data Output	175
LVB3P	Output	B-Link Positive LVDS Differential Data Output	174
LVBCKM	Output	B-Link Negative LVDS Differential Data Output	177
LVBCKP	Output	B-Link Positive LVDS Differential Data Output	176

GPO Interface

Pin Name	Pin Type	Function	Pin
PWM0	Output	GPO with PWM Function; 4mA driving strength	200
PWM1	Output	GPO with PWM Function; 4mA driving strength	201
GPO[1]	I/O	GPO / FIELD input; 4mA driving strength	78
GPO[2]	I/O	GPO / Digital VSYNC Input; 4mA driving strength	77
GPO[3]	I/O	GPO / DE Input; 4mA driving strength	76
GPO[4]	I/O	GPO / Secondary Video Clock Input; 4mA driving strength	52
GPO[5]	I/O	GPO / Digital HSYNC Input; 4mA driving strength	51

DRAM Interface

Pin Name	Pin Type	Function	Pin
MVREF	Input	Reference Voltage for DDR SDRAM Interface	104
MCLKE	Output	DRAM Memory Clock Enable	105
MCLKZ	Output	DRAM Memory clock Complementary /Input (for differential clocks)	106
MCLK	Output	DRAM Memory Clock	107
RASZ	Output	Row Address Strobe, active low	112
CASZ	Output	Column Address Strobe, active low	115
WEZ	Output	Write Enable, active low	116
DQM[1:0]	Output	Data Mask Byte Enable	101, 133
DQS[3:0]	Output	Data Strobe	81, 100, 134, 153
BADR[1:0]	Output	Memory Bank Address	110, 111
MADR[11:0]	Output	Memory Address	130-127, 124-117
MDATA[31:0]	I/O	Memory Data	82-85, 88-99, 135-138, 141-152

Misc. Interface

Pin Name	Pin Type	Function	Pin
XIN	Crystal Oscillator Input	Crystal Oscillator Input	203
XOUT	Crystal Oscillator Output	Crystal Oscillator Output	202
DDCD_DA	I/O w/ 5V-tolerant	HDCP Serial Bus Data / DDC data of DVI port; 4mA driving strength	14
DDCD_CK	Input w/ 5V-Tolerant	HDCP Serial Bus Clock / DDC Clock of DVI Port	15
BYPASS		For External Bypass Capacitor	158
VCTRL	Output	Regulator Control	62

Power Pins

Pin Name	Pin Type	Function	Pin
AVDD_DVI	3.3V Power	DVI Power	4, 10
AVDD_ADC	3.3V Power	ADC Power	17, 34
AVDD_PLL	3.3V Power	PLL Power	12
AVDD_PLL2	3.3V Power	PLL Power	109
AVDD_APLL	1.8V Power	Audio PLL Power	49
AVDD_MPLL	3.3V Power	PLL Power	204

Pin Name	Pin Type	Function	Pin
VDDM	3.3V Power (SDR SDRAM) / 2.5V Power (DDR SDRAM)	DRAM Interface Power	86, 102, 113, 125, 139, 154
VDDP	3.3V Power	Digital Output Power	66, 162, 182
VDDC	1.8V Power	Digital Core Power	63, 79, 131, 156, 173, 185, 195
GND	Ground	Ground	1, 7, 13, 16, 35, 50, 64, 65, 80, 87, 103, 108, 114, 126, 132, 140, 155, 157, 159, 163, 172, 183, 184, 194, 205, 206

ELECTRICAL SPECIFICATIONS

Analog Interface Characteristics

Parameter	Min	Typ	Max	Unit
Resolution		8		Bits
DC ACCURACY				
Differential Nonlinearity		±0.5	+1.50/-1.0	LSB
Integral Nonlinearity		±1		LSB
No Missing Codes		Guaranteed		
ANALOG INPUT				
Input Voltage Range				
Minimum			0.5	V p-p
Maximum	1.0			V p-p
Input Bias Current			1	uA
Input Full-Scale Matching		1.5		%FS
Brightness Level Adjustment		62		%FS
SWITCHING PERFORMANCE				
Maximum Conversion Rate	165			MSPS
Minimum Conversion Rate			12	MSPS
HSYNC Input Frequency	15		200	kHz
PLL Clock Rate	12		165	MHz
PLL Jitter		500		ps p-p
Sampling Phase Tempco		TBD		ps/°C
DIGITAL INPUTS				
Input Voltage, High (V_{IH})	2.5			V
Input Voltage, Low (V_{IL})			0.8	V
Input Current, High (I_{IH})			-1.0	uA
Input Current, Low (I_{IL})			1.0	uA
Input Capacitance		5		pF
DIGITAL OUTPUTS				
Output Voltage, High (V_{OH})	VDDP-0.1			V
Output Voltage, Low (V_{OL})			0.1	V
Duty Cycle				
DCK, /DCK	45	50	55	%
Output Coding		Binary		
DYNAMIC PERFORMANCE				
Analog Bandwidth, Full Power		250		MHz
Channel to Channel Matching		0.5%		Full-Scale

Specifications subject to change without notice.

Absolute Maximum Ratings

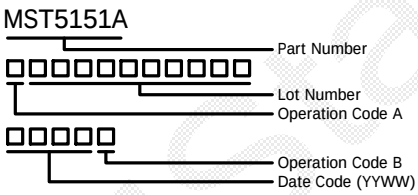
Parameter	Symbol	Min	Typ	Max	Units
3.3V Supply Voltages	V_{VDD_33}	-0.3		3.6	V
2.5V Supply Voltages	V_{VDD_25}	-0.3		2.75	V
1.8V Supply Voltages	V_{VDD_18}	-0.3		1.98	V
Input Voltage (5V tolerant inputs)	$V_{IN5Vtol}$	-0.3		5.0	V
Input Voltage (non 5V tolerant inputs)	V_{IN}	-0.3		V_{VDD_33}	V
Ambient Operating Temperature	T_A	0		70	°C
Storage Temperature	T_{STG}	-40		150	°C
Junction Temperature	T_J			150	°C
Thermal Resistance (Junction to Air) Natural Conversion	θ_{JA}		21		°C/W
Thermal Resistance (Junction to Case) Natural Conversion	θ_{JC}		2.0		°C/W

Note: Stress above those listed under Absolute Maximum Rating may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
MST5151A	0°C to +70°C	PQFP	208

MARKING INFORMATION



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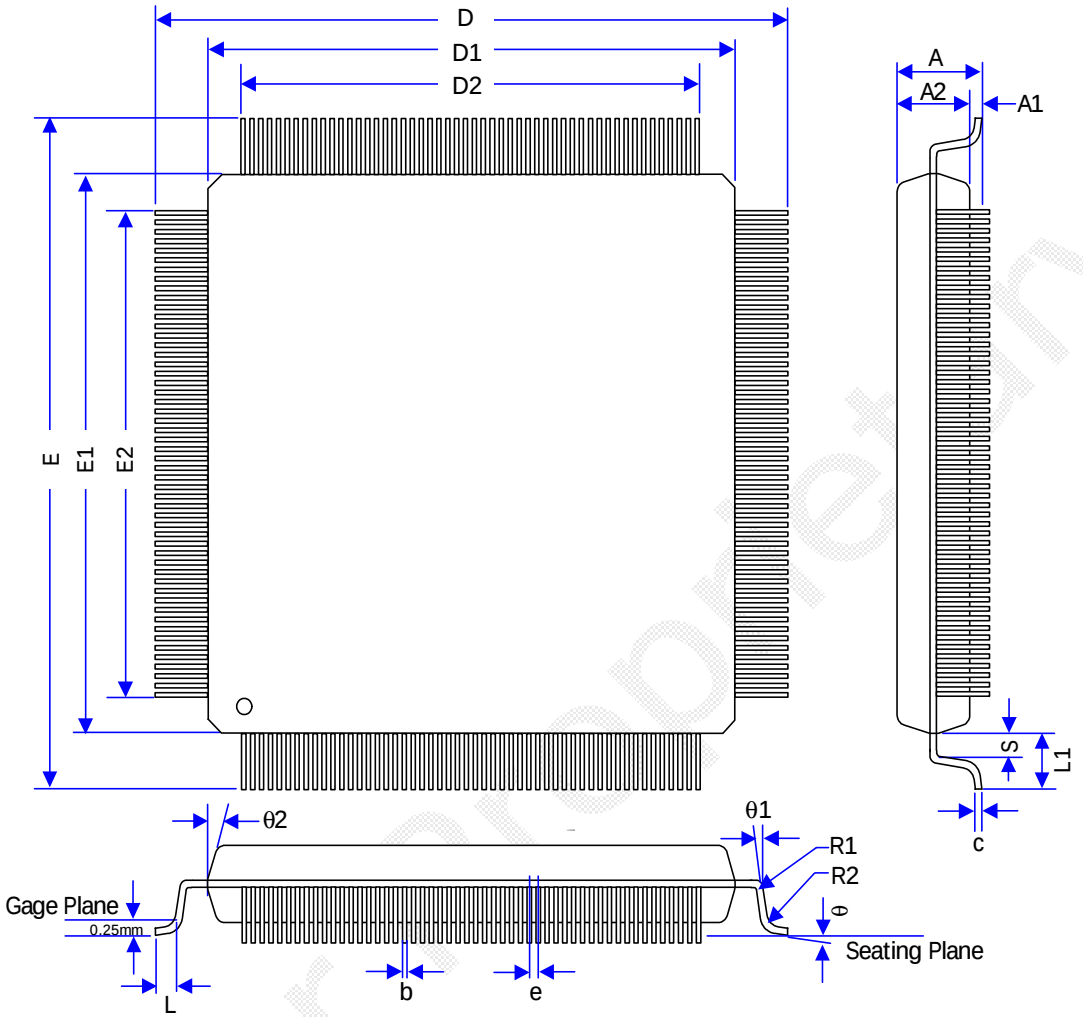
Electrostatic charges accumulate on both test equipment and human body and can discharge without detection. MST5151A comes with ESD protection circuitry, however, the device may be permanently damaged when subjected to high energy discharges. The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.

REVISION HISTORY

Document	Description	Date
MST5151A_pb_v01	Ÿ Initial release	Jul 2004
MST5151A_pb_v02	Ÿ Updated Features Ÿ Updated Absolute Maximum Ratings Ÿ Updated Electrical Specifications \ Analog Interface Characteristics \ Digital Inputs	Aug 2004

MECHANICAL DIMENSIONS



Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	4.10	-	-	0.161
A1	0.25	-	-	0.010	-	-
A2	3.20	3.32	3.60	0.126	0.131	0.142
D	31.20			1.228		
D1	28.00			1.102		
D2	25.50			1.004		
E	31.20			1.228		
E1	28.00			1.102		
E2	25.50			1.004		
R1	0.13	-	-	0.005	-	-
R2	0.13	-	0.30	0.005	-	0.012

Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
θ	0°	-	7°	0°	-	7°
θ1	0°	-	-	0°	-	-
θ2	8° Ref			8° Ref		
b	0.17	0.20	0.27	0.007	0.008	0.011
c	0.11	0.15	0.23	0.004	0.006	0.009
e	0.50 BSC.			0.020 BSC.		
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60 Ref			0.063 Ref		
S	0.20	-	-	0.008	-	-