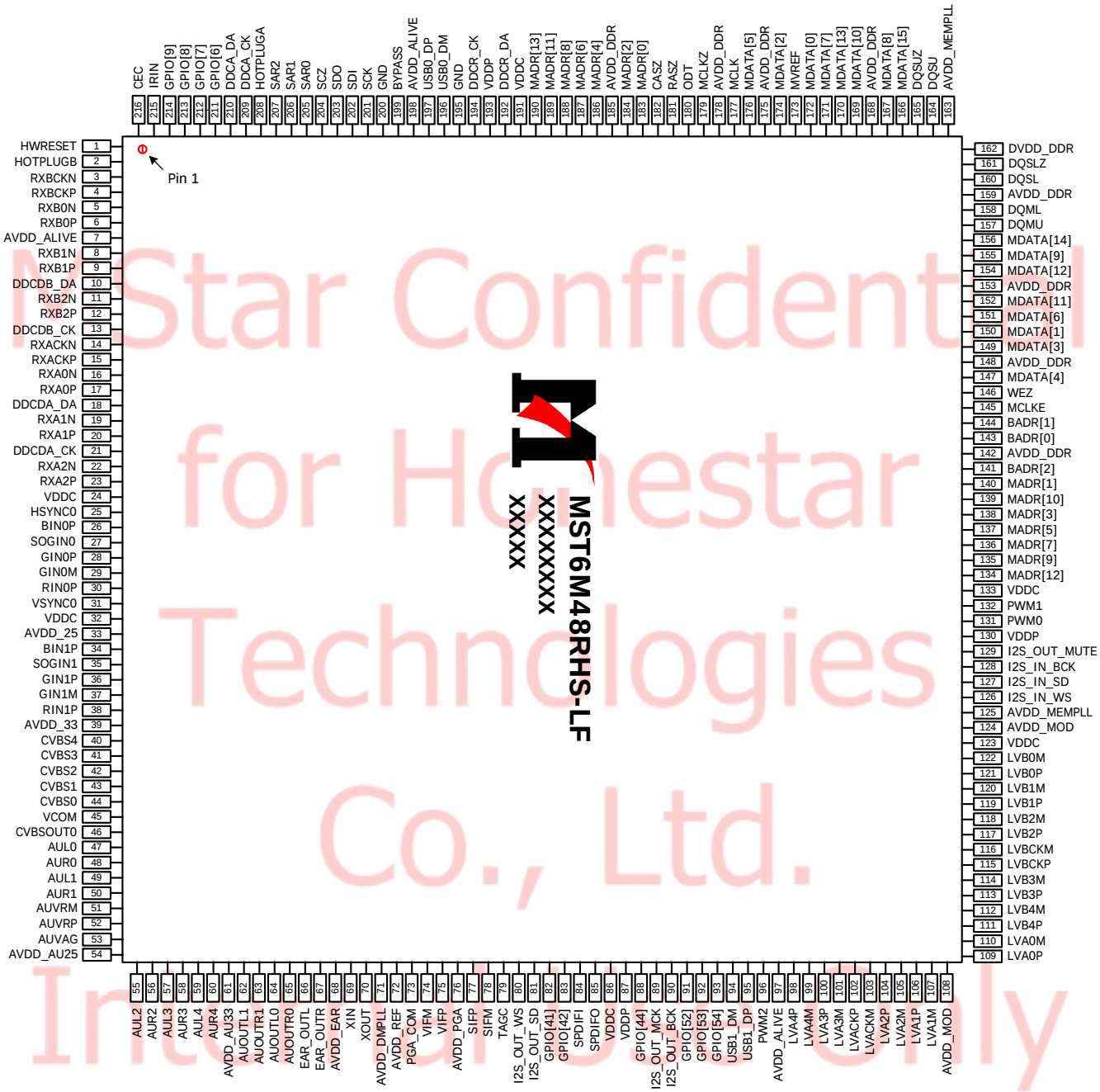
PIN DIAGRAM (MST6M48RHS)



PIN DESCRIPTION

Analog Interface

Pin Name	Pin Type	Function	Pin
HSYNC0	Schmitt Trigger Input w/ 5V-tolerant	HSYNC / Composite Sync for VGA Input from channel 0	25
VSYNC0	Schmitt Trigger Input w/ 5V-tolerant	VSYNC for VGA Input from channel 0	31
BIN0P	Analog Input	Analog Blue Input from Channel 0	26
SOGIN0	Analog Input	Sync On Green Input from Channel 0	27
GIN0P	Analog Input	Analog Green Input from Channel 0	28
GIN0M	Analog Input	Reference Ground for Analog Green Input from Channel 0	29
RIN0P	Analog Input	Analog Red Input from Channel 0	30
BIN1P	Analog Input	Analog Blue Input from Channel 1	34
SOGIN1	Analog Input	Sync On Green Input from Channel 1	35
GIN1P	Analog Input	Analog Green Input from Channel 1	36
GIN1M	Analog Input	Reference Ground for Analog Green Input from Channel 1	37
RIN1P	Analog Input	Analog Red Input from Channel 1	38

Analog Video Input/Output Interface

Pin Name	Pin Type	Function	Pin
CVBS4	Analog Input	CVBS (Composite) Video Input Channel 4	40
CVBS3	Analog Input	CVBS (Composite) Video Input Channel 3	41
CVBS2	Analog Input	CVBS (Composite) Video Input Channel 2	42
CVBS1	Analog Input	CVBS (Composite) Video Input Channel 1	43
CVBS0	Analog Input	CVBS (Composite) Video Input Channel 0	44
VCOM	Analog Input	CVBS Input Reference Ground	45
CVBSOUT0	Analog Output	CVBS (Composite) Video Output Channel 0	46

Analog Audio Input/Output Interface

Pin Name	Pin Type	Function	Pin
SIFP	Analog Input	SIF Audio Input	77
SIFM	Analog Input	Reference Ground for SIF Audio Input	78
I2S_OUT_WS	I/O w/ 5V-tolerant	Word Select Output; 4mA driving strength / Universal Asynchronous Receiver 2 (UART2_RX)	80
I2S_OUT_SD	I/O w/ 5V-tolerant	Audio Serial Data Output; 4mA driving strength / Universal Asynchronous Transmitter 2 (UART2_TX)	81

Pin Name	Pin Type	Function	Pin
SPDIFI	Input w/ 5V-tolerant	S/PDIF Audio Input / Pulse Width Modulation Output; 4mA driving strength (PWM3) / Universal Asynchronous Receiver 1 (UART1_RX)	84
SPDIFO	Output	S/PDIF Audio Output; 4mA driving strength	85
I2S_OUT_MCK	Output w/ 5V-tolerant	Audio Master Clock Output	89
I2S_OUT_BCK	Output w/ 5V-tolerant	Audio Bit Clock Output	90
I2S_IN_WS	I/O	Word Select Input / Universal Asynchronous Receiver 3 (UART3_RX) / Pulse Width Modulation Output; 4mA driving strength (PWM0/PWM4)	126
I2S_IN_SD	Input	Audio Serial Data Input / Universal Asynchronous Transmitter 3 (UART3_TX) / Pulse Width Modulation Output; 4mA driving strength (PWM1/PWM5)	127
I2S_IN_BCK	I/O	Audio Bit Clock Input / Pulse Width Modulation Output; 4mA driving strength (PWM2)	128
I2S_OUT_MUTE	I/O	Audio Output Mute Control / Pulse Width Modulation Output; 4mA driving strength (PWM3)	129
AUL0	Analog Input	Audio Line Input Left Channel 0	47
AUR0	Analog Input	Audio Line Input Right Channel 0	48
AUL1	Analog Input	Audio Line Input Left Channel 1	49
AUR1	Analog Input	Audio Line Input Right Channel 1	50
AUL2	Analog Input	Audio Line Input Left Channel 2	55
AUR2	Analog Input	Audio Line Input Right Channel 2	56
AUL3	Analog Input	Audio Line Input Left Channel 3	57
AUR3	Analog Input	Audio Line Input Right Channel 3	58
AUL4	Analog Input	Audio Line Input Left Channel 4	59
AUR4	Analog Input	Audio Line Input Right Channel 4	60
AUVRM	Analog Output	Negative Reference Voltage for Audio ADC	51
AUVRP	Analog Output	Positive Reference Voltage for Audio ADC	52
AUVAG	Analog Output	Reference Voltage for Audio Common Mode	53
AUOUTL1	Analog Output	Main Audio Output Left Channel 1	62
AUOUTR1	Analog Output	Main Audio Output Right Channel 1	63
AUOUTL0	Analog Output	Main Audio Output Left Channel 0	64

Pin Name	Pin Type	Function	Pin
AUOUTR0	Analog Output	Main Audio Output Right Channel 0	65
EAR_OUTL	Analog Output	Audio DAC Earphone Left Channel Output	66
EAR_OUTR	Analog Output	Audio DAC Earphone Right Channel Output	67

LVDS Interface

Pin Name	Pin Type	Function	Pin
LVA0M	Output	LVDS A-Link Channel 0 Negative Data Output	110
LVA0P	Output	LVDS A-Link Channel 0 Positive Data Output	109
LVA1M	Output	LVDS A-Link Channel 1 Negative Data Output	107
LVA1P	Output	LVDS A-Link Channel 1 Positive Data Output	106
LVA2M	Output	LVDS A-Link Channel 2 Negative Data Output	105
LVA2P	Output	LVDS A-Link Channel 2 Positive Data Output	104
LVA3M	Output	LVDS A-Link Channel 3 Negative Data Output	101
LVA3P	Output	LVDS A-Link Channel 3 Positive Data Output	100
LVA4M	Output	LVDS A-Link Channel 4 Negative Data Output	99
LVA4P	Output	LVDS A-Link Channel 4 Positive Data Output	98
LVACKM	Output	LVDS A-Link Negative Clock Output	102
LVACKP	Output	LVDS A-Link Positive Clock Output	103
LVB0M	Output	LVDS B-Link Channel 0 Negative Data Output	122
LVB0P	Output	LVDS B-Link Channel 0 Positive Data Output	121
LVB1M	Output	LVDS B-Link Channel 1 Negative Data Output	120
LVB1P	Output	LVDS B-Link Channel 1 Positive Data Output	119
LVB2M	Output	LVDS B-Link Channel 2 Negative Data Output	118
LVB2P	Output	LVDS B-Link Channel 2 Positive Data Output	117
LVB3M	Output	LVDS B-Link Channel 3 Negative Data Output	114
LVB3P	Output	LVDS B-Link Channel 3 Positive Data Output	113
LVB4M	Output	LVDS B-Link Channel 4 Negative Data Output	112
LVB4P	Output	LVDS B-Link Channel 4 Positive Data Output	111
LVBCKM	Output	LVDS B-Link Negative Clock Output	116
LVBCKP	Output	LVDS B-Link Positive Clock Output	117

DVI/HDMI Interface

Pin Name	Pin Type	Function	Pin
RXACKN	DVI/HDMI Input	Negative DVI/HDMI Input for A Link Clock Channel	14
RXACKP	DVI/HDMI Input	Positive DVI/HDMI Input for A Link Clock Channel	15

Pin Name	Pin Type	Function	Pin
RXA0N	DVI/HDMI Input	Negative DVI/HDMI Input for A Link Data Channel 0	16
RXA0P	DVI/HDMI Input	Positive DVI/HDMI Input for A Link Data Channel 0	17
RXA1N	DVI/HDMI Input	Negative DVI/HDMI Input for A Link Data Channel 1	19
RXA1P	DVI/HDMI Input	Positive DVI/HDMI Input for A Link Data Channel 1	20
RXA2N	DVI/HDMI Input	Negative DVI/HDMI Input for A Link Data Channel 2	22
RXA2P	DVI/HDMI Input	Positive DVI/HDMI Input for A Link Data Channel 2	23
RXBCKN	DVI/HDMI Input	Negative DVI/HDMI Input for B Link Clock Channel	3
RXBCKP	DVI/HDMI Input	Positive DVI/HDMI Input for B Link Clock Channel	4
RXB0N	DVI/HDMI Input	Negative DVI/HDMI Input for B Link Data Channel 0	5
RXB0P	DVI/HDMI Input	Positive DVI/HDMI Input for B Link Data Channel 0	6
RXB1N	DVI/HDMI Input	Negative DVI/HDMI Input for B Link Data Channel 1	8
RXB1P	DVI/HDMI Input	Positive DVI/HDMI Input for B Link Data Channel 1	9
RXB2N	DVI/HDMI Input	Negative DVI/HDMI Input for B Link Data Channel 2	11
RXB2P	DVI/HDMI Input	Positive DVI/HDMI Input for B Link Data Channel 2	12

Serial Flash Interface

Pin Name	Pin Type	Function	Pin
SCK	Output	SPI Flash Serial Clock	201
SDI	Output	SPI Flash Serial Data Input	202
SDO	Input w/ 5V-tolerant	SPI Flash Serial Data Output	203
SCZ	Output	SPI Flash Chip Select	204
IRIN	Input w/ 5V-tolerant	IR Receiver Input	215

GPIO Interface

Pin Name	Pin Type	Function	Pin
GPIO[42:41]	I/O w/ 5V-tolerant	General Purpose Input/Output; 4mA driving strength	83, 82
GPIO[44]	I/O w/ 5V-tolerant	General Purpose Input/Output; 4mA driving strength	88
GPIO[54:52]	I/O w/ 5V-tolerant	General Purpose Input/Output; 4mA driving strength	93-91
GPIO[6]	I/O	General Purpose Input/Output / Word Select Output; 4mA driving strength (I2S_OUT_WS) / Universal Asynchronous Transmitter 0 (UART0_TX)	211
GPIO[7]	I/O	General Purpose Input/Output; 4mA driving strength	212
GPIO[8]	I/O	General Purpose Input/Output / Universal Asynchronous Receiver 0 (UART0_RX)	213

Pin Name	Pin Type	Function	Pin
GPIO[9]	I/O	General Purpose Input/Output; 4mA driving strength	214
PWM2	I/O	Pulse Width Modulation Output; 4mA driving strength (PWM2) / Universal Asynchronous Transmitter 1 (UART1_TX)	96
PWM1	Output w/ 5V-tolerant	Pulse Width Modulation Output; 4mA driving strength	132
PWM0	Output w/ 5V-tolerant	Pulse Width Modulation Output; 4mA driving strength	131
SAR2	Analog Input	SAR Low Speed ADC Input 2	207
SAR1	Analog Input	SAR Low Speed ADC Input 1	206
SAR0	Analog Input	SAR Low Speed ADC Input 0	205

DRAM Interface

Pin Name	Pin Type	Function	Pin
BADR[2:0]	Output	DRAM Memory Bank Address	141, 144, 143
MCLKE	Output	DRAM Memory Clock Enable	145
WEZ	Output	Write Enable; active low	146
DQMU	Output	Data Mask for Upper Byte; active high	157
DQML	Output	Data Mask for Lower Byte; active high	158
DQSL	I/O	Data Strobe for Lower Byte	160
DQSLZ	I/O	Data Strobe Inverse for Lower Byte	161
DQSU	I/O	Data Strobe for Upper Byte	164
DQSUZ	I/O	Data Strobe Inverse for Upper Byte	165
MVREF	Input	Reference Voltage for DDR SDRAM Interface	173
MCLK	Output	DRAM Memory Positive Differential Clock	177
MCLKZ	Output	DRAM Memory Negative Differential Clock	179
ODT	I/O	Reserved for future On-Die Termination	180
RASZ	Output	Row Address Strobe; active low	181
CASZ	Output	Column Address Strobe; active low	182
MADR[13:0]	Output	DRAM Memory Address	190, 134, 189, 139, 135, 188, 136, 187, 137, 186, 138, 184, 140, 183
MDATA[15:0]	I/O	DRAM Memory Data Bus	166, 156, 170, 154, 152, 169, 155, 167, 171, 151, 176, 147, 149, 174, 150, 172

USB Interface

Pin Name	Pin Type	Function	Pin
USB0_DP	Analog I/O	USB Non Inverting Data Input/Output for Port 0	197
USB0_DM	Analog I/O	USB Inverting Data Input/Output for Port 0	196
USB1_DP	Analog I/O	USB Non Inverting Data Input/Output for Port 1	95
USB1_DM	Analog I/O	USB Inverting Data Input/Output for Port 1	94

VIF Interface

Pin Name	Pin Type	Function	Pin
VIFM	Analog Input	Negative Video IF Input	74
VIFP	Analog Input	Positive Video IF Input	75
TAGC	Analog Output	Tuner Automatic Gain Control Output	79
PGA_COM	Analog Input	VIF PGA Negative Source	73

Misc. Interface

Pin Name	Pin Type	Function	Pin
HWRESET	Schmitt Trigger Input w/ 5V-tolerant	Hardware Reset; active high	1
DDCDA_DA	I/O w/ 5V-tolerant	HDCP Serial Bus Data / DDC Data of DVI/HDMI Port A	18
DDCDA_CK	Input w/ 5V-tolerant	HDCP Serial Bus Clock / DDC Clock of DVI/HDMI Port A	21
DDCDB_DA	I/O w/ 5V-tolerant	HDCP Serial Bus Data / DDC Data of DVI/HDMI Port B	10
DDCDB_CK	Input w/ 5V-tolerant	HDCP Serial Bus Clock / DDC Clock of DVI/HDMI Port B	13
DDCR_DA	I/O w/ 5V-tolerant	DDC Data for ROM	192
DDCR_CK	Input w/ 5V-tolerant	DDC Clock for ROM	194
HOTPLUGA	I/O w/ 5V-tolerant	Hot-plug control for DVI/HDMI Port A	208
HOTPLUGB	I/O w/ 5V-tolerant	Hot-plug control for DVI/HDMI Port B	2
DDCA_DA	I/O w/ 5V-tolerant	DDC Data for Analog port	210
DDCA_CK	I/O w/ 5V-tolerant	DDC Clock for Analog port	209
XIN	Crystal Oscillator Input	Crystal Oscillator Input	69
XOUT	Crystal Oscillator Output	Crystal Oscillator Output	70
BYPASS		For External Bypass Capacitor	199
CEC	I/O	Consumer Electronics Control	216

Power Pins

Pin Name	Pin Type	Function	Pin
AVDD_33	3.3V Power	Analog 3.3V Power	39
AVDD_25	2.5V Power	Analog 2.5V Power	33
AVDD_AU25	2.5V Power	Audio 2.5V Power	54
AVDD_AU33	3.3V Power	Audio 3.3V Power	61
AVDD_EAR	3.3V Power	Earphone Driver Power	68
AVDD_DMPLL	3.3V Power	Crystal Power	71
AVDD_REF	2.5V Power	Demod ADC Power	72
AVDD_PGA	2.5V Power	Demod PGA Power	76
AVDD_MOD	2.5V Power	MOD 2.5V Power	108, 124
AVDD_MEMPLL	3.3V Power	PLL Power	125, 163
AVDD_DDR	1.8V Power	DDR Power	142, 148, 153, 159, 168, 175, 178, 185,
DVDD_DDR	1.26V Power	DDR 1.26V Power	162
AVDD_ALIVE	3.3V Power	Alive Domain IO Power	7, 97, 198
VDDC	1.26V Power	Digital Core Power	24, 32, 86, 123, 133, 191
VDDP	3.3V Power	Digital Input/Output Power	87, 130, 193
GND	Ground	Ground	195, 200

REVISION HISTORY

Document	Description	Date
MST6M48RHS_pin_v01	• Initial release	Dec 2009
MST6M48RHS_pin_v02	• Updated Pin 51 in Pin Diagram and Pin Description	Feb 2010