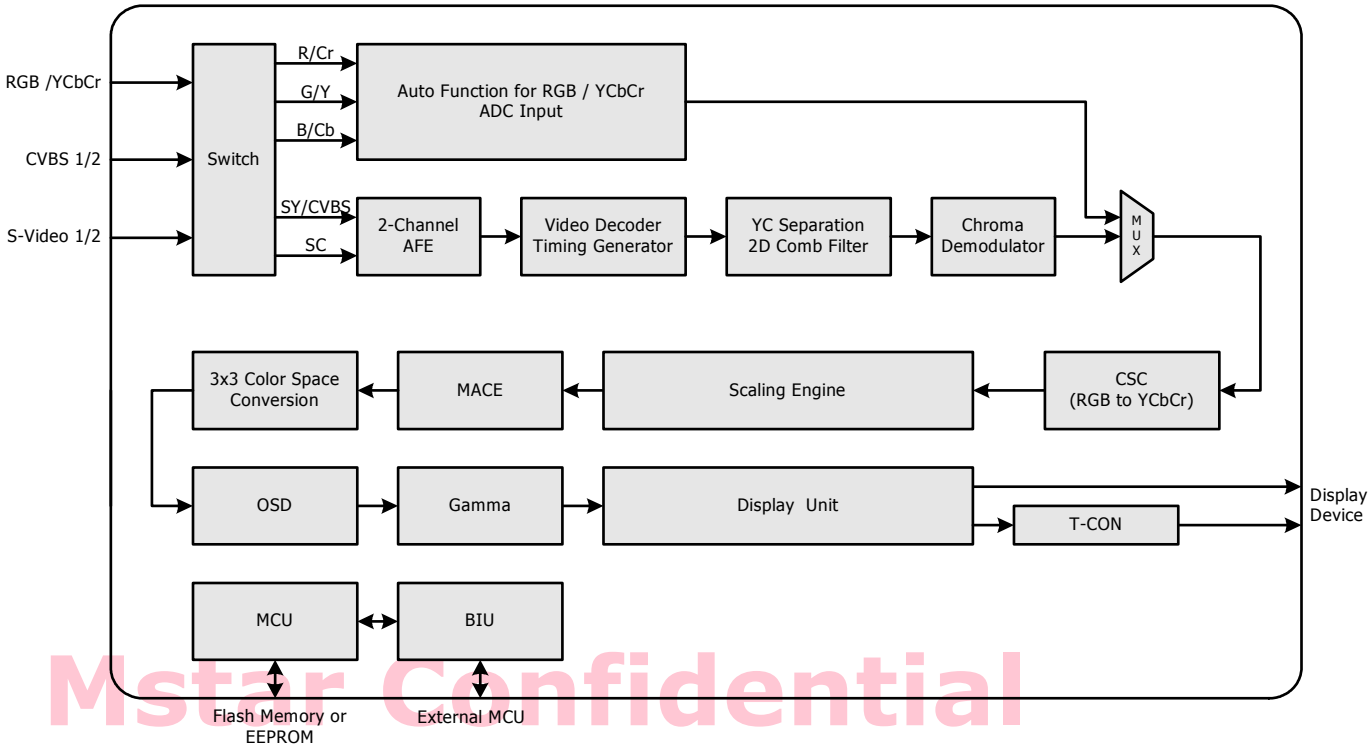
# FEATURES

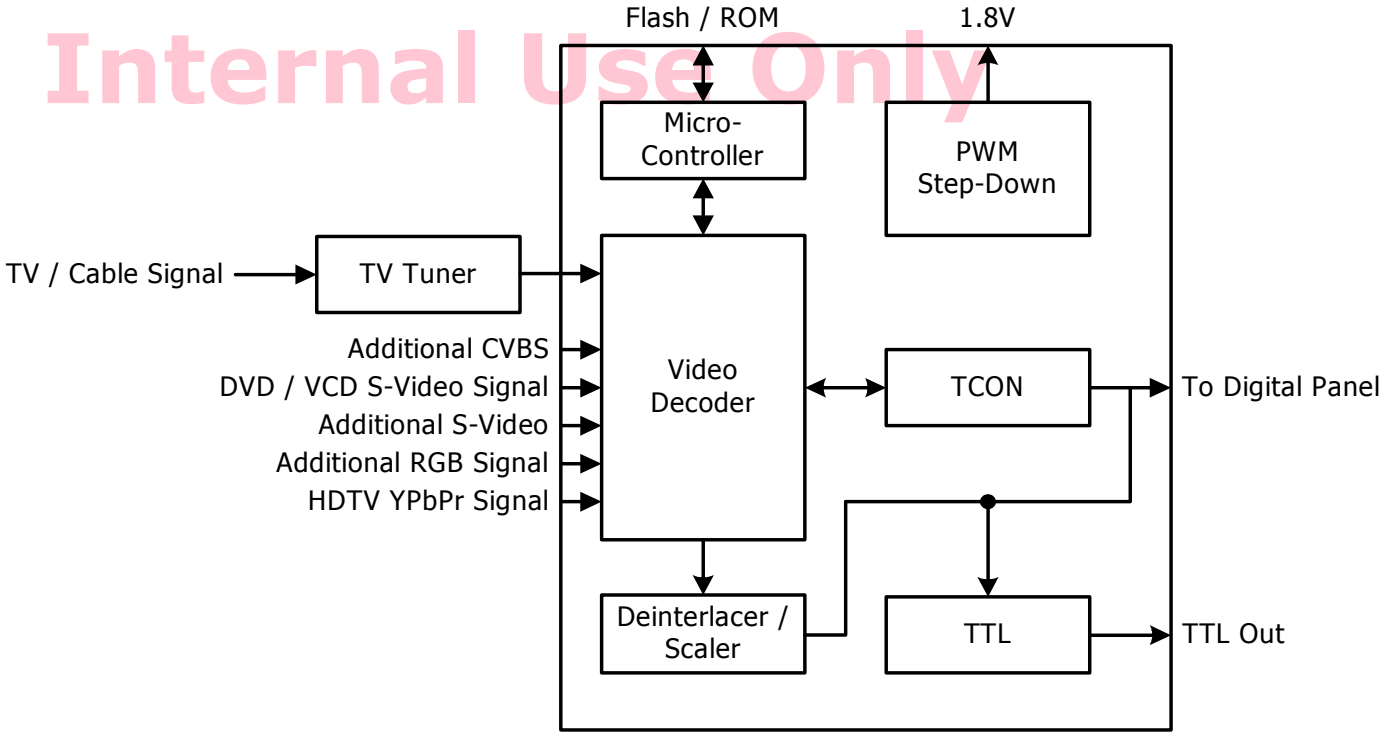
- Video Decoder
  - Supports NTSC, PAL and SECAM video input formats
  - 2D NTSC and PAL comb-filter for Y/C separation of CVBS input
  - Multiple CVBS and S-video inputs
  - ACC, AGC, and DCGC (Digital Chroma Gain Control)
- Analog Input
  - Supports RGB input format from PC, camcorders and GPS
  - Supports YCbCr inputs from conventional video source and HDTV
  - Supports video input 480i, 480p, 576i, 576p, 720p, 1080i; 1080P; RGB input resolution in 640x480, 800x480, and 800x600, 1024x768, 1280x1024
  - 3-channel low-power 10-bit ADCs integration for YCbCr and RGB
  - Supports RGB composite sync input (CSYNC), SOY, SOG, HSYNC, and VSYNC
  - On-chip clock synthesizer and PLL
  - Auto-position adjustment, auto-phase adjustment, auto-gain adjustment, and auto-mode detection
- Color Engine
  - Brightness, contrast, saturation, and hue adjustment
  - 9-tap programmable multi-purpose FIR (Finite Impulse Response) filter
  - Differential 3-band peaking engine
  - Luminance Transient Improvement (LTI)
  - Chrominance Transient Improvement (CTI)
  - Black Level Extension (BLE)
  - White Level Extension (WLE)
  - Favor Color Compensation (FCC)
  - 3-channel gamma curve adjustment
- Scaling Engine/Panel Interface
  - Supports LVDS panel up to 1366x768
  - Supports TTL/TCON and analog TCON panel
  - Supports single 8-bit TTL panel output
  - Supports various displaying modes
  - Supports horizontal panorama scaling
- Miscellaneous
  - Built-in MCU
  - Supports CCIR656 digital input
  - Built-in internal OSD with 256 programmable fonts, 16-color palettes, and 12-bit color resolution
  - Spread spectrum clocks
  - 3.3V output pads with programmable driving current
  - 100-pin LQFP package

## BLOCK DIAGRAM





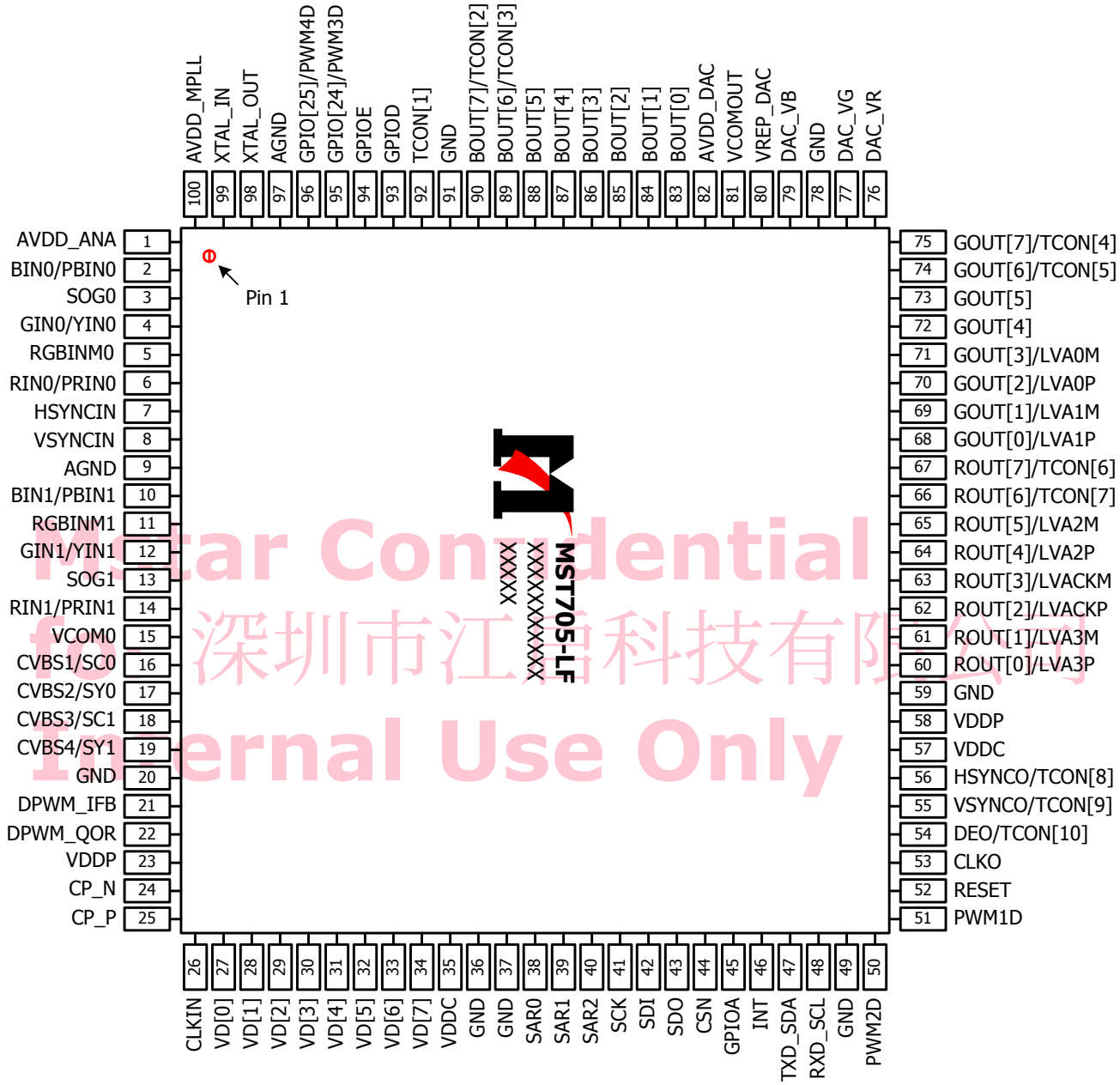

## SYSTEM APPLICATION DIAGRAM



## GENERAL DESCRIPTION

The MST705 is a high quality ASIC for NTSC/PAL/SECAM car TV application. It receives analog NTSC/PAL/SECAM CVBS and S-Video inputs from TV tuners, DVD or VCR sources, including weak and distorted signals, as well as analog YCbCr input from HDTV/SDTV systems. Automatic gain control (AGC) and 10-bit 3-channel A/D converters provide high resolution video quantization. With automatic video source and mode detection, users can easily switch and adjust variety of signal sources. Multiple internal adaptive PLLs precisely extract pixel clock from video source and perform sharp color demodulation. Built-in line-buffer supports adaptive 2-D comb-filter, 2-D sharpening, and synchronization stabler in a condense manner. The output format of MST705 supports 6-bit TTL/TCON and LVDS digital TFT-LCD modules.

# PIN DIAGRAM (MST705)



# PIN DESCRIPTION

## Analog Panel Output Interface

| Pin Name | Pin Type | Function | Pin |
|---|---|---|---|
| DAC_VR | Analog Output | Red Channel Output 3.0 Vp-p | 76 |
| DAC_VG | Analog Output | Green Channel Output 3.0 Vp-p | 77 |
| DAC_VB | Analog Output | Blue Channel Output 3.0 Vp-p | 79 |
| VREP_DAC | Analog Input | DAC Top Reference Voltage Decoupling Cap. 1uF to Ground | 80 |
| VCOMOUT | Analog Output | Pulse Output for Common Voltage. | 81 |

## Analog Interface

| Pin Name | Pin Type | Function | Pin |
|---|---|---|---|
| BIN0/PBIN0 | Analog Input | Analog Blue Input from Channel 0 | 2 |
| SOG0 | Analog Input | Sync On Green Signal Input from Channel 0 | 3 |
| GIN0/YIN0 | Analog Input | Analog Green Input from Channel 0 | 4 |
| RGBINM0 | Analog Input | Reference Ground for Analog Green Input from Channel 0 | 5 |
| RIN0/PRIN0 | Analog Input | Analog Red Input from Channel 0 | 6 |
| HSYNCIN | Schmitt Trigger Input w/ 5V-tolerant | HSYNC / Composite Sync for VGA Input | 7 |
| VSYNCIN | Schmitt Trigger Input w/ 5V-tolerant | VSYNC for VGA Input | 8 |
| BIN1/PBIN1 | Analog Input | Analog Blue Input from Channel 1 | 10 |
| RGBINM1 | Analog Input | Reference Ground for Analog Green Input from Channel 1 | 11 |
| GIN1/YIN1 | Analog Input | Analog Green Input from Channel 1 | 12 |
| SOG1 | Analog Input | Sync On Green Signal Input from Channel 1 | 13 |
| RIN1/PRIN1 | Analog Input | Analog Red Input from Channel 1 | 14 |
| VCOM0 | Analog Input | Common Analog Input Reference Ground 0 | 15 |
| CVBS1/SC0 | Analog Input | CVBS0 or S-Video (Y/C) Input Channel 0 | 16 |
| CVBS2/SY0 | Analog Input | CVBS1 or S-Video (Y/C) Input Channel 0 | 17 |
| CVBS3/SC1 | Analog Input | CVBS2 or S-Video (Y/C) Input Channel 1 | 18 |
| CVBS4/SY1 | Analog Input | CVBS3 or S-Video (Y/C) Input Channel 1 | 19 |

## Switching Power and PWM Interface

| Pin Name | Pin Type | Function | Pin |
|---|---|---|---|
| CP_N | Output | Charge Pump Negative Pulse for DC-DC Positive Voltage Converter | 24 |
| CP_P | Output | Charge Pump Positive Pulse for DC-DC Positive Voltage Converter | 25 |

## Internal MCU Interface with Serial Flash Memory

| Pin Name | Pin Type | Function | Pin |
|---|---|---|---|
| SAR2 | Analog Input | SAR Low Speed ADC Input 2 | 40 |
| SAR1 | Analog Input | SAR Low Speed ADC Input 1 | 39 |
| SAR0 | Analog Input | SAR Low Speed ADC Input 0 | 38 |
| SCK | Output | SPI Interface Sampling Clock | 41 |
| SDI | Output | SPI Interface Data-In | 42 |
| SDO | Input w/ 5V-tolerant | SPI Interface Data-Out | 43 |
| CSN | Output | SPI Interface Chip Select | 44 |
| INT | Input | Interrupt Input for IR Receiver | 46 |
| TXD_SDA | I/O w/ 5V-tolerant, w/ pull-up resistor | Serial Bus Data | 47 |
| RXD_SCL | Input w/ 5V-tolerant | Serial Bus Clock | 48 |
| PWM2D | Output | Pulse Width Modulation Output; 4mA driving strength | 50 |
| PWM1D | Output | Pulse Width Modulation Output; 4mA driving strength | 51 |
| GPIO[25]/PWM4D | I/O w/ 5V-tolerant | General Purpose Input/Output / Pulse Width Modulation Output; 4mA driving strength | 96 |
| GPIO[24]/PWM3D | I/O w/ 5V-tolerant | General Purpose Input/Output / Pulse Width Modulation Output; 4mA driving strength | 95 |



## Digital Panel Output Interface

| Pin Name | Pin Type | Function | Pin |
|---|---|---|---|
| CLKO | Output | Display Clock Output | 53 |
| DEO/TCON[10] | Output | Display Enable Output | 54 |
| VSYNCO/TCON[9] | Output | Vertical Sync Output / TCON Output[9] | 55 |
| HSYNCO/TCON[8] | Output | Horizontal Sync Output / TCON Output[8] | 56 |

| Pin Name | Pin Type | Function | Pin |
|---|---|---|---|
| ROUT[7]/TCON[6] | Output | Red channel Output [7] / TCON Output[6] | 67 |
| ROUT[6]/TCON[7] | Output | Red channel Output [6] / TCON Output[7] | 66 |
| ROUT[5]/LVA2M | Output | Red channel Output [5] /<br>LVDS A-Link Channel 2 Negative Data Output | 65 |
| ROUT[4]/LVA2P | Output | Red channel Output [4] /<br>LVDS A-Link Channel 2 Positive Data Output | 64 |
| ROUT[3]/LVACKM | Output | Red channel Output [3] /<br>LVDS A-Link Negative Clock Output | 63 |
| ROUT[2]/LVACKP | Output | Red channel Output [2] /<br>LVDS A-Link Positive Clock Output | 62 |
| ROUT[1]/LVA3M | Output | Red channel Output [1] /<br>LVDS A-Link Channel 3 Negative Data Output | 61 |
| ROUT[0]/LVA3P | Output | Red channel Output [0] /<br>LVDS A-Link Channel 3 Positive Data Output | 60 |
| GOUT[7]/TCON[4] | Output | Green channel Output [7] / TCON Output[4] | 75 |
| GOUT[6]/TCON[5] | Output | Green channel Output [6] / TCON Output[5] | 74 |
| GOUT[5:4] | Output | Green channel Output [5:4] | 73, 72 |
| GOUT[3]/LVA0M | Output | Green channel Output [3] /<br>LVDS A-Link Channel 0 Negative Data Output | 71 |
| GOUT[2]/LVA0P | Output | Green channel Output [2] /<br>LVDS A-Link Channel 0 Positive Data Output | 70 |
| GOUT[1]/LVA1M | Output | Green channel Output [1] /<br>LVDS A-Link Channel 1 Negative Data Output | 69 |
| GOUT[0]/LVA1P | Output | Green channel Output [0] /<br>LVDS A-Link Channel 1 Positive Data Output | 68 |
| BOUT[7]/TCON[2] | Output | Blue channel Output [7] / TCON Output[2] | 90 |
| BOUT[6]/TCON[3] | Output | Blue channel Output [6] / TCON Output[3] | 89 |
| BOUT[5:0] | Output | Blue channel Output [5:0] | 88-83 |
| TCON[0] | Output | TCON Output[1] | 92 |



## Digital Video Input Interface

| Pin Name | Pin Type | Function | Pin |
|---|---|---|---|
| CLKIN | Input w/5V-tolerant | Sample Clock ITU656 Video Input | 26 |
| VD[7:0] | Input w/5V-tolerant | ITU656 Video Data bus | 34-27 |

## Switching Power and PWM Interface

| Pin Name | Pin Type | Function | Pin |
|---|---|---|---|
| CP_N | Output | Charge Pump Negative Pulse for DC-DC Positive Voltage Converter | 24 |
| CP_P | Output | Charge Pump Positive Pulse for DC-DC Positive Voltage Converter | 25 |

## GPIO Interface

| Pin Name | Pin Type | Function | Pin |
|---|---|---|---|
| GPIOA | I/O w/ 5V-tolerant | General Purpose Input Output; 4mA driving strength | 45 |
| GPIOD | I/O w/ 5V-tolerant | General Purpose Input Output; 4mA driving strength | 93 |
| GPIOE | I/O w/ 5V-tolerant | General Purpose Input Output; 4mA driving strength | 94 |

## Digital PWM Interface

| Pin Name | Pin Type | Function | Pin |
|---|---|---|---|
| DPWM_IFB | Analog Input | Input for DPWM Feedback Loop | 21 |
| DPWM_QOR | Output | DPWM Output | 22 |



## Misc. Interface

| Pin Name | Pin Type | Function | Pin |
|---|---|---|---|
| RESET | Schmitt Trigger Input w/ 5V-tolerant | Hardware Reset; active high | 52 |
| XTAL_IN | Analog Input | Crystal Oscillator Input | 99 |
| XTAL_OUT | Analog Output | Crystal Oscillator Output | 98 |

## Power Pins

| Pin Name | Pin Type | Function | Pin |
|---|---|---|---|
| AVDD_ANA | 3.3V Power | Analog ADC Power | 1 |
| AVDD_DAC | 3.3V Power | Voltage DAC Power | 82 |
| AVDD_MPLL | 3.3V Power | MPLL Power | 100 |
| VDDC | 1.2V Power | Digital Core Power | 35, 57 |
| VDDP | 3.3V Power | Digital Input/Output Power | 23, 58 |
| AGND | Ground | Analog Ground | 9, 97 |
| GND | Ground | Ground | 20, 36, 37, 49, 59, 78, 91 |

# ELECTRICAL SPECIFICATIONS

## Absolute Maximum Ratings

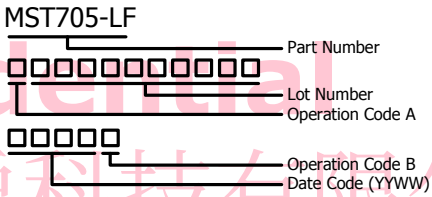
| Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|
| 3.3V Supply Voltages | $V_{VDD\_33}$ | | 3.63 | V |
| 1.2V Supply Voltages | $V_{VDD\_12}$ | | 1.32 | V |
| Input Voltage (5V tolerant inputs) | $V_{IN5Vtol}$ | | 5.0 | V |
| Input Voltage (non 5V tolerant inputs) | $V_{IN}$ | | $V_{VDD\_33}$ | V |
| Ambient Operating Temperature | $T_A$ | 0 | 70 | °C |
| Storage Temperature | $T_{STG}$ | -40 | 125 | °C |
| Junction Temperature | $T_J$ | | 125 | °C |

**Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and does not imply functional operation of the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.**

# ORDERING GUIDE

| Part Number | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| MST705-LF | 0°C to +70°C | LQFP | 100 |

# MARKING INFORMATION






# DISCLAIMER

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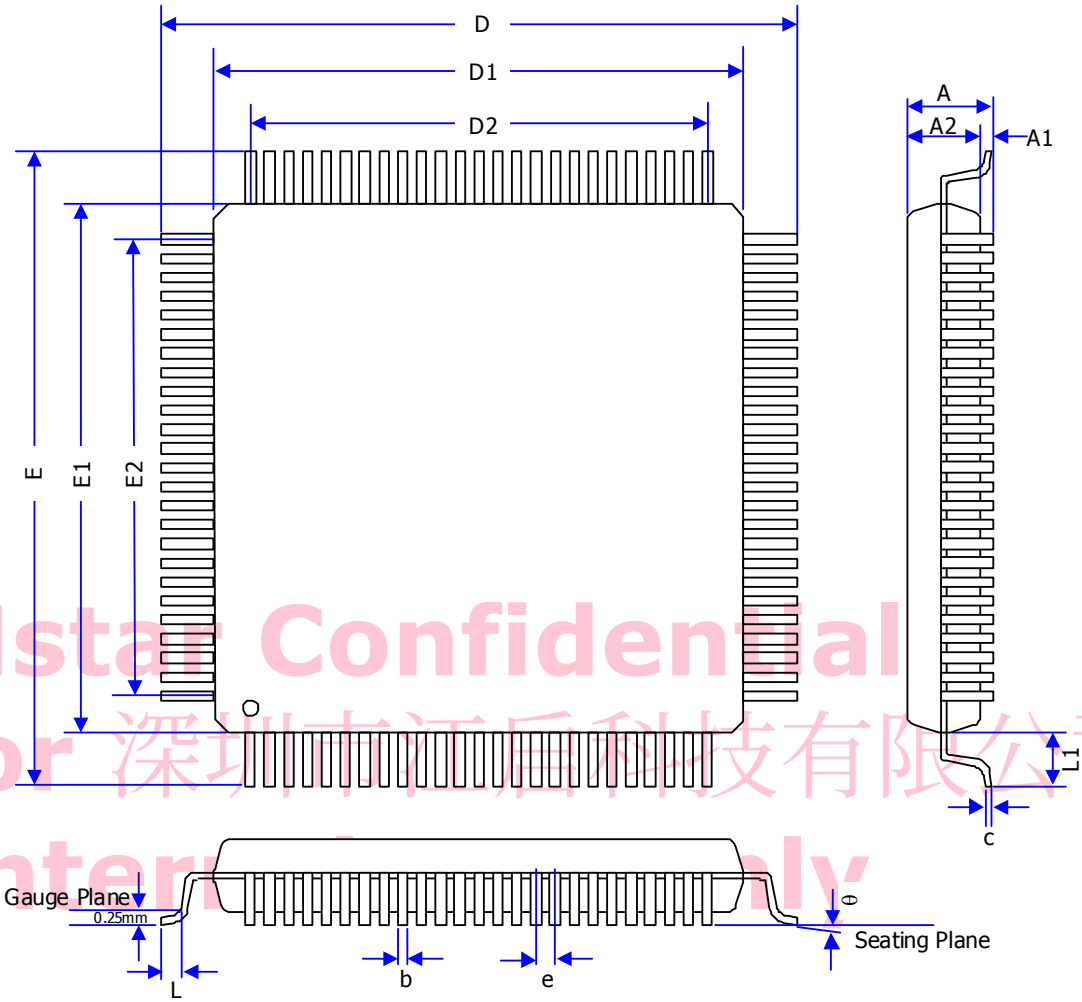
**Electrostatic charges accumulate on both test equipment and human body and can discharge without detection. MST705 comes with ESD protection circuitry; however, the device may be permanently damaged when subjected to high energy discharges. The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.**

# REVISION HISTORY

| Document | Description | Date |
|---|---|---|
| MST705_ds_v01 | • Initial release | Nov 2010 |

# MECHANICAL DIMENSIONS






| Symbol | Millimeter | | | Inch | | |
|---|---|---|---|---|---|---|
| | Min. | Nom. | Max. | Min. | Nom. | Max. |
| A | - | - | 1.60 | - | - | 0.063 |
| A1 | 0.05 | - | 0.15 | 0.002 | - | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| D | 16.00 BSC. | | | 0.630 BSC. | | |
| D1 | 14.00 BSC. | | | 0.551 BSC. | | |
| D2 | 12.00 | | | 0.472 | | |
| E | 16.00 BSC. | | | 0.630 BSC. | | |
| E1 | 14.00 BSC. | | | 0.551 BSC. | | |
| E2 | 12.00 | | | 0.472 | | |

| Symbol | Millimeter | | | Inch | | |
|---|---|---|---|---|---|---|
| | Min. | Nom. | Max. | Min. | Nom. | Max. |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| b | 0.17 | 0.20 | 0.27 | 0.007 | 0.008 | 0.011 |
| c | 0.09 | - | 0.20 | 0.004 | - | 0.008 |
| e | 0.50 BSC. | | | 0.020 BSC. | | |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 1.00 Ref | | | 0.039 Ref | | |

# REGISTER DESCRIPTION

## General Control Register

| General Control Register | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| **00h** | **REGBK** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | XTAL_OK (RO) | 7 | Crystal ready. | |
| | MCU_SEL (RO) | 6 | 0: Embedded MCU.<br>1: External serial bus interface. | |
| | - | 5:4 | Reserved. | |
| | AINC | 3 | Serial bus address auto Increase.<br>0: Enable.<br>1: Disable. | |
| | - | 2 | Reserved. | |
| | REGBK[1:0] | 1:0 | Register Bank Select.<br>00: Register of scaler.<br>01: Register of ADC/ACE/MCU.<br>10: Register of Video Decoder Front End (VFE).<br>11: Register of Video Decoder 2D Comb Filter (VCF). | |
| | REGBK[2:0] | 2:0 | Register Bank Select.<br>000: Register of scaler.<br>001: Register of ADC/ACE/MCU.<br>010: Register of Video Decoder Front End (VFE).<br>011: Register of Video Decoder 2D Comb Filter (VCF).<br>100: Register of LVDS/DPWM. | |
| **01h ~ FFh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |

## Scaler Register (Bank = 00, Registers 01h ~ 9Fh)

| Scaler Register (Bank=00, Registers 01h ~ 9Fh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| **01h** | **DBFC** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | DBL[1:0] | 2:1 | Double Buffer Load.<br>00: Keep old register value.<br>01: Load new data (auto reset to 00 when load finish).<br>10: Automatically load data at VSYNC blanking.<br>11: Reserved. | |
| | DB_EN | 0 | Double Buffer Enable.<br>0: Disable.<br>1: Enable. | |
| **02h** | **ISELECT** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | NIS | 7 | No Input Source.<br>0: Input source active.<br>1: Input source inactive, output is free-run. | |
| | STYPE[1:0] | 6:5 | Input Sync Type.<br>00: Auto detected.<br>01: Input is separated HSYNC and VSYNC.<br>10: Input is Composite sync.<br>11: Input is sync-on-green (SOG). | |
| | COMP | 4 | CSYNC/SOG select (only useful when STYPE = 00).<br>0: CSYNC.<br>1: SOG. | |
| | ICS | 3 | Input Color Space.<br>0: RGB.<br>1: YCbCr. | |
| | IHSU | 2 | Input Sync Usage.<br>When EXTVD=0:<br>0: Use HSYNC to perform mode detection, HSOUT from ADC to sample pixel.<br>1: Use HSYNC only.<br>When EXTVD=1:<br>0: Normal.<br>1: Output black at blanking. | |
| | BYPASSMD | 1 | By-Pass Mode for interlace-input-interlace-output. | |
| | EXTVD | 0 | 0: Select analog input (CVBS/S-Video/RGB/YCbCr).<br>1: Select digital input (CCIR656). | |
| **03h** | **IPCTRL2** | **7:0** | **Default : 0x18** | **Access : R/W** |

| Scaler Register (Bank=00, Registers 01h ~ 9Fh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| | VDS_EN | 7 | Input data double sample<br>In CCIR input mode,<br>0: for horizontal output resolution less than 720 pixels.<br>1: for horizontal output resolution more than 720 pixels.<br>In analog input mode,<br>0: half sample of input data.<br>1: original sample of input data. | |
| | VDS_MTHD | 6 | Input data double sample Method.<br>0: Using average.<br>1: Using advance GT filter. | |
| | IVDS | 5 | Input VSYNC Delay Select.<br>0: Delay 1/4 input HSYNC (recommended).<br>1: No delay. | |
| | HES | 4 | Input HSYNC reference Edge Select.<br>0: From HSYNC leading edge, default value.<br>1: From HSYNC tailing edge. | |
| | VES | 3 | Input VSYNC reference Edge Select.<br>0: From VSYNC leading edge, default value.<br>1: From VSYNC tailing edge. | |
| | ESLS | 2 | Early Sample Line Select.<br>0: 8 lines.<br>1: 16 lines. | |
| | VWRP | 1 | Input image Vertical Wrap.<br>0: Disable.<br>1: Enable. | |
| | HWRP | 0 | Input image Horizontal Wrap.<br>0: Disable.<br>1: Enable. | |
| **04h** | **ISCTRL** | **7:0** | **Default : 0x10** | **Access : R/W** |
| | DDE | 7 | Direct DE mode for CCIR input.<br>0: Disable direct DE.<br>1: Enable direct DE. | |
| | DEGR[2:0] | 6:4 | DE or HSYNC post Glitch removal Range. | |
| | HSFL | 3 | Input HSYNC Filter.<br>0: Filter off.<br>1: Filter on. | |

| Scaler Register (Bank=00, Registers 01h ~ 9Fh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| | ISSM | 2 | Input Sync Sample Mode.<br>0: Normal.<br>1: Glitch-removal. | |
| | MVD_SEL | 1:0 | MVD mode Select<br>0: CVBS.<br>1: S-Video.<br>2: YCbCr.<br>3: RGB. | |
| **05h** | **SPRVST_L** | **7:0** | **Default : 0x10** | **Access : R/W, DB** |
| | SPRVST[7:0] | 7:0 | Image vertical sample start point, count by input HSYNC (lower 8 bits). | |
| **06h** | **SPRVST_H** | **7:0** | **Default : 0x00** | **Access : R/W, DB** |
| | - | 7:3 | Reserved. | |
| | SPRVST[10:8] | 2:0 | Image vertical sample start point, count by input HSYNC (higher 3 bits). | |
| **07h** | **SPRHST_L** | **7:0** | **Default : 0x01** | **Access : R/W, DB** |
| | SPRHST[7:0] | 7:0 | Image horizontal sample start point, count by input dot clock (higher 8 bits). | |
| **08h** | **SPRHST_H** | **7:0** | **Default : 0x00** | **Access : R/W, DB** |
| | - | 7:3 | Reserved. | |
| | SPRGST[10:8] | 2:0 | Image horizontal sample start point, count by input dot clock (lower 3 bits). | |
| **09h** | **SPRVDC_L** | **7:0** | **Default : 0x10** | **Access : R/W, DB** |
| | SPRVDC[7:0] | 7:0 | Image vertical resolution (vertical display enable area count by line; lower 8 bits). | |
| **0Ah** | **SPRVDC_H** | **7:0** | **Default: 0x00** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | SPRVDC[10:8] | 2:0 | Image vertical resolution (vertical display enable area count by line; higher 3 bits). | |
| **0Bh** | **SPRHDC_L** | **7:0** | **Default : 0x10** | **Access : R/W** |
| | SPRHDC[7:0] | 7:0 | Image horizontal resolution (horizontal display enable area count by pixel; lower 8 bits). | |
| **0Ch** | **SPRHDC_L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | SPRHDC[10:8] | 2:0 | Image horizontal resolution (horizontal display enable area count by pixel; higher 3 bits). | |

## Scaler Register (Bank=00, Registers 01h ~ 9Fh)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| **0Dh** | **LYL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | LYL[3:0] | 3:0 | Lock Y Line. | |
| **0Eh** | **INTLX** | **7:0** | **Default : 0x00** | **Access : -** |
| | ITU_EXT_FIELD | 7 | Using External FIELD for ITU interface.<br>0: Using EAV/SAV.<br>1: Using external FIELD. | |
| | ITU_EXT_HS | 6 | Using External HSYNC for ITU interface.<br>0: Using EAV/SAV.<br>1: Using external HSYNC. | |
| | ITU_EXT_VS | 5 | Using External VSYNC for ITU interface.<br>0: Using EAV/SAV.<br>1: Using external VSYNC. | |
| | VDOE | 4 | Video reference Edge (for non-standard signal). | |
| | INTLAC_LOCKAVG | 3 | Averaging Locking timing. | |
| | LHC_MD | 2 | Long Horizontal Counter Mode.<br>1: On.<br>0: Off. | |
| | - | 1:0 | Reserved. | |
| **0Fh** | **ASCTRL** | **7:0** | **Default : 0x90** | **Access : R/W** |
| | IVB (RO) | 7 | Input VSYNC Blanking status.<br>0: In display.<br>1: In blanking. | |
| | DLINE[2:0] | 6:4 | Line buffer read delay in number of lines. | |
| | INTLAC_MANSTD | 3 | NTSC/PAL Manual Mode | |
| | INTLAC_SETSTD | 2 | NTSC/PAL Setting in manual mode under run status.<br>0: NTSC.<br>1: PAL. | |
| | UNDER (RO) | 1 | Under run status. | |
| | OVER (RO) | 0 | Over run status. | |
| **10h** | **COCTRL1** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | AVI_SEL | 5 | Analog Video Input Select.<br>0: PC.<br>1: Component analog video. | |

| Scaler Register (Bank=00, Registers 01h ~ 9Fh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| | DLYV | 4 | Analog Delay line for component analog Video input.<br>0: Delay 1 line.<br>1: Do not delay. | |
| | CSC_MD | 3 | Composite SYNC Cut Mode.<br>0: Disable.<br>1: Enable. | |
| | EXVS | 2 | External VSYNC polarity (only used when COVS is 1).<br>0: Normal.<br>1: Invert. | |
| | COV_SEL | 1 | Coast VSYNC Select.<br>0: Internal VSEP.<br>1: External VSYNC. | |
| | CADC | 0 | Coast to ADC.<br>0: Disable.<br>1: Enable. | |
| **11h** | **COCTRL2** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | COST[7:0] | 7:0 | Front tuning.<br>00: Coast start from 1 HSYNC leading edge.<br>01: Coast start from 2 HSYNC leading edge, default value.<br>…<br>254: Coast start from 255 HSYNC leading edge.<br>255: Coast start from 256 HSYNC leading edge. | |
| **12h** | **COCTRL3** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | COEND[7:0] | 7:0 | End tuning.<br>00: Coast end at 1 HSYNC leading edge.<br>01: Coast end at 2 HSYNC leading edge, default value.<br>…<br>254: Coast end at 255 HSYNC leading edge.<br>255: Coast end at 256 HSYNC leading edge. | |
| **13h** | **VFAC_OINI** | **7:0** | **Default: 0x00** | **Access : R/W** |
| | VFACOINI[7:0] | 7:0 | Vertical Factor Odd Initial value. | |
| **14h** | **VFAC_EINI** | **7:0** | **Default: 0x80** | **Access : R/W** |
| | VFACEINI[7:0] | 7:0 | Vertical Factor Even Initial value | |
| **15h** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **16h** | **INTCTROL** | **7:0** | **Default : 0x00** | **Access : R/W** |

| Scaler Register (Bank=00, Registers 01h ~ 9Fh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| | CHG_HMD | 7 | Change H Mode for INT.<br>0: Only in leading/tailing of CHG period.<br>1: Every line generating INT pulse during CHG period. | |
| | - | 6:4 | Reserved. | |
| | IVSI | 3 | Input VSYNC interrupt generated by:<br>0: Leading edge.<br>1: Tailing edge. | |
| | OVSI | 2 | Output VSYNC interrupt generated by:<br>0: Leading edge.<br>1: Tailing edge. | |
| | TRGC | 1 | Trigger Condition.<br>0: Active low for level trigger/tailing edge trigger.<br>1: Active high for level trigger/leading edge trigger. | |
| | INT_TRIG | 0 | Interrupt Trigger.<br>0: Generate an edge trigger interrupt.<br>1: Generate a level trigger interrupt. | |
| **17h** | **INTPULSE** | **7:0** | **Default : 0x0F** | **Access : R/W** |
| | INTPULSE[7:0] | 7:0 | Interrupt Pulse width by reference clock. | |
| **18h** | **INTSTA** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | INTSTA[7:0] | 7:0 | Interrupt Status byte A.<br>Bit 7: MVD input NOT "no signal".<br>Bit 6: MVD "HSYNC lock".<br>Bit 5: MVD NOT "no color".<br>Bit 4: MVD degree error.<br>Bit 3: MVD input "no signal".<br>Bit 2: MVD NOT "HSYNC lock".<br>Bit 1: MVD "no color".<br>Bit 0: MVD HSYNC change. | |
| **19h** | **INTENA** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | INTENA[7:0] | 7:0 | Interrupt Enable control byte A.<br>0: Disable interrupt.<br>1: Enable interrupt. | |
| **1Ah** | **INTSTB** | **7:0** | **Default : 0x00** | **Access : R/W** |

| Scaler Register (Bank=00, Registers 01h ~ 9Fh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| | INTSTB[7:0] | 7:0 | Interrupt Status byte B.<br>Bit 7: MCU D2B interrupt 2.<br>Bit 6: MCU D2B interrupt 1.<br>Bit 5: MCU D2B interrupt 0.<br>Bit 4: MVD CC interrupt.<br>Bit 3: MVD SECAM detect.<br>Bit 2: MVD PAL switch error.<br>Bit 1: MVD "ADC7_0ACT".<br>Bit 0: MVD NOT "ADC7_0ACT". | |
| **1Bh** | **INTENB** | **7:0** | **Default : 0x00** | **Access : R/C** |
| | INTENB[7:0] | 7:0 | Interrupt Enable control byte B.<br>0: Disable interrupt.<br>1: Enable interrupt. | |
| **1Ch** | **INTSTC** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | INTSTC[7:0] | 7:0 | Interrupt Status byte C.<br>Bit 7: Output VSYNC interrupt.<br>Bit 6: Input VSYNC interrupt.<br>Bit 5: ATG ready interrupt.<br>Bit 4: ATP ready interrupt.<br>Bit 3: ATS ready interrupt.<br>Bit 2: MVD probe ready interrupt.<br>Bit 1: MCU D2B interrupt 4.<br>Bit 0: MCU D2B interrupt 3. | |
| **1Dh** | **INTENC** | **7:0** | **Default : 0x00** | **Access : R/C** |
| | INTENC[7:0] | 7:0 | Interrupt Enable control byte C.<br>0: Disable interrupt.<br>1: Enable interrupt. | |
| **1Eh** | **INTSTD** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | INTSTD[7:0] | 7:0 | Interrupt Status byte D.<br>Bit 7: WDT interrupt.<br>Bit 6: Keypad wake-up interrupt.<br>Bit 5: Jitter interrupt.<br>Bit 4: Horizontal total change interrupt.<br>Bit 3: Vertical total change interrupt.<br>Bit 2: Horizontal lost count interrupt.<br>Bit 1: Vertical lost count interrupt.<br>Bit 0: Standard change interrupt. | |
| **1Fh** | **INTEND** | **7:0** | **Default : 0x00** | **Access : R/C** |

| Scaler Register (Bank=00, Registers 01h ~ 9Fh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| | INTEND[7:0] | 7:0 | Interrupt Enable control byte D.<br>0: Disable interrupt.<br>1: Enable interrupt. | |
| **20h ~ 21h** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **22h** | **MPL_M** | **7:0** | **Default : 0x6F** | **Access : R/W** |
| | MP_ICTRL[2:0] | 7:5 | Charge pump current set. | |
| | MPL_M[4:0] | 4:0 | MPLL divider ratio setting. | |
| **23h** | **OPL_CTL0** | **7:0** | **Default : 0x40** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | SSC_EN | 6 | Output PLL spread spectrum.<br>0: Disable.<br>1: Enable. | |
| | SD_MD | 5 | Output PLL spread spectrum Mode.<br>0: Normal.<br>1: Reverse for mode 1. | |
| | - | 4:0 | Reserved. | |
| **24h** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **25h** | **OPL_SET0** | **7:0** | **Default : 0x44** | **Access : R/W, DB** |
| | OPL_SET[7:0] | 7:0 | Output PLL Set. | |
| **26h** | **OPL_SET1** | **7:0** | **Default : 0x55** | **Access : R/W, DB** |
| | OPL_SET[15:8] | 7:0 | See description for OPL_SET [7:0]. | |
| **27h** | **OPL_SET2** | **7:0** | **Default : 0x24** | **Access : R/W, DB** |
| | OPL_SET [23:16] | 7:0 | See description for OPL_SET [7:0]. | |
| **28h** | **OPL_STEP0** | **7:0** | **Default : 0x20** | **Access : R/W, DB** |
| | OPL_STEP[7:0] | 7:0 | Output PLL spread spectrum Step. | |
| **29h** | **OPL_STEP1** | **7:0** | **Default : 0x00** | **Access : R/W, DB** |
| | - | 7 | Reserved. | |
| | - | 6 | Reserved. | |
| | - | 5 | Reserved. | |
| | - | 4:3 | Reserved. | |
| | OPL_STEP[10:8] | 2:0 | See description for OPL_STEP[7:0]. | |
| **2Ah** | **OPL_SPAN** | **7:0** | **Default : 0x00** | **Access : R/W, DB** |
| | OPL_SPAN[7:0] | 7:0 | Output PLL spread spectrum Span. | |

| Scaler Register (Bank=00, Registers 01h ~ 9Fh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| **2Bh** | **OPL_SPAN** | **7:0** | **Default : 0x00** | **Access : R/W, DB** |
| | READ_FRAME | 7 | 0: OPL_SET stores line-based value.<br>1: OPL_SET stores frame-based value. | |
| | OPL_SPAN[14:8] | 6:0 | See description for OPL_SPAN[7:0]. | |
| **2Ch ~ 2Fh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **30h** | **HSR_L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | HSR [7:0] | 7:0 | Horizontal Scaling ratio (20 bits fraction) for scaling down 1/2^20 to (2^20-1)/2^20 (lower 8 bits). | |
| **31h** | **HSR_M** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | HSR[15:8] | 7:0 | Horizontal Scaling ratio (20 bits fraction) for scaling down 1/2^20 to (2^20-1)/2^20 (middle 8 bits). | |
| **32h** | **HSR_H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | HS_EN | 7 | Horizontal Scaling Enable.<br>0: Disable.<br>1: Enable. | |
| | CBILINEAR_EN | 6 | Complemental Bi-Linear Enable. | |
| | FORCEBICOLOR | 5 | 0: Chrominance using same setting as Luminance defined by CBILINEAR.<br>1: Chrominance always using bi-linear algorithm. | |
| | - | 4 | Reserved. | |
| | HSR[19:16] | 3:0 | Horizontal Scaling Ratio (20 bits fraction) for scaling down 1/2^20 to (2^20-1)/2^20 (higher 8 bits). | |
| **33h** | **VSR_L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | VSR[7:0] | 7:0 | Vertical Scaling ratio (2 bits integer, 20 bits fraction) for scaling down to 1/2.9999 (lower 8 bits).<br>xx.xxxxxxxxxxxxxxxxxxx | |
| **34h** | **VSR_M** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | VSR[15:8] | 7:0 | Vertical Scaling ratio (2 bits integer, 20 bits fraction) for scaling down to 1/2.9999 (middle 8 bits).<br>xx.xxxxxxxxxxxxxxxxxxx | |
| **35h** | **VSR_H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | VS_EN | 7 | Vertical Scaling Enable.<br>0: Disable.<br>1: Enable. | |

| Scaler Register (Bank=00, Registers 01h ~ 9Fh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| | VSM_SEL | 6 | Vertical Scaling Method Select.<br>0: Original.<br>1: New. | |
| | VSR[21:16] | 5:0 | Vertical Scaling ratio (2 bits integer, 20 bits fraction) for scaling down to 1/2.9999 (higher 8 bits).<br>xx.xxxxxxxxxxxxxxxxxxx | |
| **36h** | **VDSUSG** | **7:0** | **Default: 0x00** | **Access : R/W** |
| | LBF_INCLK | 7 | Line-Buffer using Input Clock. | |
| | LBF_OUTCLK | 6 | Line-Buffer using Output Clock. | |
| | LBF_LIVE | 5 | Line-Buffer always Live. | |
| | OUTCLK_DIV3 | 4 | Output Clock is 1/3 frequency of OPLL output. | |
| | EN_OFST | 3 | Enable Offset for even/odd scaling. | |
| | OFST_INV | 2 | Offset Inverting for even/odd scaling. | |
| | LBFCLK_DIV2 | 1 | Line-Buffer Clock frequency is divided by 2. | |
| | VSD_DITH_EN | 0 | VSD Dither Enable. | |
| **37h** | **DIRSCAL_CTL** | **7:0** | **Default: 0x00** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | GOAL2_SEL | 2 | Goal2 Select. | |
| | DITH_ON | 1 | Dithering control.<br>0: Off.<br>1: On. | |
| | DIRSCAL_EN | 0 | Function Enable. | |
| **38h** | **NLDTI** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | NL_EN | 7 | Non-Linear scaling Enable. | |
| | NLSIO[6:0] | 6:0 | Non-Linear Scaling section Initial Offset. | |
| **39h** | **NLDT0** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | NLIOS | 7 | Non-Linear scaling section Initial Offset Sign.<br>0: Positive value.<br>1: Negative value. | |
| | NLDT0[6:0] | 6:0 | Non-Linear Scaling Delta for Section 0, bit 7 is sign bit. | |
| **3Ah** | **NLDT1** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7 | Reserved | |
| | NLDT1[6:0] | 6:0 | Non-Linear scaling Delta for Section 1, bit 7 is sign bit. | |
| **3Bh** | **NLDC0** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | NLDC0[7:0] | 7:0 | Non-Linear scaling section 0 Dot Count/2. | |

| Scaler Register (Bank=00, Registers 01h ~ 9Fh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| **3Ch** | **NLDC1** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | NLDC1[7:0] | 7:0 | Non-Linear scaling section 1 Dot Count/2. | |
| **3Dh** | **NLDC2** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | NLDC2[7:0] | 7:0 | Non-Linear scaling section 2 Dot Count/2. | |
| **3Eh** | **DIRSCAL_TH1** | **7:0** | **Default: 0x80** | **Access : R/W** |
| | DETTH[7:0] | 7:0 | Threshold of maximum value for detection | |
| **3Fh** | **DIRSCAL_TH2** | **7:0** | **Default: 0x80** | **Access : R/W** |
| | PCTTH[7:0] | 7:0 | Threshold of maximum value for protection | |
| **40h** | **VFDEST_L** | **7:0** | **Default : 0x01** | **Access : R/W** |
| | VFDEST[7:0] | 7:0 | Output frame DE Vertical Start (lower 8 bits). | |
| **41h** | **DEVST_H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | VFDEST[10:8] | 2:0 | Output frame DE Vertical Start (higher 3 bits). | |
| **42h** | **HFDEST_L** | **7:0** | **Default : 0x03** | **Access : R/W** |
| | HFDEST[7:0] | 7:0 | Output frame DE Horizontal Start (lower 8 bits). | |
| **43h** | **HFDEST_H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | HFDEST[10:8] | 2:0 | Output frame DE Horizontal Start (higher 3 bits). | |
| **44h** | **VFDEEND_L** | **7:0** | **Default : 0xEA** | **Access : R/W** |
| | VFDEEND[7:0] | 7:0 | Output frame DE Vertical END (lower 8 bits). | |
| **45h** | **VFDEEND_H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | DEVEND[10:8] | 2:0 | Output frame DE Vertical END (higher 3 bits). | |
| **46h** | **HFDEEND_L** | **7:0** | **Default : 0xE0** | **Access : R/W** |
| | HFDEEND[7:0] | 7:0 | Output frame DE Horizontal END (lower 8 bits). | |
| **47h** | **HFDEEND_H** | **7:0** | **Default : 0x01** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | HFDEEND[10:8] | 2:0 | Output frame DE Horizontal END (higher 3 bits). | |
| **48h** | **SIHST_L** | **7:0** | **Default : 0x01** | **Access : R/W** |
| | SIHST[7:0] | 7:0 | Scaling Image window Horizontal Start (lower 8 bits). | |
| **49h** | **SIHST_H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | SIHST[10:8] | 2:0 | Scaling Image window Horizontal Start (higher 3 bits). | |

## Scaler Register (Bank=00, Registers 01h ~ 9Fh)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| **4Ah** | **SIVEND_L** | **7:0** | **Default : 0xEA** | **Access : R/W** |
| | SIVEND[7:0] | 7:0 | Scaling Image window Vertical END (lower 8 bits). | |
| **4Bh** | **SIVEND_H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | SIVEND[10:8] | 2:0 | Scaling Image window Vertical END (higher 3 bits). | |
| **4Ch** | **SIHEND_L** | **7:0** | **Default : 0xEA** | **Access : R/W** |
| | SIHEND[7:0] | 7:0 | Scaling Image window Horizontal END (lower 8 bits). | |
| **4Dh** | **SIHEND_H** | **7:0** | **Default : 0x01** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | SIHEND[10:8] | 2:0 | Scaling Image window Horizontal END (higher 3 bits). | |
| **4Eh** | **VDTOT_L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | VDTOT[7:0] | 7:0 | Output Vertical Total (lower 8 bits). | |
| **4Fh** | **VDTOT_H** | **7:0** | **Default : 0x02** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | VDTOT[10:8] | 2:0 | Output Vertical Total (higher 3 bits). | |
| **50h** | **VSST_L** | **7:0** | **Default : 0xEA** | **Access : R/W** |
| | VSST[7:0] | 7:0 | Output VSYNC start (lower 8 bits). | |
| **51h** | **VSST_H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | VSRU | 3 | VSYNC Register Usage.<br>0: Registers 20h – 23h are used to define output VSYNC.<br>1: Registers 20h and 21h are used to define No signal VSYNC. Registers 22h and 23h are used to define minimum H total. | |
| | VSST[10:8] | 2:0 | Output VSYNC start (higher 3 bits). | |
| **52h** | **VSEND_L** | **7:0** | **Default : 0x06** | **Access : R/W** |
| | VSEND[7:0] | 7:0 | Output VSYNC END (lower 8 bits). | |
| **53h** | **VSEND_H** | **7:0** | **Default : 0x00** | **Access : R/W DB** |
| | - | 7:3 | Reserved. | |
| | VSEND[10:8] | 2:0 | Output VSYNC END (higher 3 bits). | |
| **54h** | **HDTOT_L** | **7:0** | **Default : 0x3C** | **Access : R/W DB** |
| | HDTOT[7:0] | 7:0 | Output Horizontal Total (lower 8 bits). | |
| **55h** | **HDTOT_H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | HDTOT[10:8] | 2:0 | Output Horizontal Total (higher 3 bits). | |

## Scaler Register (Bank=00, Registers 01h ~ 9Fh)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| **56h** | **HSEND** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | HSEND[7:0] | 7:0 | Output HSYNC END (lower 8 bits). | |
| **57h** | **OSCTRL1** | **7:0** | **Default : 0x4C** | **Access : R/W** |
| | AOVS | 7 | Auto Output VSYNC.<br>0: OVSYNC is defined automatically.<br>1: OVSYNC is defined manually (register 0x50 – 0x53). | |
| | LCM | 6 | Frame Lock Mode.<br>0: Mode 0.<br>1: Mode 1. | |
| | HRSM | 5 | HSYNC Remove Mode.<br>0: Normal.<br>1: Remove HSYNC. | |
| | - | 4:3 | Reserved. | |
| | Scal_1 | 2 | Scaling range add 1. | |
| | AHRT | 1 | Auto H total and Read start Tuning enable.<br>0: Disable.<br>1: Enable. | |
| | CTRL | 0 | ATCTRL function enable.<br>0: Disable.<br>1: Enable. | |
| **58h** | **BRIGHTNESS_EN** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:1 | Reserved. | |
| | BRI_EN | 0 | Brightness function Enable.<br>0: Disable.<br>1: Enable. | |
| **59h** | **BRI_R** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | BRI_R[7:0] | 7:0 | Brightness coefficient–Red color. | |
| **5Ah** | **BRI_G** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | BRI_G[7:0] | 7:0 | Brightness coefficient–Green color. | |
| **5Bh** | **BRI_B** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | BRI_B[7:0] | 7:0 | Brightness coefficient–Blue color. | |
| **5Ch** | **FRAME_COLOR_1** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | FCG[4:3] | 7:6 | Frame Color G[4:3]. | |
| | FCB[7:3] | 5:1 | Frame Color B[7:3]. | |

| Scaler Register (Bank=00, Registers 01h ~ 9Fh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| | FC_EN | 0 | Frame Color Enable.<br>0: Diable.<br>1: Enable. | |
| **5Dh** | **FRAME_COLOR_2** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | FCR[7:3] | 7:3 | Frame Color R[7:3]. | |
| | FCG[7:5] | 2:0 | Frame Color G[7:5]. | |
| **5Eh** | **PATTERN** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | EXT_OSD | 7 | EXT OSD pin as GPIO. | |
| | EXT_VD | 6 | EXT VD pin as GPIO. | |
| | - | 5:3 | Reserved. | |
| | PTNWT | 2 | Pattern White. | |
| | PTNBLK | 1 | Pattern Black. | |
| | PTNRVS | 0 | Pattern Reverse. | |
| **5Fh** | **EXT_OSD_CTRL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | EXTOSD_EN | 7 | External OSD function Enable.<br>0: Diable.<br>1: Enable. | |
| | DATEXTMD[1:0] | 6:5 | Data Extend Mode. | |
| | CKEY_EN | 4 | Color Key Enable.<br>0: Disable.<br>1: Enable. | |
| | INVCKEY_EN | 3 | Inverse Color Key Enable.<br>0: Diable.<br>1: Enable. | |
| | R_KEY | 2 | R color Key selected. | |
| | G_KEY | 1 | G color Key selected. | |
| | B_KEY | 0 | B color Key selected. | |
| **60h** | **DITHCTRL** | **7:0** | **Default : 0x02** | **Access : R/W** |
| | DITHG[1:0] | 7:6 | Dither coefficient for G channel. | |
| | DITHB[1:0] | 5:4 | Dither coefficient for B channel. | |
| | SROT | 3 | Spatial coefficient Rotate.<br>0: Disable.<br>1: Enable. | |
| | TROT | 2 | Temporal coefficient Rotate.<br>0: Disable.<br>1: Enable. | |

| Scaler Register (Bank=00, Registers 01h ~ 9Fh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| | OBN | 1 | Output Bits Number<br>0: 8-bit output.<br>1: 6-bit output (power on default value). | |
| | DITH | 0 | Dither function.<br>0: Off.<br>1: On. | |
| **61h** | **DITHCOEF** | **7:0** | **Default : 0x2D** | **Access : R/W** |
| | TL[1:0] | 7:6 | Top-Left dither coefficient. | |
| | TR[1:0] | 5:4 | Top-Right dither coefficient. | |
| | BL[1:0] | 3:2 | Bottom-Left dither coefficient. | |
| | BR[1:0] | 1:0 | Bottom-Right dither coefficient. | |
| **62h** | **DITHCTL1** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | PSRD | 7 | Pseudo Random, resets every 4 frames.<br>0: Enable.<br>1: Disable. | |
| | ND_MD | 6 | Noise Dithering Method. | |
| | AUTO_DTH | 5 | Auto Dither. | |
| | PSDO_EN | 4 | Pseudo Enable.<br>0: Disable.<br>1: Enable. | |
| | DTH_MNUS | 3 | Dither Minus. | |
| | ABM[2:0] | 2:0 | Alpha Blending Mode.<br>000: No alpha blending.<br>001: Background alpha blending.<br>010: Foreground alpha blending.<br>011: Color key alpha blending.<br>100: Not color key alpha blending.<br>101: Entire OSD alpha blending.<br>11x: Reserved. | |
| **63h** | **OSD_CTL** | **7:0** | **Default : 0x00** | **Access : R/W** |

| Scaler Register (Bank=00, Registers 01h ~ 9Fh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| | CKIND[3:0] | 7:4 | Color Index of Color Key.<br>0000: Color index 0.<br>0001: Color index 1.<br>… …<br>1111: Color index 15.<br>When OSD register 0x10[7]=1, OSD is not backward compatible.<br>When OSD register 0x10[7]=0, OSD is backward compatible.<br>When 8-color palette is selected, only CKIND[2:0] are used.<br>When 16-color palette is selected, OSD0xE0 bit[6] is color key bit[3] instead of using CKIND[3]. | |
| | NEW_BLND_MTHD | 3 | New Blending Level.<br>0: Original blending level (BLENDL=000 means 0% transparency).<br>1: New blending level (BLENDL=000 means 12.5% transparency). | |
| | OSD_BLND_MD | 2:0 | OSD alpha blending Level.<br>000: 12.5% transparency.<br>001: 25.0% transparency.<br>010: 37.5% transparency.<br>011: 50.0%% transparency.<br>100: 62.5% transparency.<br>101: 75.0% transparency.<br>110: 87.5% transparency.<br>111: 100% transparency. | |
| **64h** | **CM11_L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CM11[7:0] | 7:0 | Color Matrix Coefficient 11 (lower 8 bits). | |
| **65h** | **CM11_H** | **7:0** | **Default : 0x04** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | CM11[12:8] | 4:0 | Color Matrix Coefficient 11 (higher 5 bits). | |
| **66h** | **CM12_L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CM12[7:0] | 7:0 | Color Matrix Coefficient 12 (lower 8 bits). | |
| **67h** | **CM12_H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | CM12[12:8] | 4:0 | Color Matrix Coefficient 12 (higher 5 bits). | |
| **68h** | **CM13_L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CM13[7:0] | 7:0 | Color Matrix Coefficient 13 (lower 8 bits). | |
| **69h** | **CM13_H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | CM13[12:8] | 4:0 | Color Matrix Coefficient 13 (higher 5 bits). | |

| Scaler Register (Bank=00, Registers 01h ~ 9Fh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| **6Ah** | **CM21_L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CM21[7:0] | 7:0 | Color Matrix Coefficient 21 (lower 8 bits). | |
| **6Bh** | **CM21_H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | CM21[12:8] | 4:0 | Color Matrix Coefficient 21 (higher 5 bits). | |
| **6Ch** | **CM22_L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CM22[7:0] | 7:0 | Color Matrix Coefficient 22 (lower 8 bits). | |
| **6Dh** | **CM22_H** | **7:0** | **Default : 0x04** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | CM22[12:8] | 4:0 | Color Matrix Coefficient 22 (higher 5 bits). | |
| **6Eh** | **CM23_L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CM23[7:0] | 7:0 | Color Matrix Coefficient 23 (lower 8 bits). | |
| **6Fh** | **CM23_H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | CM23[12:8] | 4:0 | Color Matrix Coefficient 23 (higher 5 bits). | |
| **70h** | **CM31_L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CM31[7:0] | 7:0 | Color Matrix Coefficient 31 (lower 8 bits). | |
| **71h** | **CM31_H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | CM31[12:8] | 4:0 | Color Matrix Coefficient 31 (higher 5 bits). | |
| **72h** | **CM32_L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CM32[7:0] | 7:0 | Color Matrix Coefficient 32 (lower 8 bits). | |
| **73h** | **CM32_H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | CM32[12:8] | 4:0 | Color Matrix Coefficient 32 (higher 5 bits). | |
| **74h** | **CM33_L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CM33[7:0] | 7:0 | Color Matrix Coefficient 33 (lower 8 bits). | |
| **75h** | **CM33_H** | **7:0** | **Default : 0x04** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | CM33[12:8] | 4:0 | Color Matrix Coefficient 33 (higher 5 bits). | |
| **76h** | **COL_MATRIX_CTL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:6 | Reserved. | |

| Scaler Register (Bank=00, Registers 01h ~ 9Fh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| | CMRND | 5 | Color Matrix Rounding control.<br>0: Disable.<br>1: Enable. | |
| | CMC | 4 | Color Matrix Control.<br>0: Disable.<br>1: Enable. | |
| | - | 3 | Reserved. | |
| | RRAN | 2 | Red Range.<br>0: 0~255.<br>1: 128~127. | |
| | GRAN | 1 | Green Range.<br>0: 0~255.<br>1: 128~127. | |
| | BRAN | 0 | Blue Range.<br>0: 0~255.<br>1: 128~127. | |
| **77h** | **FBL_CTL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:5 | Reserved | |
| | ODDF | 3 | Shift Odd Field.<br>0: Shift even field.<br>1: Shift odd field. | |
| | SLN[2:0] | 2:0 | Shift Line Number.<br>000: Shift 0 line between odd and even fields.<br>001: Shift 1 line between odd and even fields.<br>010: Shift 2 line between odd and even fields.<br>011: Shift 3 line between odd and even fields.<br>1xx: Shift 4 line between odd and even fields. | |
| **78h** | **LCK_VCNT_L** | **7:0** | **Default : -** | **Access : RO** |
| | LCK_VCNT[7:0] | 7:0 | Lock V total low byte [7:0]. | |
| **79h** | **LCK_VCNT_H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | SWCH_STS | 7 | Switch Status. | |
| | - | 6:3 | Reserved. | |
| | LCK_VCNT[10:8] | 2:0 | Lock V total high byte [10:8]. | |
| **7Ah** | **CAP_VCNT_L** | **7:0** | **Default : -** | **Access : RO** |
| | CAP_VCNT[7:0] | 7:0 | Cap V total low byte [7:0]. | |
| **7Bh** | **CAP_VCNT_H** | **7:0** | **Default : -** | **Access : RO** |

| Scaler Register (Bank=00, Registers 01h ~ 9Fh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| | - | 7:3 | Reserved. | |
| | CAP_VCNT[10:8] | 2:0 | Cap V total high byte [10:8]. | |
| **7Ch** | **CAP_HCNT_L** | **7:0** | **Default : -** | **Access : RO** |
| | CAP_HCNT[7:0] | 7:0 | Cap H total low byte [7:0]. | |
| **7Dh** | **CAP_HCNT_H** | **7:0** | **Default : -** | **Access : RO** |
| | - | 7:3 | Reserved. | |
| | CAP_HCNT[10:8] | 2:0 | Cap H total high byte [10:8]. | |
| **7Eh** | **EST_VCNT_L** | **7:0** | **Default : -** | **Access : RO** |
| | EST_VCNT[7:0] | 7:0 | Est V total low byte [7:0]. | |
| **7Fh** | **EST_VCNT_H** | **7:0** | **Default : -** | **Access : RO** |
| | - | 7:3 | Reserved. | |
| | EST_VCNT[10:8] | 2:0 | Est V total high byte [10:8]. | |
| **80h** | **EST_HCNT_L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | EST_HCNT[7:0] | 7:0 | Est H total low byte [7:0]. | |
| **81h** | **EST_HCNT_H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | EST_HCNT[10:8] | 2:0 | Est H total low byte [10:8]. | |
| **82h** | **SSC_TLRN** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | SSC_TLRN[7:0] | 7:0 | SSC Tolerance. | |
| **83h** | **Delta_L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | DELTA[7:0] | 2:0 | Delta[7:0]. | |
| **84h** | **Delta_H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | DELTA[12:8] | 4:0 | Delta[12:8]. | |
| **85h** | **SSC_SHIFT** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | SSC_SHIFT[7:0] | 7:0 | SSC Shift. | |
| **86h** | **FNTN_TST** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | MSK_SHRT_LN_CLK | 5 | Mask the Clock when in Short Line. | |
| | - | 4 | Reserved. | |
| | SYNC_GATE_MD | 3 | Mask HYSNC and Clock Mode. | |
| | RB_SWAP | 2 | Output channel RB Swap. | |
| | LM_SWAP_6 | 1 | Output Channel MSB LSB Swap in 6-bit bus mode. | |

| Scaler Register (Bank=00, Registers 01h ~ 9Fh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| | LM_SWAP_8 | 0 | Output Channel MSB LSB Swap in 8-bit bus mode. | |
| **87h** | **DEBUG** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | EOCK | 6 | Select External ODCLK. | |
| | - | 5:4 | Reserved. | |
| | PTEN | 3 | PLL Test register protect bit Enable.<br>0: Disable.<br>1: Enable. | |
| | - | 2:0 | Reserved. | |
| **88h** | **SL_CNTRL_1** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | LIM_HS | 5 | Limit HSYNC period enable. | |
| | - | 4:3 | Reserved. | |
| | INT_CAP_EN | 2 | Interlace Capture Enable. | |
| | SHLN_FLD | 1 | Select Short Line Field. | |
| | FRZ_SHLN | 0 | Stop Short Line Update. | |
| **89h** | **SL_TUNE _1** | **7:0** | **Default : 0x70** | **Access : R/W** |
| | TNCOEF | 7:5 | Tune Coefficient. | |
| | LCK_THRHD | 4:0 | Lock Threshold. | |
| **8Ah** | **SL_TUNE_2** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | LMT_D5D6D7_H | 7:0 | Limit PLL_SET High byte. | |
| **8Bh** | **SL_TUNE_3** | **7:0** | **Default : 0xC0** | **Access : R/W** |
| | LMT_D5D6D7_L | 7:0 | Limit PLL_SET Low byte. | |
| **8Ch** | **TARGET_SL_L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | TARGET_SL_L | 7:0 | Target Short Line Low byte. | |
| **8Dh** | **TARGET_SL_H** | **7:0** | **Default : 0x01** | **Access : R/W** |
| | TARGET_SL_H | 7:0 | Target Short Line High byte. | |
| **8Eh ~ 8Fh** | **-** | **7:0** | **Default : -** | **Access : RO** |
| | **-** | | Reserved. | |
| **90h** | **GAMMA_EN** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:2 | Reserved. | |
| | ADR_INC_EN | 1 | Address Increase Enable.<br>0: Disable.<br>1: Enable. | |

| Scaler Register (Bank=00, Registers 01h ~ 9Fh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| | GAMMA_EN | 0 | Gamma Enable.<br>0: Disable.<br>1: Enable. | |
| **91h** | **GAMMA_ADR_PORT** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | GMA_ADR_PORT[7:0] | 7:0 | Gamma Address Port [7:0]. | |
| **92h** | **GAMMA_DAT_PORT** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | GMA_DAT_PORT[7:0] | 7:0 | Gamma Data Port [7:0]. | |
| **93h** | **R_BIAS** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | R_BIAS[7:0] | 7:0 | DC level in R channel positive part. | |
| **94h** | **R_RATIO** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | R_RATIO[7:0] | 7:0 | Ratio in R channel positive part. | |
| **95h** | **G_BIAS** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | G_BIAS[7:0] | 7:0 | DC level in G channel positive part. | |
| **96h** | **G_RATIO** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | G_RATIO[7:0] | 7:0 | Ratio in G channel positive part. | |
| **97h** | **B_BIAS** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | B_BIAS[7:0] | 7:0 | DC level in B channel positive part. | |
| **98h** | **B_RATIO** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | B_RATIO[7:0] | 7:0 | Ratio in B channel positive part. | |
| **99h** | **R_BIASN** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | R_BIASN[7:0] | 7:0 | Dc level in R channel negative part. | |
| **9Ah** | **R_RATION** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | R_RATION[7:0] | 7:0 | Ratio in R channel negative part. | |
| **9Bh** | **G_BIASN** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | G_BIASN[7:0] | 7:0 | DC level in G channel negative part. | |
| **9Ch** | **G_RATION** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | G_RATION[7:0] | 7:0 | Ratio in G channel negative part. | |
| **9Dh** | **B_BIASN** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | B_BIASN[7:0] | 7:0 | DC level in B channel negative part. | |
| **9Eh** | **B_RATION** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | B_RATION[7:0] | 7:0 | Ratio in B channel negative part. | |
| **9Fh** | **-** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:0 | Reserved. | |

## OSD Register (Bank = 00, Registers A0h ~ AAh)

| OSD Register (Bank=00) | | | | |
|---|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** | |
| **A0h** | **OSDIOA** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | TOSB_MD | 7 | OSD SRAM I/O Access Burst Mode.<br>0: Disable.<br>1: Enable. | |
| | CLR | 6 | OSD Clear Bit (write only).<br>0: Normal.<br>1: Clear code with 00h, attribute with 00h. | |
| | - | 5 | Reserved. | |
| | RF | 4 | OSD RAM Font I/O Access.<br>0: Disable.<br>1: Enable. | |
| | DC | 3 | OSD Display Code I/O Access.<br>0: Disable.<br>1: Enable. | |
| | DA | 2 | OSD Display Attribute I/O Access.<br>0: Disable.<br>1: Enable. | |
| | ORBW_MD | 1 | OSD Register Burst Write Mode.<br>0: Disable.<br>1: Enable. | |
| | ORBR_MD | 0 | OSD Register Burst Read Mode.<br>0: Disable.<br>1: Enable. | |
| **A1h** | **OSDRA** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | OSDRA | 5:0 | OSD Register Address Port. | |
| **A2h** | **OSDRD** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | OSDRD | 7:0 | OSD Register Data Port. | |
| **A3h** | **OSDFA** | **7:0** | **Default : -** | **Access : WO** |
| | OSDFA | 7:0 | OSD RAM Font Address Port. | |
| **A4h** | **OSDFD** | **7:0** | **Default : -** | **Access : WO** |
| | OSDFD | 7:0 | OSD RAM Font Data Port. | |
| **A5h** | **DISPCA_L** | **7:0** | **Default : -** | **Access : WO** |
| | DISPCA[7:0] | 7:0 | OSD Display Code Address Port. | |
| **A6h** | **DISPCA_H** | **7:0** | **Default : -** | **Access : WO** |

## OSD Register (Bank=00)

| Index | Mnemonic | Bits | Description | |
|---|---|---|---|---|
| | - | 7:3 | Reserved. | |
| | DISPCA[10:8] | 2:0 | OSD Display Code Address Port. | |
| **A7h** | **DISPCD** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | DISPCD[7:0] | 7:0 | OSD Display Code Data Port (When write access disabled, this port report display code data). | |
| **A8h** | **DISPAA_L** | **7:0** | **Default : -** | **Access : WO** |
| | DISPAA[7:0] | 7:0 | OSD Display Attribute Address port. | |
| **A9h** | **DISPAA_H** | **7:0** | **Default : -** | **Access : WO** |
| | - | 7:3 | Reserved. | |
| | DISPAA[10:8] | 2:0 | OSD Display Attribute Address port. | |
| **AAh** | **DISPAD** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | DISPAD[7:0] | 7:0 | OSD Display Attribute Data Port (When write access disabled, this port report display attribute data). | |
| **AEh** | **DISPCA_CTL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | DISPAD_RE[8] | 6 | When write access disabled, this bit report display attribute data (bit 8). | |
| | - | 5 | Reserved. | |
| | DISPCD_RE[8] | 4 | When write access disabled, this bit report display code data (bit 8). | |
| | - | 3 | Reserved. | |
| | INS_DATA | 2 | OSD Code/Attribute 9th bit Data (Code (A7h)/Attribute (AAh) Data Extend bit). | |
| | - | 1 | Reserved. | |
| | CA_NO_WRITE | 0 | OSD Display Code and Attribute Write disable. | |
| | **OSD CODE (9th bit)** | | | |
| | ITALIC | 8 | OSD Italic Control<br>0: Disable.<br>1: Enable.<br>(Please refer AEh bit 0 INS_DATA) | |
| | **OSD Attribute (8-Color Palette)** | | | |
| | HALF_TRAN | 8 | OSD Half-transparency Control.<br>0: Disable.<br>1: Enable.<br>(Please refer AEh[0]: INS_DATA and 42h[2]: ALF_TRANEN) | |

| OSD Register (Bank=00) | | | |
|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** |
| | BLNK_CTRL | 7 | OSD Blink Control.<br>0: Disable.<br>1: Enable. |
| | FGCLR[2:0] | 6:4 | OSD Foreground Color Select.<br>000: Color index 0.<br>001: Color index 1.<br>…<br>111: Color index 7. |
| | BDER_CTRL | 3 | OSD Character Border Control.<br>0: Disable.<br>1: Enable.<br>(Please refer 42h[5] UNDERLINE_MD) |
| | BGCLR[2:0] | 2:0 | OSD Background Color select.<br>000: color index 0.<br>001: color index 1.<br>…<br>111: color index 7. |
| | **OSD Attribute ( 16 Color Palette)** | | |
| | FGCLR[3:0] | 7:4 | OSD Foreground Color Select.<br>0000: color index 0.<br>0001: color index 1.<br>…<br>1111: color index 15. |
| | BGCLR[3:0] | 3:0 | OSD Background Color Select.<br>0000: color index 0.<br>0001: color index 1.<br>…<br>1111: color index 15. |

## OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)

| OSD Register (Indirect mapping to Bank 00, Registers A1h/A2) | | | | |
|---|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** | |
| **01h** | **OSDDBC** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | DBL[1:0] | 2:1 | Double Buffer Load.<br>00: Keep old register value.<br>01: Load new data (auto reset to 00 when loading completes).<br>10: Automatically load data at VSYNC blanking.<br>11: Reserved. | |
| | DB_EN | 0 | Double Buffer Enable.<br>0: Disable.<br>1: Enable. | |
| **02h** | **OHSTA-L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | OHSTA[7:0] | 7:0 | OSD windows Horizontal Start position (pixel) (lower 8 bits). | |
| **03h** | **OHSTA-H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | OHSTA[10:8] | 2:0 | OSD windows Horizontal Start position (higher 3 bits). | |
| **04h** | **OVSTA-L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | OVSTA[7:0] | 7:0 | OSD windows Vertical Start position (line) (lower 8 bits). | |
| **05h** | **OVSTA-H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:2 | Reserved. | |
| | OVSTA[9:8] | 1:0 | OSD windows Vertical Start position (higher 2 bits). | |
| **06h** | **OSDW** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | OSDW[5:0] | 5:0 | OSD windows Width (OSDW + 1 (column)), maximum 64 columns. | |
| **07h** | **OSDH** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | OSDH[5:0] | 5:0 | OSD windows Height (OSDH + 1 (row)), maximum 64 rows. | |
| **08h** | **OHSPA** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | OHSPA[5:0] | 5:0 | OSD windows Horizontal Space start position (OHSPA + 1 (column)). | |
| **09h** | **OVSPA** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | OVSPA[4:0] | 4:0 | OSD windows Vertical Space start position (OVSPA + 1 (row)). | |

## OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)

| Index | Mnemonic | Bits | Description | |
|---|---|---|---|---|
| **0Ah** | **OSPW** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | OSPW[7:0] | 7:0 | OSD Space Width (8 * OSPW (pixel)). | |
| **0Bh** | **OSPH** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | OSPH[7:0] | 7:0 | OSD Space Height (8 * OSPH (line)). | |
| **0Ch** | **IOSDC1** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | OVS[1:0] | 7:6 | OSD Vertical Scaling.<br>00: Vertical normal size.<br>01: Vertical enlarged x2 by repeated pixels.<br>10: Vertical enlarged x3 by repeated pixels.<br>11: Vertical enlarged x4 by repeated pixels. | |
| | OHS[1:0] | 5:4 | OSD Horizontal Scaling.<br>00: Horizontal normal size.<br>01: Horizontal enlarged x2 by repeated pixels.<br>10: Horizontal enlarged x3 by repeated pixels.<br>11: Horizontal enlarged x4 by repeated pixels. | |
| | - | 3:1 | Reserved. | |
| | MWIN | 0 | OSD Main Window display.<br>0: Off.<br>1: On. | |
| **0Dh** | **IOSDC2** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | BDC | 5 | OSD Character Border type select.<br>0: All direction font boundary (border).<br>1: Bottom-right direction font boundary (shadow). | |
| | BDW | 4 | OSD character Border Width control.<br>0: One pixel with for all scale.<br>1: Scale with OVS[1:0] and OHS[1:0]. | |
| | - | 3 | Reserved. | |
| | BCLR[2:0] | 2:0 | OSD Border Color index.<br>000: color index 0.<br>001: color index 1.<br>…<br>111: color index 7. | |
| **0Eh** | **IOSDC3** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:6 | Reserved. | |

| OSD Register (Indirect mapping to Bank 00, Registers A1h/A2) | | | | |
|---|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** | |
| | SHALL | 5 | OSD Shadow with All Direction.<br>0: Shadow with Bottom-Right direction (shadow).<br>1: Shadow with all direction (border). | |
| | SDC | 4 | OSD Window Shadow Control.<br>0: Off.<br>1: On. | |
| | SCLR[3:0] | 3:0 | OSD window Shadow Color index.<br>0000: Color index 0.<br>0001: Color index 1.<br>…<br>1111: Color index 15. | |
| **0Fh** | **OSHC** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | OSDSH[3:0] | 7:4 | OSD Shadow Height. | |
| | OSDSW[3:0] | 3:0 | OSD Shadow Width. | |
| **10h** | **IOSDC4** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | LINE_SHIFT_EN | 7 | OSD line shift Enable (Please refer 45h bit 4~2 LINE_SHIFT_VAL). | |
| | FIELD_POL | 6 | OSD line shift Field Polarity. | |
| | - | 5 | Reserved. | |
| | EN_M4C | 4 | 4 Color Font Enable.<br>0: Disable.<br>1: Enable. | |
| | F16H | 3 | OSD font high control.<br>0: Font height is 18.<br>1: Font height is 16. | |
| | PEXT | 2 | OSD 16 color palette extent method.<br>0: Extend with palette bit 3.<br>1: Extend with 0. | |
| | TRANEN | 1 | OSD Transparency Enable.<br>0: No transparency.<br>1: Color index which hit OSD Color index for transparency[2:0] is transparent of 8 color palette/<br>Color index which hit OSD Color index for transparency[3:0] is transparent of 16 color palette.<br>(Please refer 42h bit 3~0 OSD Color index for transparency.) | |
| | T16C | 0 | OSD 16 Color Palette select.<br>0: 8 color palette.<br>1: 16 color palette. | |
| **12h** | **OCBUFO** | **7:0** | **Default : 0x00** | **Access : R/W** |

| OSD Register (Indirect mapping to Bank 00, Registers A1h/A2) | | | | |
|---|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** | |
| | CO_SEL | 7 | OSD Code buffer Offset Select.<br>0: Use OSDW[5:0] as offset.<br>1: Use OOFFSET[5:0] as offset. | |
| | - | 6 | Reserved. | |
| | OOFFSET[5:0] | 5:0 | OSD code buffer Offset Value. | |
| **13h** | **OSDBA-L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | OSDBA[7:0] | 7:0 | OSD code Base Address (lower 8 bits). | |
| **14h** | **OSDBA-H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | OSDBA[10:8] | 2:0 | OSD code Base Address (higher 3 bits)<br>(Please refer 45h bit7 CCRAM608X2.<br>When CCRAM608X2 = 0, OSDBA[10:0] is programming from 0 to 4BFh;<br>when CCRAM608X2 = 1, OSDBA[9:0] is programming from 0 to 25fh and OSDBA[10] is programming to select low or high part code/attribute SRAM). | |
| **15h** | **GCCTRL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | GVS[1:0] | 7:6 | Gradually color Vertical Scaling.<br>00: Vertical normal size.<br>01: Vertical enlarged x2 by repeated pixels.<br>10: Vertical enlarged x3 by repeated pixels.<br>11: Vertical enlarged x4 by repeated pixels. | |
| | GHS[1:0] | 5:4 | Gradually color Horizontal Scaling.<br>00: Horizontal normal size.<br>01: Horizontal enlarged x2 by repeated pixels.<br>10: Horizontal enlarged x3 by repeated pixels.<br>11: Horizontal enlarged x4 by repeated pixels. | |
| | GRAD | 3 | Enable OSD Gradual color function.<br>0: Disable.<br>1: Enable. | |
| | ADC_PG | 2 | ADC Pattern Generator select.<br>0: Normal.<br>1: ADC. | |
| | SVM_SEL | 1:0 | SVM Mask signal Select.<br>00: Original active signal.<br>01: 2T early.<br>10: 4T early.<br>11: 6T early. | |

## OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)

| Index | Mnemonic | Bits | Description | |
|---|---|---|---|---|
| **16h** | **GRADCLR** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | FCLR | 7 | Gradual color by Frame Color.<br>0: Use RCLR, GCLR, BCLR as starting gradual color.<br>1: Use Frame Color as starting gradual color. | |
| | - | 6 | Reserved. | |
| | RCLR[1:0] | 5:4 | Red starting gradual Color.<br>00: Red color is 00h.<br>01: Red color is 55h.<br>10: Red color is AAh.<br>11: Red color is FFh. | |
| | GCLR[1:0] | 3:2 | Green starting gradual Color.<br>00: Green color is 00h.<br>01: Green color is 55h.<br>10: Green color is AAh.<br>11: Green color is FFh. | |
| | BCLR[1:0] | 1:0 | Blue starting gradual Color.<br>00: Blue color is 00h.<br>01: Blue color is 55h.<br>10: Blue color is AAh.<br>11: Blue color is FFh. | |
| **17h** | **HGRADCR** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | SR | 7 | Sign bit of Red color.<br>0: Increase.<br>1: Decrease. | |
| | IRH | 6 | Inverse bit of Red color.<br>0: Normal.<br>1: Invert. | |
| | R_GRADH[5:0] | 5:0 | Increase/decrease value of Red color. | |
| **18h** | **HGRADCG** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | SG | 7 | Sign bit of Green color.<br>0: Increase.<br>1: Decrease. | |
| | IGH | 6 | Inverse bit of Green color.<br>0: Normal.<br>1: Invert. | |
| | G_GRADH[5:0] | 5:0 | Increase/decrease value of Green color. | |
| **19h** | **HGRADCB** | **7:0** | **Default : 0x00** | **Access : R/W** |

| OSD Register (Indirect mapping to Bank 00, Registers A1h/A2) | | | | |
|---|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** | |
| | SB | 7 | Sign bit of Blue color.<br>0: Increase.<br>1: Decrease. | |
| | IBH | 6 | Inverse bit of Blue color.<br>0: Normal.<br>1: Invert. | |
| | B_GRADH[5:0] | 5:0 | Increase/decrease value of Blue color. | |
| **1Ah** | **HGRADSR** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | HGRADSR[7:0] | 7:0 | Horizontal Gradual Step of Red color. | |
| **1Bh** | **HGRADSG** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | HGRADSG[7:0] | 7:0 | Horizontal Gradual Step of Green color. | |
| **1Ch** | **HGRADSB** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | HGRADSB[7:0] | 7:0 | Horizontal Gradual Step of Blue color. | |
| **1Dh** | **VGRADCR** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | SR | 7 | Sign bit of Red color.<br>0: Increase.<br>1: Decrease. | |
| | IRV | 6 | Inverse bit of Red color.<br>0: Normal.<br>1: Invert. | |
| | R_GRADV[5:0] | 5:0 | Increase/decrease value of Red color. | |
| **1Eh** | **VGRADCG** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | SG | 7 | Sign bit of Green color.<br>0: Increase.<br>1: Decrease. | |
| | IGV | 6 | Inverse bit of Green color.<br>0: Normal.<br>1: Invert. | |
| | G_GRADV[5:0] | 5:0 | Increase/Decrease value of Green color. | |
| **1Fh** | **VGRADCB** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | SB | 7 | Sign bit of Blue color.<br>0: Increase.<br>1: Decrease. | |
| | IBV | 6 | Inverse bit of Blue color.<br>0: Normal.<br>1: Invert. | |

| OSD Register (Indirect mapping to Bank 00, Registers A1h/A2) | | | | |
|---|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** | |
| | B_GRADV[5:0] | 5:0 | Increase/decrease value of Blue color. | |
| **20h** | **VGRADSR** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | VGRADSR[7:0] | 7:0 | Vertical Gradual Step of Red color. | |
| **21h** | **VGRADSG** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | VGRADSG[7:0] | 7:0 | Vertical Gradual Step of Green color. | |
| **22h** | **VGRADSB** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | VGRADSB[7:0] | 7:0 | Vertical Gradual Step of Blue color. | |
| **23h ~ 25h** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **26h** | **TIMECTRL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | FRG_EN | 4 | OSD Font Ram Gated Enable.<br>0: Disable.<br>1: Enable. | |
| | - | 3:2 | Reserved | |
| | VSTDLY | 1 | OSD Vertical Start Delay.<br>0: Normal.<br>1: Vertical Delay 1 line. | |
| | - | 0 | Reserved. | |
| **27h** | **OSDRTP** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | RTPT | 2 | OSD Random Test Pattern Type.<br>0: RGB is the same.<br>1: RGB is different. | |
| | OSDRTP[1:0] | 1:0 | OSD Random Test Pattern.<br>00: Disable.<br>01: 1 random bit.<br>10: 2 random bit.<br>11: Reserved. | |
| **OSD Color Palette when T16_C = 0** | | | | |
| **28h** | **CLR0R** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR0R[7:0] | 7:0 | Red Color Index 0. | |
| **29h** | **CLR0G** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR0G[7:0] | 7:0 | Green Color Index 0. | |
| **2Ah** | **CLR0B** | **7:0** | **Default : 0x00** | **Access : R/W** |

| OSD Register (Indirect mapping to Bank 00, Registers A1h/A2) | | | | |
|---|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** | |
| | CLR0B[7:0] | 7:0 | Blue Color Index 0. | |
| **2Bh** | **CLR1R** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR1R[7:0] | 7:0 | Red Color Index 1. | |
| **2Ch** | **CLR1G** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR1G[7:0] | 7:0 | Green Color Index 1. | |
| **2Dh** | **CLR1B** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR1B[7:0] | 7:0 | Blue Color Index 1. | |
| **2Eh** | **CLR2R** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR2R[7:0] | 7:0 | Red Color Index 2. | |
| **2Fh** | **CLR2G** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR2G[7:0] | 7:0 | Green Color Index 2. | |
| **30h** | **CLR2B** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR2B[7:0] | 7:0 | Blue Color Index 2. | |
| **31h** | **CLR3R** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR3R[7:0] | 7:0 | Red Color Index 3. | |
| **32h** | **CLR3G** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR3G[7:0] | 7:0 | Green Color Index 3. | |
| **33h** | **CLR3B** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR3B[7:0] | 7:0 | Blue Color Index 3. | |
| **34h** | **CLR4R** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR4R[7:0] | 7:0 | Red Color Index 4. | |
| **35h** | **CLR4G** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR4G[7:0] | 7:0 | Green Color Index 4. | |
| **36h** | **CLR4B** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR4B[7:0] | 7:0 | Blue Color Index 4. | |
| **37h** | **CLR5R** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR5R[7:0] | 7:0 | Red Color Index 5. | |
| **38h** | **CLR5G** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR5G[7:0] | 7:0 | Green Color Index 5. | |
| **39h** | **CLR5B** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR5B[7:0] | 7:0 | Blue Color Index 5. | |
| **3Ah** | **CLR6R** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR6R[7:0] | 7:0 | Red Color Index 6. | |

| OSD Register (Indirect mapping to Bank 00, Registers A1h/A2) | | | | |
|---|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** | |
| **3Bh** | **CLR6G** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR6G[7:0] | 7:0 | Green Color Index 6. | |
| **3Ch** | **CLR6B** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR6B[7:0] | 7:0 | Blue Color Index 6. | |
| **3Dh** | **CLR7R** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR7R[7:0] | 7:0 | Red Color Index 7. | |
| **3Eh** | **CLR7G** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR7G[7:0] | 7:0 | Green Color Index 7. | |
| **3Fh** | **CLR7B** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR7B[7:0] | 7:0 | Blue Color Index 7. | |
| **OSD Color Palette when T16_C = 1 (16 color format: col[7:4], 4'b0 or col[7:4], {4{col[4]}})** | | | | |
| **28h** | **CLR0R** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR0R[7:4] | 7:4 | Red Color Index 0. | |
| | CLR8R[3:0] | 3:0 | Red Color Index 8. | |
| **29h** | **CLR0G** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR0G[7:4] | 7:4 | Green Color Index 0. | |
| | CLR8G[3:0] | 3:0 | Green Color Index 8. | |
| **2Ah** | **CLR0B** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR0B[7:4] | 7:4 | Blue Color Index 0. | |
| | CLR8B[3:0] | 3:0 | Blue Color Index 8. | |
| **2Bh** | **CLR1R** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR1R[7:4] | 7:4 | Red Color Index 1. | |
| | CLR9R[3:0] | 3:0 | Red Color Index 9. | |
| **2Ch** | **CLR1G** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR1G[7:4] | 7:4 | Green Color Index 1. | |
| | CLR9G[3:0] | 3:0 | Green Color Index 9. | |
| **2Dh** | **CLR1B** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR1B[7:4] | 7:4 | Blue Color Index 1. | |
| | CLR9B[3:0] | 3:0 | Blue Color Index 9. | |
| **2Eh** | **CLR2R** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR2R[7:4] | 7:4 | Red Color Index 2. | |
| | CLR10R[3:0] | 3:0 | Red Color Index 10. | |
| **2Fh** | **CLR2G** | **7:0** | **Default : 0x00** | **Access : R/W** |

| OSD Register (Indirect mapping to Bank 00, Registers A1h/A2) | | | | |
|---|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** | |
| | CLR2G[7:4] | 7:4 | Green Color Index 2. | |
| | CLR10G[3:0] | 3:0 | Green Color Index 10. | |
| **30h** | **CLR2B** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR2B[7:4] | 7:4 | Blue Color Index 2. | |
| | CLR10B[3:0] | 3:0 | Blue Color Index 10. | |
| **31h** | **CLR3R** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR3R[7:4] | 7:4 | Red Color Index 3. | |
| | CLR11R[3:0] | 3:0 | Red Color Index 11. | |
| **32h** | **CLR3G** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR3G[7:4] | 7:4 | Green Color Index 3. | |
| | CLR11G[3:0] | 3:0 | Green Color Index 11. | |
| **33h** | **CLR3B** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR3B[7:4] | 7:4 | Blue Color Index 3. | |
| | CLR11B[3:0] | 3:0 | Blue Color Index 11. | |
| **34h** | **CLR4R** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR4R[7:4] | 7:4 | Red Color Index 4. | |
| | CLR12R[3:0] | 3:0 | Red Color Index 12. | |
| **35h** | **CLR4G** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR4G[7:4] | 7:4 | Green Color Index 4. | |
| | CLR12G[3:0] | 3:0 | Green Color Index 12. | |
| **36h** | **CLR4B** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR4B[7:4] | 7:4 | Blue Color Index 4. | |
| | CLR12B[3:0] | 3:0 | Blue Color Index 12. | |
| **37h** | **CLR5R** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR5R[7:4] | 7:4 | Red Color Index 5. | |
| | CLR13R[3:0] | 3:0 | Red Color Index 13. | |
| **38h** | **CLR5G** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR5G[7:4] | 7:4 | Green Color Index 5. | |
| | CLR13G[3:0] | 3:0 | Green Color Index 13. | |
| **39h** | **CLR5B** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR5B[7:4] | 7:4 | Blue Color Index 5. | |
| | CLR13B[3:0] | 3:0 | Blue Color Index 13. | |
| **3Ah** | **CLR6R** | **7:0** | **Default : 0x00** | **Access : R/W** |

| OSD Register (Indirect mapping to Bank 00, Registers A1h/A2) | | | | |
|---|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** | |
| | CLR6R[7:4] | 7:4 | Red Color Index 6. | |
| | CLR14R[3:0] | 3:0 | Red Color Index 14. | |
| **3Bh** | **CLR6G** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR6G[7:4] | 7:4 | Green Color Index 6. | |
| | CLR14G[3:0] | 3:0 | Green Color Index 14. | |
| **3Ch** | **CLR6B** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR6B[7:4] | 7:4 | Blue Color Index 6. | |
| | CLR14B[3:0] | 3:0 | Blue Color Index 14. | |
| **3Dh** | **CLR7R** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR7R[7:4] | 7:4 | Red Color Index 7. | |
| | CLR15R[3:0] | 3:0 | Red Color Index 15. | |
| **3Eh** | **CLR7G** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR7G[7:4] | 7:4 | Green Color Index 7. | |
| | CLR15G[3:0] | 3:0 | Green Color Index 15. | |
| **3Fh** | **CLR7B** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLR7B[7:4] | 7:4 | Blue Color Index 7. | |
| | CLR15B[3:0] | 3:0 | Blue Color Index 15. | |
| **40h** | **SCRLSPD** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | SCRLSPD[7:0] | 7:0 | OSD Scroll function speed (the numbers of VSYNC). | |
| **41h** | **SCRLLINE** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | SCREN | 7 | OSD Scroll function Enable.<br>0: Disable.<br>1: Enable. | |
| | VSCR_FAST | 6 | Scroll at every VSYNC. | |
| | TRUC_EN | 5 | Truncate code/attribute Enable.<br>0: Disable.<br>1: Enable. | |
| | SCRLLINE[4:0] | 4:0 | OSD Scroll function (the numbers of scan lines per scroll). | |
| **42h** | **UNDERLINE** | **7:0** | **Default : 0x0F** | **Access : R/W** |
| | UNDERLINE_1 | 7 | OSD Underline at last line. | |
| | UNDERLINE_2 | 6 | OSD Underline at second last line. | |
| | UNDERLINE_MD | 5 | OSD Underline Mode enable (When this bit is asserted, OSD Attribute (8 Color) bit 3. (BDER) Character Boder Control change function to OSD Character Underline Control). | |

| OSD Register (Indirect mapping to Bank 00, Registers A1h/A2) | | | | |
|---|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** | |
| | HALF_TRANEN | 4 | OSD Half-Transparency Enable (When this bit is asserted, OSD Attribute (8 Color) bit 9 (HALF_TRAN) is active.). | |
| | TRAN_INDEX[3:0] | 3:0 | OSD Color Index for Transparency (Define which color index is transparent). | |
| **43h** | **TRUNCATE** | **7:0** | **Default : 0x 1D** | **Access : R/W** |
| | TRUNCATENUM | 7:0 | OSD Truncate number (Please refer 45h bit7 CCRAM608X2. When CCRAM608X2=0, final row=(11'h4bf-TRUNCATENUM); when CCRAM608X2=1, final row=(11'h25f-TRUNCATENUM)). | |
| **44h** | **ITALIC** | **7:0** | **Default : 0x 00** | **Access : R/W** |
| | ITALIC_OFFSET | 7:6 | OSD Italic right shift Offset (00: 1, 01: 2, 10: 3, 11: 4 (pixel)). | |
| | ITALIC_1ST_LINE | 5:4 | OSD Italic start scan Line (00: 0, 01: 1, 10: 2, 11: 3 (line)). | |
| | ITALIC_STEP | 3:2 | OSD Italic left shift Step (00: 0.001, 01: 0.010, 10: 0.011, 11: 0.100 (pixel , binary)). | |
| | ITALIC_EN | 1 | OSD Italic function Enable.<br>0: Disable.<br>1: Enable. | |
| | - | 0 | Reserved. | |
| **45h** | **MISC_CTL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CCRAM608X2 | 7 | OSD 2 608 code/attribute SRAM (When CCRAM608X2 = 0, there is one 1216 code/attribute SRAM for using; when CCRAM608X2 = 1, there are two 608 code/attribute SRAM for using.). | |
| | - | 6:5 | Reserved. | |
| | LINE_SHIFT_VAL[2:0] | 4:2 | OSD Line shift value (Line shift number, 000: 1, …, 111: 8). | |
| | CARHG_EN | 1 | OSD code/attribute high part ram gated Enable.<br>0: Disable.<br>1: Enable. | |
| | - | 0 | Reserved. | |
| **46h** | **OSD4CFFA** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | OSD4CFFA[7:0] | 7:0 | OSD 4 Color Font RAM start Address (must be even number). | |
| **47h ~ 49h** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **4Ah** | **OHVSTA-H** | **7:0** | **Default : 0x00** | **Access : RO** |
| | VSCR_OPT | 7 | Vscroll Option.<br>0: Original.<br>1: Fixed. | |
| | - | 6 | Reserved. | |

## OSD Register (Indirect mapping to Bank 00, Registers A1h/A2)

| Index | Mnemonic | Bits | Description | |
|---|---|---|---|---|
| | OVSTA[9:8] | 5:4 | OSD windows Vertical Start position (Read only). | |
| | - | 3 | Reserved. | |
| | OHSTA[10:8] | 2:0 | OSD windows Horizontal Start position. (Read only). | |
| **4Bh ~ 4Ch** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **4Dh** | **OSDBRI** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | OSDBRI_EN | 7 | OSD Brightness Enable.<br>0: Disable.<br>1: Enable. | |
| | OSDBRI_DIR | 6 | OSD Brightness Control.<br>0: Add.<br>1: Subtract. | |
| | OSDBRI_VAL[5:0] | 5:0 | OSD Brightness Value. | |
| **4Eh ~ 4Fh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **50h** | **CODECLRDATA_L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CODECLRDATA[7:0] | 7:0 | OSD Code Clear Data. | |
| **51h** | **ATRCLRDATA_L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | ATRCLRDAT[7:0] | 7:0 | OSD Attribute Clear Data (lower 8 bits). | |
| **52h** | **OSDCLRDATA** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | ATRCLRDAT[8] | 4 | OSD Attribute Clear Data. | |
| | - | 3:1 | Reserved. | |
| | CODECLRDAT[8] | 0 | OSD Code Clear Data. | |
| **53h** | **OSDCLRADR_L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | OSDCLR_ADR[7:0] | 7:0 | OSD Clear Starting address (lower 8 bits). | |
| **54h** | **OSDCLRADR_H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | ATR1_CLREN | 7 | OSD Attribute High Clear Enable. | |
| | ATR0_CLREN | 6 | OSD Attribute Low Clear Enable. | |
| | CODE1_CLREN | 5 | OSD Code High Clear Enable. | |
| | CODE0_CLREN | 4 | OSD Code Low Clear Enable. | |
| | - | 3:2 | Reserved. | |
| | OSDCLR_ADR[9:8] | 1:0 | OSD Clear Starting Address. | |
| **55h** | **OSDCLR_OFST** | **7:0** | **Default : 0x00** | **Access : R/W** |

| OSD Register (Indirect mapping to Bank 00, Registers A1h/A2) | | | | |
|---|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** | |
| | - | 7 | Reserved | |
| | OSDCLR_OFST[6:0] | 6:0 | OSD Clear Offset. | |
| **56h** | **OSDCLR_WID** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | OSDCLR_WID[6:0] | 6:0 | OSD Clear Width. | |
| **57h** | **OSDCLR_HIGT** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | OSDCLR_HIGT[6:0] | 6:0 | OSD Clear Height. | |
| **58h** | **OSDCLR_CTRL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:1 | Reserved. | |
| | BLK_CLR_EN | 0 | OSD Block Clear Enable. | |
| **59h ~ 9Fh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |

## Gamma Register (Indirect mapping to Bank 00, Registers 91h/92h)

| Gamma Register (Indirect mapping to Bank 00, Registers 91h/92h) | | | | |
|---|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** | |
| **00h** | **Gamma_R00** | **7:0** | **Default : 0d00** | **Access : R/W** |
| | Gamma_R00 | 7:0 | Gamma_table R00 value. | |
| **01h** | **Gamma_R01** | **7:0** | **Default : 0d07** | **Access : R/W** |
| | Gamma_R01 | 7:0 | Gamma_table R01 value. | |
| **02h** | **Gamma_R02** | **7:0** | **Default : 0d15** | **Access : R/W** |
| | Gamma_R02 | 7:0 | Gamma_table R02 value. | |
| **03h** | **Gamma_R03** | **7:0** | **Default : 0d23** | **Access : R/W** |
| | Gamma_R03 | 7:0 | Gamma_table R03 value. | |
| **04h** | **Gamma_R04** | **7:0** | **Default : 0d31** | **Access : R/W** |
| | Gamma_R04 | 7:0 | Gamma_table R04 value. | |
| **05h** | **Gamma_R05** | **7:0** | **Default : 0d39** | **Access : R/W** |
| | Gamma_R05 | 7:0 | Gamma_table R05 value. | |
| **06h** | **Gamma_R06** | **7:0** | **Default : 0d47** | **Access : R/W** |
| | Gamma_R06 | 7:0 | Gamma_table R06 value. | |
| **07h** | **Gamma_R07** | **7:0** | **Default : 0d55** | **Access : R/W** |
| | Gamma_R07 | 7:0 | Gamma_table R07 value | |
| **08h** | **Gamma_R08** | **7:0** | **Default : 0d63** | **Access : R/W** |
| | Gamma_R08 | 7:0 | Gamma_table R08 value. | |
| **09h** | **Gamma_R09** | **7:0** | **Default : 0d71** | **Access : R/W** |
| | Gamma_R09 | 7:0 | Gamma_table R09 value. | |
| **0Ah** | **Gamma_R10** | **7:0** | **Default : 0d79** | **Access : R/W** |
| | Gamma_R10 | 7:0 | Gamma_table R10 value. | |
| **0Bh** | **Gamma_R11** | **7:0** | **Default : 0d87** | **Access : R/W** |
| | Gamma_R11 | 7:0 | Gamma_table R11 value. | |
| **0Ch** | **Gamma_R12** | **7:0** | **Default : 0d95** | **Access : R/W** |
| | Gamma_R12 | 7:0 | Gamma_table R12 value. | |
| **0Dh** | **Gamma_R13** | **7:0** | **Default : 0d103** | **Access : R/W** |
| | Gamma_R13 | 7:0 | Gamma_table R13 value. | |
| **0Eh** | **Gamma_R14** | **7:0** | **Default : 0d111** | **Access : R/W** |
| | Gamma_R14 | 7:0 | Gamma_table R14 value. | |
| **0Fh** | **Gamma_R15** | **7:0** | **Default : 0d119** | **Access : R/W** |
| | Gamma_R15 | 7:0 | Gamma_table R15 value. | |

| Gamma Register (Indirect mapping to Bank 00, Registers 91h/92h) | | | | |
|---|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** | |
| **10h** | **Gamma_R16** | **7:0** | **Default : 0d127** | **Access : R/W** |
| | Gamma_R16 | 7:0 | Gamma_table R16 value. | |
| **11h** | **Gamma_R17** | **7:0** | **Default : 0d135** | **Access : R/W** |
| | Gamma_R17 | 7:0 | Gamma_table R17 value. | |
| **12h** | **Gamma_R18** | **7:0** | **Default : 0d143** | **Access : R/W** |
| | Gamma_R18 | 7:0 | Gamma_table R18 value. | |
| **13h** | **Gamma_R19** | **7:0** | **Default : 0d151** | **Access : R/W** |
| | Gamma_R49 | 7:0 | Gamma_table R19 value. | |
| **14h** | **Gamma_R20** | **7:0** | **Default : 0d159** | **Access : R/W** |
| | Gamma_R20 | 7:0 | Gamma_table R20 value. | |
| **15h** | **Gamma_R21** | **7:0** | **Default : 0d167** | **Access : R/W** |
| | Gamma_R21 | 7:0 | Gamma_table R21 value. | |
| **16h** | **Gamma_R22** | **7:0** | **Default : 0d175** | **Access : R/W** |
| | Gamma_R22 | 7:0 | Gamma_table R22 value. | |
| **17h** | **Gamma_R23** | **7:0** | **Default : 0d183** | **Access : R/W** |
| | Gamma_R23 | 7:0 | Gamma_table R23 value. | |
| **18h** | **Gamma_R24** | **7:0** | **Default : 0d191** | **Access : R/W** |
| | Gamma_R24 | 7:0 | Gamma_table R24 value. | |
| **19h** | **Gamma_R25** | **7:0** | **Default : 0d199** | **Access : R/W** |
| | Gamma_R25 | 7:0 | Gamma_table R25 value. | |
| **1Ah** | **Gamma_R26** | **7:0** | **Default : 0d207** | **Access : R/W** |
| | Gamma_R26 | 7:0 | Gamma_table R26 value. | |
| **1Bh** | **Gamma_R27** | **7:0** | **Default : 0d215** | **Access : R/W** |
| | Gamma_R27 | 7:0 | Gamma_table R27 value. | |
| **1Ch** | **Gamma_R28** | **7:0** | **Default : 0d223** | **Access : R/W** |
| | Gamma_R28 | 7:0 | Gamma_table R28 value. | |
| **1Dh** | **Gamma_R29** | **7:0** | **Default : 0d232** | **Access : R/W** |
| | Gamma_R29 | 7:0 | Gamma_table R29 value. | |
| **1Eh** | **Gamma_R30** | **7:0** | **Default : 0d239** | **Access : R/W** |
| | Gamma_R30 | 7:0 | Gamma_table R30 value. | |
| **1Fh** | **Gamma_R31** | **7:0** | **Default : 0d247** | **Access : R/W** |
| | Gamma_R31 | 7:0 | Gamma_table R31 value. | |
| **20h** | **Gamma_R32** | **7:0** | **Default : 0d255** | **Access : R/W** |

| Gamma Register (Indirect mapping to Bank 00, Registers 91h/92h) | | | | |
|---|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** | |
| | Gamma_R32 | 7:0 | Gamma_table R32 value. | |
| **21h** | **Gamma_G00** | **7:0** | **Default : 0d00** | **Access : R/W** |
| | Gamma_G00 | 7:0 | Gamma_table G00 value. | |
| **22h** | **Gamma_G01** | **7:0** | **Default : 0d07** | **Access : R/W** |
| | Gamma_G01 | 7:0 | Gamma_table G01 value. | |
| **23h** | **Gamma_G02** | **7:0** | **Default : 0d15** | **Access : R/W** |
| | Gamma_G02 | 7:0 | Gamma_table G02 value. | |
| **24h** | **Gamma_G03** | **7:0** | **Default : 0d23** | **Access : R/W** |
| | Gamma_G03 | 7:0 | Gamma_table G03 value. | |
| **25h** | **Gamma_G04** | **7:0** | **Default : 0d31** | **Access : R/W** |
| | Gamma_G04 | 7:0 | Gamma_table G04 value. | |
| **26h** | **Gamma_G05** | **7:0** | **Default : 0d39** | **Access : R/W** |
| | Gamma_G05 | 7:0 | Gamma_table G05 value. | |
| **27h** | **Gamma_G06** | **7:0** | **Default : 0d47** | **Access : R/W** |
| | Gamma_G06 | 7:0 | Gamma_table G06 value. | |
| **28h** | **Gamma_G07** | **7:0** | **Default : 0d55** | **Access : R/W** |
| | Gamma_G07 | 7:0 | Gamma_table G07 value. | |
| **29h** | **Gamma_G08** | **7:0** | **Default : 0d63** | **Access : R/W** |
| | Gamma_G08 | 7:0 | Gamma_table G08 value. | |
| **2Ah** | **Gamma_G09** | **7:0** | **Default : 0d71** | **Access : R/W** |
| | Gamma_G09 | 7:0 | Gamma_table G09 value. | |
| **2Bh** | **Gamma_G10** | **7:0** | **Default : 0d79** | **Access : R/W** |
| | Gamma_G10 | 7:0 | Gamma_table G10 value. | |
| **2Ch** | **Gamma_G11** | **7:0** | **Default : 0d87** | **Access : R/W** |
| | Gamma_G11 | 7:0 | Gamma_table G11 value. | |
| **2Dh** | **Gamma_G12** | **7:0** | **Default : 0d95** | **Access : R/W** |
| | Gamma_G12 | 7:0 | Gamma_table G12 value. | |
| **2Eh** | **Gamma_G13** | **7:0** | **Default : 0d103** | **Access : R/W** |
| | Gamma_G13 | 7:0 | Gamma_table G13 value. | |
| **2Fh** | **Gamma_G14** | **7:0** | **Default : 0d111** | **Access : R/W** |
| | Gamma_G14 | 7:0 | Gamma_table G14 value. | |
| **30h** | **Gamma_G15** | **7:0** | **Default : 0d119** | **Access : R/W** |
| | Gamma_G15 | 7:0 | Gamma_table G15 value. | |

| Gamma Register (Indirect mapping to Bank 00, Registers 91h/92h) | | | | |
|---|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** | |
| **31h** | **Gamma_G16** | **7:0** | **Default : 0d127** | **Access : R/W** |
| | Gamma_G16 | 7:0 | Gamma_table G16 value. | |
| **32h** | **Gamma_G17** | **7:0** | **Default : 0d135** | **Access : R/W** |
| | Gamma_G17 | 7:0 | Gamma_table G17 value. | |
| **33h** | **Gamma_G18** | **7:0** | **Default : 0d143** | **Access : R/W** |
| | Gamma_G18 | 7:0 | Gamma_table G18 value. | |
| **34h** | **Gamma_G19** | **7:0** | **Default : 0d151** | **Access : R/W** |
| | Gamma_G49 | 7:0 | Gamma_table G19 value. | |
| **35h** | **Gamma_G20** | **7:0** | **Default : 0d159** | **Access : R/W** |
| | Gamma_G20 | 7:0 | Gamma_table G20 value. | |
| **36h** | **Gamma_G21** | **7:0** | **Default : 0d167** | **Access : R/W** |
| | Gamma_G21 | 7:0 | Gamma_table G21 value. | |
| **37h** | **Gamma_G22** | **7:0** | **Default : 0d175** | **Access : R/W** |
| | Gamma_G22 | 7:0 | Gamma_table G22 value. | |
| **38h** | **Gamma_G23** | **7:0** | **Default : 0d183** | **Access : R/W** |
| | Gamma_G23 | 7:0 | Gamma_table G23 value. | |
| **39h** | **Gamma_G24** | **7:0** | **Default : 0d191** | **Access : R/W** |
| | Gamma_G24 | 7:0 | Gamma_table G24 value. | |
| **3Ah** | **Gamma_G25** | **7:0** | **Default : 0d199** | **Access : R/W** |
| | Gamma_G25 | 7:0 | Gamma_table G25 value. | |
| **3Bh** | **Gamma_G26** | **7:0** | **Default : 0d207** | **Access : R/W** |
| | Gamma_G26 | 7:0 | Gamma_table G26 value. | |
| **3Ch** | **Gamma_G27** | **7:0** | **Default : 0d215** | **Access : R/W** |
| | Gamma_G27 | 7:0 | Gamma_table G27 value. | |
| **3Dh** | **Gamma_G28** | **7:0** | **Default : 0d223** | **Access : R/W** |
| | Gamma_G28 | 7:0 | Gamma_table G28 value. | |
| **3Eh** | **Gamma_G29** | **7:0** | **Default : 0d232** | **Access : R/W** |
| | Gamma_G29 | 7:0 | Gamma_table G29 value. | |
| **3Fh** | **Gamma_G30** | **7:0** | **Default : 0d239** | **Access : R/W** |
| | Gamma_G30 | 7:0 | Gamma_table G30 value. | |
| **40h** | **Gamma_G31** | **7:0** | **Default : 0d247** | **Access : R/W** |
| | Gamma_G31 | 7:0 | Gamma_table G31 value. | |
| **41h** | **Gamma_G32** | **7:0** | **Default : 0d255** | **Access : R/W** |

| Gamma Register (Indirect mapping to Bank 00, Registers 91h/92h) | | | | |
|---|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** | |
| | Gamma_G32 | 7:0 | Gamma_table G32 value. | |
| **42h** | **Gamma_B00** | **7:0** | **Default : 0d00** | **Access : R/W** |
| | Gamma_B00 | 7:0 | Gamma_table B00 value. | |
| **43h** | **Gamma_B01** | **7:0** | **Default : 0d07** | **Access : R/W** |
| | Gamma_B01 | 7:0 | Gamma_table B01 value. | |
| **44h** | **Gamma_B02** | **7:0** | **Default : 0d15** | **Access : R/W** |
| | Gamma_B02 | 7:0 | Gamma_table B02 value. | |
| **45h** | **Gamma_B03** | **7:0** | **Default : 0d23** | **Access : R/W** |
| | Gamma_B03 | 7:0 | Gamma_table B03 value. | |
| **46h** | **Gamma_B04** | **7:0** | **Default : 0d31** | **Access : R/W** |
| | Gamma_B04 | 7:0 | Gamma_table B04 value. | |
| **47h** | **Gamma_B05** | **7:0** | **Default : 0d39** | **Access : R/W** |
| | Gamma_B05 | 7:0 | Gamma_table B05 value. | |
| **48h** | **Gamma_B06** | **7:0** | **Default : 0d47** | **Access : R/W** |
| | Gamma_B06 | 7:0 | Gamma_table B06 value. | |
| **49h** | **Gamma_B07** | **7:0** | **Default : 0d55** | **Access : R/W** |
| | Gamma_B07 | 7:0 | Gamma_table B07 value. | |
| **4Ah** | **Gamma_B08** | **7:0** | **Default : 0d63** | **Access : R/W** |
| | Gamma_B08 | 7:0 | Gamma_table B08 value. | |
| **4Bh** | **Gamma_B09** | **7:0** | **Default : 0d71** | **Access : R/W** |
| | Gamma_B09 | 7:0 | Gamma_table B09 value. | |
| **4Ch** | **Gamma_B10** | **7:0** | **Default : 0d79** | **Access : R/W** |
| | Gamma_B10 | 7:0 | Gamma_table B10 value. | |
| **4Dh** | **Gamma_B11** | **7:0** | **Default : 0d87** | **Access : R/W** |
| | Gamma_B11 | 7:0 | Gamma_table B11 value. | |
| **4Eh** | **Gamma_B12** | **7:0** | **Default : 0d95** | **Access : R/W** |
| | Gamma_B12 | 7:0 | Gamma_table B12 value. | |
| **4Fh** | **Gamma_B13** | **7:0** | **Default : 0d103** | **Access : R/W** |
| | Gamma_B13 | 7:0 | Gamma_table B13 value. | |
| **50h** | **Gamma_B14** | **7:0** | **Default : 0d111** | **Access : R/W** |
| | Gamma_B14 | 7:0 | Gamma_table B14 value. | |
| **51h** | **Gamma_B15** | **7:0** | **Default : 0d119** | **Access : R/W** |
| | Gamma_B15 | 7:0 | Gamma_table B15 value. | |

| Gamma Register (Indirect mapping to Bank 00, Registers 91h/92h) | | | | |
|---|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** | |
| **52h** | **Gamma_B16** | **7:0** | **Default : 0d127** | **Access : R/W** |
| | Gamma_B16 | 7:0 | Gamma_table B16 value. | |
| **53h** | **Gamma_B17** | **7:0** | **Default : 0d135** | **Access : R/W** |
| | Gamma_B17 | 7:0 | Gamma_table B17 value. | |
| **54h** | **Gamma_B18** | **7:0** | **Default : 0d143** | **Access : R/W** |
| | Gamma_B18 | 7:0 | Gamma_table B18 value. | |
| **55h** | **Gamma_B19** | **7:0** | **Default : 0d151** | **Access : R/W** |
| | Gamma_B49 | 7:0 | Gamma_table B19 value. | |
| **56h** | **Gamma_B20** | **7:0** | **Default : 0d159** | **Access : R/W** |
| | Gamma_B20 | 7:0 | Gamma_table B20 value. | |
| **57h** | **Gamma_B21** | **7:0** | **Default : 0d167** | **Access : R/W** |
| | Gamma_B21 | 7:0 | Gamma_table B21 value. | |
| **58h** | **Gamma_B22** | **7:0** | **Default : 0d175** | **Access : R/W** |
| | Gamma_B22 | 7:0 | Gamma_table B22 value. | |
| **59h** | **Gamma_B23** | **7:0** | **Default : 0d183** | **Access : R/W** |
| | Gamma_B23 | 7:0 | Gamma_table B23 value. | |
| **5Ah** | **Gamma_B24** | **7:0** | **Default : 0d191** | **Access : R/W** |
| | Gamma_B24 | 7:0 | Gamma_table B24 value. | |
| **5Bh** | **Gamma_B25** | **7:0** | **Default : 0d199** | **Access : R/W** |
| | Gamma_B25 | 7:0 | Gamma_table B25 value. | |
| **5Ch** | **Gamma_B26** | **7:0** | **Default : 0d207** | **Access : R/W** |
| | Gamma_B26 | 7:0 | Gamma_table B26 value. | |
| **5Dh** | **Gamma_B27** | **7:0** | **Default : 0d215** | **Access : R/W** |
| | Gamma_B27 | 7:0 | Gamma_table B27 value. | |
| **5Eh** | **Gamma_B28** | **7:0** | **Default : 0d223** | **Access : R/W** |
| | Gamma_B28 | 7:0 | Gamma_table B28 value. | |
| **5Fh** | **Gamma_B29** | **7:0** | **Default : 0d232** | **Access : R/W** |
| | Gamma_B29 | 7:0 | Gamma_table B29 value. | |
| **60h** | **Gamma_B30** | **7:0** | **Default : 0d239** | **Access : R/W** |
| | Gamma_B30 | 7:0 | Gamma_table B30 value. | |
| **61h** | **Gamma_B31** | **7:0** | **Default : 0d247** | **Access : R/W** |
| | Gamma_B31 | 7:0 | Gamma_table B31 value. | |
| **62h** | **Gamma_B32** | **7:0** | **Default : 0d255** | **Access : R/W** |

| Gamma Register (Indirect mapping to Bank 00, Registers 91h/92h) | | | |
|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** |
| | Gamma_B32 | 7:0 | Gamma_table B32 value. |

## Scaler Register (Bank = 00, Registers B0h ~ FFh)

| Scaler Register (Bank=00, Registers B0h ~ FFh) | | | | |
|---|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** | |
| **B0h** | **LINE_SHIFT** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | SEL_V_CLR | 6 | Select Vcounter Clear by DOWNCNT_EQ1 or EARLY_VS. | |
| | - | 5 | Reserved. | |
| | VCR_FF_MODE | 4 | Enable output VSYNC follow input VSYNC mode. | |
| | FIELD_INV_VS | 3 | Line shift vs Field Inverse. | |
| | LINE_SHIFT_NUM[2:0] | 2:0 | Line Shift Numbers. | |
| **B1h** | **SYNC_CONTROL** | **7:0** | **Default : 0x08** | **Access : R/W** |
| | CLK_DLY[3:0] | 7:4 | Output clock delay select. | |
| | CLK_INV | 3 | Output Clock invert enable. | |
| | DE_INV | 2 | Output DE Invert enable. | |
| | VS_INV | 1 | Output VSYNC Invert enable. | |
| | HS_INV | 0 | Output HSYNC Invert enable. | |
| **B2h** | **SYNC_SEL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | **-** | 7:4 | Reserved. | |
| | SEL_VDE | 3 | Select VDE output to VSYNC pin. | |
| | SEL_HDE | 2 | Select HDE output to HSYNC pin. | |
| | DATA_SKEW | 1:0 | Bus data Skew select. | |
| **B3h** | **SVM_CLK** | **7:0** | **Default : 0x10** | **Access : R/W** |
| | **-** | 7 | Reserved. | |
| | GB_SWAP | 6 | Data Bus G, B Swap. | |
| | RG_SWAP | 5 | Data Bus R, G Swap. | |
| | SVM_CLK_INV | 4 | SVM Clock Inverse. | |
| | SVM_CLKDLY | 3:0 | SVM Clock delay select. | |
| **B4h ~ BFh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **C0h** | **HSPRDL_L** | **7:0** | **Default : -** | **Access : RO** |
| | HSPRDL[7:0] | 7:0 | Number of system clock count at 512 HSYNCs. | |
| **C1h** | **HSPRDL_M** | **7:0** | **Default : -** | **Access : RO** |
| | HSPRDL[15:8] | 7:0 | Number of system clock count at 512 HSYNCs. | |
| **C2h** | **HSPRDL_H** | **7:0** | **Default : -** | **Access : RO** |
| | HSPRDL[23:16] | 7:0 | Number of system clock count at 512 HSYNCs. | |

| Scaler Register (Bank=00, Registers B0h ~ FFh) | | | | |
|---|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** | |
| **C3h** | **YCDLYCTL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | LNBF4_MD | 7 | Four Line Buffer Mode. | |
| | VSD_PIPE | 6 | VSD Pipe select.<br>0: Original.<br>1: Early pipe 2 cycle. | |
| | - | 5:3 | Reserved. | |
| | YC_DLY_CTL | 2:0 | YC Delay Control.<br>000: Normal.<br>001: Y early 1 cycle.<br>010: Y early 2 cycles.<br>011: Y early 3 cycles.<br>100: Normal.<br>101: C early 1 cycle.<br>110: C early 2 cycles.<br>111: C early 3 cycles. | |
| **C4h** | **VTOTAL_MAX_L** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | TOTAL_MAX[7:0] | 7:0 | Vertical Max Total (lower 8 bits). | |
| **C5h** | **VTOTAL_MAX_H** | **7:0** | **Default : 0x07** | **Access : R/W** |
| | **-** | 7:3 | Reserved. | |
| | TOTAL_MAX[10:8] | 2:0 | Vertical Max Total (higher 3 bits). | |
| **C6h ~ C7h** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **C8h** | **ATGCTRL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | MAXR (RO) | 7 | Max value flag for Red channel (read only).<br>0: Normal.<br>1: Max value (255) value when AGR = 0.<br>Output over max value (255) when AGR = 1. | |
| | MAXG (RO) | 6 | Max value flag for Green channel (read only).<br>0: Normal.<br>1: Max value (255) value when AGR = 0.<br>Output over max value (255) when AGR = 1. | |
| | MAXB (RO) | 5 | Max value flag for Blue channel (read only).<br>0: Normal.<br>1: Max value (255) value when AGR = 0.<br>Output over max value (255) when AGR = 1. | |

| Scaler Register (Bank=00, Registers B0h ~ FFh) | | | | |
|---|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** | |
| | AC_EN | 4 | ADC Calibration Enable.<br>0: Disable.<br>1: Enable. | |
| | AGR | 3 | Auto Gain Result selection.<br>0: Output has max/min value.<br>1: Output is overflow/underflow. | |
| | ATGM | 2 | Auto Gain Mode.<br>0: Normal mode (result will be cleared every frame).<br>1: History mode (result remains not cleared till ATGE = 0). | |
| | ATGR (RO) | 1 | Auto Gain Result Ready.<br>0: Result not ready.<br>1: Result ready. | |
| | ATGE | 0 | Auto Gain Function Enable.<br>0: Disable.<br>1: Enable. | |
| **C9h** | **ATGST** | **7:0** | **Default : -** | **Access : R/W** |
| | VCLP | 7 | Video auto gain mode.<br>0: RGB mode.<br>1: YPbPr Mode. | |
| | - | 6 | Reserved. | |
| | CALR (RO) | 5 | Calibration value flag for Red channel.<br>0: Normal.<br>1: Calibration result (needs to increase offset) when ACE=1. | |
| | CALG (RO) | 4 | Calibration value flag for Green channel.<br>0: Normal.<br>1: Calibration result (needs to increase offset) when ACE=1. | |
| | CALB (RO) | 3 | Calibration value flag for Blue channel.<br>0: Normal.<br>1: Calibration result (needs to increase offset) when ACE=1. | |
| | MINR (RO) | 2 | Min value flag for Red channel.<br>0: Normal.<br>1: Min value (0) present when AGR = 0, ACE = 0.<br>Output under min value (0) when AGR = 1, ACE = 0.<br>Calibration result (needs to decrease offset) when ACE = 1. | |

| Scaler Register (Bank=00, Registers B0h ~ FFh) | | | | |
|---|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** | |
| | MING (RO) | 1 | Min value flag for Green channel.<br>0: Normal.<br>1: Min value (0) present when AGR = 0, ACE = 0.<br>Output under min value (0) when AGR = 1, ACE = 0.<br>Calibration result (needs to decrease offset) when ACE = 1. | |
| | MINB (RO) | 0 | Min value flag for Blue channel.<br>0: Normal.<br>1: Min value (0) present when AGR = 0, ACE = 0.<br>Output under min value (0) when AGR = 1, ACE = 0.<br>Calibration result (needs to decrease offset) when ACE = 1. | |
| **CAh** | **ATFCHSEL** | **7:0** | **Default: 0x00** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | ATPCHSEL[1:0] | 5:4 | Auto Phase R/G/B channel select<br>00: R/G/B 3 channels<br>01: only R channel<br>10: only G channel<br>11: only B channel | |
| | - | 3 | Reserved. | |
| | ATGCHSEL[2:0] | 2:0 | Auto Gain R/G/B channel min/max value select.<br>000: R min value<br>001: G min value<br>010: B min value<br>011: R max value<br>100: G max value<br>101: B max value<br>11x: Reserved | |
| **CBh** | **ATOCTRL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | JITLR | 7 | Jitter function Left / Right result for 86h and 87h.<br>0: Left result.<br>1: right result. | |
| | JITS | 6 | Jitter Software clear.<br>0: Not clear.<br>1: Clear. | |
| | - | 5 | Reserved. | |
| | JITM | 4 | Jitter function Mode.<br>0: Update every frame.<br>1: Keep the history value. | |

| Scaler Register (Bank=00, Registers B0h ~ FFh) | | | | |
|---|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** | |
| | JITR | 3 | Jitter function Result (Read Only).<br>0: No jitter.<br>1: Jitter present. | |
| | ATOM | 2 | Auto position function Mode.<br>0: Update every frame.<br>1: Keep the history value. | |
| | ATOR | 1 | Auto position result Ready (Read Only).<br>0: Result ready.<br>1: Result not ready. | |
| | ATOE | 0 | Auto position function Enable.<br>0: Disable.<br>1: Enable.<br>Disable-to-enable needs at least 2 frame apart for ready bit to settle. | |
| **CCh** | **AOVDV** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | AOVDV[3:0] | 7:4 | Auto position Valid Data Value.<br>0000: Valid if data >= 0000 0000.<br>0001: Valid if data >= 0001 0000.<br>0010: Valid if data >= 0010 0000.<br>... ...<br>1111: Valid if data >= 1111 0000. | |
| | - | 3:0 | Reserved. | |
| **CDh** | **ATGVALUE (RO)** | **7:0** | **Default: -** | **Access : RO** |
| | ATGVALUE[7:0] | 7:0 | Auto Gain result based on 7Ah[2:0]. | |
| **CEh** | **AOVST-L (RO)** | **7:0** | **Default : -** | **Access : RO** |
| | AOVST [7:0] | 7:0 | Auto position detected result Vertical Starting point. | |
| **CFh** | **AOVST-H (RO)** | **7:0** | **Default : -** | **Access : RO** |
| | - | 7:3 | Reserved. | |
| | AOVST[10:8] | 2:0 | See description for AOVST [7:0]. | |
| **D0h** | **AOHST-L (RO)** | **7:0** | **Default : -** | **Access : RO** |
| | AOHST[7:0] | 7:0 | Auto position detected result Horizontal Starting point. | |
| **D1h** | **AOHST-H (RO)** | **7:0** | **Default : -** | **Access : DB** |
| | - | 7:3 | Reserved. | |
| | SPRGST[10:8] | 2:0 | Image horizontal sample start point, count by input dot clock. | |
| **D2h** | **AOVEND-L (RO)** | **7:0** | **Default : -** | **Access : RO** |
| | AOVEND[7:0] | 7:0 | Auto position detected result Vertical End point. | |

## Scaler Register (Bank=00, Registers B0h ~ FFh)

| Index | Mnemonic | Bits | Description | |
|---|---|---|---|---|
| **D3h** | **AOVEND-H (RO)** | **7:0** | **Default : -** | **Access : RO** |
| | - | 7:3 | Reserved. | |
| | AOVEND[10:8] | 2:0 | See description for AOVEND[7:0]. | |
| **D4h** | **AOHEND-L (RO)** | **7:0** | **Default : -** | **Access : RO** |
| | AOHEND[7:0] | 7:0 | Auto position detected result Horizontal End point. | |
| **D5h** | **AOHEND-H (RO)** | **7:0** | **Default : -** | **Access : RO** |
| | - | 7:4 | Reserved. | |
| | AOHEND[11:8] | 2:0 | See description for AOHEND[7:0]. | |
| **D6h** | **JLR-L (RO)** | **7:0** | **Default : -** | **Access : RO** |
| | JLR[7:0] | 7:0 | Jitter function detected Left/Right most point state (previous frame) depend on Reg_7Bh[7]. | |
| **D7h** | **JLR-H (RO)** | **7:0** | **Default : -** | **Access : RO** |
| | - | 7:3 | Reserved. | |
| | JLR[10:8] | 2:0 | See description for JLR[7:0]. | |
| **D8h** | **ANRF** | **7:0** | **Default : -** | **Access : RO** |
| | - | 7:6 | Reserved. | |
| | HNEN | 5 | High level Noise reduction Enable.<br>0: Disable.<br>1: Enable. | |
| | BGEN | 4 | Background Noise reduction Enable.<br>0: Disable.<br>1: Enable. | |
| | - | 3 | Reserved. | |
| | ANLV[2:0] | 2:0 | Auto Noise Level,<br>000: Noise level = 1,<br>001: Noise level = 2,<br>010: Noise level = 4,<br>011: Noise level = 8,<br>100: Noise level = 9,<br>101: Noise level = 10,<br>110: Noise level = 12,<br>111: Noise level = 16. | |
| **D9h** | **ATPGTH** | **7:0** | **Default : 0x01** | **Access : R/W** |
| | ATPGTH[7:0] | 7:0 | Auto Phase Gray scale Threshold for ATPV3 when ATPN4 = 0. | |
| **DAh** | **ATPTTH** | **7:0** | **Default : 0x10** | **Access : R/W** |

| Scaler Register (Bank=00, Registers B0h ~ FFh) | | | | |
|---|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** | |
| | ATPTTH[7:0] | 7:0 | Auto Phase Text Threshold for ATPV4. | |
| **DBh** | **ATPCTRL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | ATP_FLTRMD | 7 | 0: Disable auto-position filter mode.<br>1: Enable auto-position filter mode. | |
| | GRY (RO) | 6 | Gray scale detect (read only). | |
| | TXT (RO) | 5 | Text detect (read only). | |
| | APMASK[2:0] | 4:2 | Nose Mask.<br>000: Mask 0 bit, default value.<br>001: Mask 1 bit.<br>010: Mask 2 bit.<br>011: Mask 3 bit.<br>100: Mask 4 bit.<br>101: Mask 5 bit.<br>110: Mask 6 bit.<br>111: Mask 7 bit. | |
| | ATPR (RO) | 1 | Auto Phase Result ready.<br>0: Result not ready.<br>1: Result ready. | |
| | ATPE | 0 | Auto Phase function Enable.<br>0: Disable.<br>1: Enable. | |
| **DCh** | **ATPV1 (RO)** | **7:0** | **Default : -** | **Access : RO** |
| | ATPVALUE[7:0] | 7:0 | Auto Phase Value. | |
| **DDh** | **ATPV2 (RO)** | **7:0** | **Default : -** | **Access : RO** |
| | ATPVALUE[15:8] | 7:0 | See description for ATPVALUE[7:0]. | |
| **DEh** | **ATPV3 (RO)** | **7:0** | **Default : -** | **Access : RO** |
| | ATPVALUE[23:16] | 7:0 | See description for ATPVALUE[7:0]. | |
| **DFh** | **ATPV4 (RO)** | **7:0** | **Default : -** | **Access : RO** |
| | ATPVALUE[31:24] | 7:0 | See description for ATPVALUE[7:0]. | |
| **E0h** | **PDMD0** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | GCLK[1:0] | 7:6 | Gated Clock for SRAM.<br>00: Normal.<br>01: V Blank.<br>10: H Blank and V Blank.<br>11: Reserved. | |

| Scaler Register (Bank=00, Registers B0h ~ FFh) | | | | |
|---|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** | |
| | AUXCLK_GAT | 5 | 0: Enable MVD MCU-support Clock.<br>1: Disable MVD MCU-support Clock. | |
| | CMBCLK_GAT | 4 | 0: Enable MVD comb-filter Clock.<br>1: Disable MVD comb-filter Clock. | |
| | - | 3 | Reserved. | |
| | EOCLK_INV | 2 | External OSD sample Clock Inverting. | |
| | IDCLK_INV | 1 | Scaler input sample Clock Inverting. | |
| | FSCCLK_INV | 0 | Sub-carrier Clock Inverting. | |
| **E1h** | **PDMD1** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | PDALL | 7 | All chip power down. | |
| | BIUCLK_GAT | 6 | 0: Enable register interface clock.<br>1: Disable register interface clock. | |
| | OSDCLK_GAT | 5 | 0: Enable OSD clock.<br>1: Disable OSD clock. | |
| | PCCLK_GAT | 4 | 0: Enable CRT output suppot clock.<br>1: Disable CRT output suppot clock. | |
| | ADCCLK_GAT | 3 | 0: Enable 3-channel ADC digital clock.<br>1: Disable 3-channel ADC digital clock. | |
| | VDCLK_GAT | 2 | 0: Enable CCIR and MVD interface clock.<br>1: Disable CCIR and MVD interface clock. | |
| | IDCLK_GAT | 1 | 0: Enable scaler clock.<br>1: Disable scaler clock. | |
| | FSCCLK_GAT | 0 | 0: Enable MVD digital front-end clock.<br>1: Disable MVD digital front-end clock. | |
| **E2h** | **SWRST0** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | REGR | 7 | Register Reset.<br>0: Normal operation.<br>1: Reset Register. | |
| | ADCR | 6 | ADC Reset.<br>0: Normal operation.<br>1: Reset ADC. | |
| | IPR | 5 | Digital Input Port Reset.<br>0: Normal operation.<br>1: Reset. | |
| | OP1R | 4 | Scaler Reset.<br>0: Normal operation.<br>1: Reset. | |

| Scaler Register (Bank=00, Registers B0h ~ FFh) | | | | |
|---|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** | |
| | OP2R | 3 | Display Port Reset.<br>0: Normal operation.<br>1: Reset. | |
| | - | 2 | Reserved. | |
| | OSDR | 1 | Internal OSD Reset.<br>0: Normal operation.<br>1: Reset internal OSD. | |
| | SWR | 0 | Software Reset (reset All digital core except system registers).<br>0: Normal operation.<br>1: Reset. | |
| **E3h** | **SWRST1** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | VFER | 7 | Video Decoder Front End Reset.<br>0: Normal operation.<br>1: Reset. | |
| | VCFR | 6 | Video Decoder Comb Filter Reset.<br>0: Normal operation.<br>1: Reset. | |
| | MCUR | 5 | Embedded MCU Reset.<br>0: Normal operation.<br>1: Reset. | |
| | MCUR | 4 | GMC digital tune Reset.<br>0: Normal operation.<br>1: Reset. | |
| | - | 3:0 | Reserved. | |
| **E4h** | **ISOVRD** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | SL | 7 | Shift Line.<br>0: Shift line method 0.<br>1: Shift line method 1 for interlace mode. | |
| | CSHS | 6 | HSYNC in coast.<br>0: HSYOUT (recommended).<br>1: Re-shaped HSYNC. | |
| | UVSP | 5 | User defined input VSYNC Polarity, active when IVSJ =1.<br>0: Active low.<br>1: Active high. | |
| | IVSJ | 4 | Input VSYNC polarity judgment.<br>0: Use result of internal circuit detection.<br>1: Defined by user (UVSP). | |

| Scaler Register (Bank=00, Registers B0h ~ FFh) | | | | |
|---|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** | |
| | UHSP | 3 | User defined input HSYNC Polarity, active when IVSJ =1.<br>0: Active low.<br>1: Active high. | |
| | IHSJ | 2 | Input HSYNC polarity judgment.<br>0: Use result of internal circuit detection.<br>1: Defined by user (UHSP). | |
| | UINT | 1 | User defined non-interlace/interlace, active when INTJ = 1.<br>0: Non-interlace.<br>1: Interlace. | |
| | INTJ | 0 | Interlace judgment.<br>0: Use result of internal circuit detection.<br>1: Defined by user (UINT). | |
| **E5h** | **MDCTRL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | IP_TEST_MD | 7:6 | IP Test-bus selection. | |
| | VERR | 5 | Video CCIR656 Error correct.<br>0: Disable.<br>1: Enable. | |
| | Field_ABSMD | 4 | Field Postion Absolute Value Mode. | |
| | VFIV | 3 | Video Field Inversion.<br>0: Normal.<br>1: Invert. | |
| | VEXF | 2 | Video External Field.<br>0: Use result of internal circuit detection.<br>1: Use external field. | |
| | INTF | 1 | Interlace Field detect method select.<br>0: Use the HSYNC numbers of a field to judge.<br>1: Use the relationship of VSYNC and HSYNC to judge. | |
| | IFI | 0 | Interlace Field Inverting.<br>0: Normal.<br>1: Invert. | |
| **E6h** | **HSPW (RO)** | **7:0** | **Default : -** | **Access : RO** |
| | HS_PW | 7:0 | HS Pulse Width | |
| **E7h** | **VFREE** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | AUTOOPCOAST_CLR | 7 | Set Auto-Coast-for-output status. | |
| | AUTOOPCOAST | 6 | Enable Auto-Coast-for-output. | |
| | MIN_VTT[5:0] | 5:0 | Minimum VTT to free-run. | |
| **E8h** | **HSTOL** | **7:0** | **Default : 0x05** | **Access : R/W** |

| Scaler Register (Bank=00, Registers B0h ~ FFh) | | | | |
|---|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** | |
| | VS2HS (RO) | 7 | Input VSYNC too close to input HSYNC. | |
| | LN4_DETMD | 6 | 4 Line Detect Mode for Hs, DE. | |
| | HSTOL[5:0] | 5:0 | HSYNC Tolerance.<br>5: Default value. | |
| **E9h** | **VSTOL** | **7:0** | **Default : 0x01** | **Access : R/W** |
| | AUTONOSIGNAL_CLR | 7 | Set Auto-No-Signal status. | |
| | AUTONOSIGNAL | 6 | Enable Auto-No-Signal function. | |
| | HTT_FILTERMD | 5 | HTT Filter Mode. | |
| | HVTT_LOSE_MD | 4 | HVTT Lose Mode.<br>0: Original.<br>1: New by WDT sample. | |
| | VS_TOL[3:0] | 3:0 | VSYNC Tolerance.<br>1: Default value. | |
| **EAh** | **HSPRD_L** | **7:0** | **Default : -** | **Access : RO** |
| | HSPRD[7:0] | 7:0 | Input Horizontal Period, count by reference clock. | |
| **EBh** | **HSPRD_H** | **7:0** | **Default : -** | **Access : RO** |
| | - | 7:5 | Reserved. | |
| | HSPRD[12:8] | 4:0 | See description for HSPRD[7:0]. | |
| **ECh** | **VTOTAL_L** | **7:0** | **Default : -** | **Access : RO** |
| | VTOTAL[7:0] | 7:0 | Input Vertical Total Length, count by HSYNC. | |
| **EDh** | **VTOTAL_H** | **7:0** | **Default : -** | **Access : RO** |
| | - | 7:3 | Reserved. | |
| | VTOTAL[10:8] | 2:0 | See description for VTOTAL[7:0]. | |
| **EEh** | **PDMD2** | **7:0** | **Default : 0x60** | **Access : RW** |
| | MCUCLK_SEL | 7 | MCU Clock Source Select.<br>0: XTAL.<br>1: MPLL divided. | |
| | MCUDIV | 6:4 | MCU Clock divided by MPLL.<br>000: 4.<br>001: 6.<br>010: 8.<br>011: 10.<br>100: 12.<br>101: 14.<br>110: 16. | |
| | - | 3:1 | Reserved. | |

| Scaler Register (Bank=00, Registers B0h ~ FFh) | | | | |
|---|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** | |
| | CC_GAT | 0 | Comb Clock Gating.<br>1: Gating mode.<br>0: No gating. | |
| **EFh** | **STATUS2 (RO)** | **7:0** | **Default : -** | **Access : RO** |
| | HTT_CHG_CS | 7 | Htotal change in CSOG. | |
| | - | 6 | Reserved. | |
| | STD_PAL | 5 | 0: NTSC.<br>1: PAL. | |
| | CSD | 4 | CSYNC Detected status.<br>0: Input is not CSYNC.<br>1: Input is detected as CSYNC. | |
| | INTM | 3 | Interlace / Non-interlace detecting result by this chip.<br>0: Non-interlace.<br>1: Interlace. | |
| | INTF | 2 | Input odd/even Field detecting result by this chip.<br>0: Even.<br>1: Odd. | |
| | IHSP | 1 | Incoming input HSYNC Polarity detecting result by this chip.<br>0: Active low.<br>1: Active high. | |
| | IVSP | 0 | Incoming input VSYNC Polarity detecting result by this chip.<br>0: Active low.<br>1: Active high. | |
| **F0h** | **CHIP_ID** | **7:0** | **Default : 0x00** | **Access : RO** |
| | CHIP_ID[7:0] | 7:0 | Chip id is 70h | |
| **F1h** | **CHIP_VERSION** | **7:0** | **Default : 0x01** | **Access : RO** |
| | CHIP_VER[7:0] | 7:0 | Version is 01h | |
| **F2h ~ F3h** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **F4h** | **TRISTATE** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | OBBUS_TRI | 4 | Output bus Tristate. | |
| | VS_TRI | 3 | Output VSYNC Tristate. | |
| | HSY_TRI | 2 | Output HSYNC Tristate. | |
| | DE_TRI | 1 | Output DE Tristate. | |

| Scaler Register (Bank=00, Registers B0h ~ FFh) | | | | |
|---|---|---|---|---|
| **Index** | **Mnemonic** | **Bits** | **Description** | |
| | CLK_TRI | 0 | Output CLK Tristate. | |
| **F7h ~ FFh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |

## Analog Register (Bank = 01)

| Analog Register (Bank = 01) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| **01h ~ 4Fh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **50h** | **LPF_TAP1** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | ROUND_SEL | 7:6 | Round Select. | |
| | LPFTAP_1[5:0] | 5:0 | LPF Coefficient 1.<br>(2's complement: -32 ~ 31) | |
| **51h** | **LPF_TAP2** | **7:0** | **Default : 0x 00** | **Access : R/W** |
| | VSD_DITH | 7 | VSD Dither method. | |
| | VSD_SEED_SEL | 6 | VSD Dither Seed Select. | |
| | LPFTAP_2[5:0] | 5:0 | LPF Coefficient 2. | |
| **52h** | **LPF_TAP3** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | VSD_ROUND_EN | 7 | VSD Rounding Enable. | |
| | SEED_SEL | 6 | LPF Dither Seed Select. | |
| | LPFTAP_3[5:0] | 5:0 | LPF Coefficient 3. | |
| **53h** | **LPF_TAP4** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CSC_DITH_EN | 7 | CSC Dither Enable. | |
| | CSC_SEED_SEL | 6 | CSC Dither Seed Select. | |
| | LPFTAP_4[5:0] | 5:0 | LPF Coefficient 4. | |
| **54h** | **LPF_TAP5** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | LPFTAP_5[5:0] | 5:0 | LPF Coefficient 5. | |
| **55h** | **LPF_CTL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CSC_EN | 7 | CSC Enable.<br>0: Disable.<br>1: Enable. | |
| | LPFTAP_EN | 6 | LPFTAP Enable.<br>0: Disable.<br>1: Enable. | |
| **56h** | **FCC_CB_1T** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | FCC_CB_1T[7:0] | 7:0 | FCC Cb 1T. | |
| **57h** | **FCC_CR_1T** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | FCC_CR_1T[7:0] | 7:0 | FCC Cr 1T. | |
| **58h** | **FCC_CB_2T** | **7:0** | **Default : 0x00** | **Access : R/W** |

## Analog Register (Bank = 01)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | FCC_CB_2T[7:0] | 7:0 | FCC Cb 2T. | |
| 59h | **FCC_CR_2T** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | FCC_CR_2T[7:0] | 7:0 | FCC Cr 2T. | |
| 5Ah | **FCC_CB_3T** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | FCC_CB_3T[7:0] | 7:0 | FCC Cb 3T. | |
| 5Bh | **FCC_CR_3T** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | FCC_CR_3T[7:0] | 7:0 | FCC Cr 3T. | |
| 5Ch | **FCC_CB_4T** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | FCC_CB_4T[7:0] | 7:0 | FCC Cb 4T. | |
| 5Dh | **FCC_CR_4T** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | FCC_CR_4T[7:0] | 7:0 | FCC Cr 4T. | |
| 5Eh | **FCC_CB_5T** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | FCC_CB_5T[7:0] | 7:0 | FCC Cb 5T. | |
| 5Fh | **FCC_CR_5T** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | FCC_CR_5T[7:0] | 7:0 | FCC Cr 5T. | |
| 60h | **FCC_CB_6T** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | FCC_CB_6T[7:0] | 7:0 | FCC Cb 6T. | |
| 61h | **FCC_CR_6T** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | FCC_CR_6T[7:0] | 7:0 | FCC Cr 6T. | |
| 62h | **FCC_CB_7T** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | FCC_CB_7T[7:0] | 7:0 | FCC Cb 7T. | |
| 63h | **FCC_CR_7T** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | FCC_CR_7T[7:0] | 7:0 | FCC Cr 7T. | |
| 64h | **FCC_CB_8T** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | FCC_CB_8T[7:0] | 7:0 | FCC Cb 8T. | |
| 65h | **FCC_CR_8T** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | FCC_CR_8T[7:0] | 7:0 | FCC Cr 8T. | |
| 66h | **WHITE_SLOP** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | WHITE_SLOP[7:0] | 7:0 | White contrast adjust slope.<br>>80h : slope >1.<br>=80h : slope=1.<br><80h : slop <1. | |
| 67h | **BLACK_SLOP** | **7:0** | **Default : 0x80** | **Access : R/W** |

## Analog Register (Bank = 01)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | BLACK_SLOP [7:0] | 7:0 | Black contrast adjust slope.<br>>80h : slope >1.<br>=80h : slope=1.<br><80h : slop <1. | |
| **68h** | **FCC_WIN1** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CB_D1U[1:0] | 7:6 | Cb D1U. | |
| | CB_D1D[1:0] | 5:4 | Cb D1D. | |
| | CR_D1U[1:0] | 3:2 | Cr D1U. | |
| | CR_D1D[1:0] | 1:0 | Cr D1D. | |
| **69h** | **FCC_WIN2** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CB_D2U[1:0] | 7:6 | Cb D2U. | |
| | CB_D2D[1:0] | 5:4 | Cb D2D. | |
| | CR_D2U[1:0] | 3:2 | Cr D2U. | |
| | CR_D2D[1:0] | 1:0 | Cr D2D. | |
| **6Ah** | **FCC_WIN3** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CB_D3U[1:0] | 7:6 | Cb D3U. | |
| | CB_D3D[1:0] | 5:4 | Cb D3D. | |
| | CR_D3U[1:0] | 3:2 | Cr D3U. | |
| | CR_D3D[1:0] | 1:0 | Cr D3D. | |
| **6Bh** | **FCC_WIN4** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CB_D4U[1:0] | 7:6 | Cb D4U. | |
| | CB_D4D[1:0] | 5:4 | Cb D4D. | |
| | CR_D4U[1:0] | 3:2 | Cr D4U. | |
| | CR_D4D[1:0] | 1:0 | Cr D4D. | |
| **6Ch** | **FCC_WIN5** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CB_D5U[1:0] | 7:6 | Cb D5U. | |
| | CB_D5D[1:0] | 5:4 | Cb D5D. | |
| | CR_D5U[1:0] | 3:2 | Cr D5U. | |
| | CR_D5D[1:0] | 1:0 | Cr D5D. | |
| **6Dh** | **FCC_WIN6** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CB_D6U[1:0] | 7:6 | Cb D6U. | |
| | CB_D6D[1:0] | 5:4 | Cb D6D. | |
| | CR_D6U[1:0] | 3:2 | Cr D6U. | |
| | CR_D6D[1:0] | 1:0 | Cr D6D. | |

## Analog Register (Bank = 01)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| **6Eh** | **FCC_WIN7** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CB_D7U[1:0] | 7:6 | Cb D7U. | |
| | CB_D7D[1:0] | 5:4 | Cb D7D. | |
| | CR_D7U[1:0] | 3:2 | Cr D7U. | |
| | CR_D7D[1:0] | 1:0 | Cr D7D. | |
| **6Fh** | **FCC_WIN8** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CB_D8U[1:0] | 7:6 | Cb D8U. | |
| | CB_D8D[1:0] | 5:4 | Cb D8D. | |
| | CR_D8U[1:0] | 3:2 | Cr D8U. | |
| | CR_D8D[1:0] | 1:0 | Cr D8D. | |
| **70h** | **FCC_WIN9** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | CB_D9[2:0] | 5:3 | Cb D9. | |
| | CR_D9[2:0] | 2:0 | Cr D9. | |
| **71h** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **72h** | **FCC_K1K2** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | FCC_K_T1[3:0] | 7 | FCC K T1. | |
| | FCC_K_T2[3:0] | 0 | FCC K T2. | |
| **73h** | **FCC_K3K4** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | FCC_K_T3[3:0] | 7 | FCC K T3. | |
| | FCC_K_T4[3:0] | 0 | FCC K T4. | |
| **74h** | **FCC_K5K6** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | FCC_K_T5[3:0] | 7 | FCC K T5 | |
| | FCC_K_T6[3:0] | 0 | FCC K T6. | |
| **75h** | **FCC_K7K8** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | FCC_K_T7[3:0] | 7 | FCC K T7. | |
| | FCC_K_T8[3:0] | 0 | FCC K T8. | |
| **76h** | **FCC_CTRL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | M_FCC_T9 | 7 | FCC T9 enable. | |
| | M_FCC_T8 | 6 | FCC T8 enable. | |
| | M_FCC_T7 | 5 | FCC T7 enable. | |
| | M_FCC_T6 | 4 | FCC T6 enable. | |

## Analog Register (Bank = 01)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | M_FCC_T5 | 3 | FCC T5 enable. | |
| | M_FCC_T4 | 2 | FCC T4 enable. | |
| | M_FCC_T3 | 1 | FCC T3 enable. | |
| | M_FCC_T1_T2 | 0 | FCC T1 and T2 enable. | |
| **77h** | **APP_CTRL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | MCME | 6 | CTI Median Filter Enable.<br>0: Disable.<br>1: Enable. | |
| | MCEN | 5 | CTI Enable.<br>0: Disable.<br>1: Enable. | |
| | MLME | 4 | LTI Median Fitler Enable.<br>0: Disable.<br>1: Enable. | |
| | MLEN | 3 | LTI Enable.<br>0: Disable.<br>1: Enable. | |
| | MPEN | 2 | Band1 and Band2 Peak Enable.<br>0: Disable.<br>1: Enable. | |
| | - | 1:0 | Reserved. | |
| **78h** | **PEAK_BAND1** | **7:0** | **Default : 0x08** | **Access : R/W** |
| | BAND1_STEP[1:0] | 7:6 | Band 1 Step Adjust.<br>00: 1.<br>01: 2.<br>10: 3.<br>11: 4. | |
| | BAND1_COEF[5:0] | 5:0 | Band 1 Coefficient.<br>(xxx.xxx) | |
| **79h** | **PEAK_BAND2** | **7:0** | **Default : 0x08** | **Access : R/W** |
| | BAND2_STEP[1:0] | 7:6 | Band 2 Step Adjust.<br>00: 1.<br>01: 2.<br>10: 3.<br>11: 4. | |

## Analog Register (Bank = 01)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | BAND2_COEF[5:0] | 5:0 | Band 2 Coefficient.<br>(xxx.xxx) | |
| **7Ah** | **LTI** | **7:0** | **Default : 0x08** | **Access : R/W** |
| | LTI_STEP[1:0] | 7:6 | LTI Step Adjust.<br>00: 1.<br>01: 2.<br>10: 3.<br>11: 4. | |
| | LTI_COEF[5:0] | 5:0 | LTI Coefficient.<br>(xxx.xxx) | |
| **7Bh** | **TERM_SEL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | P_T1[1:0] | 7:6 | Peaking Term1 Select.<br>00, 01: Band 1.<br>10: Band 2.<br>11: LTI. | |
| | P_T2[1:0] | 5:4 | Peaking Term2 Select.<br>00, 01: Band 1.<br>10: Band 2.<br>11: LTI. | |
| | P_T3[1:0] | 3:2 | Peaking Term3 Select.<br>00, 01: Band 1.<br>10: Band 2.<br>11: LTI. | |
| | P_T4[1:0] | 1:0 | Peaking Term4 Select.<br>00, 01: Band 1.<br>10: Band 2.<br>11: LTI. | |
| **7Ch** | **CORING** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CTH_2[3:0] | 7:4 | Coring Threshold 2. | |
| | CTH_1[3:0] | 3:0 | Coring Threshold 1. | |
| **7Dh** | **CTI** | **7:0** | **Default : 0x08** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | CTI_STEP[1:0] | 6:5 | CTI Step Adjust.<br>00: 1.<br>01: 2.<br>10: 3.<br>11: 4. | |

## Analog Register (Bank = 01)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | CTI_COEF[4:0] | 4:0 | CTI Coefficient.<br>(xx.xxx) | |
| **7Eh** | **VIP_Y_CTRL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:2 | Reserved. | |
| | WLEEN | 1 | White Level Extension Enable.<br>0: Disable.<br>1: Enable. | |
| | BLEEN | 0 | Black Level Extension Enable.<br>0: Disable.<br>1: Enable. | |
| **7Fh** | **WHITE_START** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | WHITE_START[7:0] | 7:0 | White contrast adjust starting point (must > or =80h); active range is from WHITE_START[7:0] to ffh. | |
| **80h** | **BLACK_START** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | BLACK_START[7:0] | 7:0 | Black contrast adjust starting point (must < 80h); active range is from 00h to BLACK_START[7:0] | |
| **81h** | **EGE_BAND1_POS** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | EGEBAND1_POS[7:0] | 7:0 | Edge Band 1 Coefficient (positive threshold for median filter max pixel). | |
| **82h** | **EGE_BAND1_NEG** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | EGEBAND1_NEG[7:0] | 7:0 | Edge Band 1 Coefficient (negative threshold for median filter min pixel). | |
| **83h** | **EGE_BAND2_POS** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | EGEBAND2_POS[7:0] | 7:0 | Edge Band 2 Coefficient (positive threshold for median filter max pixel). | |
| **84h** | **EGE_BAND2_NEG** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | EGEBAND2_NEG[7:0] | 7:0 | Edge Band 2 Coefficient (negative threshold for median filter min pixel). | |
| **85h** | **BRI** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | BRI[7:0] | 7:0 | Window Brightness (2's complement: -128 ~ 127). | |
| **86h** | **EGE_LTI_POS** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | EGELTI_POS[7:0] | 7:0 | Edge LTI Coefficient (positive threshold for median filter max pixel). | |
| **87h** | **EGE_LTI_NEG** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | EGELTI_NEG[7:0] | 7:0 | Edge LTI Coefficient (negative threshold for median filter min pixel). | |

## Analog Register (Bank = 01)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| **88h** | **YC_LPF** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | C_LPF_MD[1:0] | 7:6 | C LPF mode.<br>00: Original.<br>01: 11.<br>10: 121.<br>11: 161. | |
| | Y_LPF_MD[1:0] | 5:4 | Y LPF mode. | |
| | B1DEN | 3 | Band 1 differentiate Enable. | |
| | B2DEN | 2 | Band 2 differentiate Enable. | |
| | - | 1:0 | Reserved. | |
| **89h** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **8Ah** | **Y_CORING_CTRL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | HPS_EN | 7 | Coring as high pass. | |
| | Y_TBL_STEP | 6:4 | Y coring table Step. | |
| | PC_MODE | 3 | Coring in PC Mode. | |
| | Y_DITHER | 2 | Y coring dither Enable. | |
| | Y_CORING_BAND2_EN | 1 | Y coring band2 Enable. | |
| | Y_CORING_BAND1_EN | 0 | Y coring band1 Enable. | |
| **8Bh** | **C_CORING_CTRL** | **7:0** | **Default : 0x00** | |
| | - | 7 | Reserved. | |
| | C_TBL_STEP | 6:4 | C coring table Step. | |
| | - | 3 | Reserved. | |
| | C_DITHER | 2 | C coring dither Enable. | |
| | C_CORING_BAND2_EN | 1 | C coring band2 Enable. | |
| | C_CORING_BAND1_EN | 0 | C coring band1 Enable. | |
| **8Ch** | **CORING_TBL1** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CORING_TABLE1[7:0] | 7:0 | Coring table 1. | |
| **8Dh** | **CORING_TBL2** | **7:0** | **Default : 0x00** | |
| | CORING_TABLE2[7:0] | 7:0 | Coring table 2. | |
| **8Eh** | **CORING_TBL3** | **7:0** | **Default : 0x00** | |
| | CORING_TABLE3[7:0] | 7:0 | Coring table 3. | |
| **8Fh** | **CORING_TBL4** | **7:0** | **Default : 0x00** | |
| | CORING_TABLE4[7:0] | 7:0 | Coring table 4. | |

## Analog Register (Bank = 01)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| **90h** | **SARADC_CTRL** | **7:0** | **Default : 0x40** | **Access : R/W** |
| | SAR_SNGL_CHNL | 1:0 | Channel selection in Single Channel mode. | |
| | - | 3:2 | Reserved. | |
| | SAR_SNGL | 4 | Single channel mode enable. Only sample channel at bit[1:0] | |
| | SAR_FREERUN | 5 | SARADC sample mode.<br>1: Freerun mode.<br>0: One shot mode. | |
| | - | 6 | Reserved. | |
| | SAR_START | 7/W | SARADC sample Start. | |
| | SAR_RDY | 7/R | SARADC sample Ready. | |
| **91h** | **SARADC_SAMPRD** | **7:0** | **Default : 0x20** | **Access : R/W** |
| | CKSAMP_PRD | 7:0 | SARADC input Sample Period in one shot mode.<br>Real_SAMP_PRD = CKSAMP_PR x 4 | |
| **92h** | **SARADC_AISEL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | SAR_AISEL | 3:0 | SAR_AISEL[3:0]: Input select of PAD_SAR_GPIO<br>SAR_AISEL[i]=1b'0: Digital GPIO Input<br>SAR_AISEL[i]=1b'1: SAR ADC Analog Input | |
| | - | 7:4 | Reserved | |
| **93h** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **94h** | **SAR_CH1_UPB** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | REG_SAR_CH1_UPB [5:0] | 5:0 | The voltage Upper Bound in MCU sleep mode for Channel 1 keypad wake up. | |
| **95h** | **SAR_CH1_LOB** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | REG_SAR_CH1_LOB [5:0] | 5:0 | The voltage Lower Bound in MCU sleep mode for Channel 1 keypad wake up. | |
| **96h** | **SAR_CH2_UPB** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:6 | Reserved | |
| | REG_SAR_CH2_UPB [5:0] | 5:0 | The voltage Upper Bound in MCU sleep mode for Channel 2 keypad wake up. | |
| **97h** | **SAR_CH2_LOB** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:6 | Reserved | |

## Analog Register (Bank = 01)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | REG_SAR_CH2_LOB [5:0] | 5:0 | The voltage Lower Bound in MCU sleep mode for Channel 2 keypad wake up. | |
| **98h** | **SAR_CH3_UPB** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:6 | Reserved | |
| | REG_SAR_CH3_UPB [5:0] | 5:0 | The voltage Upper Bound in MCU sleep mode for Channel 3 keypad wake up. | |
| **99h** | **SAR_CH3_LOB** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | REG_SAR_CH3_LOB [5:0] | 5:0 | The voltage Lower Bound in MCU sleep mode for Channel 3 keypad wake up. | |
| **9Ah ~ 9Bh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **9Ch** | **ADC_MD_CTRL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | ADC_DCTRL | 7:6 | Reserved for ADC DCTRL. | |
| | GSHIFT_R | 5 | 1: Enable ADC R Gain Range Shift for VD Mode. | |
| | GSHIFT_G | 4 | 1: Enable ADC G Gain Range Shift for VD Mode. | |
| | GSHIFT_B | 3 | 1: Enable ADC B Gain Range Shift for VD Mode. | |
| | ADC_VCTRL | 2:0 | ADC Voltage Control (Recommend Setting = 3'b011). | |
| **9Dh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **9Eh** | **CAL_CTRL3** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | CAL_STSWEN | 6 | 1: Enable Write to Internal CAL Registers through STATUS_CAL. | |
| | CAL_SWOV | 5:4 | 00: Normal Mode.<br>01: Switch ADC Input to Offset CAL Reference Voltage.<br>10: Reserved.<br>11: Reserved. | |
| | CAL_HOLD | 3 | 1: Hold Current CAL Result for Display. | |
| | CAL_INPUT | 2 | 0: CAL to Internal Offset Reference Voltage.<br>1: CAL to ADC Input. | |
| | CAL_HYS | 1 | 1: Enable CAL Update Hytheresis. | |
| | DOFFS_EN | 0 | 1: Enable Digital Offset Adjustment. | |
| **9Fh** | **ADCTOUT** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | ADCTOUT_SYNC | 3 | 1: Enable ADC Test Out Sync to CKEXT. | |

## Analog Register (Bank = 01)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | ADCTOUT_DIV | 2:0 | Select ADC Test Out Decimation Ratio (1~8). | |
| **A0h** | **RG_DRV** | **7:0** | **Default : 0x55** | **Access : R/W** |
| | G[7:6]_DRV[1:0] | 7:6 | Pad G[7:4] Driving select. | |
| | G[5:4]_DRV[1:0] | 5:4 | Pad G[3:0] Driving select. | |
| | R[3:2]_DRV[1:0] | 3:2 | Pad R[7:4] Driving select. | |
| | R[1:0]_DRV[1:0] | 1:0 | Pad R[3:0] Driving select. | |
| **A1h** | **RG_DRV** | **7:0** | **Default : 0x55** | **Access : R/W** |
| | HS_DRV[1:0] | 7:6 | Pad Hsync Driving select. | |
| | VS_DRV[1:0] | 5:4 | Pad Vsync Driving select. | |
| | B[7:4]_DRV[1:0] | 3:2 | Pad B[7:4] Driving select. | |
| | B[3:0]_DRV[1:0] | 1:0 | Pad B[3:0] Driving select. | |
| **A2h** | **RG_DRV** | **7:0** | **Default : 0x55** | **Access : R/W** |
| | PWM2_DRV[1:0] | 7:6 | Pad PWM2 Driving select. | |
| | PWM1_DRV[1:0] | 5:4 | Pad PWM1 Driving select. | |
| | CLK_DRV[1:0] | 3:2 | Pad CLK Driving select. | |
| | DE_DRV[1:0] | 1:0 | Pad DE Driving select. | |
| **A3h** | **EPD_R** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | EPD_R[7:0] | 7:0 | Enable Pull Down in R channel. | |
| **A4h** | **EPD_G** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | EPD_G[7:0] | 7:0 | Enable Pull Down in G channel. | |
| **A5h** | **EPD_B** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | EPD_B[7:0] | 7:0 | Enable Pull Down in B channel. | |
| **A6h** | **EPD_R** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | EPD_PWM2 | 5 | Enable pull down in PWM2 pad. | |
| | EPD_PWM1 | 4 | Enable pull down in PWM2 pad. | |
| | EPD_CLK | 3 | Enable pull down in CLK pad. | |
| | EPD_DE | 2 | Enable pull down in DE pad. | |
| | EPD_HS | 1 | Enable pull down in HSYNC pad. | |
| | EPD_VS | 0 | Enable pull down in VSYNC pad. | |
| **A7h ~ AAh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **ABh** | **VDAC_ADJ2** | **7:0** | **Default : 0x00** | **Access : R/W** |

## Analog Register (Bank = 01)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | - | 7:5 | Reserved. | |
| | ED[4:0] | 4:0 | Testing control for voltage DAC. | |
| **ACh ~ AFh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **B0h** | **SVMCTL0** | **7:0** | **Default : 0x50** | **Access : R/W** |
| | SMEN | 7 | SVM Main window Enable. | |
| | SMTE | 6 | SVM Main window Tap Enable. | |
| | SMFT[1:0] | 5:4 | SVM Main window Filter Tap.<br>00: 2 tap.<br>01: 3 tap.<br>10: 4 tap.<br>11: 5 tap. | |
| | - | 3:0 | Reserved. | |
| **B1h** | **SVMCTL1** | **7:0** | **Default : 0x08** | **Access : R/W** |
| | OSDY | 7 | OSD color Space.<br>0: OSD color space.<br>1: OSD is YUV color space. | |
| | SINV | 6 | SMV polarity Invert.<br>0: Normal.<br>1: Invert. | |
| | SVMBYS[1:0] | 5:4 | SVM Bypass Y Select.<br>0x: SMV data.<br>10: Original Y data.<br>11: Y with tap filter. | |
| | SCORING[3:0] | 3:0 | SVM Coring. | |
| **B2h** | **SVMLMT** | **7:0** | **Default : 0x70** | **Access : R/W** |
| | SVMLMT[7:0] | 7:0 | SVM Limit. | |
| **B3h** | **SMSG** | **7:0** | **Default : 0x4A** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | SMSTEP[2:0] | 6:4 | SVM Main window Step.<br>000: 1 step.<br>001: 2 steps.<br>...<br>111: 8 steps. | |

## Analog Register (Bank = 01)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | SMGAIN[3:0] | 3:0 | SVM Main window Gain.<br>0000: 1/16/<br>0001: 1/8.<br>0010: 1/4.<br>0011: 3/8.<br>0100: 1/2.<br>0101: 5/8.<br>0110: 3/4.<br>0111: 1.<br>1110: 9/8.<br>1001: 5/4.<br>1010: 3/2.<br>1011: 2.<br>1100: 3.<br>1101: 4.<br>1110: 5.<br>1111: 8. | |
| **B4h** | **SVMADJ** | **7:0** | **Default : 0x26** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | SVMPIP[1:0] | 6:5 | SVM pipe adjust. | |
| | SVMDLY[4:0] | 4:0 | SVM Delay adjust.<br>00000: 8 clocks ahead.<br>00001: 7 clocks ahead.<br>...<br>11111: Delay 23 clocks. | |
| **B5h** | **OVERLAP _SEL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | SVM_SEP_DLY | 7 | SVM Separate Delay Enable. | |
| | OVERLAP_SEL[1:0] | 6:5 | Overlap Select.<br>00: Average.<br>01: No Action.<br>10: Keep slow down result.<br>11: Keep speed up result. | |
| | SVM_SD_DLY[4:0] | 4:0 | SVM Slow down delay. | |
| **B6h** | **LCK_THR_FPLL** | **7:0** | **Default : 0x03** | **Access : R/W** |
| | LCK_THR[7:0] | 7:0 | Lock Threshold. | |
| **B7h** | **LMT_LPLL_OFST_L** | **7:0** | **Default : 0xF0** | **Access : R/W** |
| | LMT_LPLL_OFST[7:0] | 7:0 | Limit LPLL Offset Low byte. | |
| **B8h** | **LMT_LPLL_OFST_H** | **7:0** | **Default : 0xFF** | **Access : R/W** |

## Analog Register (Bank = 01)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | LMT_LPLL_OFST [15:8] | 7:0 | Limit LPLL Offset High byte. | |
| **B9h** | **COEF_FPLL** | **7:0** | **Default : 0x50** | **Access : R/W** |
| | TUNE_COEF[3:0] | 7:4 | Tune Coefficient. | |
| | TUNE_COEF_RK[3:0] | 3:0 | Tune Coefficient RK. | |
| **BAh** | **RK_HOLD_GAIN_L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | RK_HOLD_GAIN[7:0] | 7:0 | RK Hold Gain Low byte. | |
| **BBh** | **RK_HOLD_GAIN_H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | RK_HOLD_GAIN [11:8] | 3:0 | RK Hold Gain High byte. | |
| **BEh** | **LPLL_STLMT_L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | LPLL_STLMT[7:0] | 7:0 | FPLL Set Limit Low byte. | |
| **BFh** | **LPLL_STLMT_H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | LPLL_STLMT[15:8] | 7:0 | FPLL Set Limit High byte. | |
| **C0h** | **TUNE_FRAME_NO** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | BND_OVWR_EN | 7 | Bonding Over-Write Enable. | |
| | - | 6:2 | Reserved. | |
| | TUNE_FRAME_NO | 1:0 | Frame pll tune per tune_frame numbers | |
| **C1h** | **BND_RST** | **7:0** | **Default : 0x7F** | **Access : R/W** |
| | MCU_SEL_OVWR | 7 | Select Internal MCU Disable. | |
| | BND_RST[6:0] | 6:0 | Bonding Reset. | |
| **C2h** | **LMT_ADD_NMB** | **7:0** | **Default : 0x17** | **Access : R/W** |
| | LMT_ADD_NMB[7:0] | 7:0 | Limit adjust Number in ACC_FPLL mode. | |
| **C3h** | **IVS_DIFF_THR** | **7:0** | **Default : 0x03** | **Access : R/W** |
| | IVS_DIFF_THR[7:0] | 7:0 | Input v.s. Different Thresholds. | |
| **C4h** | **IVS_STALBE_THR** | **7:0** | **Default : 0x03** | **Access : R/W** |
| | IVS_STB_THR[7:0] | 7:0 | Input v.s. Stable Thresholds. | |
| **C5h** | **CH_CH_MODE** | **7:0** | **Default : 0x02** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | CH_CH_MD1 | 5 | ACC FPLL Mode 1. | |
| | - | 4 | Reserved. | |
| | FPLL_DIS | 3 | FPLL Stop. | |

## Analog Register (Bank = 01)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | - | 2 | Reserved. | |
| | ADD_LINE_SEL | 1 | Select Add Line into frame or pixel into line. | |
| | CH_CH_MD0 | 0 | ACC FPLL Mode 0. | |
| **C6h** | **ACC1_SEL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | TUNE_CLK_FF | 4 | Tune Clock Enable when FF Mode. | |
| | - | 3:2 | Reserved. | |
| | ACC1_SEL[1:0] | 1:0 | Select modify numbers.<br>00: 3/4 diff numbers.<br>01: 1/2 diff numbers.<br>others:1/4 diff numbers. | |
| **C7h** | **IVS_PRD_NUM_L** | **7:0** | **Default : 0x03** | **Access : R/W** |
| | IVS_PRD_NUM[7:0] | 7:0 | Count Number per Input v.s Low byte. | |
| **C8h** | **IVS_PRD_NUM_H** | **7:0** | **Default : 0x03** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | IVS_PRD_NUM[11:8] | 3:0 | Count Number per Input v.s 4 High bytes. | |
| **CAh** | **POL_SET0** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | POL_OUT_INV | 7 | POL Output Invert. | |
| | POL_TP | 6:0 | POL Transition Point. | |
| **CBh** | **POL_SET1** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | POL_SEL | 4 | 0: VSYNC Frequency POL.<br>1: HSYNC Frequency POL. | |
| | POL_PVI_10IN | 3 | POL Output to SEQ_MOD Pin if EFh[7] = 0. | |
| | - | 2:0 | Reserved. | |
| **CCh** | **SCAL_ACT** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | TC_CLK_DIV2 | 5 | TC Clock Divide 2. | |
| | - | 4 | Reserved. | |
| | LINE_ACT_D1L | 3 | Line Active Delay One Line time. | |
| | LINE_ACT_EN | 2 | TCON Line_Extract Mode work with Digital V_Scaling. | |
| | - | 1:0 | Reserved. | |
| **CDh** | **GPO_OEV2_WIDTH** | **7:0** | **Default : 0x54** | **Access : R/W** |
| | GPO_OEV2_DIS | 7 | OEV2 Disable. | |

## Analog Register (Bank = 01)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | GPO_OEV2_WIDTH [6:0] | 6:0 | OEV2 Pulse Width. | |
| **CEh** | **GPO_OEV3_WIDTH** | **7:0** | **Default : 0x54** | **Access : R/W** |
| | GPO_OEV3_DIS | 7 | OEV3 Disable. | |
| | GPO_OEV3_WIDTH [6:0] | 6:0 | OEV3 Pulse Width. | |
| **CFh** | **GPO_OEV_ DELTA** | **7:0** | **Default : 0x54** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | GPO_OEV_ DELTA[3:0] | 3:0 | Adjust OEV distance. | |
| **D0h** | **PTC_MODE1** | **7:0** | **Default : 0x8C** | **Access : R/W** |
| | TC_MD | 7 | TC signal output enable.<br>0: Disable set low.<br>1: Enable. | |
| | OEV_DELTA_EN | 6 | OEV distance adjust Enable. | |
| | DOU_EXTR_MD[1:0] | 5:4 | 00: Normal mode.<br>01: Paranoma extract mode.<br>10: Full extract mode.<br>11: Line duplicate mode. | |
| | FRAME_INV_EN | 3 | 0: Disable.<br>1: Enable. | |
| | EARLY_VS | 2 | Early vs. | |
| | FIELD_SEL | 1 | Select field inverse from IP. | |
| | LN_SHIFT | 0 | Field Line Shift enable. | |
| **D1h** | **PTC_MODE2** | **7:0** | **Default : 0x3E** | **Access : R/W** |
| | TCCLK_CONF[1:0] | 7:6 | 7: 13 CLK swap.<br>6: 3 CLK inverse. | |
| | SEQ_MD | 5 | 0: Single clock output mode.<br>1: Three clock output mode. | |
| | TCCLK_MD | 4 | Select 3TC CLK or 1 TC CLK. | |
| | STHLR_SEL | 3 | 0: STHR.<br>1: STHL. | |
| | STVLR_SEL | 2 | 0: STVR.<br>1: STVL. | |
| | L_R | 1 | 0: L_R equal 0.<br>1: L_R equal 1. | |

## Analog Register (Bank = 01)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | U_D | 0 | 0: U_D=0.<br>1: U_D=1. | |
| D2h | **PTC_MODE3** | **7:0** | **Default : 0x84** | **Access : R/W** |
| | SET_TCCLK23_VALUE | 7 | Set TCCLK23 High/Low. | |
| | LG_MD | 6 | LG_panel Mode enable. | |
| | DF_EXT_LN | 5 | Different frame, Different Extract Line mode.<br>0: Disable.<br>1: Enable. | |
| | LN_DUP_MD[1:0] | 4:3 | Duplicate 2/3 Line Mode.<br>4: OEV3 enable.<br>3: OEV2 enable. | |
| | FIELD_IN_SEL | 2 | Select Field source from OP2 or free-run. | |
| | LINE_INV_DIS | 1 | Line Inverse Disable.<br>0: Enable.<br>1: Disable. | |
| | FRP_VCOM_INV | 0 | VCOM Inverse to FRP. | |
| D3h | **LN_EXTR_CNT_LMT** | **7:0** | **Default : 0xDD** | **Access : R/W** |
| | LN_EXTR_CNT_LMT2 | 7:4 | Line Extract/duplicate Counter 2. | |
| | LN_EXTR_CNT_LMT1 | 3:0 | Line Extract/duplicate Counter 1. | |
| D4h | **LN_EXTR_SET1_H** | **7:0** | **Default : 0x2F** | **Access : R/W** |
| | LN_EXTR_SET1[7:0] | 7:0 | Line Extract/duplicate set 1 High byte. | |
| D5h | **LN_EXTR_SET1_L** | **7:0** | **Default : 0xEF** | **Access : R/W** |
| | LN_EXTR_SET1[15:8] | 7:0 | Line Extract/duplicate set 1 Low byte. | |
| D6h | **LN_EXTR_SET2_H** | **7:0** | **Default : 0x1F** | **Access : R/W** |
| | LN_EXTR_SET2[7:0] | 7:0 | Line Extract/duplicate set 2 High byte. | |
| D7h | **LN_EXTR_SET2_L** | **7:0** | **Default : 0xE7** | **Access : R/W** |
| | LN_EXTR_SET2[15:8] | 7:0 | Line Extract/duplicate set 2 Low byte. | |
| D8h | **EXTR_STT_LN1** | **7:0** | **Default : 0x02** | **Access : R/W** |
| | EXTR_STT_LN1[7:0] | 7:0 | Line Extract/duplicate Start Line 1. | |
| D9h | **EXTR_END_LN1** | **7:0** | **Default : 0x30** | **Access : R/W** |
| | EXTR_END_LN1[7:0] | 7:0 | Line Extract/duplicate End Line 1. | |
| DAh | **EXTR_STT_LN2** | **7:0** | **Default : 0x50** | **Access : R/W** |
| | EXTR_STT_LN2[7:0] | 7:0 | Line Extract/duplicate Start Line 2. | |
| DBh | **EXTR_END_LN2** | **7:0** | **Default : 0x77** | **Access : R/W** |
| | EXTR_END_LN2[7:0] | 7:0 | Line Extract/duplicate End Line 2. | |

## Analog Register (Bank = 01)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| **DCh** | **GPO_FRP_TRAN** | **7:0** | **Default : 0x13** | **Access : R/W** |
| | OUT_INV | 7 | Output Inverse. | |
| | GPO_FRP_TRAN_MULT [1:0] | 6:5 | 00: x1.<br>01: x4.<br>10: x8.<br>11: x16. | |
| | GPO_FRP_TRAN[4:0] | 4:0 | FRP Transition position. | |
| **DDh** | **GPO_STH_STT** | **7:0** | **Default : 0x46** | **Access : R/W** |
| | OUT_INV | 7 | Output Inverse. | |
| | GPO_STH_STT_MULT [1:0] | 6:5 | 00: x1.<br>01: x4.<br>10: x8.<br>11: x16. | |
| | GPO_STH_STT[4:0] | 4:0 | STH pulse Start position. | |
| **DEh** | **GPO_STH_WIDTH** | **7:0** | **Default : 0x01** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | GPO_STH_WIDTH_ MULT[1:0] | 5:4 | 00: x1.<br>01: x4.<br>10: x8.<br>11: x16. | |
| | GPO_STH_WIDTH [3:0] | 3:0 | STH pulse Width. | |
| **DFh** | **GPO_OEH_STT** | **7:0** | **Default : 0xA3** | **Access : R/W** |
| | OUT_INV | 7 | Output Inverse. | |
| | GPO_OEH_STT_MULT [1:0] | 6:5 | 00: x1.<br>01: x4.<br>10: x8.<br>11: x16. | |
| | GPO_OEH_ STT[4:0] | 4:0 | OEH pulse Start position. | |
| **E0h** | **GPO_OEH_WIDTH** | **7:0** | **Default : 0x0B** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | GPO_OEH_WIDTH_ MULT[1:0] | 5:4 | 00: x1.<br>01: x4.<br>10: x8.<br>11: x16. | |
| | GPO_OEH_WIDTH [3:0] | 3:0 | OEH pulse Width. | |

## Analog Register (Bank = 01)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| **E1h** | **GPO_ OEV _STT** | **7:0** | **Default : 0x01** | **Access : R/W** |
| | OUT_INV | 7 | Output Inverse. | |
| | GPO_OEV_STT_MMULT [1:0] | 6:5 | 00: x1.<br>01: x4.<br>10: x8.<br>11: x16. | |
| | GPO_OEV_STT[1:0] | 4:0 | OEV pulse Start. | |
| **E2h** | **GPO_OEV_WIDTH** | **7:0** | **Default : 0x6D** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | GPO_OEV_WIDTH_ MULT[1:0] | 5:4 | 00: x1.<br>01: x4.<br>10: x8.<br>11: x16. | |
| | GPO_OEV_WIDTH [3:0] | 3:0 | OEV pulse Width. | |
| **E3h** | **GPO_CKV_STT** | **7:0** | **Default : 0x2D** | **Access : R/W** |
| | OUT_INV | 7 | Output Inverse. | |
| | CKV_STT_ MULT[1:0] | 6:5 | 00: x1.<br>01: x4.<br>10: x8.<br>11: x16. | |
| | GPO_ CKV_STT[4:0] | 4:0 | CKV pulse Start. | |
| **E4h** | **GPO_CKV_STT2** | **7:0** | **Default : 0x04** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | CKV_STT2_MULT [1:0] | 5:4 | 00: x1.<br>01: x4.<br>10: x8.<br>11: x16. | |
| | GPO_ CKV_ST2[3:0] | 3:0 | CKV pulse Start 2. | |
| **E5h** | **GPO_CKV_WIDTH** | **7:0** | **Default : 0x5F** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | CKV_WIDTH_ MULT[1:0] | 6:5 | 00: x1.<br>01: x4.<br>10: x8.<br>11: x16. | |
| | GPO_ CKV_WIDTH[4:0] | 4:0 | CKV pulse width. | |

| Analog Register (Bank = 01) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| **E6h** | **GPO_STV_LN_TH** | **7:0** | **Default : 0x46** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | GPO_STV_1LN | 6 | STV width is 1 Line. | |
| | GPO_ STV _LINE_TH | 5:0 | STV line position | |
| **E7h** | **GPO_ STV _STT** | **7:0** | **Default : 0x29** | **Access : R/W** |
| | OUT_INV | 7 | Output Inverse. | |
| | STV_STT_MULT[1:0] | 6:5 | 00: x1.<br>01: x4.<br>10: x8.<br>11: x16. | |
| | GPO_ STV_STT[4:0] | 4:0 | STV pulse Start. | |
| **E8h** | **GPO_STV_ WIDTH** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | STV_WIDTH_MULT [1:0] | 5:4 | 00: x1.<br>01: x4.<br>10: x8.<br>11: x16. | |
| | GPO_STV_WIDTH [3:0] | 3:0 | STV pulse Width. | |
| **E9h** | **GPO_OEV2_STT** | **7:0** | **Default : 0x04** | **Access : R/W** |
| | OUT_INV | 7 | Output Inverse. | |
| | OEV2_STT_MULT [1:0] | 6:5 | 00: x1.<br>01: x4.<br>10: x8.<br>11: x16. | |
| | GPO_OEV2_STT[4:0] | 4:0 | OEV2 pulse Start. | |
| **EAh** | **GPO_OEV3_STT** | **7:0** | **Default : 0x04** | **Access : R/W** |
| | OUT_INV | 7 | Output Inverse. | |
| | OEV3_STT_MULT [1:0] | 6:5 | 00: x1.<br>01: x4.<br>10: x8.<br>11: x16. | |
| | GPO_OEV3_STT[4:0] | 4:0 | OEV3 pulse Start. | |
| **EBh** | **HSTT_DLY_L** | **7:0** | **Default :0x04** | **Access : R/W** |
| | HSTT_DLY[7:0] | 7:0 | H Start Delay numbers Low byte. | |
| **ECh** | **HSTT_DLY_H** | **7:0** | **Default :0xA4** | **Access : R/W** |

## Analog Register (Bank = 01)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | EXT_DIS_RNG | 7:4 | Extraction start point in line extraction mode. | |
| | - | 3 | Reserved. | |
| | HSTT_DLY_EN | 2 | H Start Delay Enable. | |
| | HSST_DLY[9:8] | 1:0 | H Start Delay numbers High byte. | |
| EDh | **CLK_DLY_SYNCOUT** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | FRPSETH | 7 | Set High to Invert RGB Data when FRP Disable (BK1_D2[1]=1). | |
| | - | 6 | Reserved. | |
| | TC_GPIO_SEL | 5 | 0: TC function.<br>1: GPIO function. | |
| | OEV_MD_SEL | 4 | 0: Normal mode.<br>1: Special mode. | |
| | CLK_DLY_SEL_TC [3:0] | 3:0 | TCCLK Delay Select. | |
| EEh | **GPO_CKV_END2** | **7:0** | **Default : 0x28** | **Access : R/W** |
| | CKV2_EN | 7 | CKV2 Enable. | |
| | CKV_END2_MULT[1:0] | 6:5 | 00: x1.<br>01: x4.<br>10: x8.<br>11: x16. | |
| | GPO_CKV_END2 | 4:0 | CKV2 End point. | |
| EFh | **Q1H_SETTING** | **7:0** | **Default : 0x08** | **Access : R/W** |
| | Q1H_ENABLE | 7 | Q1H output from SEQ_MODE pin, toggle point is using OEV3 signal start point. | |
| | TCCLK_INV_MODE | 6:3 | 0001: TCCLK invert every field.<br>0011: TCCLK invert when Q1H is high.<br>0101: TCCLK invert when Q1H and field are high.<br>1001: TCCLK invert when Q1H is low and field is high. | |
| | - | 2 | Reserved. | |
| | INTOUT_OEN | 1 | Testmode. PAD_INTOUT output enable control.<br>0: Output.<br>1: Input. | |
| | CLKIN_SEL | 0 | Testmode External Clock Select.<br>0: PAD_INTOUT.<br>1: PAD_CLKIN. | |
| F0h | **WDT0** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | WDT_TESTMD | 7 | CSOG test mode for WDT counter. | |

## Analog Register (Bank = 01)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | WDT_LD | 6 | Watch Dog Timer Load Value by SW. | |
| | WDT_EN | 5 | Watch Dog Timer Enable Bit. | |
| | - | 4:0 | Reserved. | |
| **F1h** | **WDT1** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | WDT_WIDTH | 7:0 | Watch Dog Timer Width. | |
| **F2h** | **WRLOCK0** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | WRLOCK0 | 7 | Register lock (work with WRLOCK1).<br>Register access is disabled when WRLOCK0 and WRLOCK1 are HIGH. Register access is enabled when WRLOCK0 and WRLOCK1 are LOW. | |
| | - | 6:0 | Reserved. | |
| **F3h** | **PWMCLK** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | DB_EN | 7 | Double Buffer Enable.<br>0: Disable.<br>1: Enable. | |
| | P2REN | 6 | PWM2 Reset every frame Enable.<br>0: Disable.<br>1: Enable. | |
| | P1REN | 5 | PWM1 Reset every frame Enable.<br>0: Disable.<br>1: Enable. | |
| | P2POL | 4 | PWM 2 Polarity when enhance PWM2 enable. | |
| | EP2EN | 3 | Enhance PWM2 Enable.<br>0: Disable.<br>1: Enable. | |
| | P1POL | 2 | PWM1 Polarity when enhance PWM1 enable. | |
| | EP1EN | 1 | Enhance PWM1 Enable.<br>0: Disable.<br>1: Enable. | |
| | PCLK | 0 | PWM1/2 base Clock select.<br>0: 14.318MHz.<br>1: 14.318MHz / 4. | |
| **F4h** | **PWM1C** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | PWM1_POL | 7 | PWM1 polarity. | |
| | PWM1_CTUN[6:0] | 6:0 | PWM1 Coarse adjustment. | |
| **F5h** | **PWM2C** | **7:0** | **Default : 0x00** | **Access : R/W** |

## Analog Register (Bank = 01)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | PWM2_POL | 7 | PWM2 polarity. | |
| | PWM2_CTUN[6:0] | 6:0 | PWM2 Coarse adjustment. | |
| **F6h** | **PWM1EPL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | EPWM1P[7:0] | 7:0 | Enhance PWM1 Period. | |
| **F7h** | **PWM1EPH** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | EPWM1P[15:8] | 7:0 | Enhance PWM1 Period. | |
| **F8h** | **PWM2EPL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | EPWM2P[7:0] | 7:0 | Enhance PWM2 Period. | |
| **F9h** | **PWM2EPH** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | EPWM2P[15:8] | 7:0 | Enhance PWM2 Period. | |
| **FAh** | **PWM5L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | PWM5[7:0] | 7:0 | PWM5 Period. | |
| **FBh** | **PWM5H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | PWM5[12:8] | 4:0 | PWM5 Period. | |
| **FCh** | **PWM6L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | PWM6[7:0] | 7:0 | PWM6 Period. | |
| **FDh** | **PWM6H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | PWM6[12:8] | 4:0 | PWM6 Period. | |
| **FEh ~ FFh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |

## Video Decoder Register (Bank = 02)

| Video Decoder Register (Bank = 02) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| **01h** | **STATUS1** | **7:0** | **Default : -** | **Access : RO** |
| | READBUS1 | 7:0 | Test bus 1. | |
| **02h** | **STATUS2** | **7:0** | **Default : -** | **Access : RO** |
| | READBUS2 | 7:0 | Test bus 2. | |
| **03h** | **STATUS3** | **7:0** | **Default : -** | **Access : RO** |
| | READBUS3 | 7:0 | Test bus 3. | |
| **04h** | **STATUS_MUX** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | READBUS_CTRL | 7:0 | VIPTESTMUX Address Control of READBUS1, READBUS2, and READBUS3. | |
| **05h ~ 06h** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **07h** | **DSP_ADD_PRT** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | DSP_ADD_PRT[7:0] | 7:0 | DSP register Address Port. | |
| **08h** | **DSP_WDAT_PRT** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | DSP_WDAT_PRT[7:0] | 7:0 | DSP register Write Data Port. | |
| **09h** | **DSP_RDAT_PRT** | **7:0** | **Default : -** | **Access : RO** |
| | DSP_RDAT_PRT[7:0] | 7:0 | DSP register Read Data Port. | |
| **10h** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **11h** | **COMB_LL_EN** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | **-** | 7:1 | Reserved. | |
| | APL_COMB_LL_EN | 0 | 1: Mux to select Com Line Lock mode. | |
| **12h ~ 13h** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **14h** | **SOFT_RST** | **7:0** | **Default : 0x10** | **Access : R/W** |
| | SOFT_RST | 7 | 1: Softrest AFEC modules. | |
| | - | 6:0 | Reserved. | |
| **15h** | **FPGA_CTRL** | **7:0** | **Default : 0xA8** | **Access : R/W** |
| | FPGA_CTRL | 7:0 | Reserved for FPGA control. | |
| **16h** | **REG_SOFT_RST2** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | REG_SOFT_RST2 | 7:0 | Reserved for HW testing. | |
| **17h** | **CLK_CTRL** | **7:0** | **Default : 0xC9** | **Access : R/W** |

## Video Decoder Register (Bank = 02)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | FSCPLL_MODE | 7 | 0: External FSC Clock Mode.<br>1: Internal FSC Clock Mode. | |
| | ADC_DOUBLE | 6 | ADC Double Sample Rate Option. | |
| | REG_CLK_VD_VIP | 5:4 | 00: 4 Fsc Clock on Digital.<br>11: 8 Fsc Clock on Digital. | |
| | REG_VCO_TYPE | 3:2 | 10: VCO 16 Fsc.<br>01: VCO 8 Fsc.<br>00: VCO 4 Fsc. | |
| | REG_ADC_CLK_LAG | 1:0 | CLK_CC / CLK_ADC Phase Diff. | |
| **18h** | **CSTATE_CTRL** | **7:0** | **Default : 0x86** | **Access : R/W** |
| | CTRL_MD | 7:5 | Default: 100b, Auto control mode. | |
| | - | 4 | Reserved. | |
| | CTRL_STATE | 3:0 | State Stable State Value; default: 0110b. | |
| **19h** | **MVDET_EN** | **7:0** | **Default : 0xC0** | **Access : R/W** |
| | MV_DETEC_EN | 7 | Microvision Detect Enable.<br>0: Disable.<br>1: Enable. | |
| | - | 6:5 | Reserved. | |
| | DSP_SYNC_ALW | 4 | Allow DSP to Control SYNC_FOUND. | |
| | DSP_APL_ALW | 3:2 | 0: Allow DSP to Control APL_FREQ_IDEAL (Center Frequency). | |
| | SECAM_MD | 1:0 | 1: Allow DSP to Control APL_FREQ and APL_PHS (Full frequency/PHS control). | |
| **1Ah** | **SVD_EN** | **7:0** | **Default : 0x40** | **Access : R/W** |
| | SVIDEO_EN | 7 | 0: Chroma Source from CVBS-Channel Input.<br>1: Chroma Source from C-Channel Input. | |
| | ADC_C_ALWY_ON | 6 | Chroma ADC 16Fsc-to-4Fsc Down-Sampling is Enabled. | |
| | CLAMDSM_CTRL[15:10] | 5:0 | Clamping 12-bit Control code; integer parts. | |
| **1Bh** | **BKLVL_FORCE1** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | DISCLAMP3 | 7 | HW Clamping frozen 3 times if SYNC magnitude is small. | |
| | CLMP_FREZ_ZERO | 6 | HW Clamping set to Zero when Frozen. | |
| | CLAMDSM_CTRL[9:4] | 5:0 | Clamping 12-bit control code; fractional parts. | |
| **1Ch** | **BKLVL_FORCE2** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | CLMFZE_VRGE | 7:0 | Clamp Freeze of V Range. | |
| **1Dh** | **VCR_VLSHT** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | CLMFZE_HRGE | 7:0 | Clamp Freeze of H Range. | |

## Video Decoder Register (Bank = 02)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| **1Eh** | **DSP_EN** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | DSP_EN_SYS | 7 | 1: Enable SW DSP Function. | |
| | - | 6:0 | Reserved. | |
| **1Fh** | **CLMP_C_EN** | **7:0** | **Default : 0x60** | **Access : R/W** |
| | CLMP_C_EN | 7 | 2nd ADC Chroma Clamping Enable. | |
| | CLMP_K1_INI | 6:0 | HW Clamping K1 when system not stable. | |
| **20h** | **APLL_CTRL1** | **7:0** | **Default : 0xBC** | **Access : R/W** |
| | APL_EN | 7 | Analog burst-lock PLL Enable. | |
| | APL_TYPE | 6:4 | APL Type. | |
| | - | 3:2 | Reserved. | |
| | APL_EN2 | 1 | No state 7, when no bust. | |
| | CLMP_6B_FORCE | 0 | Clamp value 6-bit test mode enable. | |
| **21h** | **APLL_CTRL2** | **7:0** | **Default : 0x18** | **Access : R/W** |
| | CLMP_2DSM | 7 | Second order Clamp method. | |
| | APL_COMB_LL_TST[1] | 6 | 0: Comb-Line-Lock Disabled if VCR.<br>1: Com-Line-Lock Enabled even for VCR. | |
| | APL_COMB_LL_TST[0] | 5 | 0: Fractional SYNC Phase is used.<br>1: Integer PD from Comb. | |
| | DPL_PHS_CAL | 4 | DPL Phase Calibration. | |
| | APL_CEZANNE | 3 | For CEZANNE FPGA Test. | |
| | PALSWH_MODE | 2:1 | PAL Switch Mode control. | |
| | APL_COMB_LL_EN | 0 | Comb Line-Locked mode Enable. | |
| **22h** | **APL_FREQ_MD** | **7:0** | **Default : 0x61** | **Access : R/W** |
| | APL_FREQ_MD[7:5] | 7:5 | APL Freq Mode. | |
| | - | 4:3 | Reserved. | |
| | ACLPZ_WDTH | 2:0 | Clamping Width. | |
| **23h** | **APLL_TRANGE** | **7:0** | **Default : 0x40** | **Access : R/W** |
| | APL_FREQ_LMT | 7:5 | Burst PLL Frequency Limitation.<br>0: 125ppm.<br>2: 250ppm.<br>4: 500ppm.<br>6: 1000ppm. | |
| | - | 4:1 | Reserved. | |
| | APL_K_FORCE | 0 | APL K value Force enable. | |
| **24h** | **APL_K1_NOISY** | **7:0** | **Default : 0x04** | **Access : R/W** |

## Video Decoder Register (Bank = 02)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | APL_K1_NOISY[7:0] | 7:0 | APLL phase tracking coefficients for Noisy broadcast. | |
| **25h** | **APL_K2_NOISY** | **7:0** | **Default : 0x02** | **Access : R/W** |
| | APL_K2_NOISY[7:0] | 7:0 | APLL frequency tracking coefficients for Noisy broadcast. | |
| **26h** | **APL_K1_NORM** | **7:0** | **Default : 0x10** | **Access : R/W** |
| | APL_K1 | 7:0 | APLL phase tracking coefficients for normal condition. | |
| **27h** | **APL_K2_NORM** | **7:0** | **Default : 0x08** | **Access : R/W** |
| | APL_K2 | 7:0 | APLL frequency tracking coefficients for normal condition. | |
| **28h** | **APL_K1_VCR** | **7:0** | **Default : 0x02** | **Access : R/W** |
| | APL_K1_VCR | 7:0 | APLL phase tracking coefficients for VCR. | |
| **29h** | **APL_K2_VCR** | **7:0** | **Default : 0x01** | **Access : R/W** |
| | APL_K2_VCR | 7:0 | APLL frequency tracking coefficients for VCR. | |
| **2Ah** | **MODE_PFSC** | **7:0** | **Default : 0x20** | **Access : R/W** |
| | MD_PFSC[7] | 7 | 0: Auto Fsc.<br>1: Manual Fsc. | |
| | MD_PFSC[6:4] | 6:4 | When bit[7]=1,<br>000: fsc=4.43361875 MHz.<br>001: fsc=4.406 MHz.<br>010: fsc=3.579545 MHz.<br>100: fsc=3.57561149 MHz.<br>110: fsc=3.58205625 MHz. | |
| | VDFD_ASWFSC | 3 | Internal blind FSC try. | |
| | VDFD_ASWFSC1 | 2 | Internal blind FSC try1. | |
| | HALFWIN_OP | 1 | Half Window period Option.<br>0: Asserted between 1/4 to 3/4 line period.<br>1: Asserted between 1/2 to 1 line period. | |
| | OEINV_MD | 0 | ODD_EVEN_INVERT bit inversion Mode.<br>0: Directly bypass.<br>1: Inverse. | |
| **2Bh** | **VDFD_CTRL1** | **7:0** | **Default : 0x7E** | **Access : R/W** |
| | VDFD_FD_L | 7:4 | Fast attack frequency tracking time period. | |
| | VDFD_PHSSTD_L | 3:0 | Monitor Phase tracking time period. | |
| **2Ch** | **VDFD_CTRL2** | **7:0** | **Default : 0x67** | **Access : R/W** |
| | PHS_DIFF_THRD | 7:4 | Phase tracking deviation large Threshold. | |
| | PHS_STD_RANGE | 3:0 | Phase tracking deviation small threshold. | |
| **2Dh** | **FD_K** | **7:0** | **Default : 0xC0** | **Access : R/W** |

## Video Decoder Register (Bank = 02)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | FD_K | 7:4 | Fast Attack Frequency Tracking Coefficient. | |
| | APL_PHS_OFST[11:8] | 3:0 | Preferred Phase Offset of the Analog Burst-locked PLL. | |
| **2Eh** | **APL_PHS_OFST** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | APL_PHS_OFST[7:0] | 7:0 | Preferred Phase Offset of the analog burst-locked PLL. | |
| **2Fh** | **BLACK_SEL** | **7:0** | **Default : 0x24** | **Access : R/W** |
| | SETUP_YES | 7:5 | 0x: Based on confirm mode auto determine.<br>NTSC: setup.<br>PAL: no setup.<br>10: Force no setup for NTSC.<br>11: Force setup for PAL. | |
| | - | 4:2 | Reserved. | |
| | - | 1:0 | Reserved. | |
| **30h** | **CLAMP_CTRL** | **7:0** | **Default : 0x01** | **Access : R/W** |
| | CLAMPDAC_CTRL[7:6] | 7:6 | 00: Auto clamping control.<br>01: Auto clamping control, but polarity inverted.<br>10: Force clamping control by bit[5:0].<br>11: Auto clamping control. | |
| | CLAMPDAC_CTRL[5:0] | 5:0 | Clamping control value. | |
| **31h** | **CLAMP_COEF1** | **7:0** | **Default : 0x40** | **Access : R/W** |
| | CLMP_TYPE_ST3BOT | 7 | CLMP_BOT function enable in STAE3. | |
| | CLMP_K1 | 6:0 | Clamping speed; the larger the faster.<br>7'b101_1000 suggested for 1.00 uF.<br>7'b100_0000 suggested for 0.10 uF. (default)<br>7'b010_1000 suggested for 0.01 uF. | |
| **32h** | **CLAMP_COEF2** | **7:0** | **Default : 0xA0** | **Access : R/W** |
| | CLMP_TYPE | 7 | Back-porch clamping enable (default =1). | |
| | CLMP_K2 | 6:0 | Leakage current tracking speed. Smaller value is preferred.<br>7'b001_0000 suggested for 1.00 uF.<br>7'b010_0000 suggested for 0.10 uF. (default).<br>7'b011_0000 suggested for 0.01 uF. | |
| **33h** | **CLAMP_COEF3** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CLMP_LKG_MODE | 7:4 | Leakage control Mode. | |
| | ADCLOSS_CNT | 3:0 | Count value of ADC Loss status. | |
| **34h** | **CLAMP_COEF4** | **7:0** | **Default : 0x82** | **Access : R/W** |
| | CLMP_BOTSPD | 7:6 | Bottom reference LPF selection. | |
| | CLMP_DLKG_MAC | 5:0 | Delta leakage is bounded by +- (CLAMP_DLKG_MAX/512). | |

## Video Decoder Register (Bank = 02)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| **35h** | **CLAMP_REF_SEL1** | **7:0** | **Default : 0x0A** | **Access : R/W** |
| | BLANKLVL_CTRL | 7 | Blank Level Control. | |
| | BLANK_LVL[8] | 6 | Blank Level bit[8]. | |
| | CLMP_LKG | 5:0 | If CLAMP_LKG_MD = 1011, leakage is forced by CLAMP_LKG[4:0] * sign;<br>where, sign=+1 if bit[5]=1, and sign=-1 if bit[5]=0.<br>Default: 6'd10. | |
| **36h** | **CLAMP_COEF5** | **7:0** | **Default : 0x45** | **Access : R/W** |
| | CLMP_BOTSEL | 7:5 | Clamp Bot Selection enable. | |
| | CLMP_ERR_MAX | 4:0 | Back porch level Error for clamping is bounded by +- CLMP_ERR_MAX*8 (Default: 5'd25). | |
| **37h** | **CLAMP_REF_SEL2** | **7:0** | **Default : 0xF0** | **Access : R/W** |
| | BLANK_LVL[7:0] | 7:0 | Blank Level. | |
| **38h** | **VSTROBE_LIMIT** | **7:0** | **Default : 0x13** | **Access : R/W** |
| | BLACKLVL_CTRL | 7 | Black Level Control. | |
| | BLACK_LVL[8] | 6 | Black Level bit[8]. | |
| | HV_VCNTSEL | 5 | 1: Enable 2nd Integration Protection for V Extraction. | |
| | HV_VLINPROT | 4 | 0: Enable Next V Extraction after 50 Lines.<br>1: Enable Next V Extraction after 200 Lines. | |
| | BOTAV_INSEL | 3 | Bottom of active video Input Selection. | |
| | BOT_INSEL | 2:0 | Bottom of whole line Input Selection. | |
| **39h** | **VSTROBE_PROTECT** | **7:0** | **Default : 0x6C** | **Access : R/W** |
| | WP_INSEL | 7:5 | Sync Input LPF BW Selection. | |
| | HV_INSEL | 4:2 | HSYNC/VSYNC slicer level Selection. | |
| | TOP_INSEL | 1:0 | Top level Input Selection. | |
| **3Ah** | **BLACK_LVL** | **7:0** | **Default : 0xCC** | **Access : R/W** |
| | BLACK_LVL[7:0] | 7:0 | Black Level value. | |
| **3Bh** | **HV_VEXTH** | **7:0** | **Default : 0x7D** | **Access : R/W** |
| | HV_VEXTH | 7:0 | 0: V Extract by Line Length Unit.<br>1: V Extract by Manual Pixel Length Units. | |
| **3Ch** | **HV_C TRL1** | **7:0** | **Default : 0x2A** | **Access : R/W** |
| | HV_VSEL | 7:6 | 00: V Extract native.<br>01: V Extrat Native Synchronize to next line start/middle.<br>Other reserved. | |

## Video Decoder Register (Bank = 02)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | HV_VTHRDSEL | 5:4 | 00: 3/8 line.<br>01: 6/8 line.<br>10: 1.25 line.<br>11: 1.75 line.<br>As Threshold for V Extract. | |
| | HV_INTCNT | 3:0 | Composite SYNC Pixel Lengths Filter for V Extract. | |
| **3Dh** | **V_POSTCOAST** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | VCOST_FEXT | 7:6 | Coast forward control. | |
| | VCOST_BEXT | 5:0 | Coast Backward control. | |
| **3Eh** | **HV_SLICTRL** | **7:0** | **Default : 0x0C** | **Access : R/W** |
| | HV_SLICTRL | 7:0 | HSYNC/VSYNC Slicer Control. | |
| **3Fh** | **HV_HSLIOFSTHYS** | **7:0** | **Default : 0xC0** | **Access : R/W** |
| | HV_HSLIOFSTHYS | 7:4 | HSYNC slicer line Offset. | |
| | AGC_FINE_LSB | 3:0 | AGC Fine gain (lower 4 bits). | |
| **40h** | **PGA_CTRL1** | **7:0** | **Default : 0xC1** | **Access : R/W** |
| | PGA_AUTO | 7 | 0: Manual PGA set by AGC_COARSE[1:0].<br>1: Auto PGA switch. | |
| | PGA_FSWT | 6 | 0: PGA switch in VSYNC.<br>1: PGA switch in HSYNC. | |
| | AGC_COARSE | 5:4 | 00: PGA x 1.<br>01: PGA x 2. | |
| | FREZ_CLMPDISBK | 3 | Freeze Clamp Function; VSYNC selection. | |
| | SYNC_MAG_LOW_TH | 2:0 | If SYNC Magnitude is Low, Freeze HW Clamping 3 times. | |
| **41h** | **PGH_TOP_TH** | **7:0** | **Default : 0xDA** | **Access : R/W** |
| | PGA_TH_TOP | 7:0 | If AGC_FINE[11:0]>=16*PGA_TH_TOP[7:0], use smaller PGA and 16*PGA_H2L[7:0]. | |
| **42h** | **PGA_BOT_TH** | **7:0** | **Default : 0x40** | **Access : R/W** |
| | PGA_TH_BOT | 7:0 | If AGC_FINE[11:0]<=16*PGA_TH_BOT[7:0], use larger PGA and 16*PGA_L2H[7:0]. | |
| **43h** | **AGC_CTRL1** | **7:0** | **Default : 0x14** | **Access : R/W** |
| | - | 7 | Reserved. | |

## Video Decoder Register (Bank = 02)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | AGC_MD | 6:5 | 00: Auto, REG_AGC_K used for both search and lock.<br>01: Auto, REG_AGC_K used for search, clipping delta-gain=-1, 0, +1 for lock.<br>10: Freeze gain.<br>11: Load gain=AGC_FINE*16.<br>Default=1. | |
| | AGC_LOCK_CTRL | 4 | AGC Lock Control. | |
| | AGC_TYPE | 3:2 | 00: Sync.<br>01: Sync.<br>10: Color bust.<br>11: Hybrid of 1 and 2.<br>Default=1, HSYNC as primary reference, color burst is for ACC. | |
| | AGC_LOWTH_PGA | 1:0 | During PGA switching, PGA must be larger than AGC_LOWTH_PGA. | |
| **44h** | **AGC_FINE** | **7:0** | **Default : 0xC0** | **Access : R/W** |
| | AGC_FINE | 7:0 | Used when AGC_MODE=11. | |
| **45h** | **AGC_CTRL2** | **7:0** | **Default : 0x42** | **Access : R/W** |
| | AGC_AVGL | 7:5 | AGC average lines=2^( AGC_AVGL + 1). | |
| | - | 4 | Reserved. | |
| | AGC_WAITL | 3:1 | Lines to wait for analog settling down=2^( AGC_WAITL) after each gain update. | |
| | - | 0 | Reserved. | |
| **46h** | **AGC_K_CTRL** | **7:0** | **Default : 0x73** | **Access : R/W** |
| | AGC_K_FAST | 7:4 | Fast-attack AGC update speed.<br>Delta_gain=+-(AGC_K_FAST*4+3)/256*gain_true. | |
| | AGC_K | 3:0 | Sync magnitude AGC update speed.<br>Delta_gain=amp_err/256*(1+ AGC_K)/32*gan_true. | |
| **47h** | **AGC_CTRL3** | **7:0** | **Default : 0x3F** | **Access : R/W** |
| | AGC_BKLCLIP | 7:5 | AGC Black level Clip enable. | |
| | AGC_CLIP | 4:0 | The sync magnitude error for AGC is bounded by +-4*REG_AGC_CLIP. | |
| **48h** | **PGA_SWTICH_TH1** | **7:0** | **Default : 0xC0** | **Access : R/W** |
| | PGA_L2H | 7:0 | Used when AGC_FINE<=PGA_TH_BOT*16.<br>Default: 3072/16=8'd192. | |
| **49h** | **PGA_SWCH_TH2** | **7:0** | **Default :** | **Access : R/W** |
| | PGA_H2L | 7:0 | Used when AGC_FINE<=PGA_TH_BOT*16.<br>Default: 1238/16 = 8'd64. | |

## Video Decoder Register (Bank = 02)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| **4Ah** | **AGC_LOWTH** | **7:0** | **Default : 0xA0** | **Access : R/W** |
| | AGC_LOWTH | 7:0 | When PGA=AGC_LOWTH_PGA, AGC_FINE[11:0] must be smaller than 16*AGC_LOWTH. | |
| **4Bh** | **PGA_OFST** | **7:0** | **Default : 0x40** | **Access : R/W** |
| | PGA_OFST | 7:0 | ADC VREF offset=VREF_min/(VREF_max-VREF_min)*4096/16. | |
| **4Ch** | **BRST_WINDOW1** | **7:0** | **Default : 0x62** | **Access : R/W** |
| | BRST_MASK_0 | 7:5 | HSYNC trailing edge trasition region Maskout for Burst Calculation. | |
| | BRST_BEG | 4:0 | Burst window Beginning position; move to SW. | |
| **4Dh** | **BRST_WINDOW2** | **7:0** | **Default : 0x40** | **Access : R/W** |
| | BRST_END | 7:0 | Burst window End position; move to SW. | |
| **4Eh** | **BK_WINDOW1** | **7:0** | **Default : 0x05** | **Access : R/W** |
| | BKPRH_CTR[8] | 7 | Back-Porch Window Center Position. | |
| | BKPRH_SEL | 6 | Back-Porch Selection. | |
| | BKPRH_AUTSW | 5:4 | Back-Porch Auto Switch. | |
| | BKPRH_WIN | 3:0 | Back-porch Window width=(*4+4). | |
| **4Fh** | **BK_WINDOW2** | **7:0** | **Default : 0x68** | **Access : R/W** |
| | BKPRH_CTR[7:0] | 7:0 | Back-Porch Window Center Position. | |
| **50h** | **BRST_TH** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | BRST_THRD | 7:4 | Burst Threshold. | |
| | BRST_AMP_THRD | 3:0 | Burst found Amplitude Threshold. | |
| **51h** | **BRSTMAG_CTRL** | **7:0** | **Default : 0x38** | **Access : R/W** |
| | BRSTMAG_CTRL | 7 | Burst Magnitude Control. | |
| | BRST_MAG[8:2] | 6:0 | Burst Magnitude value. | |
| **52h** | **COMB_LL_CTRL** | **7:0** | **Default : 0x04** | **Access : R/W** |
| | BRST_MAG[1:0] | 7:6 | Burst Magnitude value. | |
| | - | 5:4 | Reserved. | |
| | PAL_BLIND_PD_EN | 3 | NTSC; 180 degree Phase Detection Enable. | |
| | BRST_PHS_CHK_MAG | 2 | Burst Phase of the current line is ignored if BRST_MAG<BRST_MAG_AVG/8. | |
| | - | 1:0 | Reserved. | |
| **53h** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **54h** | **BRST_WINDOW3** | **7:0** | **Default : 0x23** | **Access : R/W** |
| | FSC_THRD_LINES | 7:5 | FSC Threshold Lines. | |

## Video Decoder Register (Bank = 02)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | - | 4:3 | Reserved. | |
| | FSC_TST_TRY[2] | 2 | Fsc selection 1.25*Fsc and 0.8*Fsc BPF magnitude type. | |
| | FSC_TST_TRY[1] | 1 | Fsc selection 1.0*Fsc BPF magnitude type. | |
| | FSC_TST_TRY[0] | 0 | Fsc selection BPF magnitude snapshop taken at the end of the burst window. | |
| **55h** | **COLOR_OFF** | **7:0** | **Default : 0x08** | **Access : R/W** |
| | KILL_CSPOUT | 7:6 | 00 or 01: Auto Color Kill.<br>10: Force Show Color.<br>11: Force Kill Color. | |
| | - | 5 | Reserved. | |
| | PAL_LINES_TH | 4:0 | Lines for PAL/NTSC detection=64 * PAL_LINES_TH. | |
| **56h** | **FSC443/357 DECT1** | **7:0** | **Default : 0x18** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | FSC_THRD1_PASS | 5:0 | FSC Threshold1 Pass. | |
| **57h** | **FSC443/357 DECT2** | **7:0** | **Default : 0x28** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | FSC_THRD1_FAIL | 5:0 | FSC Threshold1 Fail. | |
| **58h** | **FSC443/357 DECT3** | **7:0** | **Default : 0x10** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | FSC_THRD0_PASS | 5:0 | FSC Threshold0 Pass. | |
| **59h** | **FSC443/357 DECT4** | **7:0** | **Default : 0x20** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | FSC_THRD0_FAIL | 5:0 | FSC Threshold0 Fail. | |
| **5Ah** | **BRST_UNKNOW_TH** | **7:0** | **Default : 0x10** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | FSC_TST_MASK | 6:4 | HSYNC trailing edge Trasition region Maskout for Fsc selection filters. | |
| | FSC_THRD_NO_BRST | 3:0 | FSC Threshold for No Burst detection. | |
| **5Bh** | **FSC443/357 DECT5** | **7:0** | **Default : 0x98** | **Access : R/W** |
| | FSC_THRD_MAG_HYST[3:2] | 7:6 | FSC Threshold Magnitude of HSYNC start. | |
| | FSC_THRD_MAG_443 | 5:0 | FSC Threshold Magnitude of 4.43 MHz. | |
| **5Ch** | **FSC443/357 DECT6** | **7:0** | **Default : 0x98** | **Access : R/W** |
| | FSC_THRD_MAG_HYST[1:0] | 7:6 | FSC Threshold Magnitude of HSYNC start. | |

## Video Decoder Register (Bank = 02)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | FSC_THRD_MAG_358 | 5:0 | FSC Threshold Magnitude of 3.58 MHz. | |
| **5Dh** | **ACC_CTRL** | **7:0** | **Default : 0x08** | **Access : R/W** |
| | ACC_CTRL | 7:6 | Auto Chroma Control.<br>01: Reset Chroma_Gain=1.<br>11: Load Chroma_Gain=ACC_GAIN[13:0]/64. | |
| | ACC_GAIN[5:0] | 5:0 | Auto-Chroma-Control Gain. | |
| **5Eh** | **ACC_GAIN** | **7:0** | **Default : 0x20** | **Access : R/W** |
| | ACC_GAIN[13:6] | 7:0 | Auto-Chroma-Control Gain. | |
| **5Fh** | **AGC_DELTA** | **7:0** | **Default : 0x28** | **Access : R/W** |
| | AGC_DELTA[7:5] | 7:5 | AGC Delta value. | |
| | WP_SIM_SPD | 4:3 | WP Simulation Speedup. | |
| | WP_LVL_SPD | 2:0 | WP Level Speedup. | |
| **60h** | **WP_CTRL1** | **7:0** | **Default : 0x15** | **Access : R/W** |
| | ACC_C_PEAK_LPF | 7:6 | Chroma Peak Detection Update Speed.<br>00: Slow, Narrow-Band-Width.<br>11: Fast, Wide-Band-Width. | |
| | - | 5 | Reserved. | |
| | WP_TH[8] | 4 | Desired white level=512+REG_WP_TH. | |
| | AGC_K_WP | 3:0 | White peaking AGC update speed.<br>Delta_gain=white_err/256*(1+REG_AGC_K)/<br>32*gain_true. | |
| **61h** | **WP_THRD** | **7:0** | **Default : 0x24** | **Access : R/W** |
| | WP_THRD[7:0] | 7:0 | White Peak Threshold value. | |
| **62h** | **AP_SYNTHRD2REAGC** | **7:0** | **Default : 0x78** | **Access : R/W** |
| | WP_SYNTHRD2REAGC | 7:0 | WP Sync Threshold of AGC. | |
| **63h ~ 64h** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **65h** | **AGC_CTRL4** | **7:0** | **Default : 0x55** | **Access : R/W** |
| | - | 7:2 | Reserved. | |
| | WP_WAITTH | 1:0 | Number of sync-mag AGC operations before WP mode.<br>00: 255 operations.<br>01: 127 operations.<br>10: 63 operations.<br>11: 31 operations. | |

## Video Decoder Register (Bank = 02)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| **66h** | **WP_CTRL2** | **7:0** | **Default : 0x70** | **Access : R/W** |
| | WP_MODE | 7:5 | 0xx: Internally automatic white-peaking control.<br>100: Disable white-peaking.<br>101: Hold sync magnitude AGC if white level is too high.<br>110: Reserved.<br>111: Normal white-peaking AGC. | |
| | WP_MONTR_SPD | 4:2 | WP Monitor Speed. | |
| | ADCOVSLE_THRD | 1:0 | WP Threshold Selection. | |
| **67h** | **WP_REDO** | **7:0** | **Default : 0x17** | **Access : R/W** |
| | ROUND_CTRL | 7:5 | AFEC signal rounding selection. | |
| | REMOV_HF_NOISE | 4 | Enable 13-tap CVBS low-pass filter to Remove High-Frequency Noise. | |
| | ROUND_CTRL[3:2] | 3:2 | 7-tap chroma-trap filter, CCTRAP, Rounding.<br>00: Truncate.<br>01: Round.<br>10: Dither. | |
| | ROUND_CTRL[1] | 1 | AFEC self-test 1D luminance Rounding.<br>0: Truncate.<br>1: Round. | |
| | ROUND_CTRL[0] | 0 | AFEC self-test 1D chroma Rounding.<br>0: Truncate.<br>1: Round. | |
| **68h** | **CLK_CTRL1** | **7:0** | **Default : 0x45** | **Access : R/W** |
| | ADC_84_ROUND | 7:6 | Round control for 8Fsc-to-4Fsc downsampling.<br>0: Truncate.<br>1: Round. | |
| | DAC_LATCH_INV | 5 | Option for Datalatch from 4Fsc to 8Fsc. | |
| | 3DAC_EN | 4 | Enable AFEC Data Output to DAC. | |
| | FILSEL | 3:2 | Filter Selection. | |
| | ADC_168_ROUND | 1:0 | Round Control for 16Fsc-to-8Fsc Downsampling.<br>0: Truncate.<br>1: Round. | |
| **69h** | **SRC_CTRL1** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | SELYC | 7 | 0: YC Source from AFEC for Testing Purpose.<br>1: YC Source from Comb for Display. | |
| | - | 6:5 | Reserved. | |
| | BYPASS_Y | 4 | Bypass CVBS Source for Testing purpose. | |

## Video Decoder Register (Bank = 02)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | COMB601H_SYNC | 3 | 1: Use the HS444 as the MVDA_HS Output. | |
| | COMB601V_SYNC | 2 | 1: Use the VS444 as the MVDA_VS Output. | |
| | COMB601F_SYNC | 1 | 1: Use the Fld444 as the MVDA_F Output. | |
| | COMBPASS_SYNC | 0 | 1: The HS444 and VS444 as the Bypass SYNC.<br>0: AFEC_HS and AFEC_VS as the Bypass SYNC Output. | |
| **6Ah** | **VCR_DETECT1** | **7:0** | **Default : 0x51** | **Access : R/W** |
| | VCR_MODE | 7:6 | VCR Mode enable. | |
| | VCR_HD_DLY | 5:4 | VCR Head switch number. | |
| | - | 3 | Reserved. | |
| | VS_STB | 2:0 | VS Strobe. | |
| **6Bh** | **VCR_DETECT2** | **7:0** | **Default : 0xAA** | **Access : R/W** |
| | VCR_LDT | 7:4 | VCR Line Margin. | |
| | FAST_VT_DET | 3 | Fast Vertical Line Detection. | |
| | VCR_THRD | 2:0 | VCR Threshold. | |
| **6Ch** | **VCR_PRECOAST** | **7:0** | **Default : 0xF0** | **Access : R/W** |
| | VCR_PRECOAST | 7:4 | Pre-Coast value for VCR mode. | |
| | HV_HSLISEL_VCR | 3:2 | HSYNC Slicer Selection for VCR mode. | |
| | HV_SLILOW_SEL | 1:0 | HSYNC/VSYNC slicer Low Selection. | |
| **6Dh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **6Eh** | **VCR_VLSET** | **7:0** | **Default : 0x14** | **Access : R/W** |
| | VCR_VLSET | 7:0 | PAC/NTSC VLine tunning. | |
| **6Fh** | | **7:0** | **Default :** | **Access :** |
| | RST_AFEC_SEL | 7 | 0: Partial reset AFEC.<br>1: Global reset AFEC. | |
| | - | 6:4 | Reserved. | |
| | DPL_DDE_EN | 3 | DPL double DE Enable. | |
| | DDE_EN | 2 | Double DE Enable. | |
| | DPL_HS_EN | 1 | DPL HS Enable. | |
| | DPL_DE_EN | 0 | DPL DE Enable. | |
| **70h** | **INI_CTRL1** | **7:0** | **Default : 0x84** | **Access : R/W** |
| | FSTAGC_EN | 7 | Fast AGC mode. | |
| | - | 6 | Reserved. | |
| | CLMP_BOTMD | 5:4 | Clamp on Bottom Mode. | |

## Video Decoder Register (Bank = 02)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | ADSMAL_THRD | 3:0 | Threshold for detecting Small AOC swing. | |
| **71h** | **BOTREF_LVL** | **7:0** | **Default : 0xA0** | **Access : R/W** |
| | BOTREF_LVL | 7:0 | Bottom Reference Level. | |
| **72h** | **HV_SLC_CTRL** | **7:0** | **Default : 0x37** | **Access : R/W** |
| | HV_SLCFZE | 7:6 | HSYNC/VSYNC Slice Freeze control. | |
| | HV_SLCDIF | 5:4 | HSYNC/VSYNC Slice Difference. | |
| | HV_SLCDLT | 3:0 | HSYNC/VSYNC Slice Limit. | |
| **73h** | **INI_CTRL1** | **7:0** | **Default : 0x52** | **Access : R/W** |
| | HV_VSLISEL | 7:6 | 00: 2/8 syn_magnitude as hslice level.<br>01: 4/8 syn_magnitude as hslice level.<br>10: 5/8 syn_magnitude as hslice level.<br>11: 6/8 syn_magnitude as hslice level. | |
| | HV_HSLISEL | 5:4 | 00: 2/8 syn_magnitude as vslice level.<br>01: 4/8 syn_magnitude as vslice level.<br>10: 5/8 syn_magnitude as vslice level.<br>11: 6/8 syn_magnitude as vslice level. | |
| | 656_HDES_VCR_OFST | 3:0 | 656 SAV Position Offset when VCR. | |
| **74h** | **SLICE_MUX** | **7:0** | **Default : 0x97** | **Access : R/W** |
| | SLICE_MUX | 7:0 | Slicer level selection. | |
| **75h** | **656_OFST** | **7:0** | **Default : 0x40** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | 656_OFST | 6:0 | 56 SAV Position Offset in VCR mode. | |
| **76h** | **656_CTRL1** | **7:0** | **Default : 0x02** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | DBCLK_TEST | 4 | Clock Testing. | |
| | - | 3 | Reserved. | |
| | 656_BLNK_MD | 2 | 656 Blank Mode. | |
| | 656_EN | 1 | Enable 656 mode. | |
| | ABNML_CHK | 0 | Abnormal check enable. | |
| **77h** | **656_BLNK_MAX** | **7:0** | **Default : 0x02** | **Access : R/W** |
| | 656_BLNK_MAX[7:0] | 7:0 | 656 Blink Max value. | |
| **78h** | **YUV** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | YUV[7:0] | 7:0 | Used as Input of the 4Fsc-to-16Fsc Up-sampling if SELUPS=3. | |
| **79h** | **656_HDES1** | **7:0** | **Default : 0x18** | **Access : R/W** |

## Video Decoder Register (Bank = 02)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | 656_HDES_O[9:2] | 7:0 | SDA start position. (656_HDESM, 656_HDESL)<br>ITU656 SAV Position.<br>For VCR, 656_HDES=656_HDES_o-656_HDES_VCR_OFST*4.<br>Otherwise, 656_HDES=656_HDES_o. | |
| **7Ah** | **656_HDES2** | **7:0** | **Default : 0x20** | **Access : R/W** |
| | 656_HDES_O[1:0] | 7:6 | ITU656 SAV position. | |
| | - | 5:2 | Reserved. | |
| | 656_INV_F | 1 | 656 Field Inverse. | |
| | - | 0 | Reserved. | |
| **7Bh** | **656_HDEW** | **7:0** | **Default : 0xB3** | **Access : R/W** |
| | 656_HDEW | 7:0 | ITU656 active data Width (*8+7). | |
| **7Ch** | **SLMIS_CTRL** | **7:0** | **Default : 0xC0** | **Access : R/W** |
| | SLMIS_CTRL[7:0] | 7:0 | Enable Slice Miss freeze. | |
| **7Dh** | **NOISE_MLINE** | **7:0** | **Default : 0x04** | **Access : R/W** |
| | NOISE_MLINE | 7:0 | Move Noise level during specify Line Number. | |
| **7Eh** | **656_CTRL2** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | 656_CLKINV | 7 | Used for FPGA testing. | |
| | 656_CLKDLY | 6:5 | Used for FPGA testing. | |
| | 656_LSTSEL | 4 | Used for FPGA testing. | |
| | 656_TEST | 3:2 | Used for FPGA testing. | |
| | TEST_MODE | 1:0 | Used for FPGA testing. | |
| **7Fh** | **444_VD_CTRL** | **7:0** | **Default : 0x62** | **Access : R/W** |
| | SELDAC | 7:6 | Source for 3 DACs.<br>00: Comb.<br>01: AFEC Test Mode.<br>10: 444.<br>11: Upsampling Source. | |
| | 3DAC_INSHV | 5 | Insert HV into Display DAC Source. | |
| | 3DAC_HSEL | 4 | Insert H's Source Selection.<br>0: Window PLL.<br>1: Display PLL. | |
| | 3DAC_INSBLACK | 3 | Insert Black Level back to DAC Source. | |
| | REG_SELFB | 2 | 0: YCbCr Source from AFEC Test Mode.<br>1: YCbCr Source from Comb444. | |

## Video Decoder Register (Bank = 02)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | REG_SELUPS | 1:0 | Upsampling Source.<br>10: Test Mode 444.<br>11: Comb YCbCr 444. | |
| **80h** | **NCO_FSC0** | **7:0** | **Default : 0x48** | **Access : R/W** |
| | FSC_NCO0[23:16] | 7:0 | {NCO_FSC0} 4.43 MHz synthesis clock.<br>Frequency Synthesizer 4*Fsc for 4.43361875 MHz.<br>(For REG_FSC_TABLE[4]=0.)<br>Syncthesis-base/(4*Fsc)*2^22/8. | |
| **81h** | **NCO_FSC0** | **7:0** | **Default : 0x2D** | **Access : R/W** |
| | FSC_NCO0[15:8] | 7:0 | {NCO_FSC0} 4.43 MHz synthesis clock. | |
| **82h** | **NCO_FSC0** | **7:0** | **Default : 0x01** | **Access : R/W** |
| | FSC_NCO0[7:0] | 7:0 | {NCO_FSC0} 4.43 MHz synthesis clock. | |
| **83h** | **NCO_FSC1** | **7:0** | **Default : 0x59** | **Access : R/W** |
| | FSC_NCO1[23:16] | 7:0 | Frequency synthesizer 4*Fsc for 3.57954545 MHz (For FSC_TABLE[4]=0). | |
| **84h** | **NCO_FSC1** | **7:0** | **Default : 0x65** | **Access : R/W** |
| | FSC_NCO1[15:8] | 7:0 | {NCO_FSC1} 3.579 MHz synthesis clock. | |
| **85h** | **NCO_FSC1** | **7:0** | **Default : 0x97** | **Access : R/W** |
| | FSC_NCO1[7:0] | 7:0 | {NCO_FSC1} 3.579 MHz synthesis clock. | |
| **86h** | **NCO_FSC2** | **7:0** | **Default : 0x59** | **Access : R/W** |
| | FSC_NCO2[23:16] | 7:0 | Frequency Syncthesizer 4*Fsc for 3.57561149 MHz (For FSC_TABLE[4] =0). | |
| **87h** | **NCO_FSC2** | **7:0** | **Default : 0x7E** | **Access : R/W** |
| | FSC_NCO2[15:8] | 7:0 | {NCO_FSC2} 3.582 MHz synthesis clock. | |
| **88h** | **NCO_FSC2** | **7:0** | **Default : 0x74** | **Access : R/W** |
| | FSC_NCO2[7:0] | 7:0 | {NCO_FSC2} 3.582 MHz synthesis clock. | |
| **89h** | **NCO_FSC3** | **7:0** | **Default : 0x59** | **Access : R/W** |
| | FSC_NCO3[23:16] | 7:0 | Frequency Sunthesizer 4*Fsc for 3.58205625 MHz (For FSC_TABLE[4] = 0). | |
| **8Ah** | **NCO_FSC3** | **7:0** | **Default : 0x55** | **Access : R/W** |
| | FSC_NCO3[15:8] | 7:0 | {NCO_FSC3} 3.576 MHz synthesis clock. | |
| **8Bh** | **NCO_FSC3** | **7:0** | **Default : 0x8B** | **Access : R/W** |
| | FSC_NCO3[7:0] | 7:0 | {NCO_FSC3} 3.576 MHz synthesis clock. | |
| **8Ch** | **REG_FSC_NCO4** | **7:0** | **Default : 0x4A** | **Access : R/W** |

## Video Decoder Register (Bank = 02)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | FSC_NCO4[23:16] | 7:0 | Requency Synthesizer 4*Fsc for 4.28515625 MHz<br>(For REG_FSC_TABLE[4] = 0). | |
| **8Dh** | **FSC_NCO4** | **7:0** | **Default : 0xAD** | **Access : R/W** |
| | FSC_NCO4[15:8] | 7:0 | Requency Synthesizer 4*Fsc for 4.28515625 MHz<br>(For REG_FSC_TABLE[4] = 0). | |
| **8Eh** | **FSC_NCO4** | **7:0** | **Default : 0x27** | **Access : R/W** |
| | FSC_NCO4[7:0] | 7:0 | Requency Synthesizer 4*Fsc for 4.28515625 MHz<br>(For REG_FSC_TABLE[4] = 0). | |
| **8Fh** | **FSC_TABLE** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | FSC_TABLE[4] | 4 | Frequency Synthesizer Control.<br>0: FSC_NCO0, 1, 2, 3, and 4 are used.<br>1: Specified by FSC_TABLE[3:2]. | |
| | FSC_TABLE[3:2] | 3:2 | Frequency Synthesizer Base.<br>00: 160MHz.<br>01: 15*14.31818MHz.<br>10: 216MHz.<br>11: 15*14.31818MHz.<br>Only valid for FSC_TABLE[4] =1. | |
| | FSC_TABLE[1:0] | 1:0 | Frequency Synthesizer Output.<br>00: 4*FSC.<br>01: 8*FSC.<br>10: 16*FSC.<br>11: 16*FSC. | |
| **90h** | **FSC_NCO_ERR_443** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | FSC_NCO_ERR_443 [15:8] | 7:0 | Frequency Synthesizer 4*Fsc Error for 4.43MHz; 2's Complement<br>(Auto scaled internally for 3.58MHz). | |
| **91h** | **FSC_NCO_ERR_443** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | FSC_NCO_ERR_443 [7:0] | 7:0 | Frequency Synthesizer 4*Fsc Error for 4.43MHz; 2's Complement<br>(Auto scaled internally for 3.58MHz). | |
| **92h** | **WINIIR_THRD_CTRL** | **7:0** | **Default : 0xA7** | **Access : R/W** |
| | WINIIR_THRD1 | 7:4 | IIR Window Threshold 1. | |
| | WINIIR_THRD0 | 3:0 | IIR Window Threshold 0. | |
| **93h** | **WINFIR_THRD_CTRL** | **7:0** | **Default : 0xA4** | **Access : R/W** |
| | WINFIR_THRD1 | 7:4 | IIR Window Threshold 1. | |
| | WINFIR_THRD0 | 3:0 | IIR Window Threshold 0. | |

## Video Decoder Register (Bank = 02)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| **94h** | **SPL_SPD_CTRL1** | **7:0** | **Default : 0x14** | **Access : R/W** |
| | SPL_SPD_FORCE | 7:5 | Coarse HSYNC PLL Tracking Speed.<br>Bit[2] forces using Bit[1:0].<br>SPL_SPD=3: Fastest.<br>SPL_SPD=0: Slowest. | |
| | SPL_SPD_SRCH | 4:3 | Coarse HSYNC PLL tracking Speed during HSYNC-Search. | |
| | SPL_SPD_CLEAN | 2:1 | Coarse HSYNC PLL tracking Speed for Clean signal. | |
| | - | 0 | Reserved. | |
| **95h** | **SPL_SPD_CTRL2** | **7:0** | **Default : 0x2A** | **Access : R/W** |
| | SPL_SPD_NOISY | 7:6 | Coarse HSYNC PLL tracking Speed for Noisy signal. | |
| | SPL_SPD_VCR | 5:4 | Coarse HSYNC PLL phase tracking Speed for VCR outside VSYNC. | |
| | SPL_SPD_VCR_V | 3:2 | Coarse HSYNC PLL Phase Tracking Speed for VCR during VSYNC. | |
| | SPL_SPD_VCR_PRE | 1:0 | Coarse HSYNC PLL HSYNC-search lines.<br>00: 48.<br>01: 64.<br>10: 80.<br>11: 96. | |
| **96h** | **EDGES_NOISY_THRD** | **7:0** | **Default : 0xA0** | **Access : R/W** |
| | NOISE_DC_SEL | 7:6 | Noise magnitude estimation DC level Selection.<br>00: IIR_8.<br>01: IIR_8.<br>10: CCTRAP_13.<br>11: CCTRAP. | |
| | EDGES_NOISY | 5:0 | Threshold of the average number of sliced Edges per Line to determine Noisy mode (/ 4). | |
| **97h** | **EDGES_CLEAN_THRD** | **7:0** | **Default : 0x05** | **Access : R/W** |
| | SYNC_INMUX[2:1] | 7:6 | Slicer input pre-filter selection.<br>00: CCTRAP.<br>01: CCTRAP_13.<br>10: IIR_8.<br>11: IIR_16. | |
| | SYNC_INMUX[0] | 5 | Slicer Auxiliary Pre-Filter Selection.<br>0: IIR_8.<br>1: IIR_16. | |
| | - | 4 | Reserved. | |

## Video Decoder Register (Bank = 02)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | EDGES_CLEAN | 3:0 | Threshold of the average number of sliced Edges per line to determine Clean mode (/ 4). | |
| **98h** | **SYNC_WIN_CTRL1** | **7:0** | **Default : 0x43** | **Access : R/W** |
| | SYNC_INMUX_VCR [2:0] | 7:5 | HSYNC slicer Input selection. | |
| | - | 4 | Reserved. | |
| | WIN_NOISY | 3:0 | Ciarse HSYNC PLL PD Limitaion Window Width for Noisy Mode (*8+7). | |
| **99h** | **SYNC_WIN_CTRL2** | **7:0** | **Default : 0x88** | **Access : R/W** |
| | SYNC_WIN | 7:4 | Coarse HSYNC PLL SYNC-lost detection Window width (*4+4). | |
| | SYNC_WIN_SRCH | 3:0 | Coarse HSYNC PLL SYNC-found detection Window width (*4+4). | |
| **9Ah** | **SYNC_CTRL1** | **7:0** | **Default : 0xF0** | **Access : R/W** |
| | SYNC_THRD_MISS | 7:4 | Coarse HSYNC PLL SYNC search fail Threshold. | |
| | - | 3:2 | Reserved. | |
| | SPL_SRCH_LENG | 1:0 | SPL Search Length. | |
| **9Bh** | **SYNC_CTRL2** | **7:0** | **Default : 0x10** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | SYNC_THRD | 5:0 | Coarse HSYNC PLL SYNC search pass (SYNC Found) Threshold (*4+3). | |
| **9Ch** | **SYNC_CTRL3** | **7:0** | **Default : 0x1C** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | SYNC_THRD_LOST | 6:0 | Coarse HSYNC PLL SYNC SYNC-Lost Threshold (*16+15). | |
| **9Dh** | **DPL_NSPL_HIGH** | **7:0** | **Default : 0x6C** | **Access : R/W** |
| | DPL_NSPL[10:3] | 7:0 | PI-Type Display PLL Number of Samples per Line (MSB); typically 864. | |
| **9Eh** | **DPL_NSPL_LOW** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | DPL_NSPL[2:0] | 7:5 | PI-type Display PLL Number of Samples per Line (LSB); typically 864. | |
| | DPLL_TRUE8FSC | 4 | DPLL under 8 Fsc mode. | |
| | - | 3:0 | Reserved. | |
| **9Fh** | **SPL_K2_VCR** | **7:0** | **Default : 0x40** | **Access : R/W** |
| | SPL_K2_VCR | 7:6 | Coarse HSYNC PLL Frequency Tracking Speed for VCR. | |
| | SPL_NSPL_LMT | 5:0 | PI-type display PLL frequency coasts if the coarse HSYNC PLL deviation is larger than +/- 4*SPL_NSPL_LMT (Try). | |
| **A0h** | **DPL_K1_FORCE** | **7:0** | **Default : 0x20** | **Access : R/W** |

## Video Decoder Register (Bank = 02)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | DPL_K_FORCE | 7 | Force DPL K value. | |
| | - | 6 | Reserved. | |
| | DPL_K1 | 5:0 | PI-type Display PLL phase tracking coefficient K1. | |
| **A1h** | **DPL_K2_FORCE** | **7:0** | **Default : 0x60** | **Access : R/W** |
| | DPL_K2 | 7:0 | PI-type Display PLL frequency tracking coefficient K2. | |
| **A2h** | **DPL_K1_NOISY** | **7:0** | **Default : 0x10** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | DPL_K1_NOISY | 5:0 | PI-type Display PLL phase tracking coefficient for Noisy broadcast. | |
| **A3h** | **DPL_K2_NOISY** | **7:0** | **Default : 0x04** | **Access : R/W** |
| | DPL_K2_NOISY | 7:0 | PI-type Display PLL frequency tracking coefficient for Noisy broadcast. | |
| **A4h** | **DPL_K1_VCR** | **7:0** | **Default : 0x34** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | DPL_K1_VCR | 5:0 | PI-type Display PLL phase tracking coefficient for VCR. | |
| **A5h** | **DPL_K2_VCR** | **7:0** | **Default : 0x6A** | **Access : R/W** |
| | DPL_K2_VCR | 7:0 | PI-type Display PLL frequency tracking coefficient for VCR. | |
| **A6h** | **DPL_K1_VCR_V** | **7:0** | **Default : 0x34** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | DPL_K1_VCR_V | 5:0 | PI-type Display PLL phase tracking coefficient for VCR during VSYNC. | |
| **A7h** | **DPL_K2_VCR** | **7:0** | **Default : 0x2C** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | DPL_VCR_FADE_SPD | 5:4 | PI-type Display PLL PD_MAX fading speed from VSYNC to active lines.<br>00: Slow.<br>11: Fast. | |
| | DPL_VCR_FADE_START | 3:0 | PI-type Display PLL PE_MAX fading Start lines (*2). | |
| **A8h** | **DPL_K1_FAST** | **7:0** | **Default : 0x30** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | DPL_K1_FAST | 5:0 | PI-type Display PLL phase tracking coefficient for Fast mode and initialization. | |
| **A9h** | **DPL_K2_FAST** | **7:0** | **Default : 0x65** | **Access : R/W** |
| | DPL_K2_FAST | 7:0 | PI-type Display PLL frequency tracking coefficient for Fast mode and initialization. | |
| **AAh** | **DPL_CTRL1** | **7:0** | **Default : 0x08** | **Access : R/W** |

## Video Decoder Register (Bank = 02)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | - | 7:4 | Reserved. | |
| | DPL_FAST_LINES | 3:0 | PI-type Display PLL Fast Mode Lines. (*256) | |
| **ABh** | **DPL_PD_MAX** | **7:0** | **Default : 0x10** | **Access : R/W** |
| | DPL_PD_MAX | 7:0 | PI-type Display PLL Phase Detector (DPL_PD) Limit.<br>If bit[7]=1, force using bit[6:0]. | |
| **ACh** | **DPL_PD_MAX_VCR** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | DPL_PD_MAX_VCR | 7:0 | PI-type Display PLL phase detector (DPL_PD) limit for VCR ouside VSYNC area. | |
| **ADh** | **REG_656_CTRL** | **7:0** | **Default : 0x3A** | **Access : R/W** |
| | REG_656_OPTION1 | 7 | Line Middle Method 0 Selection. | |
| | REG_656_OPTION0 | 6 | Line Middle Method 1 Selection. | |
| | REG_DPL_WAIT_LENG | 5:4 | DPL Wait Length. | |
| | REG_DPL_NCO_RST | 3 | DPL NCO Reset enable. | |
| | DPL_FAST_RE_DO | 2 | PI-type Display PLL Re-Do Fast Mode. | |
| | DPL_NO_STOP | 1 | PI-type Display PLL Never Stops. (Free Run when HSYNC not found.) | |
| | DPL_COAST_T_FORCE | 0 | PI-type Display PLL Frequency Frozen Always. (except when Fast Mode and Initialization) | |
| **AEh** | **DPL_COAST_CTRL** | **7:0** | **Default : 0xB8** | **Access : R/W** |
| | VSYNC_SEL | 7 | VSYNC source Selection. | |
| | - | 6 | Reserved. | |
| | COAST_V_ALWAYS | 5 | Always V Coast function. | |
| | DPL_COAST_T_LINES | 4:0 | Lines where 656 PLL coast frequency during V.<br>PI-type Display PLL Frequency Frozen Lines during VSYNC. (*2) | |
| **AFh** | **DPL_CTRL2** | **7:0** | **Default : 0x85** | **Access : R/W** |
| | DPL_LOST_LINES | 7:4 | PI-type Dislay PLL Threshold on Lines to Determine Out-of –Lock. (*64). | |
| | DPL_LOST_WIN | 3:0 | PI-type Display PLL HSYNC Window Width to Detect Out-of-Lock. (*8) | |
| **B0h** | **DPL_K1_FREE** | **7:0** | **Default : 0x86** | **Access : R/W** |
| | DPL_K1_FREE | 7:4 | PI-type Dipslay PLL Phase Tracking Coefficient during HSYNC not found. | |
| | BKPRH_JUMP_MAX | 3:0 | Back-Porch-Jump Maximal Lines. (Try.) (Can move to SW Clmp.) | |
| **B1h** | **BKPRH_JUMP_CTRL** | **7:0** | **Default : 0x06** | **Access : R/W** |

## Video Decoder Register (Bank = 02)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | - | 7 | Reserved. | |
| | BKPRH_JUMP_MV_EN | 6:5 | Back-Porch-Jump used to Pause Clamping when Macrovision found (if set 01). (Try.) (Can move to SW Clmp.) | |
| | BKPRH_JUMP_THRD | 4:0 | Back-Porch-Jump Threshold. (*32+32). (Try.) (Can move to SW Clmp.) | |
| **B2h** | **SPL_DELAY_FIR** | **7:0** | **Default : 0x19** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | SPL_DELAY_FIR | 5:0 | Coarse HSYNC PLL Delay with Respect to the Actual HSYNC Leading Edge if SYNC_INMUX selects CCTRAP or CCTRAP_13. | |
| **B3h** | **SPL_DELAY_IIR** | **7:0** | **Default : 0x1E** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | SPL_DELAY_IIR | 6:0 | Coarse HSYNC PLL Delay with Respect to the Actual HSYNC Leading Edge if SYNC_INMUX selects IIR_8 or IIR_16. | |
| **B4h** | **REG_PB_CTRL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | REG_PB_EN | 7 | 0: Hold ADC Data Probe.<br>1: Enable ADC Data Probe. | |
| | REG_PB_4FSC | 6 | 0: Probe 8Fsc ADC Data when 8Fsc Clock.<br>1: Probe 4Fsc ADC Data when 8Fsc Clock. | |
| | REG_PB_LINE | 5:4 | 1: Probe ADC Data in Next Line. | |
| | REG_PB_YC | 3 | 0: Probe Y(CBVS) ADC Data.<br>1: Probe C ADC Data. | |
| | REG_PB_10B | 2 | 0: Probe 8 bit Data.<br>1: Probe 10 bit Data. | |
| | - | 1:0 | Reserved. | |
| **B5h** | **PROBE_OUT** | **7:0** | **Default : 0x00** | **Access : R** |
| | PROBE_OUT | 7:0 | ADC Probe Data.<br>(RP_LSB) ? {6'b0, PROBE_OUT1[1:0]} : PROBE_OUT1[9:2]. | |
| **B6h** | **REG_PB_HPOS** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | REG_PB_HPOS[7:0] | 7:0 | Start Probe Horizontal Position. (lower 8 bits) | |
| **B7h** | **REG_PB_BPOS1** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | REG_PB_VPOS[10:8] | 5:4 | Start Probe Vertical Position. (upper 3 bits) | |
| | REG_PB_HPOS[10:8] | 2:0 | Start Probe Horizontal Position. (upper 3 bits) | |

| Video Decoder Register (Bank = 02) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| **B8h** | **REG_PB_VPOS2** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | REG_PB_VPOS[7:0] | 7:0 | Start Probe Vertical Position. (lower 8 bits) | |
| **B9h** | **REG_WP_HOVER THRD** | **7:0** | **Default : 0x1F** | **Access : R/W** |
| | REG_WP_HOVER THRD[7:0] | 7:0 | Overflow Threshold of ADC Value. | |
| **BAh** | **REG_WP_HUNDERT HRD** | **7:0** | **Default : 0x1F** | **Access : R/W** |
| | REG_WP_HUNDER THRD[7:0] | 7:0 | Underflow Threshold of ADC Value. | |
| **BBh ~ FFh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |

## Comb-Filter Register (Bank = 03, Registers 01h ~ 9Fh)

| Comb-Filter Register (Bank=03, Registers 01h ~ 9Fh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| **00h ~ 09h** | **-** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:0 | Reserved. | |
| **10h** | **COMBCFGA** | **7:0** | **Default : 0x12** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | SVDOCBP | 6 | Band Pass Filter for S-Video C Channel to kill the DC Level. | |
| | DIRADCIN | 5 | Direct use ADC Input (Bypass AFEC). | |
| | DDETSRCSEL | 4 | Degree Detect Source Select.<br>0: Without ACC.<br>1: After ACC. | |
| | MANUCOMB | 3 | 0: Auto Select Working Mode.<br>1: Manual Select Working Mode. | |
| | WORKMD | 2:0 | Working Mode.<br>000: Off.<br>001: Notch.<br>010: 2D Comb.<br>011: 3D Comb.<br>100: 3D Comb with History. | |
| **11h** | **COMBCFGB** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | FORCE8BIT | 7 | Force 8 bit. | |
| | GOODHS | 6 | Using Free Run HSYNC in Standard Input. | |
| | AFEC_DEM | 5 | Select AFEC Demodulation. | |
| | PALCMINV | 4 | PalCmpUp Inverse. | |
| | - | 3 | Reserved. | |
| | SYNCONY | 2 | SYNC on Y. | |
| | CRMA_OFF | 1 | Turn Off the Chroma of video decoder output.<br>0: Normal.<br>1: Off. | |
| | BST_OFF | 0 | Turn Off the Color Burst of video decoder output.<br>0: Normal.<br>1: Off. | |
| **12h** | **COMBCFGC** | **7:0** | **Default : 0x10** | **Access : R/W** |
| | FREESYNC | 7 | H/V SYNC Free Run. | |
| | FREECNTMD | 6 | Free Run Counter Mode.<br>0: NTSC.<br>1: PAL. | |

| Comb-Filter Register (Bank=03, Registers 01h ~ 9Fh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| | SNOWTYPE | 5:4 | Snow Type.<br>00: Never snow.<br>01: Snow when VDOMD = 7.<br>10, 11: Force snow. | |
| | RND_MD | 3:2 | Rounding Mode.<br>00: Truncate.<br>01: Rounding.<br>10: Dithering.<br>11: Error Feedback. | |
| | - | 1:0 | Reserved. | |
| **13h** | **YGAIN** | **7:0** | **Default : 0xC8** | **Access : R/W** |
| | YGAIN | 7:0 | Luma Gain for U/V Demodulation.<br>Out=In*Gain+16.<br>0: 0.<br>128: 1.<br>255: 1.992. | |
| **14h** | **CBGAIN** | **7:0** | **Default : 0x96** | **Access : R/W** |
| | CBGAIN | 7:0 | Cb Gain for U/V Demodulation. | |
| **15h** | **CRGAIN** | **7:0** | **Default : 0x6A** | **Access : R/W** |
| | CRGAIN | 7:0 | Cr Gain for U/V Demodulation. | |
| **16h** | **DITHCTRLA** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | CTSTDITHEN | 6 | Dithering when Contrast Adjustment. | |
| | CTSTDITHPOS | 5:4 | Dithering Position (Offset) of Contrast. | |
| | - | 3 | Reserved. | |
| | SATDITHEN | 2 | Dithering when Saturation Adjustment. | |
| | SATDITHPOS | 1:0 | Dithering Position (Offset) of Saturation. | |
| **17h** | **DITHCTRLB** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | YDEMDITHEN | 6 | Dithering when Demodulation Y-Gain. | |
| | YDEMDITHPOS | 5:4 | Dithering Position (Offset) of Y Gain. | |
| | - | 3 | Reserved. | |
| | CDEMDITHEN | 2 | Dithering when Demodulation C-Gain. | |
| | CDEMDITHPOS | 1:0 | Dithering Position (Offset) of C Gain. | |
| **18h** | **HORSTPOS** | **7:0** | **Default : 0xC0** | **Access : R/W** |

## Comb-Filter Register (Bank=03, Registers 01h ~ 9Fh)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | HORSTPOS[7:0] | 7:0 | Horizontal Starting Position.<br>0..255 : -128..127. | |
| **19h** | **FRHTOTL** | **7:0** | **Default : 0x8D** | **Access : R/W** |
| | FRHTOTL | 7:0 | Free Run HSYNC Total Low Byte. | |
| **1Ah** | **FRHTOTH** | **7:0** | **Default : 0x03** | **Access : R/W** |
| | FRHTOTH | 7:0 | Free Run HSYNC Total High Byte. | |
| **1Bh** | **PHSDETCFG** | **7:0** | **Default : 0x83** | **Access : R/W** |
| | PHSDETEN | 7 | Line-Lock Phase Detection Enable. | |
| | PHSDETINV | 6 | Output Inverse. | |
| | - | 5:3 | Reserved. | |
| | PHSDETSFT | 2:0 | Shift Bit Number.<br>000: Only output integer.<br>001: Output shift right 1 bit.<br>...<br>111: Output shift right 7 bit. | |
| | **CTRLSWCH** | **7:0** | **Default : 0xF0** | **Access : R/W** |
| | HSFRAFEC | 7 | H-SYNC from AFEC. | |
| | VSFRAFEC | 6 | V-SYNC from AFEC. | |
| | BLKFRAFEC | 5 | Black Level from AFEC. | |
| | DEGFRAFEC | 4 | Demodulation Degree from AFEC. | |
| | - | 3:2 | Reserved. | |
| | STDSEL | 1:0 | NTSC/PAL Decision.<br>01: force NTSC.<br>10: force PAL.<br>Other: Auto detect. | |
| **20h** | **COMB2DCFGA** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:0 | Reserved. | |
| **21h** | **COMB2DCFGB** | **7:0** | **Default : 0xD4** | **Access : R/W** |
| | CRMATRP_EN | 7 | C-Trap of C Enable. | |
| | NCHMD_Y[2:0] | 6:4 | Notch Mode of Y. | |
| | CHRMFLT_EN | 3 | Chroma Median Filter Enable.<br>0: Off<br>1: Enable | |
| | NCHMD_C[2:0] | 2:0 | Notch Mode of C. | |
| **22h** | **COMB2DCFGC** | **7:0** | **Default : 0x83** | **Access : R/W** |

## Comb-Filter Register (Bank=03, Registers 01h ~ 9Fh)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | LNENDPOS | 7:4 | Line End Offset.<br>0~15: -8~7. | |
| | SHARP2DMD | 3:2 | Sharpness Mode of 2D Comb.<br>00: Off.<br>01: Mode 1.<br>10: Mode 2.<br>11: Mode 3. | |
| | CDEMCHK | 1 | Chroma Vertical Check (dem). | |
| | FORCE5LN | 0 | Force use 5 Line even in 1D. | |
| **23h** | **HDYGAIN** | **7:0** | **Default : 0x40** | **Access : R/W** |
| | HDYGAIN | 7:0 | Gain of Chroma Trap for Hanging Dots. | |
| **24h** | **HDCGAIN** | **7:0** | **Default : 0x20** | **Access : R/W** |
| | HDCGAIN | 7:0 | Gain of Chroma Trap for Hanging Dots. | |
| **25h** | **ETPREF** | **7:0** | **Default : 0x18** | **Access : R/W** |
| | ETPREF | 7:0 | Gain of Chroma Trap for Hanging Dots. | |
| **26h** | **ETPTHH** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | ETPTHH | 7:0 | Horizontal Entropy Threshold for Chroma Trap in 2D Comb. | |
| **27h** | **ETPTHV** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | ETPTHV | 7:0 | Vertical Entropy Threshold for Chroma Trap in 2D Comb. | |
| **28h** | **THDEM** | **7:0** | **Default : 0x10** | **Access : R/W** |
| | THDEM | 7:0 | Thresholds for 2D Comb Filter; check separated chroma complement with up/down line or not. | |
| **29h ~ 2Eh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **2Fh** | **IFCOEF** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | IFCOEF | 7:0 | If compensation Coefficient.<br>2-bit integer, 6-bit fraction.<br>Crma=C_cn–(Coef*(C_left+C_right)). | |
| **30h ~ 3Fh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **40h** | **HVDETCFG** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | SENSSYNCLVL | 7:5 | Sensitivity of SYNC Level Detect. | |
| | - | 4:3 | Reserved. | |

## Comb-Filter Register (Bank=03, Registers 01h ~ 9Fh)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | BLNKDETMD | 2 | Blank Level Detect Mode.<br>0: Either 240 or 252.<br>1: 230~262 is possible. | |
| | VDETMD | 1:0 | Vertical Timing Detect Mode.<br>00, 01: Auto detect.<br>10: force 525 line system.<br>11: force 625 line system. | |
| **41h** | **SENSSIGDET** | **7:0** | **Default : 0x08** | **Access : R/W** |
| | SENSSIGDET | 7:0 | Sensitivity of Signal Detect. | |
| **42h** | **SYNCLVLTLRN** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | SYNCLVLTLRN | 7:0 | SYNC Level Tolerance. | |
| **43h** | **VCRCOASTLEN** | **7:0** | **Default : 0x60** | **Access : R/W** |
| | VCRCOASTLEN | 7:0 | VCR Coast Length. | |
| **44h** | **REGHBIDLY** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REGHBIDLY | 7:0 | Horizontal Blanking Region Delay.<br>0 ... 255 : Delay -128 .. 127 pixels. | |
| **45h ~ 47h** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **48h** | **DEGDETCFG** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | YCPIPE | 7:6 | Y/C Pipe Delay. | |
| | DEGPIPE | 5:4 | Degree Pipe Delay. | |
| | DEG1LNMD | 3 | Using just one line's Burst Determine the Degree. | |
| | DEGSENS | 2:0 | Sensitivity of Degree Detect.<br>000: Directly use AFEC degree.<br>001: Tolerate 16384 errors.<br>010: Tolerate 8192 errors.<br>011: Tolerate 4096 errors.<br>100: Tolerate 2048 errors.<br>101: Tolerate 1024 errors.<br>110: Tolerate 512 errors.<br>111: Tolerate 256 errors. | |
| **49h** | **THBURST** | **7:0** | **Default : 0x1E** | **Access : R/W** |
| | THBURST | 7:0 | Degree Detection Tolerance Registers. | |
| **4Ah** | **TLRNSWCHERR** | **7:0** | **Default : 0xC8** | **Access : R/W** |
| | TLRNSWCHERR | 7:0 | Degree Detection Tolerance Registers. | |
| **4Bh** | **HSLEADRGN** | **7:0** | **Default : 0x80** | **Access : R/W** |

| Comb-Filter Register (Bank=03, Registers 01h ~ 9Fh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| | HSLEADRGN | 7:0 | HSYNC Leading Edge Range, for Even/Odd Detect. | |
| **4Ch ~ 4Fh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **50h** | **TIMDETCFGA** | **7:0** | **Default : 0x07** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | AUTOSTOPSYNC | 3 | Automatic Stop H/V Sync when No Input. | |
| | LNFREEMD | 2:0 | Line Buffer Free Run Mode.<br>000: Off (always synchronize).<br>001: 909 return.<br>010: 910 return.<br>011: 917 return.<br>100: 1127 return.<br>101: 1135 return.<br>110: Decided by register.<br>111: Automatic. | |
| **51h** | **TIMDETCFGB** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | STBCNTMD | 7:6 | Stable Counter Mode.<br>00: div 16.<br>01: div 32.<br>10: div 64.<br>11: div 128. | |
| | HSSTBDEC | 5:0 | HSYNC Stable Counter Decrease Speed. | |
| **52h** | **HRETPOSL** | **7:0** | **Default : 0x8E** | **Access : R/W** |
| | HRETPOSL | 7:0 | Horizontal Return Position in Line Buffer Free Run Mode. | |
| **53h** | **HRETPOSH** | **7:0** | **Default : 0x03** | **Access : R/W** |
| | HRETPOSH | 7:0 | Horizontal Return Position in Line Buffer Free Run Mode. | |
| **54h** | **TILTTLRN** | **7:0** | **Default : 0x02** | **Access : R/W** |
| | TILTTLRN | 7:0 | Line Position Tilt Tolerance. | |
| **55h** | **JITTLRN3D** | **7:0** | **Default : 0x08** | **Access : R/W** |
| | JITTLRN3D | 7:0 | 3D Timing Detection Tolerance. | |
| **56h** | **LCKSTEP** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | LCKSTEP | 7:0 | 3D Lock Counter Go Back Distance when SYNC Unstable. | |
| **57h** | **LCK3DTHU** | **7:0** | **Default : 0x33** | **Access : R/W** |
| | LCK3DTHU | 7:0 | 3D Timing Detection Threshold. | |
| **58h** | **LCK3DTHL** | **7:0** | **Default : 0x11** | **Access : R/W** |
| | LCK3DTHL | 7:0 | 3D Timing Detection Threshold. | |

| Comb-Filter Register (Bank=03, Registers 01h ~ 9Fh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| **59h** | **JITTLRN1** | **7:0** | **Default : 0x08** | **Access : R/W** |
| | JITTLRN1 | 7:0 | Tolerance of H-SYNC Jitter. | |
| **5Ah** | **JITTLRN2** | **7:0** | **Default : 0x20** | **Access : R/W** |
| | JITTLRN2 | 7:0 | Tolerance of H-SYNC Jitter. | |
| **5Bh** | **HSLCKTHU** | **7:0** | **Default : 0x10** | **Access : R/W** |
| | HSLCKTHU | 7:0 | Upper Bound Threshold of Hysteresis H-SYNC Lock Counter. | |
| **5Ch** | **HSLCKTHL** | **7:0** | **Default : 0x08** | **Access : R/W** |
| | HSLCKTHL | 7:0 | Lower Bound Threshold of Hysteresis H-SYNC Lock Counter. | |
| **5Dh** | **HSCHGTLRN** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | HSCHGTLRN | 7:0 | Tolerance of HSYNC Counter Change Times.<br>Even HSYNC locked, but if timing drifted too many times, systme still should turn off 2D/3D.<br>00h: immediately stop 2D/3D when HsChg happen.<br>FFh: Never stop 2D/3D if HsLock. | |
| **5Eh** | **SYNCDLY** | **7:0** | **Default : 0x14** | **Access : R/W** |
| | SYNCDLY | 7:0 | H SYNC (from Decoder to Scaler) Pipe Delay. | |
| **5Fh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **60h** | **IMGCTRL** | **7:0** | **Default : 0xF0** | **Access : R/W** |
| | COLKILLMD | 7:6 | Color Kill Mode.<br>00: Off.<br>01: Auto.<br>10, 11: Decided by MCU. | |
| | CGMODE | 5:4 | Auto Chroma Gain Mode.<br>00: Off.<br>01: Auto.<br>10, 11: Manual. | |
| | AC_MD | 3 | Auto Contrast Mode.<br>0: Double at most.<br>1: 4 times at most. | |
| | AUTO_CSTS | 2 | Auto Contrast Adjustment. | |
| | - | 1 | Reserved. | |
| | AUTO_SAT | 0 | Auto Saturation Adjustment. | |
| **61h** | **RSPNTIME** | **7:0** | **Default : 0x10** | **Access : R/W** |
| | RSPNTIME | 7:0 | Response Time of Contrast/Brightness Adjust.<br>0... 255 => 1... 256 field. | |

## Comb-Filter Register (Bank=03, Registers 01h ~ 9Fh)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| **62h** | **REGBSTHGHT** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | REGBSTHGHT | 7:0 | Burst Height for Auto Chroma Gain.<br>0: Auto, 112 for NTSC and 117 for PAL.<br>Other: use RegBstHght/DetBstHght as C Gain. | |
| **63h** | **REGCTST** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REGCTST | 7:0 | Contrast adjustment Coefficient.<br>0... 255 => 0... (255/128). | |
| **64h** | **REGBRHT** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REGBRHT | 7:0 | Brightness adjustment Coefficient.<br>0... 255 => -128... 127 in 8-bit precision. | |
| **65h** | **REGSAT** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REGSAT | 7:0 | Saturation adjustment Coefficient.<br>0... 255 => (0... 255)/128. | |
| **66h** | **CKTHU** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | CKTHU | 7:0 | Upper Bound Threshold of Color Kill. | |
| **67h** | **CKTHL** | **7:0** | **Default : 0x30** | **Access : R/W** |
| | CKTHL | 7:0 | Lower Bound Threshold of Color Kill. | |
| **68h** | **CRMAGAINL** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | CRMAGAINL | 7:0 | Chroma Gain Value for Manu Chroma Gain. | |
| **69h** | **CRMAGAINH** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | CRMAGAINH | 7:0 | Chroma Gain Value for Manu Chroma Gain. | |
| **6Ah** | **MAXLUMA** | **7:0** | **Default : 0xB0** | **Access : R/W** |
| | MACLUMA | 7:0 | Max Luminance for Auto Contrast Adjust. | |
| **6Bh** | **MAXSAT** | **7:0** | **Default : 0xC0** | **Access : R/W** |
| | MAXSAT | 7:0 | MAX Saturation for Auto Saturation Adjust. | |
| **6Ch** | **MAXCRMA** | **7:0** | **Default : 0xC0** | **Access : R/W** |
| | MAXCRMA | 7:0 | MAX Chrominance for Auto Saturation Adjust. | |
| **6Dh** | **SNOWDELAY** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | SNOWDELAY | 7:0 | Latency of Snow Output after Signal Missing. | |
| **6Eh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **6Fh** | **CBCRLPCFG** | **7:0** | **Default : 0x04** | **Access : R/W** |

| Comb-Filter Register (Bank=03, Registers 01h ~ 9Fh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| | CTIIIRMD | 7:6 | IIR Coeficient for CTI.<br>00: 1/4.<br>01: 1/8.<br>10: 1/16.<br>11: 1/32. | |
| | CTIMODE | 5:4 | CTI Mode.<br>00: Off.<br>01: Weak.<br>10: Normal.<br>11: Strong. | |
| | YPIPDLY | 3:2 | Luma Pipe Delay.<br>00: -1 cycle.<br>01: 0 cycle.<br>10: 1 cycle.<br>11: 2 cycle. | |
| | CBCRLPMD | 1:0 | Cb/Cr Low Pass Mode.<br>0: Off.<br>01: Cut off at 2.0MHz.<br>10: Cut off at 1.5MHz.<br>11: Cut off at 1.0MHz | |
| **70h** | **COMBSTATUSA** | **7:0** | **Default : -** | **Access : Write one clear** |
| | HSLOCK | 7 | HSYNC Lock Happen. | |
| | LOCK3D | 6 | Good Timing (Lock3D) Happen. | |
| | - | 5:4 | Reserved. | |
| | HSLOCKZ | 3 | HSYNC Unlock Happen. | |
| | LOC3DZ | 2 | Good Timing (Lock3D) Disappear. | |
| | HSCHG | 1 | H-SYNC Counter Change. | |
| | - | 0 | Reserved. | |
| **71h** | **COMBSTATUSB** | **7:0** | **Default : -** | **Access : Write one clear** |
| | - | 7:6 | Reserved. | |
| | CCHNLACT | 5 | C-channel Active (maybe S-Video Input). | |
| | CCHNLACT | 4 | C-channel Quiet (maybe CVBS Input0. | |
| | - | 3 | Reserved. | |
| | FLDCNTCHG | 2 | Field Counter Change. | |
| | PALSWCHERR | 1 | PAL Switch Error. | |
| | DEGERR | 0 | Degree Error (Degree Detect). | |

## Comb-Filter Register (Bank=03, Registers 01h ~ 9Fh)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| **72h** | **COMBSTATUSC** | **7:0** | **Default : -** | **Access : RO** |
| | LN525 | 7 | 525 Line System. | |
| | LN625 | 6 | 625 Line System. | |
| | F358 | 5 | 3.58 MHz System. | |
| | F443 | 4 | 4.43 MHz System. | |
| | NOINPUT | 3 | No Input. | |
| | VDOMD | 2:0 | Video Mode.<br>000: NTSC(M).<br>001: NTSC(443).<br>010: PAL (M).<br>011: PAL(B,D,G,H,I,N).<br>100: PAL(Nc).<br>101: PAL(60).<br>110: Input without Burst.<br>111: Unknown. | |
| **73h** | **DETBLANKLVL** | **7:0** | **Default : -** | **Access : RO** |
| | DETBLANKLVL | 7:0 | Detected Blanking Level. | |
| **74h** | **CURBLANKLVL** | **7:0** | **Default : -** | **Access : RO** |
| | CURBLANKLVL | 7:0 | Detected Blanking Level. | |
| **75h** | **DETSYNCLVL** | **7:0** | **Default :-** | **Access : RO** |
| | DETSYNCLVL | 7:0 | Detected Sync Level. | |
| **76h** | **DETSYNCHGHT** | **7:0** | **Default : -** | **Access : RO** |
| | DETSYNCHGHT | 7:0 | Detected SYNC Height. | |
| **77h** | **DETBURSTHGHT** | **7:0** | **Default : -** | **Access : RO** |
| | DETBURSTHGHT | 7:0 | Detected Burst Level. | |
| **78h** | **DETHORTOTALL** | **7:0** | **Default : -** | **Access : RO** |
| | DETHORTOTALL | 7:0 | | |
| **79h** | **DETHORTOTALH** | **7:0** | **Default : -** | **Access : R** |
| | DETHORTOTALH | 7:0 | | |
| **7Ah ~ 7Ch** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **7Dh** | **COMBCTRL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | COMBCTRL | 7:0 | Some Control Signals for FPGA. | |
| **7Eh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |

| Comb-Filter Register (Bank=03, Registers 01h ~ 9Fh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| **7Fh** | **FPGACTRL** | **7:0** | **Default : 0xE0** | **Access : R/W** |
| | FPGACTRL | 7:0 | Some Control Signals for FPGA. | |
| **80h ~ 9Fh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |

## SECAM Register (Bank 03, Registers A0h ~ FFh)

| SECAM Register (Bank=03, Registers A0h ~ FFh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| **A0h** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **A1h** | **SCM_IDSET1** | **7:0** | **Default : 0x02** | **Access : R/W** |
| | RST_FLT | 7 | Filter Reset.<br>Set to 1 to Reset the vaules of Filter Taps. | |
| | MIXC_EN | 6 | Chroma Mixing Enable.<br>0: Disable.<br>1: Enable. | |
| | WFUNC_ISO | 5:4 | Chroma Weighting Function Isolation. | |
| | SVEN | 3 | S-Video Input Enable.<br>Set to 1 if the input is from S-Video interface. | |
| | ID_MODE | 2 | Identification Mode Selection.<br>Set to 1 only if using frame ID for SECAM detection. | |
| | BS_TYPE | 1 | Band-Stop Filter TYPE.<br>0: Notch Dr Frequency.<br>1: Notch Db Frequency. | |
| | SCMID_EN | 0 | SECAM Identification Forced Enable.<br>0: Disbale.<br>1: Enable. | |
| **A2h** | **SAMPLE_START** | **7:0** | **Default : 0x90** | **Access : R/W** |
| | SAMPLE_ST[7:0] | 7:0 | Start of Sample Point (lower 8 bits). | |
| **A3h** | **SAMPLE_LENGTH** | **7:0** | **Default : 0x10** | **Access : R/W** |
| | SAMPLE_LEN | 7:0 | Length of Sample Numbers. | |
| **A4h** | **LINE_START_A** | **7:0** | **Default : 0x07** | **Access : R/W** |
| | LINE_STA | 7:0 | Start of Line Number of Odd Filed. | |
| **A5h** | **LINE_START_B** | **7:0** | **Default : 0x40** | **Access : R/W** |
| | LINE_STB[7:0] | 7:0 | Start of Line Number of Even Filed (lower 8 bits). | |
| **A6h** | **SCM_IDSET2** | **7:0** | **Default : 0x01** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | SAMPLE_ST[10:8] | 6:4 | Start of Sample Point (upper 3 bits). | |
| | CMBGCLK_OPT | 3 | Comb Clock Gating Option.<br>0: Diable.<br>1: Enable ClkComb gating. | |
| | - | 2 | Reserved. | |

## SECAM Register (Bank=03, Registers A0h ~ FFh)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | LINE_STB[9:8] | 1:0 | Start of Line Number of Even Filed (upper 2 bits). | |
| **A7h** | **LINE_LENGTH** | **7:0** | **Default : 0x02** | **Access : F/W** |
| | LINE_LEN | 7:0 | Length of Observation Line. | |
| **A8h** | **ACT_MULTIPLE** | **7:0** | **Default : 0x96** | **Access : R/W** |
| | ACT_MULTIPLE | 7:0 | Integer Multiple of LINE_LEN, combined to form Length of the Active Video Line. | |
| **A9h** | **MAG_THRSD_L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | MAG_THRSD[7:0] | 7:0 | Magnitude Threshold (lower 8 bits). | |
| **AAh** | **MAG_THRSD_M** | **7:0** | **Default : 0x06** | **Access :** |
| | MAG_THRSD[15:8] | 7:0 | Magnitude Threshold (middle 8 bits). | |
| **ABh** | **MAG_THRSD_H** | **7:0** | **Default : 0x40** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | LINE_PIXNUM[10:8] | 6:4 | Pixel Number of Line Buffer (upper 3 bits). | |
| | MAG_THRSD[19:16] | 3:0 | Magnitude Threshold (upper 4 bits). | |
| **ACh** | **LINE_PIXNUMBER** | **7:0** | **Default : 0x48** | **Access : R/W** |
| | LINE_PIXNUM[7:0] | 7:0 | Pixel Number of Line Buffer (lower 8 bits).<br>(if the number is 1097, program 11'h448) | |
| **ADh** | **ID_THRSD** | **7:0** | **Default : 0x06** | **Access : R/W** |
| | ID_THRSD | 7:0 | Threshold for SECAM Identification. | |
| **AEh** | **SCM_THRSD** | **7:0** | **Default : 0x66** | **Access : R/W** |
| | NONSCM_THRSD | 7:4 | Non-SECAM Decision Threshold. | |
| | SCM_THRSD | 3:0 | SECAM Decision Threshold. | |
| **AFh ~ CFh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **D0h** | **SCM_IDSTATUS** | **7:0** | **Default : -** | **Access : R** |
| | SCMID_DONE | 7 | SECAM Identification Done Indication. | |
| | SCMID_YES | 6 | SECAM Signal Found Bit. | |
| | DR_LINE | 5 | Dr Line Indication. | |
| | DB_LINE | 4 | Db Line Indication. | |
| | - | 3 | Reserved. | |
| | SCMID_STS | 2:0 | SECAM ID Status.<br>000: Idle<br>001, 010, 011: ID Progress<br>110: SECAM<br>111: No SECAM Signal Discovery | |

## SECAM Register (Bank=03, Registers A0h ~ FFh)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| **D1h** | **MAG_INT_L** | **7:0** | **Default : -** | **Access : R** |
| | MAG_INT[7:0] | 7:0 | Magnitude Accumulated Values for Observation (lower 8 bits). | |
| **D2h** | **MAG_INT_M** | **7:0** | **Default : -** | **Access : R** |
| | MAG_INT[15:8] | 7:0 | Magnitude Accumulated Values for Observation (middle 8 bits). | |
| **D3h** | **MAG_INT_H** | **7:0** | **Default : -** | **Access : R** |
| | MAG_INTB[19:16] | 7:4 | Magnitude Accumulated Values for Observation (upper 4 bits). | |
| | MAG_INT[19:16] | 3:0 | Magnitude Accumulated Values for Observation (upper 4 bits). | |
| **D4h** | **MAG_INT_B_L** | **7:0** | **Default : -** | **Access : R** |
| | MAG_INTB[7:0] | 7:0 | Magnitude Accumulated Values for Observation (lower 8 bits). | |
| **D5h** | **MAG_INT_B_M** | **7:0** | **Default : -** | **Access : R** |
| | MAG_INTB[15:8] | 7:0 | Magnitude Accumulated Values for Observation (meddle 8 bits). | |
| **D6h** | **SCM_FSC** | **7:0** | **Default : -** | **Access : R** |
| | - | 7:2 | Reserved. | |
| | SCM_FSC | 1:0 | Fsc Status from AFEC_TOP.<br>00: NTSC 3.58MHz<br>01: PAL 4.43MHz<br>10: SECAM 4.285156MHz | |
| **D7h ~ F1h** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **F2h** | **WR_LK1** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | WR_LK1 | 7 | Register Lock (work with WR_LK0).<br>Register access is disabled when WR_LK0 and WR_LK1 are HIGH.<br>Register access is enabled when WR_LK0 and WR_LK1 are LOW. | |
| | - | 6:0 | Reserved. | |
| **F3h** | **PWMCLK** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | DB_EN | 7 | Double Buffer Enable.<br>0: Disable.<br>1: Enable. | |
| | P4REN | 6 | PWM4 Reset every frame Enable.<br>0: Disable.<br>1: Enable. | |
| | P3REN | 5 | PWM3 Reset every frame Enable.<br>0: Disable.<br>1: Enable. | |
| | P4POL | 4 | PWM 4 Polarity when enhance PWM4 enable. | |

| SECAM Register (Bank=03, Registers A0h ~ FFh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| | EP4EN | 3 | Enhance PWM4 Enable.<br>0: Disable.<br>1: Enable. | |
| | P3POL | 2 | PWM3 Polarity when enhance PWM3 enable. | |
| | EP3EN | 1 | Enhance PWM3 Enable.<br>0: Disable.<br>1: Enable. | |
| | PCLK | 0 | PWM3/4 base Clock select.<br>0: 14.318MHz.<br>1: 14.318MHz / 4. | |
| **F4h** | **PWM3C** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | PWM_14BIT_EN | 7 | 14bit PWM Enable.<br>0: Disable, then PWM3C[6:0] = PWM3_CTUN[6:0].<br>1: Enable, then PWM3C[3:0] = PWM_DIV. | |
| | PWM3_CTUN[6:0] | 6:0 | PWM3 Coarse adjustment,<br>when PWM_14BIT_EN = 0. | |
| | - | 6:4 | Reserved. | |
| | PWM_DIV | 3:0 | Clock Divider,<br>when PWM_14BIT_EN = 1. | |
| **F5h** | **PWM4C** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | PWM4_POL | 7 | PWM4 Polarity. | |
| | PWM4_CTUN[6:0] | 6:0 | PWM4 Coarse adjustment. | |
| **F6h** | **PWM3EPL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | EPWM0P[7:0] | 7:0 | Enhance PWM3 Period, when PWM_14BIT_EN = 0. | |
| | PWM_FINE_TUNE | 7:0 | Fine Tune PWM Pulse, when PWM_14BIT_EN = 1. | |
| **F7h** | **PWM3EPH** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | EPWM0P[15:8] | 7:0 | Enhance PWM3 Period, when PWM_14BIT_EN = 0. | |
| | PWM_MASK_BIT | 5:0 | Mask PWN Period Bits, when PWM_14BIT_EN = 1. | |
| **F8h** | **PWM4EPL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | EPWM4P[7:0] | 7:0 | Enhance PWM4 Period. | |
| **F9h** | **PWM4EPH** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | EPWM4P[15:8] | 7:0 | Enhance PWM4 Period. | |
| **FAh** | **PWM3C_T** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | PWM3_POL | 4 | PWM3 Polarity. | |

| SECAM Register (Bank=03, Registers A0h ~ FFh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| | - | 3:0 | Reserved. | |
| **FBh ~ FFh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |

# Embedded MCU Register (Address mapping from C000h to C0FFh)

| Embedded MCU Register Bank – General Control Register | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| **00h ~ 07h** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **08h** | **WDT_KEY_L** | **7:0** | **Default : 0xAA** | **Access : R/W** |
| | WDT_KEY[7:0] | 7:0 | Watchdog timer disable key low byte<br>Watchdog timer will be enabled<br>If (WDT_Key_L != 8'hAA) or<br>(WDT_Key_H != 8'h55) | |
| **09h** | **WDT_Key_H** | **7:0** | **Default : 0x55** | **Access : R/W** |
| | WDT_KEY[15:8] | 7:0 | Refer to C008h. | |
| **0Ah** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **10h** | **DDC2Bi_INT_EN** | **6:0** | **Default: 0x00** | **Access : R/W** |
| | START_EN | 6 | DDC2Bi Start interrupt Enable. | |
| | STOP_EN | 5 | DDC2Bi Stop interrupt Enable. | |
| | DATR_EN | 4 | DDC2Bi Data Reda interrupt Enable. | |
| | DATW_EN | 3 | DDC2Bi Data Write interrupt Enable. | |
| | DATRW_EN | 2 | DDC2Bi Data Read/Write interrupt Enable. | |
| | WADR | 1 | DDC2Bi Word Address interrupt. | |
| | ID | 0 | DDC2Bi ID interrupt. | |
| **11h** | **DDC2Bi_Flag** | **6:0** | **Default : 0x00** | **Access : R/C** |
| | DDC2Bi_FLAG | | DDC 2Bi interrupt flag and clear | |
| **12h** | **DDC2Bi_W_BUF** | **7:0** | **Default : -** | **Access : RO** |
| | | | DDC2Bi write, MCU read buffer | |
| **13h** | **DDC2Bi_R_BUF** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | DDC2Bi_R_BUF[7:0] | 7:0 | DDC2Bi read, MCU write buffer | |
| **14h ~ 17h** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **18h** | **DDC2Bi_CTRL** | **1:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:2 | Reserved. | |
| | EN_NO_ACK | 1 | DDC2Bi does not send ack if data buffer has not been read.<br>0: Disable.<br>1: Enable. | |
| | - | 0 | Reserved. | |

## Embedded MCU Register Bank – General Control Register

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| **19h** | **DDC2Bi_ID** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | DDC2Bi_EN | 7 | DDC2Bi Enable. | |
| | DDC2Bi_ID[6:0] | 6:0 | DDCBi ID. | |
| **1Ah ~ 1Fh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **20h** | **KEY_ADC1** | **5:0** | **Default : -** | **Access : RO** |
| | KEY_ADC1[5:0] | | Key Pad ADC channel 1 value. | |
| **21h** | **KEY_ADC2** | **5:0** | **Default : -** | **Access : RO** |
| | KEY_ADC2[5:0] | | Key Pad ADC channel 2 value. | |
| **22h** | **KEY_ADC3** | **5:0** | **Default : -** | **Access : RO** |
| | KEY_ADC3[5:0] | | Key Pad ADC channel 3 value. | |
| **23h ~ 2Fh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **30h** | **P0_CTRL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | P0_CTRL[7:0] | 7:0 | MCU Port 0 output enable Control. | |
| **31h** | **P0_OE** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | P0_OE[7:0] | 7:0 | MCU Port 0 Output Enable. | |
| **32h** | **P0_IN** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | P0_IN[7:0] | 7:0 | MCU Port 0 output enable from output data. | |
| **33h** | **P1_CTRL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | P1_CTRL[7:0] | 7:0 | MCU Port 1 output enable Control. | |
| **34h** | **P1_OE** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | P1_OE[7:0] | 7:0 | MCU Port 1 Output Enable. | |
| **35h** | **P1_IN** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | P1_IN[7:0] | 7:0 | MCU Port 1 output enable from output data. | |
| **36h** | **P2_CTRL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | P2_CTRL[7:0] | 7:0 | MCU Port 2 output enable Control. | |
| **37h** | **P2_OE** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | P2_OE[7:0] | 7:0 | MCU Port 2 Output Enable. | |
| **38h** | **P2_IN** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | P2_IN[7:0] | 7:0 | MCU Port 2 output enable from output data. | |
| **39h** | **P3_CTRL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | P3_CTRL[7:0] | 7:0 | MCU Port 3 output enable Control. | |

| Embedded MCU Register Bank – General Control Register | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| **3Ah** | **P3_OE** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | P3_OE[7:0] | 7:0 | MCU Port 3 Output Enable. | |
| **3Bh** | **P3_IN** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | P3_IN[7:0] | 7:0 | MCU Port 3 output enable from output data. | |
| **3Ch** | **P4_CTRL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | P4_CTRL[7:0] | 7:0 | MCU Port 4 output enable Control. | |
| **3Dh** | **P4_OE** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | P4_OE[7:0] | 7:0 | MCU Port 4 Output Enable. | |
| **3Eh** | **P4_IN** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | P4_IN[7:0] | 7:0 | MCU Port 4 output enable from output data. | |
| **3Fh** | **SSPI_STS_OP** | **7:0** | **Default : 0x05** | **Access : R/W** |
| | SPPI_STS_OP[7:0] | 7:0 | Soft-trigger SPI check status OP code. | |
| **40h** | **SSPI_WD0** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | SSPI_WD0 | 7:0 | Soft-trigger SPI Write byte 0. | |
| **41h** | **SSPI_WD1** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | SSPI_WD1 | 7:0 | Soft-trigger SPI Write byte 1. | |
| **42h** | **SSPI_WD2** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | SSPI_WD2 | 7:0 | Soft-trigger SPI Write byte 2. | |
| **43h** | **SSPI_WD3** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | SSPI_WD3 | 7:0 | Soft-trigger SPI Write byte 3. | |
| **44h** | **SSPI_WD4** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | SSPI_WD4 | 7:0 | Soft-trigger SPI Write byte 4. | |
| **45h** | **SSPI_WD5** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | SSPI_WD5 | 7:0 | Soft-trigger SPI Write byte 5. | |
| **46h** | **SSPI_WD6** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | SSPI_WD06 | 7:0 | Soft-trigger SPI Write byte 6. | |
| **47h** | **SSPI_WD7** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | SSPI_WD7 | 7:0 | Soft-trigger SPI Write byte 7. | |
| **48h** | **SSPI_TRIG** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | SSPI_START | 7 | Trigger soft-SPI<br>0: NOP.<br>1: Start soft -SPI. | |
| | SSPI_CHK_BZY | 6 | Auto Check Busy after soft-SPI. | |
| | SSPI_CHK_BIT | 5:3 | Check busy bit position | |

## Embedded MCU Register Bank – General Control Register

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | SSPI_Length | 2:0 | SSPI command length. | |
| **49h** | **SSPI_RD1** | **7:0** | **Default : -** | **Access : RO** |
| | SSPI_RD1[7:0] | 7:0 | SSPI read byte 1. | |
| **4Ah** | **SSPI_RD2** | **7:0** | **Default : -** | **Access : RO** |
| | SSPI_RD2[7:0] | 7:0 | SSPI read byte21. | |
| **4Bh** | **SSPI_RD3** | **7:0** | **Default : -** | **Access : RO** |
| | SSPI_RD3[7:0] | 7:0 | SSPI read byte 3. | |
| **4Ch** | **SSPI_RD4** | **7:0** | **Default : -** | **Access : RO** |
| | SSPI_RD4[7:0] | 7:0 | SSPI read byte 4. | |
| **4Dh** | **SSPI_RD5** | **7:0** | **Default : -** | **Access : RO** |
| | SSPI_RD5[7:0] | 7:0 | SSPI read byte 5. | |
| **4Eh** | **SSPI_RD6** | **7:0** | **Default : -** | **Access : RO** |
| | SSPI_RD6[7:0] | 7:0 | SSPI read byte 6. | |
| **4Fh** | **SSPI_RD7** | **7:0** | **Default : -** | **Access : RO** |
| | SSPI_RD7[7:0] | 7:0 | SSPI read byte 7. | |
| **50h** | **ISP_PA0** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | ISP_PA[7:0] | 7:0 | Parallel flash ISP Address[7:0]. | |
| **51h** | **ISP_PA1** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | ISP_PA[15:8] | 7:0 | Parallel flash ISP Address[15:8]. | |
| **52h** | **ISP_PA2** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | ISP_PA[17:16] | 7:0 | Parallel flash ISP Address[17:16]. | |
| **53h** | **ISP_PD_W** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | ISP_PD_W[7:0] | 7:0 | Parallel flash ISP Write Data. | |
| **54h** | **ISP_PCtr** | **4:0** | **Default : 0x0A** | **Access : R/W** |
| | ISP_PMD_EN | 4 | Parallel flash ISP mode enable. | |
| | ISP_PWEZ | 3 | Parallel flash WEZ at ISP mode. | |
| | ISP_POEZ | 2 | Parallel flash OEZ at ISP mode. | |
| | ISP_PDBUE | 1 | Parallel flash data bus output enable at ISP mode. | |
| | ISP_PCEZ | 0 | Parallel flash CEZ at ISP mode. | |
| **55h** | **ISP_PD_R** | **7:0** | **Default :-** | **Access : RO** |
| | ISP_PD_R[7:0] | 7:0 | Parallel flash ISP mode read data. | |
| **56h ~ FFh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |

## LVDS Register (Bank = 04, Registers 01h ~ 6Ah)

| LVDS Register (Bank = 04, Registers 01h ~ 6Ah) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| **01h ~ 0Fh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **10h** | **GPOA_CTRL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | GCS | 7:5 | Select GPO Source. | |
| | GTS | 4:3 | Control Skip Line Number. | |
| | - | 2 | Reserved. | |
| | GTC | 1 | Select GPO_I Source. | |
| | GOP | 0 | Select GPO_I Source. | |
| **11h** | **GAVST_L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | GPOA_VST[7:0] | 7:0 | GPOA Vstar Point (lower 8 bits). | |
| **12h** | **GAVST_H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | GPOA_VST[10:8] | 2:0 | GPOA Vstar Point (upper 3 bits). | |
| **13h** | **GAVEND_L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | GPOA_VEND[7:0] | 7:0 | GPOA Vend (lower 8 bits). | |
| **14h** | **GAVEND_H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | GPOA_VEND[10:8] | 2:0 | GPOA Vend (upper 3 bits). | |
| **15h** | **GAHST_L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | GPOA_HST[7:0] | 7:0 | GPOA Hstar (lower 8 bits). | |
| **16h** | **GAHST_H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | GPOA_HST[10:8] | 2:0 | GPOA Hstar (upper 3 bits). | |
| **17h** | **GAHEND_L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | GPOA_HEND[7:0] | 7:0 | GPOA Hend (lower 8 bits). | |
| **18h** | **GA_HEND_H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | GPOA_HEND[10:8] | 3:0 | GPOA Hend (upper 3 bits). | |
| **19h** | **LVDS_CTRL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | GPOA_GATED_EN | 5 | Clock Gated using GPOA Singal. | |
| | ADD_1 | 4 | Hard Clock Gated Pulse Width Add One. | |

## LVDS Register (Bank = 04, Registers 01h ~ 6Ah)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | T_LVDSSEL | 3 | LVDS Test Enable. | |
| | CH_SWAP | 2 | Channel Switch. | |
| | CH_POLARITY | 1 | Channel Value Invert. | |
| | LVDS_TI | 0 | LVDS TI Type. | |
| **1Ah** | **LVDS_TEST** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | TESTER_PIX | 7:0 | LVDS Test Pixel. | |
| **1Bh** | **MOD_TDR0** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | DRVN_TTL[7:0] | 7:0 | Output Driving of N_channel when MOD is TTL output (lower 8 bits). | |
| **1Ch** | **MOD_TDR1** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | DRVP_TTL[5:0] | 7:2 | Output Driving of P_channel when MOD is TTL output (lower 6 bits). | |
| | DRVN_TTL[9:8] | 1:0 | Output Driving of N_channel when MOD is TTL output (upper 2 bits). | |
| **1Dh** | **MOD_TDR2** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | DRVP_TTL[9:6] | 3:0 | Output Driving of P_channel when MOD is TTL output (upper 4 bits). | |
| **1Eh** | **MOD_CTRL** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | MOD_PWDN | 2 | MOD Power Down. | |
| | MOD_CLK_EN | 1 | MOD Clock Enable. | |
| | HALF_SWING_EN | 0 | LVDS_Output Swing Reduce Half. | |
| **1Fh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **20h** | **MOD_SEL0** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | SELGPO | 4:0 | Select GPO. | |
| **21h** | **MOD_SEL1** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | SELTTL | 4:0 | Select TTL. | |
| **22h** | **LVDS_T0** | **7:0** | **Default : 0x06** | **Access : R/W** |
| | TEST_LVDS[7:0] | 7:0 | LVDS Test Bits (lower 8 bits). | |
| **23h** | **LVDS_T1** | **7:0** | **Default : 0x00** | **Access : R/W** |

## LVDS Register (Bank = 04, Registers 01h ~ 6Ah)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | TEST_LVDS[15:8] | 7:0 | LVDS Test Bits (upper 8 bits). | |
| 24h | **LVDS_TRI0** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | LVDS_TRI[7:0] | 7:0 | LVDS Tri_State (lower 8 bits). | |
| 25h | **LVDS_TRI1** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | - | 7:2 | Reserved. | |
| | LVDS_TRI[15:8] | 1:0 | LVDS Tri_State (upper 8 bits). | |
| 26h (044Ch) | **REG044C** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | 26H_DATA[7:0] | 7:0 | [7:0]:Low byte of BVCOM_DC[8:0], PAD_VCOMDC voltage adjust, DC : 1.165V~2.327V. | |
| 27h (044Eh) | **REG044E** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | 27H_DATA[7:0] | 7:0 | [7:4]: TST_IVCOM, Vcom opamps driving strength select.<br>[3]: Reserve.<br>[2]: High bit of BVCOM_DC[8:0], PAD_VCOMDC voltage adjust, DC : 1.165V~2.327V.<br>[1]: TST_VCOMBGO, VBG output to PAD_VCOMOUT.<br>[0]: PWDN_VCOM, VCOM power down control, 1: power down. | |
| 28h (0450h) | **REG0450** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | 28H_DATA[7:0] | 7:0 | [7:0]: BVCOM_OUT, PAD_VCOMOUT voltage adjust, Vlow/Vhigh : 0.45V/2.55V~1.05V/1.95V. | |
| 29h (0452h) | **REG0452** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | 29H_DATA[7:0] | 7:0 | [7]: GCR_CAL_EN_SW, Enable software Calibration function for LVDS output.<br>[6]: GCR_CAL_SRC_SEL, Select calibration source, 0: CH2, 1: floating.<br>[5:4]: GCR_CAL_LEVEL_SEL, Select calibration target voltage. (may change before tape-out).<br>00: 250mV, 01:300mV, 10: 350mV, 11: 200mV.<br>[3]: GCR_SEL_VDD25: MOD supply selection, 0: 3.3V, 1: 2.5V.<br>[2:1]: GCR_SELVCM: Common-mode selection of CH[?:0].<br>2.5V 00 = 1.19789 V 01 = 698.769 mV 10 = 1.19789 V 11 = 898.418 mV.<br>3.3V 00 = 1.58165 V 01 = 922.627 mV 10 = 1.58165 V 11 = 1.18623 V.<br>[0]: GCR_CKEN, TX clock enable,(LVDS) This pin is used for CH0~CH4. | |
| 2Ah (0454h) | **REG0454** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | 2AH_DATA[7:0] | 7:0 | [7:6]: GCR_OUTCONF_CH3_BIT, Output mode configuration for channel 3. | |

| LVDS Register (Bank = 04, Registers 01h ~ 6Ah) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| | | | [5:4]: GCR_OUTCONF_CH2_BIT, Output mode configuration for channel 2.<br>[3:2]: GCR_OUTCONF_CH1_BIT, Output mode configuration for channel 1.<br>[1:0]: GCR_OUTCONF_CH0_BIT, Output mode configuration for channel 0.<br>2'b00: TTL mode/Standby mode.<br>2'b01: LVDS/EPI/RSDS/mini-LVDS data output mode.<br>2'b10: RSDS/miniLVDS clock output mode.<br>2'b11: Test clock output mode. | |
| **2Bh (0456h)** | **REG0456** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | 2BH_DATA[7:0] | 7:0 | [7:6]: skew_reg_g, TTL G data channel output skew control.<br>[5:4]: skew_reg_b, TTL B data channel output skew control.<br>[3]: Reserve.<br>[2]: DAC test dc level source select, 1:{G7,G4,G3,G2,R6,R2,R1,R0}, 0: htotal[7:0].<br>[1:0]: GCR_OUTCONF_CH4_BIT, Output mode configuration for channel 4.<br>2'b00: TTL mode/Standby mode.<br>2'b01: LVDS/EPI/RSDS/mini-LVDS data output mode.<br>2'b10: RSDS/miniLVDS clock output mode.<br>2'b11: Test clock output mode. | |
| **2Ch (0458h)** | **REG0458** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | 2CH_DATA[7:0] | 7:0 | [7:5]: GCR_OUTSWING_CLK_BIT[2:0], swing control low bit for CH1,3 when not enable calibration.<br>[4:0]: GCR_OUTSWING_DATA_BIT, swing control for CH0,2,4 when not enable calibration. | |
| **2Dh (045Ah)** | **REG045A** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | 2DH_DATA[7:0] | 7:0 | [7:3]: GCR_DS_POL_CH.<br>[2]: GCR_CAL_EN_HW, Enable hardware Calibration function for LVDS output.<br>[1:0]: GCR_OUTSWING_CLK_BIT[4:3], swing control high bit for CH1,3 when not enable calibration. | |
| **2Eh (045Ch)** | **REG045C** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | 2EH_DATA[7:0] | 7:0 | [7:6]: GCR_PEADJ_CH3_BIT[1:0], Differential output pre-emphasis level adjust, low bit of CH3.<br>[5:4]: GCR_PEADJ_CH2_BIT[1:0], Differential output pre-emphasis level adjust, low bit of CH2.<br>[3:2]: GCR_PEADJ_CH1_BIT[1:0], Differential output pre-emphasis | |

| LVDS Register (Bank = 04, Registers 01h ~ 6Ah) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| | | | level adjust, low bit of CH1.<br>[1:0]: GCR_PEADJ_CH0_BIT[1:0], Differential output data/clock pre-emphasis level adjust, low bit of CH0.<br>(1X means 0.25mA).<br>0: 0X, 1: 1X, 2: 2X, 3: 3X &. | |
| **2Fh (045Eh)** | **REG045E** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | 2FH_DATA[7:0] | 7:0 | [7:3]: GCR_PE_EN_CH, Differential output pre-emphasis enable for channel [4:0].<br>[2]: GCR_PEADJ_MAX_BIT, Differential output pre-emphasis level adjust, hight bit of CH0-4.<br>[1:0]: GCR_PEADJ_CH4_BIT[1:0], Differential output pre-emphasis level adjust, low bit of CH4. | |
| **30h (0460h)** | **REG0460** | **7:0** | **Default : 0x00** | **Access : RO** |
| | 30H_READ[7:0] | 7:0 | [7]: Reserve.<br>[6]: DDA_OUT, Calibration output.<br>[5]: Reg_hw_mod_cal_ready, hardware calibration function finish.<br>[4:0]: reg_gcr_ibcal_hw[4:0], hardware calibration function result. | |
| **31h (0462h)** | **REG0462** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | 31H_DATA[7:0] | 7:0 | [7]: Reg_tpat_en, OP2 test pattern enable.<br>[6]: Reg_patyuv, YUV type test pattern enable.<br>[5]: Reg_pathd,.<br>[4]: Reg_patint,.<br>[3:0]: reg_patsel. | |
| **32h (0464h)** | **REG0464** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | 32H_DATA[7:0] | 7:0 | [7:4]: reg_vpatbsize, vertical size select for test pattern.<br>[7]: Enable down count for fix vertical bp.<br>[3:0]: reg_hpatbsize, horizontal size select for test pattern. | |
| **33h (0466h)** | **REG0466** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | 33H_DATA[7:0] | 7:0 | [7]: Reserve.<br>[6:0]: reg_vsync_dcnt, down count line number for fix vertical bp. | |

## Digital PWM Register (Bank = 04, Registers 6Bh ~ FFh)

| Digital PWM Register (Bank = 04, Registers 6Bh ~ FFh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| **6Bh** | **PROTECT_BIT** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | PROTECT_BIT | 7:0 | Have to set as 1 in that could view all PWM register setting. | |
| **6Ch** | **STUS_RPRT** | **7:0** | **Default : -** | **Access : RO** |
| | - | 7:3 | Reserved. | |
| | STUS_RPRT[2] | 2 | 1: FAULTZ is high. | |
| | STUS_RPRT[1] | 1 | 1: FB2 mode is on. | |
| | STUS_RPRT[0] | 0 | 1: VIN is OK. | |
| **6Dh** | **PWM_SWCH** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:2 | Reserved. | |
| | PWM_SWCH[1:0] | 1:0 | Control PWM on/off; must set to "00" or "11".<br>00: PWM off.<br>11: PWM on.<br>Others: Off (not recommended). | |
| **6Eh** | **OP_MD** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | PWM_SWRST | 6 | Software-Reset bit to reset PWM.<br>0: No action.<br>1: Software reset and remain in initial state using a single pulse. | |
| | VSYNC_PLRTY_SEL | 5 | VSYNC polarity setting.<br>0: Same polarity to VSYNC.<br>1: Opposite polarity. | |
| | VSYNC_SEL | 4 | Use TCON's VSYNC for VSYNC-mode.<br>0: Use normal VSYNC.<br>1: Use TCON's VSYNC. | |
| | PWM_EN | 3 | PWM function on/off.<br>0: Use external controller.<br>1: User internal controller. | |
| | FAULTZ_H_MD_EN | 2 | FAULTZ High Mode on/off.<br>0: Off.<br>1: On. | |
| | VSYNC_MD_EN | 1 | VSYNC Mode on/off.<br>0: Off.<br>1: On. | |

| Digital PWM Register (Bank = 04, Registers 6Bh ~ FFh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| | BRST_MD_EN | 0 | Burst Mode on/off.<br>0: Off.<br>1: On. | |
| **6Fh** | **VIN_STAB_CNT** | **7:0** | **Default : 0x0A** | **Access : R/W** |
| | VIN_STAB_CNT | 7:0 | VIN Stable Count number. | |
| **70h** | **VIN_OV_CNT** | **7:0** | **Default : 0x0A** | **Access : R/W** |
| | VIN_OV_CNT | 7:0 | VIN Over-Voltage Count number. | |
| **71h** | **VIN_UV_CNT** | **7:0** | **Default : 0x0A** | **Access : R/W** |
| | VIN_UV_CNT | 7:0 | VIN Under-Voltage Count number. | |
| **72h** | **VIN_WRK_H_THRD** | **7:0** | **Default : 0xC3** | **Access : R/W** |
| | VIN_WRK_H_THRD | 7:0 | VIN Working High Threshold. | |
| **73h** | **VIN_STRTUP_H_THRD** | **7:0** | **Default : 0xBB** | **Access : R/W** |
| | VIN_STRTUP_H_THRD | 7:0 | VIN Startup High Threshold. | |
| **74H** | **VIN_STRTUP_L_THRD** | **7:0** | **Default : 0x99** | **Access : R/W** |
| | VIN_STRTUP_L_THRD | 7:0 | VIN Startup Low Threshold. | |
| **75h** | **VIN_WRK_L_THRD** | **7:0** | **Default : 0x90** | **Access : R/W** |
| | VIN_WRK_L_THRD | 7:0 | VIN Working Low Threshold. | |
| **76h** | **VIN_WAIT_CNT_L** | **7:0** | **Default : 0xFA** | **Access : R/W** |
| | VIN_WAIT_CNT[7:0] | 7:0 | VIN Waiting Count number (lower 8 bits). | |
| **77h** | **VIN_WAIT_CNT_H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | VINWAIT_CNT[11:8] | 3:0 | VIN Waiting Count number (upper 4 bits) | |
| **When 6E[2] = 0, please refer to the following as register settings of 78h ~ 7Bh:** | | | | |
| **78h** | **FAULTZ_H_VAL** | **7:0** | **Default : 0xAA** | **Access : R/W** |
| | FAULTZ_H_VAL[7:0] | 7:0 | FAULTZ High boundary. | |
| **79h** | **FAULTZ_L_VAL** | **7:0** | **Default : 0x55** | **Access : R/W** |
| | FAULTZ_L_VAL[7:0] | 7:0 | FAULTZ Low boundary. | |
| **7Ah** | **FAULTZ_STB** | **7:0** | **Default : 0x0A** | **Access : R/W** |
| | FAULTZ_STB[7:0] | 7:0 | Counts for FAULTZ Stable. | |
| **7Bh** | **FAULTZ_DROP** | **7:0** | **Default : 0x0A** | **Access : R/W** |
| | FAULTZ_H_GO_LOW | 7:0 | Counts for FAULTZ High Go Low. | |
| **When 6E[2] = 1, please refer to the following as register settings of 78h ~ 7Bh:** | | | | |

| Digital PWM Register (Bank = 04, Registers 6Bh ~ FFh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| **78h** | **FAULTZ_H_VALUE** | **7:0** | **Default : 0xAA** | **Access : R/W** |
| | FB2_DET_TIME[7:0] | 7:0 | FB2 Detection Time after burst high when system is in FAULTZ high mode (lower 8 bits). | |
| **79h** | **FAULTZ_L_VALUE** | **7:0** | **Default : 0x55** | **Access : R/W** |
| | - | 7:2 | Reserved. | |
| | FB2_DETECT_TIME[9:8] | 1:0 | FB2 Detection Time after burst high when system is in FAULTZ high mode (higher 2 bits). | |
| **7Ah** | **FAULTZ_STB_CNT** | **7:0** | **Default : 0x0A** | **Access : R/W** |
| | FB2_DET_FAIL_T | 7:0 | Counts for FB2 failure is True. | |
| **7Bh** | **FAULTZ_DROP** | **7:0** | **Default : 0x0A** | **Access : R/W** |
| | FB2_L_FAULTZ_H_MD | 7:0 | FB2 Low Bound in FAULTZ High Mode. | |
| **7Ch** | **MSUR_OFST_ L** | **7:0** | **Default : 0x0E** | **Access : R/W** |
| | MSUR_OFST[7:0] | 7:0 | Measure Offset time to get Data (lower 8 bits). | |
| **7Dh** | **MSUR_OFST_H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:2 | Reserved. | |
| | MSUR_OFST[9:8] | 1:0 | Measure Offset time to get Data (higher 2 bits). | |
| **7Eh** | **2US** | **7:0** | **Default : 0x48** | **Access : R/W** |
| | 2US_CNT | 7:0 | Counts for 2us. | |
| **7Fh** | **2US_MSUR** | **7:0** | **Default : 0x14** | **Access : R/W** |
| | 2US_MSUR | 7:0 | Counts to get Data when PWM on time ≤ 2us. | |
| **80h** | **FB1_COM** | **7:0** | **Default : 0xAA** | **Access : RO** |
| | FB1_COM[7:0] | 7:0 | FB1 Command. | |
| **81h** | **FB2_STRTUP** | **7:0** | **Default : 0xAA** | **Access : R/W** |
| | FB2_STRTUP | 7:0 | Start-up FB2 Command. | |
| **82h** | **FB2_SET** | **7:0** | **Default : 0xAA** | **Access : R/W** |
| | FB2_SET | 7:0 | FB2 Command; adjust for continuous output adjusting. | |
| **83h** | **CONT_AB** | **7:0** | **Default : 0xB7** | **Access : R/W** |
| | CONT_A | 7:4 | A-value for Continuous-mode. | |
| | CONT_B | 3:0 | B-value for Continuous-mode. | |
| **84h** | **BRST_AB** | **7:0** | **Default : 0xB7** | **Access : R/W** |
| | BRST_A | 7:4 | A-value for Burst-mode. | |
| | BRST_B | 3:0 | A-value for Burst-mode. | |

| Digital PWM Register (Bank = 04, Registers 6Bh ~ FFh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| **85h** | **STRK1_ L** | **7:0** | **Default : 0xA9** | **Access : R/W** |
| | STRK1_CNT[7:0] | 7:0 | 1st ignition and normal operation Count for PWM frequency; double buffer must fill-in from high to low. | |
| **86h** | **STRK1_ H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:2 | Reserved. | |
| | STRK1 [9:8] | 1:0 | 1st Ignition and normal operation count for PWM frequency; double buffer must fill-in from high to low. | |
| **87h** | **STRK1_LMT_L** | **7:0** | **Default : -** | **Access : RO** |
| | STRK1_LMT[7:0] | 7:0 | Maximum duty for 1st ignition and normal operation; count for PWM frequency (lower 8 bits). | |
| **88h** | **STRK1_LMT_H** | **7:0** | **Default : -** | **Access : RO** |
| | - | 7:2 | Reserved. | |
| | STRK1_LMT[9:8] | 1:0 | Maximum duty for 1st ignition and normal operation; count for PWM frequency (higher 2 bits). | |
| **89h** | **STRK2_ L** | **7:0** | **Default : 0xA9** | **Access : R/W** |
| | STRK2_CNT[7:0] | 7:0 | 2nd ignition count for PWM frequency; double-buffer must fill-in from high to low (lower 8 bits). | |
| **8Ah** | **STRK2_ H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:2 | Reserved. | |
| | STRK2 [9:8] | 1:0 | 2nd ignition count for PWM frequency; double-buffer must fill-in from high to low (higher 2 bits). | |
| **8Bh** | **STRK2_LMT** | **7:0** | **Default : -** | **Access : RO** |
| | STRK2_LMT[7:0] | 7:0 | Maximum duty of 2nd ignition; count for PWM frequency. | |
| **8Ch** | **STRK2_LMT** | **7:0** | **Default : -** | **Access : RO** |
| | - | 7:2 | Reserved. | |
| | STRK2_LMT[9:8] | 1:0 | Maximum duty for 2nd ignition; count for PWM frequency. | |
| **8Dh** | **CNT_MD** | **7:0** | **Default : 0x55** | **Access : R/W** |
| | FB2_MD_CTRL | 7:4 | Counts for entering FB2 Mode Control. | |
| | FAULTZ_OVP | 3:0 | Counts for FAULTZ Over-Voltage Protection. | |
| **8Eh** | **BRST_L** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | BRST_CNT[7:0] | 7:0 | Counts for Burst-mode frequency (lower 8 bits; filling sequence: 8Fh, 8Eh, 91h, 90h). | |
| **8Fh** | **BRST_H** | **7:0** | **Default : 0x00** | **Access : R/W** |

## Digital PWM Register (Bank = 04, Registers 6Bh ~ FFh)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | - | 7:2 | Reserved. | |
| | BRST_CNT[9:8] | 1:0 | Counts for Burst-mode frequency (higher 2 bits; filling sequence: 8Fh, 8Eh, 91h, 90h). | |
| **90h** | **BRST_DUTY_L** | **7:0** | **Default : 0x10** | **Access : R/W** |
| | BRST_DUTY[7:0] | 7:0 | Counts for Burst-mode Duty (lower 8 bits; filling sequence: 8Fh, 8Eh, 91h, 90h). | |
| **91h** | **BRST_DUTY_H** | **7:0** | **Default : 0x01** | **Access : R/W** |
| | - | 7:2 | Reserved. | |
| | BRST_DUTY[9:8] | 1:0 | Counts for Burst-mode Duty (higher 2 bits; filling sequence: 8Fh, 8Eh, 91h, 90h). | |
| **92h** | **STRK1_TIME_L** | **7:0** | **Default : 0x50** | **Access : R/W** |
| | STRK1_TIME[7:0] | 7:0 | Counts for 1st ignition Time (lower 8 bits). | |
| **93h** | **STRK1_TIME_M** | **7:0** | **Default : 0xC3** | **Access : R/W** |
| | STRK1_TIME[15:8] | 7:0 | Counts for 1st Ignition Time (middle 8 bits). | |
| **94h** | **STRK1_TIME_H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | STRK1_TIME[19:16] | 3:0 | Counts for 1st ignition time (higher 4 bits). | |
| **95h** | **TTAL_STRK_TIME_L** | **7:0** | **Default : 0x38** | **Access : R/W** |
| | TTAL_STRK_TIME[7:0] | 7:0 | Counts for 1st ignition time + 2nd ignition time (lower 8 bits). | |
| **96h** | **TTAL_STRK_TIME_M** | **7:0** | **Default : 0xC1** | **Access : R/W** |
| | TTAL_STRK_TIME[15:8] | 7:0 | Counts for 1st ignition time + 2nd ignition time (middle 8 bits). | |
| **97h** | **TTAL_STRK_TIME_H** | **7:0** | **Default : 0x01** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | TTAL_STRK_TIME[19:16] | 3:0 | Counts for 1st ignition time + 2nd ignition time (higher 4 bits). | |
| **98h** | **BRST_RAMP1** | **7:0** | **Default : 0x22** | **Access : Reserved** |
| | BRST_RAMP1[7:0] | 7:0 | Burst-mode Ramp control (lower 8 bits). | |
| **99h** | **BRST_RAMP2** | **7:0** | **Default : 0x11** | **Access : Reserved** |
| | PWM_MAX_DUTY | 7 | PWM Maximum Duty.<br>0: STRIKE minus 16.<br>1: STRIKE minus 32. | |
| | STEPS | 6:4 | Counts for Steps. | |
| | BRST_RAMP1[11:8] | 3:0 | Burst-mode Ramp control (higher 4 bits).<br>Four steps: 99[3:1], {99[0], 98[7:6]}, 98[5:3], 98[2:0]. | |
| **9Ah** | **KEY_PRTEC** | **7:0** | **Default : 0x00** | **Access : R/W** |

## Digital PWM Register (Bank = 04, Registers 6Bh ~ FFh)

| Index | Name | Bits | Description | |
|---|---|---|---|---|
| | KEY_PRTEC | 7:0 | Key, code=CF. | |
| **9Bh** | **FAIL_STUS** | **7:0** | **Default : -** | **Access : RO** |
| | FAIL_SAFE_ON | 7 | Fail-Safe finds PWM is over max-on time. | |
| | FAULTZ_H_MD_FB2_F | 6 | FAULTZ High-Mode, FB2 Fail. | |
| | FB1_OVP | 5 | FB1 Over-Voltage Protection while FAULTZ is high. | |
| | STRK_FAIL | 4 | Unable to force FAULTZ=1 after 2-step Striking. | |
| | FAULTZ_ABNRM | 3 | FAULTZ accidentally goes from high to low. | |
| | VIN_OV | 2 | VIN Over-Voltage. | |
| | VIN_UV | 1 | VIN Under-Voltage. | |
| | STRTUP_VIN_F | 0 | Startup VIN Fail. | |
| **9Ch** | **SAR_FB2_DAT** | **7:0** | **Default : -** | **Access : RO** |
| | SAR_FB2_DAT | 7:0 | SAR FB2 Data. | |
| **9Dh** | **SAR_FB1_DAT** | **7:0** | **Default : -** | **Access : RO** |
| | SAR_FB1_DAT | 7:0 | SAR FB1 Data. | |
| **9Eh** | **SAR_FAULTZ_DAT** | **7:0** | **Default : -** | **Access : RO** |
| | SAR_FAULTZ_DAT | 7:0 | SAR FAULTZ Data. | |
| **9Fh** | **SAR_VIN_DAT** | **7:0** | **Default : -** | **Access : RO** |
| | SAR_VIN_DAT | 7:0 | SAR VIN Data. | |
| **A0h** | **DUTY_RPRT1** | **7:0** | **Default : -** | **Access : RO** |
| | DUTY_RPRT1[7:0] | 7:0 | PWM Duty. | |
| **A1h** | **DUTY_RPRT2** | **7:0** | **Default : -** | **Access : RO** |
| | DUTY_RPRT2[7:0] | 7:0 | PWM Duty. | |
| **A2h** | **DUTY_RPRT3** | **7:0** | **Default : -** | **Access : RO** |
| | - | 7:4 | Reserved. | |
| | DUTY_RPRT3[5:0] | 5:0 | PWM Duty. | |
| **A4h** | **SAR_SET1** | **7:0** | **Default : 0x09** | **Access : R/W** |
| | FS_Q2_EN | 7 | Enable Q2-Fail Safe. | |
| | FS_Q1_EN | 6 | Enable Q1-Fail Safe. | |
| | SAR_CLK_SEL | 5 | Select SAR Clock source.<br>0: PWM clock.<br>1: MPLL_CLK_OUT. | |
| | SAR_CLK_DIV_RATIO | 4:0 | Divide Ratio for SAR Clock. | |
| **A5h** | **SAR_SET2** | **7:0** | **Default : 0x00** | **Access : R/W** |

| Digital PWM Register (Bank = 04, Registers 6Bh ~ FFh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| | - | 7:4 | Reserved. | |
| | SAR_CH_SEL | 3:2 | Channel Select for SAR. | |
| | SAR_DEBUNCE_SET | 1:0 | De-bounce Setting for SAR. | |
| **A6h** | **SAR_SET3** | **7:0** | **Default : 0x0B** | **Access : R/W** |
| | SAR_SAMPLE_PRD | 7:0 | System clock counts for Sample Period. | |
| **A7h** | **SAR_SET4** | **7:0** | **Default : 0x30** | **Access : R/W** |
| | C1_Q2 | 7 | Setting for programmable IO. | |
| | C1_Q1 | 6 | Setting for programmable IO. | |
| | C0_Q2 | 5 | Setting for programmable IO. | |
| | C0_Q1 | 4 | Setting for programmable IO. | |
| | EPD_Q2 | 3 | Enable input PAD_Q2 pull-down (default unused). | |
| | EPD_Q1 | 2 | Enable input PAD_Q1 pull-down (default unused). | |
| | EN33V_DPWM | 1 | Enable 3.3V supply for AVDD_SAR. | |
| | SAR_TST | 0 | Set SAR ADC input to zero. | |
| **ABh** | **HSYNC_PLL_SET** | **7:0** | **Default : 0x93** | **Access : R/W** |
| | USE_CLKDIV_EN | 7 | Enable Bit for using Clock Divider instead of using PLL.<br>0: Disable.<br>1: Enable. | |
| | PLL_LOCK | 6 | PLL Lock. | |
| | STRK1_SEL | 5 | Choose to use STRIKE1 or synchronized STRIKE1. | |
| | CLKIN_SEL | 4 | Select to use MPLL_CLK_OUT/(MPLL_CLK_OUT/2). | |
| | PLL_MODE | 3:2 | PLL-Mode setting. | |
| | HSYNC_SOURCE_SEL | 1 | Select-bit for Selecting the Source of HSYNC. | |
| | HSYNC_PLL_EN | 0 | Enable bit for HSYNC PLL. | |
| **ACh** | **PLL_CD** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | PLL_M_CD | 7:4 | PLL M-Code; must be>0. | |
| | PLL_N_CD | 3:0 | PLL N-Code; must be>0. | |
| **ADh** | **PLL_STUS1** | **7:0** | **Default : -** | **Access : RO** |
| | PLL_STUS_RPRT | 7:0 | HSYNC PLL Status Report. | |
| **AEh** | **PLL_STUS2** | **7:0** | **Default : -** | **Access : RO** |
| | HSYNC_IN | 7 | Monitor Input HSYNC. | |
| | PLL_STUS_RPRT | 6:0 | HSYNC PLL Status Report. | |
| **AFh** | **DIVD_RATIO** | **7:0** | **Default : 0x30** | **Access : R/W** |
| | HSYNC_DIVD_RATIO | 7:0 | Divide-Ratio while PLL is in divider-mode. | |

| Digital PWM Register (Bank = 04, Registers 6Bh ~ FFh) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| **B0h** | **WDT_L** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | WDT[7:0] | 7:0 | Counts for WDT; (wanted PWM maximum on-time)/(BIU Clock) (lower 8 bits). | |
| **B1h** | **WDT_H** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | WDT[9:8] | 1:0 | Counts for WDT; (wanted PWM maximum on-time) / (BIU Clock) (higher 2 bits). | |
| **B2h** | **PLL_SET** | **7:0** | **Default : 0x20** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | HSYNC_SAFE_MD | 5 | HSYNC Safe-Mode. | |
| | PLL_CLMP_RATIO | 4:0 | PLL Clamp Value. | |
| **B3h ~ FFh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |

## Misc Register (Bank = 05)

| Misc Register (Bank = 05) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| **00h ~ 09h** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:1 | Reserved. | |
| **10h** | **REG_VD_10** | **7:0** | **Default : 0x69** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | REG_LSCTDIS_EN | 2 | White peak detect bypass the coast signal Enable. | |
| | REG_PREMAV_EN | 1 | First field macro-vision output Enable. | |
| | REG_OSDTST_EN | 0 | OSD test pattern input ADC path Enable. | |
| **11h ~ 1Fh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **20h** | **REG_CALG** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_CALG_EN | 7 | 0: Disable.<br>1: Enable gain auto CAL procedure. | |
| | REG_CALG_TRIG | 6 | Write an 1 to start gain CAL procedure. | |
| | REG_CALG_UPD | 5 | 1: Auto update gain cal result. | |
| | REG_CALG_STSSEL | 4 | Select gain CAL status for CAL status reg. | |
| | REG_CALG_INI | 3:2 | Select intrinsic ADC gain for 0.7Vpp input.<br>00: 0x6f.<br>01: 0x67.<br>10: 0x5f.<br>11: 0x57. | |
| | REG_CALO_BLK | 1 | 0: Use DOUT code 0 as offset CAL target.<br>1: Use DOUT code 16 (8-bit) as offset CAL target. | |
| | REG_CAL_LOCK | 0 | 1: Ignode PLL lock for CAL. | |
| **21h** | **REG_GAIN_AGC0** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_GAIN_AGC0 | 7:0 | PGA control for VD AGC range 0. | |
| **22h** | **REG_GAIN_AGC1** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_GAIN_AGC1 | 7:0 | PGA control for VD AGC range 1. | |
| **23h** | **REG_GAIN_AGC2** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_GAIN_AGC2 | 7:0 | PGA control for VD AGC range 2. | |
| **24h** | **REG_ADC_OV** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_VREF_OV | 7 | 0: Disable.<br>1: Enable ADC VREF override by register. | |

| Misc Register (Bank = 05) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| | REG_GSHIFT_OV | 6 | 0: Disable.<br>1: Enable ADC GSHIFT override by register. | |
| | REG_GAIN_OV | 5 | 0: Disable.<br>1: Enable ADC gain override by register. | |
| | REG_OFFSET_OV | 4 | 0: Disable.<br>1: Enable ADC offset override by register. | |
| | REG_AGC_NEWMAP | 3 | 0: Disable.<br>1: Enable PGA controlled by register for VD AGC. | |
| | REG_GSHIFT_AGC | 2:0 | GSHIFT control for VD AGC range 0,1,2 | |
| **25h** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **26h** | **REG_ADC_ICTRL** | **7:0** | **Default : 0x05** | **Access : R/W** |
| | REG_ADC_ICTRL | 7:0 | ADC current control for pipeline stages. | |
| **27h** | **REG_ADC** | **7:0** | **Default : 0x05** | **Access : R/W** |
| | REG_RDAC_ICTRL | 7:6 | ADC R-DAC current control. | |
| | REG_ADC_IMODE | 5:4 | ADC current mode control. | |
| | - | 3 | Reserved. | |
| | REG_ADC_VCTRL | 2:0 | ADC bias voltage control. | |
| **28h** | **REG_CLAMP** | **7:0** | **Default : 0x05** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | REG_REF_TST | 5:4 | ADC Reference circuit Test mode. | |
| | REG_VCLAMP_D | 3:0 | Select VD input Clamp voltage level. | |
| **29h** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |
| **30h** | **REG_MICROCODE_0_H** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_MICROCODE_0_H | 7:0 | Microcode_0[15:8]. | |
| **31h** | **REG_GAIN_AGC1** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_GAIN_AGC1 | 7:0 | Microcode_0[7:0]. | |
| **32h** | **REG_MICROCODE_1_H** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_MICROCODE_1_H | 7:0 | Microcode_1[15:8]. | |
| **33h** | **REG_MICROCODE_1_L** | **7:0** | **Default : 0x80** | **Access : R/W** |

| Misc Register (Bank = 05) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| | REG_MICROCODE_1_L | 7:0 | Microcode_1[7:0]. | |
| **34h** | **REG_MICROCODE_2_H** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_MICROCODE_2_H | 7:0 | Microcode_2[15:8]. | |
| **35h** | **REG_MICROCODE_2_L** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_MICROCODE_2_L | 7:0 | Microcode_2[7:0]. | |
| **36h** | **REG_MICROCODE_3_H** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | **REG_MICROCODE_3_H** | 7:0 | Microcode_3[15:8]. | |
| **37h** | **REG_MICROCODE_3_L** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_MICROCODE_3_L | 7:0 | Microcode_3[7:0]. | |
| **38h** | **REG_MICROCODE_4_H** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_MICROCODE_4_H | 7:0 | Microcode_4[15:8]. | |
| **39h** | **REG_MICROCODE_4_L** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_MICROCODE_4_L | 7:0 | Microcode_4[7:0]. | |
| **3Ah** | **REG_MICROCODE_5_H** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_MICROCODE_5_H | 7:0 | Microcode_5[15:8]. | |
| **3Bh** | **REG_MICROCODE_5_L** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_MICROCODE_5_L | 7:0 | Microcode_5[7:0]. | |
| **3Ch** | **REG_MICROCODE_6_H** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_MICROCODE_6_H | 7:0 | Microcode_6[15:8]. | |
| **3Dh** | **REG_MICROCODE_6_L** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_MICROCODE_6_L | 7:0 | Microcode_6[7:0]. | |
| **3Eh** | **REG_MICROCODE_7_H** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_MICROCODE_7_H | 7:0 | Microcode_7[15:8]. | |

| Misc Register (Bank = 05) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| **3Fh** | **REG_MICROCODE_7_L** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_MICROCODE_7_L | 7:0 | Microcode_7[7:0]. | |
| **40h** | **REG_MICROCODE_8_H** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_MICROCODE_8_H | 7:0 | Microcode_8[15:8]. | |
| **41h** | **REG_MICROCODE_8_L** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_MICROCODE_8_L | 7:0 | Microcode_8[7:0]. | |
| **42h** | **REG_MICROCODE_9_H** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_MICROCODE_9_H | 7:0 | Microcode_9[15:8]. | |
| **43h** | **REG_MICROCODE_9_L** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_MICROCODE_9_L | 7:0 | Microcode_9[7:0]. | |
| **44h** | **REG_MICROCODE_A_H** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_MICROCODE_A_H | 7:0 | Microcode_a[15:8]. | |
| **45h** | **REG_MICROCODE_A_L** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_MICROCODE_A_L | 7:0 | Microcode_a[7:0]. | |
| **46h** | **REG_MICROCODE_B_H** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_MICROCODE_B_H | 7:0 | Microcode_b[15:8]. | |
| **47h** | **REG_MICROCODE_B_L** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_MICROCODE_B_L | 7:0 | Microcode_b[7:0]. | |
| **48h** | **REG_MICROCODE_C_H** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_MICROCODE_C_H | 7:0 | Microcode_c[15:8]. | |
| **49h** | **REG_MICROCODE_C_L** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_MICROCODE_C_L | 7:0 | Microcode_c[7:0]. | |
| **4Ah** | **REG_MICROCODE_D_H** | **7:0** | **Default : 0x80** | **Access : R/W** |

| Misc Register (Bank = 05) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| | REG_MICROCODE_D_H | 7:0 | Microcode_d[15:8]. | |
| **4Bh** | **REG_MICROCODE_D_L** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_MICROCODE_D_L | 7:0 | Microcode_d[7:0]. | |
| **4Ch** | **REG_MICROCODE_E_H** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_MICROCODE_E_H | 7:0 | Microcode_e[15:8]. | |
| **4Dh** | **REG_MICROCODE_E_L** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_MICROCODE_E_L | 7:0 | Microcode_e[7:0]. | |
| **4Eh** | **REG_MICROCODE_F_H** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_MICROCODE_F_H | 7:0 | Microcode_f[15:8]. | |
| **4Fh** | **REG_MICROCODE_F_L** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_MICROCODE_F_L | 7:0 | Microcode_f[7:0]. | |
| **50h** | **REG_BIST** | **7:0** | **Default : 0x80** | **Access : R** |
| | - | 7:2 | Reserved. | |
| | ANY_BIST_FAIL | 1 | Any BIST Fail. | |
| | BIST_DONE | 0 | BIST Done. | |
| **51h** | **REG_BIST_EN** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | RSTPATGEN | 2 | Reset Pat Gen. | |
| | BIST_EN | 1 | BIST Enable. | |
| | BIST_MODE | 0 | BIST Mode. | |
| **52h** | **PATTERN[15:8]** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | PATTERN[15:8] | 7:0 | Pattern[15:8]. | |
| **53h** | **PATTERN[7:0]** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | PATTERN[7:0] | 7:0 | Pattern[7:0]. | |
| **54h** | **MIN_ADDR[15:8]** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | MIN_ADDR[15:8] | 7:0 | Min_Addr[15:8]. | |
| **55h** | **MIN_ADDR[7:0]** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | MIN_ADDR[7:0] | 7:0 | Min_Addr [7:0]. | |
| **56h** | **MAX_ADDR[15:8]** | **7:0** | **Default : 0x80** | **Access : R/W** |

| Misc Register (Bank = 05) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| | MAX_ADDR[15:8] | 7:0 | Max_Addr [15:8]. | |
| **57h** | **MAX_ADDR[7:0]** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | MAX_ADDR[7:0] | 7:0 | Max_Addr [7:0]. | |
| **58h** | **RETENTION_CNTR [31:24]** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | RETENTION_CNTR [31:24] | 7:0 | Retention_Counter[31:24]. | |
| **59h** | **RETENTION_CNTR [23:16]** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | RETENTION_CNTR [23:16] | 7:0 | Retention_Counter[23:16]. | |
| **5Ah** | **RETENTION_CNTR [15:8]** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | RETENTION_CNTR [15:8] | 7:0 | Retention_Counter[15:8]. | |
| **5Bh** | **RETENTION_CNTR [7:0]** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | RETENTION_CNTR[7:0] | 7:0 | Retention_Counter[7:0]. | |
| **5Ch** | **BIST_FAIL_BUS [31:24]** | **7:0** | **Default : 0x80** | **Access : R** |
| | BIST_FAIL_BUS[31:24] | 7:0 | BIST_Fail_Bus[31:24]. | |
| **5Dh** | **BIST_FAIL_BUS [23:16]** | **7:0** | **Default : 0x80** | **Access : R** |
| | BIST_FAIL_BUS[23:16] | 7:0 | BIST_Fail_Bus[23:16]. | |
| **5Eh** | **BIST_FAIL_BUS [15:8]** | **7:0** | **Default : 0x80** | **Access : R** |
| | BIST_FAIL_BUS[15:8] | 7:0 | BIST_Fail_Bus[15:8]. | |
| **5Fh** | **BIST_FAIL_BUS[7:0]** | **7:0** | **Default : 0x80** | **Access : R** |
| | BIST_FAIL_BUS[7:0] | 7:0 | BIST_Fail_Bus[7:0]. | |
| **60h** | **REG_IP_VSYNC0** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_IP_VSYNC0 | 7:0 | Reg_IP_VSYNC0. | |
| **61h** | **REG_IP_VSYNC1** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_IP_VSYNC1 | 7:0 | Reg_IP_VSYNC1. | |
| **62h** | **REG_IP_SC0** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_IP_SC0 | 7:0 | Reg_IP_SC0. | |

| Misc Register (Bank = 05) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| **63h** | **REG_IP_SC1** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_IP_SC1 | 7:0 | Reg_IP_SC1. | |
| **64h** | **REG_IP_SC2** | **7:0** | **Default : 0x80** | **Access : R** |
| | REG_IP_SC2 | 7:0 | Reg_IP_SC2. | |
| **65h** | **REG_CCFL_65** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_CCFL_65 | 7:0 | Reg_CCFL_65. | |
| **66h** | **REG_CCFL_66** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_CCFL_66 | 7:0 | Reg_CCFL_66. | |
| **67h** | **REG_OSD_PAD00_2ND** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_OSD_PAD00_2ND | 7:0 | Reg_OSD_pad00_2nd. | |
| **68h** | **REG_OSD_PAD01_2ND** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_OSD_PAD01_2ND | 7:0 | Reg_OSD_pad01_2nd. | |
| **69h** | **REG_OSD_PAD02_2ND** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_OSD_PAD02_2ND | 7:0 | Reg_OSD_pad02_2nd. | |
| **6Ah** | **REG_OSD_PAD03_2ND** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_OSD_PAD03_2ND | 7:0 | Reg_OSD_pad03_2nd | |
| **6Bh** | **REG_OSD_PAD04_2ND** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_OSD_PAD04_2ND | 7:0 | Reg_OSD_pad04_2nd. | |
| **6Ch** | **REG_OSD_PAD05_2ND** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_OSD_PAD05_2ND | 7:0 | Reg_OSD_pad05_2nd. | |
| **6Dh** | **REG_OSD_PAD06_2ND** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_OSD_PAD06_2ND | 7:0 | Reg_OSD_pad06_2nd. | |
| **6Eh** | **REG_OSD_PAD07_2ND** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_OSD_PAD07_2ND | 7:0 | Reg_OSD_pad07_2nd. | |
| **6Fh** | **REG_OSD_PAD08_2ND** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_OSD_PAD08_2ND | 7:0 | Reg_OSD_pad08_2nd. | |

| Misc Register (Bank = 05) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| **70h** | **REG_OSD_PAD09_2ND** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_OSD_PAD09_2ND | 7:0 | Reg_OSD_pad09_2nd. | |
| **71h** | **REG_OSD_PAD0A_2ND** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_OSD_PAD0A_2ND | 7:0 | Reg_OSD_pad0a_2nd. | |
| **72h** | **REG_OSD_PAD0B_2ND** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_OSD_PAD0B_2ND | 7:0 | reg_osd_pad0b_2nd | |
| **73h** | **REG_OSD_PAD0C_2ND** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_OSD_PAD0C_2ND | 7:0 | Reg_OSD_pad0c_2nd. | |
| **74h** | **REG_OSD_PAD0D_2ND** | **7:0** | **Default : 0x80** | **Access : R** |
| | REG_OSD_PAD0D_2ND | 7:0 | Reg_OSD_pad0d_2nd. | |
| **75h** | **REG_OSD_PAD0E_2ND** | **7:0** | **Default : 0x80** | **Access : R** |
| | REG_OSD_PAD0E_2ND | 7:0 | Reg_OSD_pad0e_2nd. | |
| **76h** | **REG_OSD_PAD0F_2ND** | **7:0** | **Default : 0x80** | **Access : R** |
| | REG_OSD_PAD0F_2ND | 7:0 | Reg_OSD_pad0f_2nd. | |
| **77h** | **REG_OSD_PAD10_2ND** | **7:0** | **Default : 0x80** | **Access : R** |
| | REG_OSD_PAD10_2ND | 7:0 | Reg_OSD_pad10_2nd. | |
| **78h** | **REG_OSD_PAD11_2ND** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_OSD_PAD11_2ND | 7:0 | Reg_OSD_pad11_2nd. | |
| **79h** | **REG_OSD_PAD12_2ND** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_OSD_PAD12_2ND | 7:0 | Reg_OSD_pad12_2nd. | |
| **7Ah** | **REG_OSD_PAD13_2ND** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_OSD_PAD13_2ND | 7:0 | Reg_OSD_pad13_2nd. | |
| **7Bh** | **REG_OSD_PAD14_2ND** | **7:0** | **Default : 0x80** | **Access : R/W** |

| Misc Register (Bank = 05) | | | | |
|---|---|---|---|---|
| **Index** | **Name** | **Bits** | **Description** | |
| | REG_OSD_PAD14_2ND | 7:0 | Reg_OSD_pad14_2nd. | |
| **7Ch** | **REG_OSD_PAD15_2ND** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_OSD_PAD15_2ND | 7:0 | Reg_OSD_pad15_2nd. | |
| **7Dh** | **REG_OSD_PAD16_2ND** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_OSD_PAD16_2ND | 7:0 | reg_osd_pad16_2nd. | |
| **7Eh** | **REG_OSD_PAD17_2ND** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_OSD_PAD17_2ND | 7:0 | Reg_OSD_pad17_2nd. | |
| **7Fh** | **REG_OSD_DEF_CHAR_HIGH_REG** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_OSD_DEF_CHAR_HIGH_REG | 7:0 | REG_OSD_DEF_CHAR_HIGH_REG. | |
| **80h** | **REG_OSD_CFONT_EXT_START_ADR** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_OSD_CFONT_EXT_START_ADR | 7:0 | REG_OSD_CFONT_EXT_START_ADR. | |
| **81h** | **REG_OSD_L_M8C_RAM_START** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_OSD_L_M8C_RAM_START | 7:0 | REG_OSD_L_M8C_RAM_START. | |
| **82h** | **REG_PAL32_CTRL** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_PAL32_CTRL | 7:0 | Reg_pal32_ctrl. | |
| **83h** | **REG_OP2_CTRL** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | REG_OP2_CTRL | 7:0 | Reg_OSD_pad0a_2nd. | |
| **84h** | **REG_OSC_SET** | **7:0** | **Default : 0x80** | **Access : R** |
| | REG_BONDING_KEY | 7 | Bonding Key status. | |
| | - | 6:3 | Reserved. | |
| | REG_RING_OSC_SEL | 2:1 | Ring-Oscillator mode Selection. | |
| | REG_RING_OSC_EN | 0 | Ring-Oscillator Enable. | |
| **85h ~ FFh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | 7:0 | Reserved. | |

## MGD Register (Bank = 05)

| MGD Register (Bank = 05) | | | | |
|---|---|---|---|---|
| **Index (Absolute)** | **Mnemonic** | **Bit** | **Description** | |
| **48h (0590h)** | **REG0590** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | HISTOGRAM_THRD_0_L[7:0] | 7:0 | Histogram threshold0 low byte. | |
| **48h (0591h)** | **REG0591** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | HISTOGRAM_THRD_0_H[7:0] | 7:0 | Histogram threshold0 high byte. | |
| **49h (0592h)** | **REG0592** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | HISTOGRAM_THRD_1_L[7:0] | 7:0 | Histogram threshold1 low byte. | |
| **49h (0593h)** | **REG0593** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | HISTOGRAM_THRD_1_H[7:0] | 7:0 | Histogram threshold1 high byte. | |
| **4Ah (0594h)** | **REG0594** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | HISTOGRAM_THRD_2_L[7:0] | 7:0 | Histogram threshold2 low byte. | |
| **4Ah (0595h)** | **REG0595** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | HISTOGRAM_THRD_2_H[7:0] | 7:0 | Histogram threshold2 high byte. | |
| **4Bh (0596h)** | **REG0596** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | HISTOGRAM_THRD_3_L[7:0] | 7:0 | Histogram threshold3 low byte. | |
| **4Bh (0597h)** | **REG0597** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | HISTOGRAM_THRD_3_H[7:0] | 7:0 | Histogram threshold3 high byte. | |
| **4Ch (0598h)** | **REG0598** | **7:0** | **Default : 0xF8** | **Access : R/W** |
| | FSTABLE[3:0] | 7:4 | DCR power on control frame count. | |
| | YAVG_ALPHA[3:0] | 3:0 | Yavg frame alpha value, 0:current yavg, f:last yavg. | |
| **4Ch (0599h)** | **REG0599** | **7:0** | **Default : 0xFE** | **Access : R/W** |
| | YAVG_RGB_EN | 7 | Select RGB max value to calculate yavg, 0:select Y for yavg. | |
| | YAVG_LIM_EN | 6 | Enable yavg_avg to limit ygain tuning step. | |
| | HIST_RGB_EN | 5 | Select RGB max value to calculate histogram. | |
| | HIST_121_EN | 4 | Histogram 121 low pass filter enable. | |
| | YOUT_RGB_EN | 3 | Select RGB max value to lookup DLC gain. | |
| | YGAIN_HIST_LIM_EN | 2 | Enable histogram to limit ygain max value. | |
| | DLC_GAIN_LIM_EN | 1 | Enable dlc gain limit function to keep detail of data. | |
| | DCR_EN | 0 | Enable DCR function. | |
| **4Dh (059Ah)** | **REG059A** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | YGAIN[7:0] | 7:0 | Gain for calculate YGAIN, 80->1x. | |

## MGD Register (Bank = 05)

| Index (Absolute) | Mnemonic | Bit | Description | |
|---|---|---|---|---|
| 4Dh (059Bh) | **REG059B** | **7:0** | **Default : 0xA0** | **Access : R/W** |
| | YGAIN_STEP[7:0] | 7:0 | Ygain jump step.<br>[7]: Enable different of ygain for ygain step,<br>[6:0]:gain of ydiff, 40 -> 1x.<br>[6:0]:ygain step x2 when [7]=0. | |
| 4Eh (059Ch) | **REG059C** | **7:0** | **Default : 0x10** | **Access : R/W** |
| | YGAIN_STEP_MAX[7:0] | 7:0 | Max value of ygain jump step. | |
| 4Eh (059Dh) | **REG059D** | **7:0** | **Default : 0x01** | **Access : R/W** |
| | YGAIN_STEP_MIN[7:0] | 7:0 | Max value of ygain jump step. | |
| 4Fh (059Eh) | **REG059E** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | YGAIN_OFFSET_L[7:0] | 7:0 | Offset for calculate ygain, /16. | |
| 4Fh (059Fh) | **REG059F** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | YGAIN_OFFSET_H[3:0] | 3:0 | Offset for calculate ygain. | |
| 50h (05A0h) | **REG05A0** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | DLC_OFFSET_L[7:0] | 7:0 | Offset for calculate DLC gain, /16. | |
| 50h (05A1h) | **REG05A1** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | DLC_OFFSET_H[3:0] | 3:0 | Offset for calculate DLC gain, /16. | |
| 51h (05A2h) | **REG05A2** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | DLC_GAIN[7:0] | 7:0 | Gain for calculate DLC gain, 80->1x. | |
| 51h (05A3h) | **REG05A3** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | PWM_FDLY[7:0] | 7:0 | PWM power on control. | |
| 52h (05A4h) | **REG05A4** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | PWM_PERIOD_L[7:0] | 7:0 | PWM period set. | |
| 52h (05A5h) | **REG05A5** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | PWM_PERIOD_H[7:0] | 7:0 | PWM period set. | |
| 53h (05A6h) | **REG05A6** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | PWM_DUTY_L[7:0] | 7:0 | PWM duty set. | |
| 53h (05A7h) | **REG05A7** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | PWM_DUTY_H[7:0] | 7:0 | PWM duty set. | |
| 54h (05A8h) | **REG05A8** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | PWM_R_OFFSET_L[7:0] | 7:0 | Offset for calculate PWM duty, /16. | |

| MGD Register (Bank = 05) | | | | |
|---|---|---|---|---|
| **Index (Absolute)** | **Mnemonic** | **Bit** | **Description** | |
| **54h (05A9h)** | **REG05A9** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | PWM_R_OFFSET_H[3:0] | 3:0 | Offset for calculate PWM duty, /16. | |
| **55h (05AAh)** | **REG05AA** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | DCR_OFFSET_L[7:0] | 7:0 | Offset for calculate PWM duty gain, /16. | |
| **55h (05ABh)** | **REG05AB** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | DCR_OFFSET_H[3:0] | 3:0 | Offset for calculate PWM duty gain, /16. | |
| **56h (05ACh)** | **REG05AC** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | DCR_GAIN[7:0] | 7:0 | Gain for calculate PWM duty gain, 80->1x. | |
| **56h (05ADh)** | **REG05AD** | **7:0** | **Default : 0x10** | **Access : R/W** |
| | PWM_HTOTAL_EN | 7 | Enable htotal for PWM period. | |
| | PWM_INV | 6 | Inverse PWM pol. | |
| | PWM_RST_SEL[1:0] | 5:4 | PWM reset select.<br>0: Period.<br>1: Vsync.<br>2: First line.<br>3: Vertical blanking. | |
| | DLC_EN | 3 | Enable DLC function. | |
| | DLC_TABLE_SEL | 2 | DLC table debug mode enable. | |
| | PWM_TABLE_EN | 1 | Select dcr table for PWM control. | |
| | - | 0 | Reserved. | |
| **57h (05AEh)** | **REG05AE** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | DLC_TABLE_DIN[7:0] | 7:0 | DLC table debug din. | |
| **57h (05AFh)** | **REG05AF** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | PWM_TABLE_DIN[7:0] | 7:0 | PWM table debug din. | |
| **58h (05B0h)** | **REG05B0** | **7:0** | **Default : 0x00** | **Access : RO** |
| | YAVG_OUT[7:0] | 7:0 | Current Frame Y Average. | |
| **58h (05B1h)** | **REG05B1** | **7:0** | **Default : 0x00** | **Access : RO** |
| | YAVG_PRE_OUT[7:0] | 7:0 | Previous Frame Y Average. | |
| **59h (05B2h)** | **REG05B2** | **7:0** | **Default : 0x00** | **Access : RO** |
| | YAVG_AVG_OUT[7:0] | 7:0 | Current and Previous Y Average by alpha. | |
| **59h** | **REG05B3** | **7:0** | **Default : 0x00** | **Access : RO** |

## MGD Register (Bank = 05)

| Index (Absolute) | Mnemonic | Bit | Description | |
|---|---|---|---|---|
| (05B3h) | YGAIN_OUT[7:0] | 7:0 | Adjustment Frame Value. | |
| 5Ah (05B4h) | **REG05B4** | **7:0** | **Default : 0x00** | **Access : RO** |
| | YGAIN_TMP_OUT[7:0] | 7:0 | Adjustment Target Frame Value. | |
| 5Ah (05B5h) | **REG05B5** | **7:0** | **Default : 0x00** | **Access : RO** |
| | YGAIN_HIST_OUT[7:0] | 7:0 | Histogram Frame Value. | |
| 5Bh (05B6h) | **REG05B6** | **7:0** | **Default : 0x00** | **Access : RO** |
| | HISTOGRAM0_L[7:0] | 7:0 | Histogram Result for Sec0[7:0]. | |
| 5Bh (05B7h) | **REG05B7** | **7:0** | **Default : 0x00** | **Access : RO** |
| | HISTOGRAM0_H[7:0] | 7:0 | Histogram Result for Sec0[15:8]. | |
| 5Ch (05B8h) | **REG05B8** | **7:0** | **Default : 0x00** | **Access : RO** |
| | HISTOGRAM1_L[7:0] | 7:0 | Histogram Result for Sec1[7:0]. | |
| 5Ch (05B9h) | **REG05B9** | **7:0** | **Default : 0x00** | **Access : RO** |
| | HISTOGRAM1_H[7:0] | 7:0 | Histogram Result for Sec1[15:8]. | |
| 5Dh (05BAh) | **REG05BA** | **7:0** | **Default : 0x00** | **Access : RO** |
| | HISTOGRAM2_L[7:0] | 7:0 | Histogram Result for Sec2[7:0]. | |
| 5Dh (05BBh) | **REG05BB** | **7:0** | **Default : 0x00** | **Access : RO** |
| | HISTOGRAM2_H[7:0] | 7:0 | Histogram Result for Sec2[15:8]. | |
| 5Eh (05BCh) | **REG05BC** | **7:0** | **Default : 0x00** | **Access : RO** |
| | HISTOGRAM3_L[7:0] | 7:0 | Histogram Result for Sec3[7:0]. | |
| 5Eh (05BDh) | **REG05BD** | **7:0** | **Default : 0x00** | **Access : RO** |
| | HISTOGRAM3_H[7:0] | 7:0 | Histogram Result for Sec3[15:8]. | |
| 5Fh (05BEh) | **REG05BE** | **7:0** | **Default : 0x00** | **Access : RO** |
| | HISTOGRAM4_L[7:0] | 7:0 | Histogram Result for Sec4[7:0]. | |
| 5Fh (05BFh) | **REG05BF** | **7:0** | **Default : 0x00** | **Access : RO** |
| | HISTOGRAM4_H[7:0] | 7:0 | Histogram Result for Sec4[15:8]. | |
| 60h (05C0h) | **REG05C0** | **7:0** | **Default : 0x00** | **Access : RO** |
| | HISTOGRAM5_L[7:0] | 7:0 | Histogram Result for Sec5[7:0]. | |
| 60h (05C1h) | **REG05C1** | **7:0** | **Default : 0x00** | **Access : RO** |
| | HISTOGRAM5_H[7:0] | 7:0 | Histogram Result for Sec5[15:8]. | |
| 61h (05C2h) | **REG05C2** | **7:0** | **Default : 0x00** | **Access : RO** |
| | HISTOGRAM6_L[7:0] | 7:0 | Histogram Result for Sec6[7:0]. | |
| 61h (05C3h) | **REG05C3** | **7:0** | **Default : 0x00** | **Access : RO** |
| | HISTOGRAM6_H[7:0] | 7:0 | Histogram Result for Sec6[15:8]. | |

| MGD Register (Bank = 05) | | | | |
|---|---|---|---|---|
| **Index (Absolute)** | **Mnemonic** | **Bit** | **Description** | |
| **62h (05C4h)** | **REG05C4** | **7:0** | **Default : 0x00** | **Access : RO** |
| | HISTOGRAM7_L[7:0] | 7:0 | Histogram Result for Sec7[7:0]. | |
| **62h (05C5h)** | **REG05C5** | **7:0** | **Default : 0x00** | **Access : RO** |
| | HISTOGRAM7_H[7:0] | 7:0 | Histogram Result for Sec7[15:8]. | |
| **63h (05C6h)** | **REG05C6** | **7:0** | **Default : 0x00** | **Access : RO** |
| | HISTOGRAM8_L[7:0] | 7:0 | Histogram Result for Sec8[7:0]. | |
| **63h (05C7h)** | **REG05C7** | **7:0** | **Default : 0x00** | **Access : RO** |
| | HISTOGRAM8_H[7:0] | 7:0 | Histogram Result for Sec8[15:8]. | |
| **64h (05C8h)** | **REG05C8** | **7:0** | **Default : 0x00** | **Access : RO** |
| | HISTOGRAM9_L[7:0] | 7:0 | Histogram Result for Sec9[7:0]. | |
| **64h (05C9h)** | **REG05C9** | **7:0** | **Default : 0x00** | **Access : RO** |
| | HISTOGRAM9_H[7:0] | 7:0 | Histogram Result for Sec9[15:8]. | |
| **65h (05CAh)** | **REG05CA** | **7:0** | **Default : 0x00** | **Access : RO** |
| | HISTOGRAM10_L[7:0] | 7:0 | Histogram Result for Sec10[7:0]. | |
| **65h (05CBh)** | **REG05CB** | **7:0** | **Default : 0x00** | **Access : RO** |
| | HISTOGRAM10_H[7:0] | 7:0 | Histogram Result for Sec10[15:8]. | |
| **66h (05CCh)** | **REG05CC** | **7:0** | **Default : 0x00** | **Access : RO** |
| | HISTOGRAM11_L[7:0] | 7:0 | Histogram Result for Sec11[7:0]. | |
| **66h (05CDh)** | **REG05CD** | **7:0** | **Default : 0x00** | **Access : RO** |
| | HISTOGRAM11_H[7:0] | 7:0 | Histogram Result for Sec11[15:8]. | |
| **67h (05CEh)** | **REG05CE** | **7:0** | **Default : 0x00** | **Access : RO** |
| | HISTOGRAM12_L[7:0] | 7:0 | Histogram Result for Sec12[7:0]. | |
| **67h (05CFh)** | **REG05CF** | **7:0** | **Default : 0x00** | **Access : RO** |
| | HISTOGRAM12_H[7:0] | 7:0 | Histogram Result for Sec12[15:8]. | |
| **68h (05D0h)** | **REG05D0** | **7:0** | **Default : 0x00** | **Access : RO** |
| | HISTOGRAM13_L[7:0] | 7:0 | Histogram Result for Sec13[7:0]. | |
| **68h (05D1h)** | **REG05D1** | **7:0** | **Default : 0x00** | **Access : RO** |
| | HISTOGRAM13_H[7:0] | 7:0 | Histogram Result for Sec13[15:8]. | |
| **69h (05D2h)** | **REG05D2** | **7:0** | **Default : 0x00** | **Access : RO** |
| | HISTOGRAM14_L[7:0] | 7:0 | Histogram Result for Sec14[7:0]. | |
| **69h (05D3h)** | **REG05D3** | **7:0** | **Default : 0x00** | **Access : RO** |
| | HISTOGRAM14_H[7:0] | 7:0 | Histogram Result for Sec14[15:8]. | |
| **6Ah** | **REG05D4** | **7:0** | **Default : 0x00** | **Access : RO** |

## MGD Register (Bank = 05)

| Index (Absolute) | Mnemonic | Bit | Description | |
|---|---|---|---|---|
| (05D4h) | HISTOGRAM15_L[7:0] | 7:0 | Histogram Result for Sec15[7:0]. | |
| 6Ah (05D5h) | **REG05D5** | **7:0** | **Default : 0x00** | **Access : RO** |
| | HISTOGRAM15_H[7:0] | 7:0 | Histogram Result for Sec15[15:8]. | |
| 6Bh (05D6h) | **REG05D6** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | HACT_L[7:0] | 7:0 | Horizontal Active Pixel Number[7:0]. | |
| 6Bh (05D7h) | **REG05D7** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | HACT_H[3:0] | 3:0 | Horizontal Active Pixel Number[11:8]. | |
| 6Ch (05D8h) | **REG05D8** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | VACT_L[7:0] | 7:0 | Vertical Active Pixel Number[7:0]. | |
| 6Ch (05D9h) | **REG05D9** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | VACT_H[3:0] | 3:0 | Vertical Active Pixel Number[11:8]. | |
| 6Dh (05DAh) | **REG05DA** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | HBLANK[7:0] | 7:0 | Horizontal Blank Position. | |
| 6Dh (05DBh) | **REG05DB** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | YGAIN_TMP_MIN[7:0] | 7:0 | Ygain tmp min value. | |
| 6Eh (05DCh) | **REG05DC** | **7:0** | **Default : 0x00** | **Access : RO** |
| | PWM_PERIOD_R[7:0] | 7:0 | PWM Period Output. | |
| 6Eh (05DDh) | **REG05DD** | **7:0** | **Default : 0x00** | **Access : RO** |
| | PWM_DUTY_R[7:0] | 7:0 | PWM Duty Output. | |
| 70h (05E0h) | **REG05E0** | **7:0** | **Default : 0x19** | **Access : R/W** |
| | VIP_3D_DITHER_EN | 7 | 3d dither enable. | |
| | VIP_3D_DITHER_OBN8_EN | 6 | 3d dither output bit number is 8 bits enable.<br>1: Output 8 bits.<br>0: Output 6 bits. | |
| | VIP_3D_DITHER_MONO_EN | 5 | 3d dither monochrome mode enable. | |
| | VIP_3D_DITHER_LSB_EN | 4 | 3d dither LSB dither enable. | |
| | VIP_3D_DITHER_LSB_SEL[1:0] | 3:2 | 3d dither LSB dither table select. | |
| | VIP_3D_DITHER_MSB_SEL[1:0] | 1:0 | 3d dither MSB dither table select. | |
| 70h (05E1h) | **REG05E1** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | VIP_3D_DITHER_ON | 7 | 3d dither on. | |
| | VIP_3D_DITHER_VCLR_EN | 6 | 3d dither vertical dither enable. | |

## MGD Register (Bank = 05)

| Index (Absolute) | Mnemonic | Bit | Description | |
|---|---|---|---|---|
| | VIP_3D_DITHER_VCLR_NO[1:0] | 5:4 | 3d dither vertical dither table number. | |
| | VIP_3D_DITHER_LSB_VCLR_EN | 3 | 3d dither LSB vertical dither enable. | |
| | VIP_3D_DITHER_10_MOD_EN | 2 | 3d dither 10 mode detect enable. | |
| | VIP_3D_DITHER_LSB_VCLR_NO[1:0] | 1:0 | 3d dither LSB vertical dither table number. | |
| **71h (05E2h)** | **REG05E2** | **7:0** | **Default : 0x99** | **Access : R/W** |
| | VIP_3D_DITHER_MSB_R_MASK[1:0] | 7:6 | 3d dither MSB R channel mask. | |
| | VIP_3D_DITHER_MSB_B_MASK[1:0] | 5:4 | 3d dither MSB B channel mask. | |
| | VIP_3D_DITHER_LSB_R_MASK[1:0] | 3:2 | 3d dither LSB R channel mask. | |
| | VIP_3D_DITHER_LSB_B_MASK[1:0] | 1:0 | 3d dither LSB B channel mask. | |
| **71h (05E3h)** | **REG05E3** | **7:0** | **Default : 0x0C** | **Access : R/W** |
| | VIP_3D_DITHER_DEBUG[7:0] | 7:0 | 3d dither Debug Use. | |
| **72h (05E4h)** | **REG05E4** | **7:0** | **Default : 0x27** | **Access : R/W** |
| | H_DITHER_TABLE0[7:0] | 7:0 | 3d dither Horizontal dither table0. | |
| **72h (05E5h)** | **REG05E5** | **7:0** | **Default : 0x8D** | **Access : R/W** |
| | H_DITHER_TABLE1[7:0] | 7:0 | 3d dither Horizontal dither table1. | |
| **73h (05E6h)** | **REG05E6** | **7:0** | **Default : 0x63** | **Access : R/W** |
| | H_DITHER_TABLE2[7:0] | 7:0 | 3d dither Horizontal dither table2. | |
| **73h (05E7h)** | **REG05E7** | **7:0** | **Default : 0x9C** | **Access : R/W** |
| | H_DITHER_TABLE3[7:0] | 7:0 | 3d dither Horizontal dither table3. | |
| **74h (05E8h)** | **REG05E8** | **7:0** | **Default : 0x4E** | **Access : R/W** |
| | V_DITHER_TABLE0[7:0] | 7:0 | 3d dither Vertical dither table0. | |
| **74h (05E9h)** | **REG05E9** | **7:0** | **Default : 0x4B** | **Access : R/W** |
| | V_DITHER_TABLE1[7:0] | 7:0 | 3d dither Vertical dither table1. | |
| **75h (05EAh)** | **REG05EA** | **7:0** | **Default : 0x93** | **Access : R/W** |
| | V_DITHER_TABLE2[7:0] | 7:0 | 3d dither Vertical dither table2. | |
| **75h (05EBh)** | **REG05EB** | **7:0** | **Default : 0x39** | **Access : R/W** |
| | V_DITHER_TABLE3[7:0] | 7:0 | 3d dither Vertical dither table3. | |

# ADC Registers (Bank 06)

## ADC_ATOP Register (Bank = 06)

| ADC_ATOP Register (Bank = 06) | | | | |
|---|---|---|---|---|
| **Index (Absolute)** | **Mnemonic** | **Bit** | **Description** | |
| **01h (0602h)** | **REG0602** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | VD_YC_EN | 2 | 1: Enable S-Video input function. | |
| | VD_EN | 1 | 1: Enable VD function. | |
| | ADC_ENA | 0 | 1: Enable ADC_A RGB function. | |
| **02h (0604h)** | **REG0604** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | MUX_BSEL[1:0] | 7:6 | BADC mux sel, 00:RGB/YPbPr ,<br>01:VD ,10:DVI,11:reserved. | |
| | MUX_GSEL[1:0] | 5:4 | GADC mux sel, 00:RGB/YPbPr ,<br>01:VD ,10:DVI,11:reserved. | |
| | MUX_RSEL[1:0] | 3:2 | RADC mux sel, 00:RGB/YPbPr ,<br>01:VD ,10:DVI,11:reserved. | |
| | AMUXA[1:0] | 1:0 | Select ADC_A RGB channel, VD FB mode RGB channel.<br>00: Selects input channel 0.<br>01: Selects input channel 1.<br>10: Selects input channel 2. | |
| **02h (0605h)** | **REG0605** | **7:0** | **Default : 0x40** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | MUX_RGB_EN | 6 | 1: Enable RGB MUX. | |
| | MUX_RGBSEL[1:0] | 5:4 | 00: Channel0 , 01:channel1, 10:channel2. | |
| | - | 3:0 | Reserved. | |
| **03h (0606h)** | **REG0606** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | MUX_VDSEL_C[3:0] | 7:4 | Select VD SC channel.<br>0000: CVBS0.<br>0001: CVBS1.<br>0010: CVBS2.<br>0011: CVBS3.<br>0100: CVBS4 (Y0).<br>0101: CVBS5 (Y1).<br>0110: CVBS6 (C0).<br>0111: CVBS7 (C1).<br>1000: R0. | |

| ADC_ATOP Register (Bank = 06) | | | |
|---|---|---|---|
| **Index (Absolute)** | **Mnemonic** | **Bit** | **Description** |
| | | | 1001: R1.<br>1010: R2.<br>Others: None. |
| | MUX_VDSEL_Y[3:0] | 3:0 | Select VD CVBS/Y channel.<br>0000: CVBS0.<br>0001: CVBS1.<br>0010: CVBS2.<br>0011: CVBS3.<br>0100: CVBS4 (Y0).<br>0101: CVBS5 (Y1).<br>0110: CVBS6 (C0).<br>0111: CVBS7 (C1).<br>1000: G0.<br>1001: G1.<br>1010: G2.<br>Others: None. |
| **03h (0607h)** | **REG0607** | **7:0** | **Default : 0x00** **Access : R/W** |
| | - | 7:6 | Reserved. |
| | TEST_CLKMUX_RGB_INV | 5 | 1: Invert RGB ADC clock phase. |
| | - | 4 | Reserved. |
| | MUX_RGBVD | 3 | 1: RGB ADC in VD mode. |
| | - | 2 | Reserved. |
| | MUX_C_EN | 1 | 1: Enable VD-C channel mux. |
| | MUX_Y_EN | 0 | 1: Enable VD-Y channel mux. |
| **04h (0608h)** | **REG0608** | **7:0** | **Default : 0xFF** **Access : R/W** |
| | PDN_PLL | 7 | 1: Power down ADC PLL. |
| | PDN_PHD | 6 | 1: Power down phase digitizer. |
| | PDN_ADCB | 5 | 1: Power down ADC_B. |
| | PDN_ADCG | 4 | 1: Power down ADC_G. |
| | PDN_ADCR | 3 | 1: Power down ADC_R. |
| | PDN_REF | 2 | 1: Power down all reference voltage. |
| | PDN_BG | 1 | 1: Power down bandgap. |
| | PDN_REF_RGB | 0 | 1: Power down RGB ADC reference voltage. |
| **04h (0609h)** | **REG0609** | **7:0** | **Default : 0x7F** **Access : R/W** |
| | - | 7 | Reserved. |

## ADC_ATOP Register (Bank = 06)

| Index (Absolute) | Mnemonic | Bit | Description | |
|---|---|---|---|---|
| | PDN_HSYNC | 6 | 1: Power down Hsync_Cmp. | |
| | PDN_SOG_MAIN | 5 | 1: Power down online SOG Main. | |
| | PDN_SOG_DAC | 4 | 1: Power down online SOG DAC. | |
| | PDN_PLL2 | 3 | 1: Power down VD PLL. | |
| | PDN_ICLP_VDC | 2 | 1: Power down I-clamp on VD-C channel. | |
| | PDN_ICLP_VDY | 1 | 1: Power down I-clamp on VD-Y channel. | |
| | PDN_ICLP_RGB | 0 | 1: Power down I-clamp on RGB channel. | |
| **05h (060Ah)** | **REG060A** | **7:0** | **Default : 0x07** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | PDN_ADCPLA_PDAC_B | 2 | 1= power down adcpla phase dac b. | |
| | PDN_ADCPLA_PDAC_G | 1 | 1= power down adcpla phase dac g. | |
| | PDN_ADCPLA_PDAC_R | 0 | 1= power down adcpla phase dac r. | |
| **06h (060Ch)** | **REG060C** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | PD_CLK[7:0] | 7:0 | Clock power down control.<br>[0]: PD_CLKXTAL.<br>[1]: PD_CLK200.<br>[2]: PD_CLK400.<br>[3]: PD_CLKPLL.<br>[4]: PD_CLKD_R.<br>[5]: PD_CLKD_G.<br>[6]: PD_CLKD_B.<br>[8]: PD_CLKD.<br>[9]: PD_CLKD_VD.<br>[10]: PD_DVIDETCLK. | |
| **06h (060Dh)** | **REG060D** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | PD_CLK[15:8] | 7:0 | See description of '060Ch'. | |
| **07h (060Eh)** | **REG060E** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | SOFTRST[7:0] | 7:0 | 1: Soft reset for ADCPLL blocks.<br>[15:6]: reserved.<br>[5]: Soft-reset PHASE DAC.<br>[4]: Soft-reset ATOP.<br>[3]: Soft-reset PLLB.<br>[2]: Soft-reset ADCB.<br>[1]: Soft-reset PLLA.<br>[0]: Soft-reset ADCA. | |
| **07h** | **REG060F** | **7:0** | **Default : 0x00** | **Access : R/W** |

| ADC_ATOP Register (Bank = 06) | | | | |
|---|---|---|---|---|
| **Index (Absolute)** | **Mnemonic** | **Bit** | **Description** | |
| **(060Fh)** | SOFTRST[15:8] | 7:0 | See description of '060Eh'. | |
| **09h (0612h)** | **REG0612** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | ADC_PLL_PORST_EN | 4 | Pull the LPF of the PLL to zero.<br>1: Zero.<br>0: Normal. | |
| | - | 3:0 | Reserved. | |
| **09h (0613h)** | **REG0613** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | VD_PLL_PORST_EN | 4 | Pull the LPF of the PLL to zero.<br>1: Zero.<br>0: Normal. | |
| | - | 3:0 | Reserved. | |
| **0Ah (0614h)** | **REG0614** | **7:0** | **Default : 0xC1** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | ADC_PLL_MOD[1:0] | 4:3 | Select the divider number of the post divider.<br>00: Normal; 01: DIV2; 10:DIV4; 11:DIV8. | |
| | ADC_PLL_MULT[2:0] | 2:0 | ADC PLL clock multiplier = N+1.<br>000: /1.<br>001: /2.<br>&&.<br>111: /8. | |
| **0Ah (0615h)** | **REG0615** | **7:0** | **Default : 0xC1** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | VD_PLL_MOD[1:0] | 4:3 | Select the divider number of the post divider.<br>00: Normal; 01: DIV2; 10:DIV4; 11:DIV8. | |
| | VD_PLL_MULT[2:0] | 2:0 | ADC PLL clock multiplier = N+1.<br>000: /1.<br>001: /2.<br>&&.<br>111: /8. | |
| **0Bh ~ 0Dh (0616h ~ 061Bh)** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| **0Fh** | **REG061E** | **7:0** | **Default : 0x00** | **Access : R/W** |

## ADC_ATOP Register (Bank = 06)

| Index (Absolute) | Mnemonic | Bit | Description | |
|---|---|---|---|---|
| (061Eh) | ADCPLA_PHASE_CC[7:0] | 7:0 | Select ADCA sampling clock phase. | |
| 0Fh (061Fh) | **REG061F** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:2 | Reserved. | |
| | ADCPLA_PHASE_CC[9:8] | 1:0 | See description of '061Eh'. | |
| 10h (0620h) | **REG0620** | **7:0** | **Default : 0x1F** | **Access : R/W** |
| | ADCPLA_PHASE_DELTA[7:0] | 7:0 | Select ADCA phase delta between CLKCC & CLKADC. | |
| 10h (0621h) | **REG0621** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:2 | Reserved. | |
| | ADCPLA_PHASE_DELTA[9:8] | 1:0 | See description of '0620h'. | |
| 11h ~ 12h (0622h ~ 0624h) | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| 13h ~ 17h (0626h ~ 062Eh) | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| 18h (0630h) | **REG0630** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:2 | Reserved. | |
| | ADCPLA_PLLDIV_DBLOAD_WAIT_VSYNC | 1 | 1 = update plldiv during phase vsync. | |
| | ADCPLA_PHASE_DBLOAD_WAIT_VSYNC | 0 | 1 = update phase during phase vsync. | |
| 18h ~ 19h (0631h ~ 0633h) | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| 20h (0640h) | **REG0640** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | HSYNC_LVL[2:0] | 2:0 | Select Hsync Cmp's reference voltage.<br>000: REFH=1.54V, REFL=1.10V.<br>001: REFH=1.54V, REFL=0.88V.<br>010: REFH=1.76V, REFL=1.10V.<br>011: REFH=1.76V, REFL=0.88V.<br>100: REFH=1.87V, REFL=1.10V.<br>101: REFH=1.87V, REFL=0.88V.<br>110: REFH=1.76V, REFL=1.32V.<br>111: REFH=1.87V, REFL=1.32V. | |
| 21h ~ 21h | **-** | **7:0** | **Default : -** | **Access : -** |

## ADC_ATOP Register (Bank = 06)

| Index (Absolute) | Mnemonic | Bit | Description | |
|---|---|---|---|---|
| (0642h ~ 0643h) | - | - | Reserved. | |
| 22h (0644h) | **REG0644** | **7:0** | **Default : 0x30** | **Access : R/W** |
| | XTAL_FREQ[7:0] | 7:0 | Set XTAL frequency for timing detection normalization (default: 12MHz, format: 6.2 MHz). | |
| 22h (0645h) | **REG0645** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:2 | Reserved. | |
| | ADC_INMSEL | 1 | 1: Enable one negative pin function. | |
| | - | 0 | Reserved. | |
| 23h (0646h) | **REG0646** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | YDIT_MD[2:0] | 5:3 | Select ADC Y dither mode for display. | |
| | CDIT_MD[2:0] | 2:0 | Select ADC C dither mode.<br>000: Off.<br>001: 1-bit noise.<br>010: 2-bit noise.<br>011: 3-bit noise.<br>100: Seq2 1-bit toggle noise.<br>101: Seq2 2-bit toggle noise.<br>110: Seq4 2-bit toggle noise.<br>110: Seq4 3-bit toggle noise. | |
| 23h (0647h) | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| 24h (0648h) | **REG0648** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | BLPF_BWM[3:0] | 7:4 | B-channel negative input LPF bandwidth. | |
| | BLPF_BWP[3:0] | 3:0 | B-channel positive input LPF bandwidth. | |
| 24h (0649h) | **REG0649** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | GLPF_BWM[3:0] | 7:4 | G-channel negative input LPF bandwidth. | |
| | GLPF_BWP[3:0] | 3:0 | G-channel positive input LPF bandwidth. | |
| 25h (064Ah) | **REG064A** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | RLPF_BWM[3:0] | 7:4 | R-channel negative input LPF bandwidth. | |
| | RLPF_BWP[3:0] | 3:0 | R-channel positive input LPF bandwidth. | |
| 25h ~ 27h (064Bh ~ 064Eh) | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |

## ADC_ATOP Register (Bank = 06)

| Index (Absolute) | Mnemonic | Bit | Description | |
|---|---|---|---|---|
| 28h (0650h) | **REG0650** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | VDLPFGAIN_C | 5 | 1: Gain=2 in VD-C LPF. | |
| | VDLPFGAIN_Y | 4 | 1: Gain=2 in VD-Y LPF. | |
| | - | 3:2 | Reserved. | |
| | VLPF_C_EN | 1 | 1: Enable VD-C LPF. | |
| | VLPF_Y_EN | 0 | 1: Enable VD-Y LPF. | |
| 28h (0651h) | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| 29h (0652h) | **REG0652** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | SOG_BW[4:0] | 4:0 | Select online SOG filter bandwidth.<br>00000: 973MHz.<br>00001: 116MHz.<br>00011: 63MHz.<br>00111: 43MHz.<br>01111: 32MHz.<br>11111: 26MHz. | |
| 29h (0653h) | **REG0653** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | SOG_CAL_EN | 5 | For rising edge trigger enable of sog online calibration 0->1. | |
| | SOG_HYS | 4 | [0]: Disable online SOG comparator hysteresis function. | |
| | SOG_CAL | 3 | [0]: Enable online SOG calibration loop. | |
| | - | 2:0 | Reserved. | |
| 2Ah (0654h) | **REG0654** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | SOG_VCLP[3:0] | 7:4 | [0]: Select online SOG clamping voltage.<br>XXX0: 1.11V.<br>XXX1: 1.2V. | |
| | SOG_SW[3:0] | 3:0 | Select online SOG input source.<br>XX00: SOGIN0.<br>XX01: SOGIN1.<br>XX10: SOGIN2.<br>XX11: SOGIN3. | |

## ADC_ATOP Register (Bank = 06)

| Index (Absolute) | Mnemonic | Bit | Description | |
|---|---|---|---|---|
| **2Bh (0656h)** | **REG0656** | **7:0** | **Default : 0x20** | **Access : R/W** |
| | SOG_VCOMP[7:0] | 7:0 | [7:0] : Select online SOG comparator threshold voltage.<br>=1.08+(1.32-1.08)/256*CODES.<br>.<br>[11:10] Select online SOG comparator hysteresis voltage.<br>00: 5mV.<br>01: 10mV.<br>10: 15mV.<br>11: 20mV. | |
| **2Bh (0657h)** | **REG0657** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | SOG_VCOMP[11:8] | 3:0 | See description of '0656h'. | |
| **2Ch (0658h)** | **REG0658** | **7:0** | **Default : 0x05** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | SOG_CONTROL_OFFSET | 2 | 1=add user offset for offset code on online. | |
| | SOG_CONTROL_BYPASS | 1 | 1= bypass online sog control register. | |
| | PDN_SOG_MUX | 0 | 1: Power down online SOG MUX. | |
| **2Dh (065Ah)** | **REG065A** | **7:0** | **Default : 0x20** | **Access : R/W** |
| | SOG_INIT_WAIT_TIME[7:0] | 7:0 | Sog online calibration initial setup waiting time. | |
| **2Dh (065Bh)** | **REG065B** | **7:0** | **Default : 0x10** | **Access : R/W** |
| | SOG_SWEEP_WAIT_TIME[7:0] | 7:0 | Sog online calibration sweep code waiting time. | |
| **2Eh (065Ch)** | **REG065C** | **7:0** | **Default : 0x08** | **Access : R/W** |
| | SOG_EVA_WAIT_TIME[7:0] | 7:0 | Sog online calibration evaluate code waiting time. | |
| **2Fh (065Eh)** | **REG065E** | **7:0** | **Default : 0x00** | **Access : RO** |
| | SOG_STATUS[7:0] | 7:0 | Sog online calibration function test status.<br>{SOG,CAL_EN,SOG_VCOMP}. | |
| **2Fh (065Fh)** | **REG065F** | **7:0** | **Default : 0x00** | **Access : RO** |
| | - | 7:2 | Reserved. | |
| | SOG_STATUS[9:8] | 1:0 | See description of '065Eh'. | |
| **34h (0668h)** | **REG0668** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | TRIM_LDO_RGB_SEL | 3 | 1: VCAL from LDO rstring for RGB 0: VCAL from trimming for RGB. | |

## ADC_ATOP Register (Bank = 06)

| Index (Absolute) | Mnemonic | Bit | Description | |
|---|---|---|---|---|
| | LDO_RGB_SEL | 2 | 1: 1.05v output voltage from LDO rstring for RGB. 0: 0.55v output votlage from LDO rstring for RGB. | |
| | VBG_EN | 1 | | |
| | LDO_EN | 0 | 1: Enable 1.05v and 0.55v output from LDO rstring 0:disable. | |
| **34h ~ 39h (0669h ~ 0673h)** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| **40h (0680h)** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| **41h ~ 44h (0682h ~ 0689h)** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| **45h (068Ah)** | **REG068A** | **7:0** | **Default : 0x01** | **Access : R/W** |
| | - | 7:2 | Reserved. | |
| | HS_ADC_SEL_MUX[1:0] | 1:0 | CLKD_ATOP select, 00/01/10/11: R/G/B/R. | |
| **45h ~ 47h (068Bh ~ 068Fh)** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| **4Ah ~ 4Dh (0694h ~ 069Bh)** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| **4Fh (069Eh)** | **REG069E** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | HSYNC_DEGLITCH_TH[7:0] | 7:0 | Select HSYNC deglitch pulse width threshold (step size = MPLL clock). | |
| **4Fh (069Fh)** | **REG069F** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | SOG_DEGLITCH_TH[7:0] | 7:0 | Select SOG deglitch pulse width threshold (step size = MPLL clock). | |
| **50h (06A0h)** | **REG06A0** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | IP_SOG_DEGLITCH | 5 | 1: Enable SOG input deglitch for IP mode detection. | |
| | IP_HSYNC_DEGLITCH | 4 | 1: Enable HSYNC input deglitch for IP mode detection. | |

## ADC_ATOP Register (Bank = 06)

| Index (Absolute) | Mnemonic | Bit | Description | |
|---|---|---|---|---|
| | PLL_SOG_DEGLITCH | 3 | 1: Enable SOG input deglitch for PLL. | |
| | PLL_HSYNC_DEGLITCH | 2 | 1: Enable HSYNC input deglitch for PLL. | |
| | ADC_SOG_DEGLITCH | 1 | 1: Enable SOG input deglitch for ADC clamp. | |
| | ADC_HSYNC_DEGLITCH | 0 | 1: Enable HSYNC input deglitch for ADC clamp. | |
| **60h (06C0h)** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| **61h ~ 61h (06C2h ~ 06C3h)** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| **70h (06E0h)** | **REG06E0** | **7:0** | **Default : 0x01** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | MPLL_CLK_ADC216M_PD | 2 | 1: Disable MPLL_CLK_ADC216M clock ou. | |
| | MPLL_CLK_ADC432M_PD | 1 | 1: Disable MPLL_CLK_ADC432M clock ou. | |
| | MPLL_PD | 0 | 1: Power down MPLLl. | |
| **71h (06E2h)** | **REG06E2** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:2 | Reserved. | |
| | MPLL_DISFRUN | 1 | Disable VCO free-run. | |
| | MPLL_IN_SELECT | 0 | Input clock selection:.<br>While TEST[5]=1'b1,.<br>1'b0 1.0V clock input;.<br>1'b1 3.3V clock input after internal level shift to 1.0V;. | |
| **71h (06E3h)** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| **72h (06E4h)** | **REG06E4** | **7:0** | **Default : 0x04** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | MPLL_OUTPUT_DIV[1:0] | 3:2 | Output-divider control:.<br>2'b00: /1;.<br>2'b01: /2; <-- default.<br>2'b10: /4;.<br>2'b11: /8:. | |
| | MPLL_INPUT_DIV[1:0] | 1:0 | Input-divider control:.<br>2'b00: /1; <-- default.<br>2'b01: /2;.<br>2'b10: /4;. | |

| ADC_ATOP Register (Bank = 06) | | | | |
|---|---|---|---|---|
| **Index (Absolute)** | **Mnemonic** | **Bit** | **Description** | |
| | | | 2'b11: /8:. | |
| **72h (06E5h)** | **REG06E5** | **7:0** | **Default : 0x12** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | MPLL_LOOP_DIV[4:0] | 4:0 | Loop-divider control:.<br>5'h00: /1; 5'h01: /1; 5'h02: /2; 5'h03: /3 &.<br>5'h1F: /31;.<br>Others are not acceptable;. | |
| **73h (06E6h)** | **REG06E6** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:2 | Reserved. | |
| | MPLL_ICP_ICTRL[1:0] | 1:0 | Charge-Pump current control:.<br>2'h00: Icp x 4.<br>2'h01: Icp x 3.<br>2'h10: Icp x 2.<br>2'h11: Icp x1. | |
| **74h (06E8h)** | **REG06E8** | **7:0** | **Default : 0x31** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | XTAL_SEL[1:0] | 5:4 | Xtal gain control. | |
| | - | 3:1 | Reserved. | |
| | XTAL_EN | 0 | Xtal enable control (active high). | |
| **75h ~ 77h (06EAh ~ 06EFh)** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| **7Fh ~ 7Fh (06FEh ~ 06FFh)** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |

## ADC_DTOP Register (Bank = 06)

| ADC_DTOP Register (Bank = 06) | | | | |
|---|---|---|---|---|
| **Index (Absolute)** | **Mnemonic** | **Bit** | **Description** | |
| **01h (0602h)** | **REG0602** | **7:0** | **Default : 0x95** | **Access : R/W** |
| | PLLDIV[7:0] | 7:0 | ADC PLL divider ratio (Htotal-3).<br>(Write sequence LSB -> MSB). | |
| **01h (0603h)** | **REG0603** | **7:0** | **Default : 0x06** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | PLLDIV[12:8] | 4:0 | See description of '0602h'. | |
| **02h (0604h)** | **REG0604** | **7:0** | **Default : 0x82** | **Access : R/W** |
| | BWCOEF[7:0] | 7:0 | ADC PLL bandwidth coefficient. | |
| **02h (0605h)** | **REG0605** | **7:0** | **Default : 0x09** | **Access : R/W** |
| | FREQCOEF[7:0] | 7:0 | ADC PLL frequency coefficient. | |
| **03h (0606h)** | **REG0606** | **7:0** | **Default : 0x05** | **Access : R/W** |
| | DAMPCOEF[7:0] | 7:0 | ADC PLL damping coefficient. | |
| **03h (0607h)** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| **04h (0608h)** | **REG0608** | **7:0** | **Default : 0x05** | **Access : R/W** |
| | PLL_STATUS_SEL[2:0] | 7:5 | Select PLL digital status. | |
| | PHD_CAL_DIS | 4 | Disable phase digitalizer calibration. | |
| | SETTLE_CNT[3:0] | 3:0 | Select phase digitalizer settling time. | |
| **04h (0609h)** | **REG0609** | **7:0** | **Default : 0xC6** | **Access : R/W** |
| | WDOG_TOL[1:0] | 7:6 | Select PLL watch dog reset tolerance. | |
| | IQCLR_TH[2:0] | 5:3 | PLL lock to unlock threshold. | |
| | IQSET_TH[2:0] | 2:0 | PLL unlock to lock threshold. | |
| **05h (060Ah)** | **REG060A** | **7:0** | **Default : 0x00** | **Access : RO** |
| | PLL_STATUS[7:0] | 7:0 | PLL digital status.<br>000: {LOCK, IQ, SLOW, FAST, FREERUN, 3'b000}. | |
| **06h ~ 06h (060Ch ~ 060Dh)** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| **07h (060Eh)** | **REG060E** | **7:0** | **Default : 0x8A** | **Access : R/W** |
| | HSYNC_POL | 7 | Input HSYNC polarity.<br>0: Low active.<br>1: High active. | |
| | SOG_EN | 6 | Select PLL locking source. | |

| ADC_DTOP Register (Bank = 06) | | | | |
|---|---|---|---|---|
| **Index (Absolute)** | **Mnemonic** | **Bit** | **Description** | |
| | | | 0: HSYNC.<br>1: SOG. | |
| | HSYNC_EDGE | 5 | Select PLL locking edge.<br>0: HSYNC leading edge.<br>1: HSYNC trailing edge. | |
| | CLAMP_EDGE | 4 | Select clamp reference edge.<br>0: HSYNC trailing edge.<br>1: HSYNC leading edge. | |
| | CCDIS | 3 | 1: Disable clamp during coast region. | |
| | WDOG_DIS | 2 | 1: Disable ADC PLL watch dog. | |
| | COAST_POL | 1 | Select coast polarity.<br>0: Low active.<br>1: High active. | |
| | - | 0 | Reserved. | |
| **07h (060Fh)** | **REG060F** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | HSOUT_PW[7:0] | 7:0 | Select extended HSOUT pulse width. | |
| **08h (0611h)** | **REG0611** | **7:0** | **Default : 0x05** | **Access : R/W** |
| | CLAMP_DUR[7:0] | 7:0 | Select clamp pulse duration. | |
| **09h (0612h)** | **REG0612** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:2 | Reserved. | |
| | HSOUT_GEN | 1 | 1: Enable HSOUT pulse extension. | |
| | - | 0 | Reserved. | |
| **09h (0613h)** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| **0Bh (0616h)** | **REG0616** | **7:0** | **Default : 0x40** | **Access : R/W** |
| | TIMEOUT_H[7:0] | 7:0 | HSYNC activity timeout period (100us). | |
| **0Bh (0617h)** | **REG0617** | **7:0** | **Default : 0x64** | **Access : R/W** |
| | TIMEOUT_V[7:0] | 7:0 | VSYNC activity timeout period (ms). | |
| **0Ch (0618h)** | **REG0618** | **7:0** | **Default : 0x00** | **Access : RO** |
| | - | 7:6 | Reserved. | |
| | OVF_RGB[5:0] | 5:0 | ADC overflow flags, { OVFB, UNFB, OVFG, UNFG, OVFR, UNFR}. | |
| **0Ch (0619h)** | **REG0619** | **7:0** | **Default : 0x00** | **Access : RO, WO** |
| | - | 7:4 | Reserved. | |

| ADC_DTOP Register (Bank = 06) | | | | |
|---|---|---|---|---|
| **Index (Absolute)** | **Mnemonic** | **Bit** | **Description** | |
| | SOG_TOG | 3 | 1: Active channel SOG toggle status. | |
| | VSYNC_TOG | 2 | 1: Active channel VSYNC toggle status. | |
| | HSYNC_TOG | 1 | 1: Active channel HSYNC toggle status. | |
| | CLROVF_RGB | 0 | Write a 1 to clear ADC_RGB overflow flags. | |
| **0Dh (061Ah)** | **REG061A** | **7:0** | **Default : 0x05** | **Access : R/W** |
| | CLAMP_DLY[7:0] | 7:0 | Select clamp pulse start position relative to input HSYNC edge. | |
| **0Dh (061Bh)** | **REG061B** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | VCLAMP_EN_HACT | 5 | 1: Enable HACT window. | |
| | VCLAMP_HSYNC_OR_HSOUT | 4 | 0: Use HSYNC, 1: use HSOUT. | |
| | CLAMP_DLY[11:8] | 3:0 | See description of '061Ah'. | |
| **10h (0620h)** | **REG0620** | **7:0** | **Default : 0x24** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | RGB_SWAP[5:0] | 5:0 | Select RGBY data to scalar.<br>[1:0]: SEL R.<br>[3:2]: SEL G.<br>[5:4]: SEL B.<br>00: R.<br>01: G.<br>10: B.<br>11: Blank. | |
| **12h (0624h)** | **REG0624** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | BMIDA[1:0] | 5:4 | 0/1=select gnd-clamp/mid-clamp for ADC B.<br>00: 10h000.<br>01: 10h040.<br>10: 10h200. | |
| | GMIDA[1:0] | 3:2 | 0/1=select gnd-clamp/mid-clamp for ADC G.<br>00: 10h000.<br>01: 10h040.<br>10: 10h200. | |
| | RMIDA[1:0] | 1:0 | 0/1=select gnd-clamp/mid-clamp for ADC R.<br>00: 10h000.<br>01: 10h040.<br>10: 10h200. | |

## ADC_DTOP Register (Bank = 06)

| Index (Absolute) | Mnemonic | Bit | Description | |
|---|---|---|---|---|
| **12h (0625h)** | **REG0625** | **7:0** | **Default : 0x28** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | HSOUT2SC_PIPEDLY[3:0] | 5:2 | Hsout pipe delay 1~16=0~F. | |
| | SYNC_SEL_YUV | 1 | Yuv sync sel 1:VD 0:scalar. | |
| | SYNC_SEL_RGB | 0 | Rgb sync sel 1:VD 0:scalar. | |
| **13h (0626h)** | **REG0626** | **7:0** | **Default : 0x84** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | DIT_DISP[2:0] | 2:0 | Select ADC RGB dither mode for display. | |
| **13h (0627h)** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| **14h (0628h)** | **REG0628** | **7:0** | **Default : 0x28** | **Access : R/W** |
| | VSSEP_TH[7:0] | 7:0 | Select VSYNC separator threshold width (unit=XTAL period*2). | |
| **14h (0629h)** | **REG0629** | **7:0** | **Default : 0x40** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | CAL_BW | 6 | 1: Enable max ADC bandwidth during CAL. | |
| | SYNC_SEL | 5 | Select sync source for ADC_DIG.<br>0: From scalar.<br>1: From ADC sync process block. | |
| | COAST_EN | 4 | Enable coast generator.<br>0: Disable coast.<br>1: Enable coast. | |
| | COAST_HS | 3 | Select HSYNC sources for coast line counter.<br>0: PLL locked HSOUT.<br>1: Input HSYNC. | |
| | VSYNC_POL | 2 | Input VSYNC polarity.<br>0: Low active.<br>1: High active. | |
| | VS_SEL | 1 | Select VSYNC input source.<br>0: VSYNC.<br>1: Separated VSYNC. | |
| | VSSEP_SEL | 0 | Select VSYNC separator input source.<br>0: HSYNC or SOG.<br>1: VSYNC. | |
| **15h** | **REG062A** | **7:0** | **Default : 0x00** | **Access : R/W** |

| ADC_DTOP Register (Bank = 06) | | | | |
|---|---|---|---|---|
| **Index (Absolute)** | **Mnemonic** | **Bit** | **Description** | |
| **(062Ah)** | PRECOAST[7:0] | 7:0 | Select PRECOAST lines before VSYNC. | |
| **15h (062Bh)** | **REG062B** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | POSTCOAST[7:0] | 7:0 | Select POSTCOAST lines after VSYNC. | |
| **16h (062Ch)** | **REG062C** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | LAT_SYNC_DLY_SEL[2:0] | 2:0 | Select postcoast lines after VSYNC. | |
| **17h (062Eh)** | **REG062E** | **7:0** | **Default : 0x14** | **Access : R/W** |
| | ICLAMP_CLPDLY[7:0] | 7:0 | Register setting for delay.<br>(to start of analog clamp). | |
| **17h (062Fh)** | **REG062F** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | ICLAMP_CLPDLY[11:8] | 3:0 | See description of '062Eh'. | |
| **18h (0630h)** | **REG0630** | **7:0** | **Default : 0x08** | **Access : R/W** |
| | ICLAMP_CALDUR[7:0] | 7:0 | Register setting for duration, only for 2^N.<br>(of analog clamp). | |
| **18h (0631h)** | **REG0631** | **7:0** | **Default : 0x04** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | ICLAMP_VEN | 3 | 1=enable clamp once every vsync. | |
| | ICLAMP_COAST_CLP_DIS | 2 | 1 = disable clamp during COAST region (synced). | |
| | ICLAMP_HSYNC_OR_HSOUT | 1 | 0: Use HSYNC, 1: use HSOUT. | |
| | ICLAMP_CLP_EDGE | 0 | 1: Raising edge, 0:falling edge. | |
| **19h (0632h)** | **REG0632** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | ICLAMP_VDLY[7:0] | 7:0 | Clamp pulse line delay for vsync mode. | |
| **19h (0633h)** | **REG0633** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | ICLAMP_CLK_RATE_IN | 7 | Analog iclamp clk polarity, 0:pass, 1:inverit. | |
| | ICLAMP_CLK_RATE[1:0] | 6:5 | 00: X1 Analog ICLAMP.<br>01: X2.<br>10: X4.<br>11: X4. | |
| | ICLAMP_COAST_EXT_CNT[2:0] | 4:2 | Coast extend 0~7 line option. | |
| | ICLAMP_EN_COAST_EXT_CNT | 1 | 1: Enable coast extend 0~7 line option. | |
| | ICLAMP_EN_HACT | 0 | 1: Enable HACT window. | |
| **1Bh** | **REG0636** | **7:0** | **Default : 0x80** | **Access : R/W** |

## ADC_DTOP Register (Bank = 06)

| Index (Absolute) | Mnemonic | Bit | Description | |
|---|---|---|---|---|
| (0636h) | ICLAMP_R_BLANK_LVL[7:0] | 7:0 | Blanking level = 128 (RGB). | |
| 1Bh (0637h) | **REG0637** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | ICLAMP_R_BLANK_LVL[11:8] | 3:0 | See description of '0636h'. | |
| 1Ch (0638h) | **REG0638** | **7:0** | **Default : 0x05** | **Access : R/W** |
| | ICLAMP_R_LOCK_LEVEL[7:0] | 7:0 | Lock level threshold. | |
| 1Ch (0639h) | **REG0639** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | ICLAMP_R_LOCK_LEVEL[11:8] | 3:0 | See description of '0638h'. | |
| 1Dh (063Ah) | **REG063A** | **7:0** | **Default : 0xD0** | **Access : R/W** |
| | ICLAMP_R_LOCK_CNT[7:0] | 7:0 | Match REG_ICLAMP_LOCK_LEVEL counter. | |
| 1Dh (063Bh) | **REG063B** | **7:0** | **Default : 0x07** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | ICLAMP_R_LOCK_CNT[12:8] | 4:0 | See description of '063Ah'. | |
| 1Eh (063Ch) | **REG063C** | **7:0** | **Default : 0x60** | **Access : R/W** |
| | ICLAMP_R_K1_STB[0] | 7 | K1 = 2^(CLMP_K1[6:3]-8-2) * (1 + CLMP_K1[2:0]/8). For Stable. | |
| | ICLAMP_R_K1_INI[6:0] | 6:0 | K1 = 2^(CLMP_K1[6:3]-8-2) * (1 + CLMP_K1[2:0]/8). For Initial. | |
| 1Eh (063Dh) | **REG063D** | **7:0** | **Default : 0x20** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | ICLAMP_R_K1_STB[6:1] | 5:0 | See description of '063Ch'. | |
| 1Fh (063Eh) | **REG063E** | **7:0** | **Default : 0xA0** | **Access : R/W** |
| | ICLAMP_R_K1_EN | 7 | Clamping = leakage + err * gain_true * k1 * k1_en;. | |
| | ICLAMP_R_K2[6:0] | 6:0 | K2 = 2^(CLMP_K2[6:3]-8) * (1 + CLMP_K2[2:0]/8);. | |
| 1Fh (063Fh) | **REG063F** | **7:0** | **Default : 0x03** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | ICLAMP_R_FREZ_CLMP[2:0] | 4:2 | Clamping = leakage.<br>Leakage is frozen.<br>(Coast).<br>K1_en = 0 and k2_en = 0.<br>FREZ_CLMP = FREZ_CLMP_1 \| FREZ_CLMP_2 \| FREZ_CLMP_3;. | |
| | ICLAMP_R_TYPE | 1 | 0: Bottom clamping, RGB/YPbPr = 0;. | |

## ADC_DTOP Register (Bank = 06)

| Index (Absolute) | Mnemonic | Bit | Description | |
|---|---|---|---|---|
| | | | 1: Back-porch calmping. | |
| | ICLAMP_R_K2_EN | 0 | Leakage = leakage + err * gain_true * k1 * k2 * k2_en;. | |
| **20h (0640h)** | **REG0640** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | ICLAMP_R_AGC_FINE[7:0] | 7:0 | Agc fine gain. | |
| **20h (0641h)** | **REG0641** | **7:0** | **Default : 0x1C** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | ICLAMP_R_AGC_COARSE[1:0] | 5:4 | Agc coarse gain. | |
| | ICLAMP_R_AGC_FINE[11:8] | 3:0 | See description of '0640h'. | |
| **21h (0642h)** | **REG0642** | **7:0** | **Default : 0x40** | **Access : R/W** |
| | ICLAMP_R_PGA_OFST[7:0] | 7:0 | Pga offset. | |
| **21h (0643h)** | **REG0643** | **7:0** | **Default : 0x05** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | ICLAMP_R_ERR_MAX[4:0] | 4:0 | Bac_porch_level error < +- REG_CLMP_ERR_MAX <= +-31 * 8 !!!. | |
| **22h (0644h)** | **REG0644** | **7:0** | **Default : 0x4A** | **Access : R/W** |
| | ICLAMP_R_LKG_MODE[1:0] | 7:6 | 001: Adaptive leakage tracking.<br>001: Adaptive leakage tracking.<br>Leakage is bounded by +- REG_ICLAMP_LKG[4:0].<br>010: Freeze leakage.<br>011: Load leakage = REG_ICLAMP_LKG[5] * REG_CLMP_LKG[4:0];.<br>100: Load K1'accu into leakage for quickly 1st order update. | |
| | ICLAMP_R_LKG[5:0] | 5:0 | [5]: Sign bit.<br>0: Posetive.<br>1: Negative.<br>[4:0] : magnitude.<br>0 ~ 31 LSB of +-10uA/32.<br>See REG_ICLAMP_LKG_MODE. | |
| **22h (0645h)** | **REG0645** | **7:0** | **Default : 0x08** | **Access : R/W** |
| | ICLAMP_R_DLKG_MAX[5:0] | 7:2 | Delta_leakage is bounded by +- (REG_CLMP_DLKG_MAX / 512).<br>+- 1/8. | |
| | ICLAMP_R_FREZ_ZERO | 1 | 1: Set CLMP_DSM = 0 when FREZ.<br>0: Set CLMP_DSM = lkg when FREZ. | |

| ADC_DTOP Register (Bank = 06) | | | | |
|---|---|---|---|---|
| **Index (Absolute)** | **Mnemonic** | **Bit** | **Description** | |
| | ICLAMP_R_LKG_MODE[2] | 0 | See description of '0644h'. | |
| **23h (0646h)** | **REG0646** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:2 | Reserved. | |
| | ICLAMP_R_2DSM | 1 | 1: 2nd-order.<br>0: 1st-order. | |
| | ICLAMP_R_FREZ_DSM | 0 | 1: Delta-sigma frozen.<br>CLAMP_fpga/chip[5:0] = round{CLMP_DSM[15:10]+CLMP_DSM[9]}.<br>0: Delta-sigma on. | |
| **23h (0647h)** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| **26h (064Ch)** | **REG064C** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | ICLAMP_G_BLANK_LVL[7:0] | 7:0 | Blanking level = 128 (RGB). | |
| **26h (064Dh)** | **REG064D** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | ICLAMP_G_BLANK_LVL[11:8] | 3:0 | See description of '064Ch'. | |
| **27h (064Eh)** | **REG064E** | **7:0** | **Default : 0x05** | **Access : R/W** |
| | ICLAMP_G_LOCK_LEVEL[7:0] | 7:0 | Lock level threshold. | |
| **27h (064Fh)** | **REG064F** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | ICLAMP_G_LOCK_LEVEL[11:8] | 3:0 | See description of '064Eh'. | |
| **28h (0650h)** | **REG0650** | **7:0** | **Default : 0xD0** | **Access : R/W** |
| | ICLAMP_G_LOCK_CNT[7:0] | 7:0 | Match REG_ICLAMP_LOCK_LEVEL counter. | |
| **28h (0651h)** | **REG0651** | **7:0** | **Default : 0x07** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | ICLAMP_G_LOCK_CNT[12:8] | 4:0 | See description of '0650h'. | |
| **29h (0652h)** | **REG0652** | **7:0** | **Default : 0x60** | **Access : R/W** |
| | ICLAMP_G_K1_STB[0] | 7 | K1 = 2^(CLMP_K1[6:3]-8-2) * (1 + CLMP_K1[2:0]/8).<br>For Stable. | |
| | ICLAMP_G_K1_INI[6:0] | 6:0 | K1 = 2^(CLMP_K1[6:3]-8-2) * (1 + CLMP_K1[2:0]/8).<br>For Initial. | |
| **29h (0653h)** | **REG0653** | **7:0** | **Default : 0x20** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | ICLAMP_G_K1_STB[6:1] | 5:0 | See description of '0652h'. | |

## ADC_DTOP Register (Bank = 06)

| Index (Absolute) | Mnemonic | Bit | Description | |
|---|---|---|---|---|
| **2Ah (0654h)** | **REG0654** | **7:0** | **Default : 0xA0** | **Access : R/W** |
| | ICLAMP_G_K1_EN | 7 | Clamping = leakage + err * gain_true * k1 * k1_en;. | |
| | ICLAMP_G_K2[6:0] | 6:0 | K2 = 2^(CLMP_K2[6:3]-8) * (1 + CLMP_K2[2:0]/8);. | |
| **2Ah (0655h)** | **REG0655** | **7:0** | **Default : 0x03** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | ICLAMP_G_FREZ_CLMP[2:0] | 4:2 | Clamping = leakage.<br>Leakage is frozen.<br>(Coast).<br>K1_en = 0 and k2_en = 0.<br>FREZ_CLMP = FREZ_CLMP_1 \| FREZ_CLMP_2 \| FREZ_CLMP_3;. | |
| | ICLAMP_G_TYPE | 1 | 0: Bottom clamping, RGB/YPbPr = 0;.<br>1: Back-porch calmping. | |
| | ICLAMP_G_K2_EN | 0 | Leakage = leakage + err * gain_true * k1 * k2 * k2_en;. | |
| **2Bh (0656h)** | **REG0656** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | ICLAMP_G_AGC_FINE[7:0] | 7:0 | Agc fine gain. | |
| **2Bh (0657h)** | **REG0657** | **7:0** | **Default : 0x1C** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | ICLAMP_G_AGC_COARSE[1:0] | 5:4 | Agc coarse gain. | |
| | ICLAMP_G_AGC_FINE[11:8] | 3:0 | See description of '0656h'. | |
| **2Ch (0658h)** | **REG0658** | **7:0** | **Default : 0x40** | **Access : R/W** |
| | ICLAMP_G_PGA_OFST[7:0] | 7:0 | Pga offset. | |
| **2Ch (0659h)** | **REG0659** | **7:0** | **Default : 0x05** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | ICLAMP_G_ERR_MAX[4:0] | 4:0 | Bac_porch_level error < +- REG_CLMP_ERR_MAX <= +-31 * 8 !!!. | |
| **2Dh (065Ah)** | **REG065A** | **7:0** | **Default : 0x4A** | **Access : R/W** |
| | ICLAMP_G_LKG_MODE[1:0] | 7:6 | 001: Adaptive leakage tracking.<br>001: Adaptive leakage tracking.<br>Leakage is bounded by +- REG_ICLAMP_LKG[4:0].<br>010: Freeze leakage.<br>011: Load leakage = REG_ICLAMP_LKG[5] * REG_CLMP_LKG[4:0];.<br>100: Load K1'accu into leakage for quickly 1st order | |

| ADC_DTOP Register (Bank = 06) | | | | |
|---|---|---|---|---|
| **Index (Absolute)** | **Mnemonic** | **Bit** | **Description** | |
| | | | update. | |
| | ICLAMP_G_LKG[5:0] | 5:0 | [5]: Sign bit.<br>0: Posetive.<br>1: Negative.<br>[4:0] : magnitude.<br>0 ~ 31 LSB of +-10uA/32.<br>See REG_ICLAMP_LKG_MODE. | |
| **2Dh (065Bh)** | **REG065B** | **7:0** | **Default : 0x08** | **Access : R/W** |
| | ICLAMP_G_DLKG_MAX[5:0] | 7:2 | Delta_leakage is bounded by +- (REG_CLMP_DLKG_MAX / 512).<br>+- 1/8. | |
| | ICLAMP_G_FREZ_ZERO | 1 | 1: Set CLMP_DSM = 0 when FREZ.<br>0: Set CLMP_DSM = lkg when FREZ. | |
| | ICLAMP_G_LKG_MODE[2] | 0 | See description of '065Ah'. | |
| **2Eh (065Ch)** | **REG065C** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:2 | Reserved. | |
| | ICLAMP_G_2DSM | 1 | 1: 2nd-order.<br>0: 1st-order. | |
| | ICLAMP_G_FREZ_DSM | 0 | 1: Delta-sigma frozen.<br>CLAMP_fpga/chip[5:0] = round{CLMP_DSM[15:10]+CLMP_DSM[9]}.<br>0: Delta-sigma on. | |
| **2Eh (065Dh)** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| **30h (0660h)** | **REG0660** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | ICLAMP_B_BLANK_LVL[7:0] | 7:0 | Blanking level = 128 (RGB). | |
| **30h (0661h)** | **REG0661** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | ICLAMP_B_BLANK_LVL[11:8] | 3:0 | See description of '0660h'. | |
| **31h (0662h)** | **REG0662** | **7:0** | **Default : 0x05** | **Access : R/W** |
| | ICLAMP_B_LOCK_LEVEL[7:0] | 7:0 | Lock level threshold. | |
| **31h (0663h)** | **REG0663** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | ICLAMP_B_LOCK_LEVEL[11:8] | 3:0 | See description of '0662h'. | |
| **32h** | **REG0664** | **7:0** | **Default : 0xD0** | **Access : R/W** |

| ADC_DTOP Register (Bank = 06) | | | | |
|---|---|---|---|---|
| **Index (Absolute)** | **Mnemonic** | **Bit** | **Description** | |
| **(0664h)** | ICLAMP_B_LOCK_CNT[7:0] | 7:0 | Match REG_ICLAMP_LOCK_LEVEL counter. | |
| **32h (0665h)** | **REG0665** | **7:0** | **Default : 0x07** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | ICLAMP_B_LOCK_CNT[12:8] | 4:0 | See description of '0664h'. | |
| **33h (0666h)** | **REG0666** | **7:0** | **Default : 0x60** | **Access : R/W** |
| | ICLAMP_B_K1_STB[0] | 7 | K1 = 2^(CLMP_K1[6:3]-8-2) * (1 + CLMP_K1[2:0]/8). For Stable. | |
| | ICLAMP_B_K1_INI[6:0] | 6:0 | K1 = 2^(CLMP_K1[6:3]-8-2) * (1 + CLMP_K1[2:0]/8). For Initial. | |
| **33h (0667h)** | **REG0667** | **7:0** | **Default : 0x20** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | ICLAMP_B_K1_STB[6:1] | 5:0 | See description of '0666h'. | |
| **34h (0668h)** | **REG0668** | **7:0** | **Default : 0xA0** | **Access : R/W** |
| | ICLAMP_B_K1_EN | 7 | Clamping = leakage + err * gain_true * k1 * k1_en;. | |
| | ICLAMP_B_K2[6:0] | 6:0 | K2 = 2^(CLMP_K2[6:3]-8) * (1 + CLMP_K2[2:0]/8);. | |
| **34h (0669h)** | **REG0669** | **7:0** | **Default : 0x03** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | ICLAMP_B_FREZ_CLMP[2:0] | 4:2 | Clamping = leakage.<br>Leakage is frozen.<br>(Coast).<br>K1_en = 0 and k2_en = 0.<br>FREZ_CLMP = FREZ_CLMP_1 \| FREZ_CLMP_2 \| FREZ_CLMP_3;. | |
| | ICLAMP_B_TYPE | 1 | 0: Bottom clamping, RGB/YPbPr = 0;.<br>1: Back-porch calmping. | |
| | ICLAMP_B_K2_EN | 0 | Leakage = leakage + err * gain_true * k1 * k2 * k2_en;. | |
| **35h (066Ah)** | **REG066A** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | ICLAMP_B_AGC_FINE[7:0] | 7:0 | Agc fine gain. | |
| **35h (066Bh)** | **REG066B** | **7:0** | **Default : 0x1C** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | ICLAMP_B_AGC_COARSE[1:0] | 5:4 | Agc coarse gain. | |
| | ICLAMP_B_AGC_FINE[11:8] | 3:0 | See description of '066Ah'. | |
| **36h** | **REG066C** | **7:0** | **Default : 0x40** | **Access : R/W** |

| ADC_DTOP Register (Bank = 06) | | | | |
|---|---|---|---|---|
| **Index (Absolute)** | **Mnemonic** | **Bit** | **Description** | |
| **(066Ch)** | ICLAMP_B_PGA_OFST[7:0] | 7:0 | Pga offset. | |
| **36h (066Dh)** | **REG066D** | **7:0** | **Default : 0x05** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | ICLAMP_B_ERR_MAX[4:0] | 4:0 | Bac_porch_level error < +- REG_CLMP_ERR_MAX <= +-31 * 8 !!!. | |
| **37h (066Eh)** | **REG066E** | **7:0** | **Default : 0x4A** | **Access : R/W** |
| | ICLAMP_B_LKG_MODE[1:0] | 7:6 | 001: Adaptive leakage tracking.<br>001: Adaptive leakage tracking.<br>Leakage is bounded by +- REG_ICLAMP_LKG[4:0].<br>010: Freeze leakage.<br>011: Load leakage = REG_ICLAMP_LKG[5] * REG_CLMP_LKG[4:0];.<br>100: Load K1'accu into leakage for quickly 1st order update. | |
| | ICLAMP_B_LKG[5:0] | 5:0 | [5]: Sign bit.<br>0: Posetive.<br>1: Negative.<br>[4:0] : magnitude.<br>0 ~ 31 LSB of +-10uA/32.<br>See REG_ICLAMP_LKG_MODE. | |
| **37h (066Fh)** | **REG066F** | **7:0** | **Default : 0x08** | **Access : R/W** |
| | ICLAMP_B_DLKG_MAX[5:0] | 7:2 | Delta_leakage is bounded by +- (REG_CLMP_DLKG_MAX / 512).<br>+- 1/8. | |
| | ICLAMP_B_FREZ_ZERO | 1 | 1: Set CLMP_DSM = 0 when FREZ.<br>0: Set CLMP_DSM = lkg when FREZ. | |
| | ICLAMP_B_LKG_MODE[2] | 0 | See description of '066Eh'. | |
| **38h (0670h)** | **REG0670** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:2 | Reserved. | |
| | ICLAMP_B_2DSM | 1 | 1: 2nd-order.<br>0: 1st-order. | |
| | ICLAMP_B_FREZ_DSM | 0 | 1: Delta-sigma frozen.<br>CLAMP_fpga/chip[5:0] = round{CLMP_DSM[15:10]+CLMP_DSM[9]}.<br>0: Delta-sigma on. | |
| **38h** | **-** | **7:0** | **Default : -** | **Access : -** |

## ADC_DTOP Register (Bank = 06)

| Index (Absolute) | Mnemonic | Bit | Description | |
|---|---|---|---|---|
| (0671h) | - | - | Reserved. | |
| 3Ah ~ 3Fh (0674h ~ 067Fh) | - | 7:0 | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| 41h (0682h) | **REG0682** | **7:0** | **Default : 0x20** | **Access : R/W** |
| | HACT_DELAY[7:0] | 7:0 | Delay for HSOUT pulse. | |
| 41h (0683h) | **REG0683** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | HACT_DELAY[11:8] | 3:0 | See description of '0682h'. | |
| 42h (0684h) | **REG0684** | **7:0** | **Default : 0x20** | **Access : R/W** |
| | HACT_DURATION[7:0] | 7:0 | Duration for HACT window. | |
| 42h (0685h) | **REG0685** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | HACT_DURATION[11:8] | 3:0 | See description of '0684h'. | |
| 44h (0688h) | **REG0688** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | UG_R_BLACK_LEVEL[7:0] | 7:0 | Black level(12). | |
| 44h (0689h) | **REG0689** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | UG_R_PIX_SEL[2:0] | 6:4 | Pixel select. | |
| | UG_R_BLACK_LEVEL[11:8] | 3:0 | See description of '0688h'. | |
| 45h (068Ah) | **REG068A** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | UG_R_USER_GAIN[7:0] | 7:0 | User gain(14.12). | |
| 45h (068Bh) | **REG068B** | **7:0** | **Default : 0x10** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | UG_R_USER_GAIN[13:8] | 5:0 | See description of '068Ah'. | |
| 46h (068Ch) | **REG068C** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | UG_R_USER_OFFSET[7:0] | 7:0 | User offset (S12). | |
| 46h (068Dh) | **REG068D** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | UG_R_DIT_MODE[1:0] | 6:5 | 00: Round, 01:truncate, 10:dithering. | |
| | UG_R_USER_OFFSET[12:8] | 4:0 | See description of '068Ch'. | |
| 47h (068Eh) | **REG068E** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | UG_G_BLACK_LEVEL[7:0] | 7:0 | Black level(12). | |

| ADC_DTOP Register (Bank = 06) | | | | |
|---|---|---|---|---|
| **Index (Absolute)** | **Mnemonic** | **Bit** | **Description** | |
| **47h (068Fh)** | **REG068F** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | UG_G_PIX_SEL[2:0] | 6:4 | Pixel select. | |
| | UG_G_BLACK_LEVEL[11:8] | 3:0 | See description of '068Eh'. | |
| **48h (0690h)** | **REG0690** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | UG_G_USER_GAIN[7:0] | 7:0 | User gain(14.12). | |
| **48h (0691h)** | **REG0691** | **7:0** | **Default : 0x10** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | UG_G_USER_GAIN[13:8] | 5:0 | See description of '0690h'. | |
| **49h (0692h)** | **REG0692** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | UG_G_USER_OFFSET[7:0] | 7:0 | User offset (S12). | |
| **49h (0693h)** | **REG0693** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | UG_G_DIT_MODE[1:0] | 6:5 | 00: Round, 01:truncate, 10:dithering. | |
| | UG_G_USER_OFFSET[12:8] | 4:0 | See description of '0692h'. | |
| **4Ah (0694h)** | **REG0694** | **7:0** | **Default : 0x80** | **Access : R/W** |
| | UG_B_BLACK_LEVEL[7:0] | 7:0 | Black level(12). | |
| **4Ah (0695h)** | **REG0695** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | UG_B_PIX_SEL[2:0] | 6:4 | Pixel select. | |
| | UG_B_BLACK_LEVEL[11:8] | 3:0 | See description of '0694h'. | |
| **4Bh (0696h)** | **REG0696** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | UG_B_USER_GAIN[7:0] | 7:0 | User gain(14.12). | |
| **4Bh (0697h)** | **REG0697** | **7:0** | **Default : 0x10** | **Access : R/W** |
| | - | 7:6 | Reserved. | |
| | UG_B_USER_GAIN[13:8] | 5:0 | See description of '0696h'. | |
| **4Ch (0698h)** | **REG0698** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | UG_B_USER_OFFSET[7:0] | 7:0 | User offset (S12). | |
| **4Ch (0699h)** | **REG0699** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | UG_B_DIT_MODE[1:0] | 6:5 | 00: Round, 01:truncate, 10:dithering. | |
| | UG_B_USER_OFFSET[12:8] | 4:0 | See description of '0698h'. | |
| **51h** | **REG06A2** | **7:0** | **Default : 0x0F** | **Access : R/W** |

| ADC_DTOP Register (Bank = 06) | | | | |
|---|---|---|---|---|
| **Index (Absolute)** | **Mnemonic** | **Bit** | **Description** | |
| **(06A2h)** | - | 7 | Reserved. | |
| | UG_RGB_OV | 6 | Override UG_BLACK/UG_GAIN/UG_OFFSET. | |
| | UG_RGB_LD_VD_DLY[5:0] | 5:0 | Delay for Load VD fine gain. | |
| **51h (06A3h)** | **REG06A3** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | UG_RGB_EN[2:0] | 2:0 | Enable UG_BLACK/UG_GAIN/UG_OFFSET register. | |
| **5Ah (06B4h)** | **REG06B4** | **7:0** | **Default : 0x44** | **Access : R/W** |
| | ANALOG_PGA_GAIN_G[3:0] | 7:4 | ADC Gain control:.<br>4'b0000 : 14/5 (Vin=0.5Vpp).<br>4'b0001 : 14/5 (Vin=0.6Vpp).<br>4'b0010 : 14/5 (Vin=0.7Vpp).<br>.<br>.<br>4'b1111 : 14/20 (Vin=2.0Vpp). | |
| | ANALOG_PGA_GAIN_R[3:0] | 3:0 | ADC Gain control:.<br>4'b0000 : 14/5 (Vin=0.5Vpp).<br>4'b0001 : 14/5 (Vin=0.6Vpp).<br>4'b0010 : 14/5 (Vin=0.7Vpp).<br>.<br>.<br>4'b1111 : 14/20 (Vin=2.0Vpp). | |
| **5Ah (06B5h)** | **REG06B5** | **7:0** | **Default : 0x04** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | ANALOG_PGA_GAIN_B[3:0] | 3:0 | ADC Gain control:.<br>4'b0000 : 14/5 (Vin=0.5Vpp).<br>4'b0001 : 14/5 (Vin=0.6Vpp).<br>4'b0010 : 14/5 (Vin=0.7Vpp).<br>.<br>.<br>4'b1111 : 14/20 (Vin=2.0Vpp). | |
| **5Ch (06B8h)** | **REG06B8** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | FIFO_BYPASS_RGB | 2 | 1=fifo bypass mode for rgb. | |
| | - | 1:0 | Reserved. | |
| **5Dh ~ 5Dh** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |

| ADC_DTOP Register (Bank = 06) | | | | |
|---|---|---|---|---|
| **Index (Absolute)** | **Mnemonic** | **Bit** | **Description** | |
| **(06BAh ~ 06BBh)** | | | | |
| **60h ~ 63h (06C0h ~ 06C7h)** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| **64h (06C8h)** | **REG06C8** | **7:0** | **Default : 0x05** | **Access : R/W** |
| | MASK_DELAY[7:0] | 7:0 | Delay for HSOUT/HSYNC pulse. | |
| **64h (06C9h)** | **REG06C9** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | MASK_EN | 4 | Enable blank ADC for CAL. | |
| | MASK_DELAY[11:8] | 3:0 | See description of '06C8h'. | |
| **65h (06CAh)** | **REG06CA** | **7:0** | **Default : 0x05** | **Access : R/W** |
| | MASK_DURATION[7:0] | 7:0 | Duration for MASK window. | |
| **65h (06CBh)** | **REG06CB** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | MASK_COAST | 7 | 1=enable mask data by coast. | |
| | MASK_CDIS | 6 | 1=disable mask during coast. | |
| | MASK_HSYNC_OR_HSOUT | 5 | 0: HSYNC, 1:HSOU. | |
| | MASK_EDGE | 4 | Select mask HSYNC start edge, 1: HSYNC rising edge, 0:falling edge. | |
| | MASK_DURATION[11:8] | 3:0 | See description of '06CAh'. | |

## ADC_DTOP2 Register (Bank = 06)

| ADC_DTOP2 Register (Bank = 06) | | | | |
|---|---|---|---|---|
| **Index (Absolute)** | **Mnemonic** | **Bit** | **Description** | |
| **01h (0602h)** | **REG0602** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | ADCB_TOGV2 | 7 | 1=ADC B channel interleaving every 2 VSYNC. | |
| | ADCB_TOGH2 | 6 | 1=ADC G channel interleaving every 2 VSYNC. | |
| | ADCG_TOGV2 | 5 | 1=ADC R channel interleaving every 2 VSYNC. | |
| | ADCG_TOGH2 | 4 | 1=ADC B channel interleaving every 2 HSYNC. | |
| | ADCR_TOGV2 | 3 | 1=ADC G channel interleaving every 2 HSYNC. | |
| | ADCR_TOGH2 | 2 | 1=ADC R channel interleaving every 2 HSYNC. | |
| | RGB_NO_VRAND | 1 | 1=no ADCA interleve V dithering. | |
| | RGB_NO_RAND | 0 | 1=no ADCA interleve H/V dithering. | |
| **01h (0603h)** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| **02h (0604h)** | **REG0604** | **7:0** | **Default : 0x02** | **Access : R/W** |
| | - | 7:2 | Reserved. | |
| | RGB_INT_V_POLARITY | 1 | 1=ADCA interleave vsync reference pulse polarity high. | |
| | RGB_INT_H_POLARITY | 0 | 1=ADCA interleave hsync reference pulse polarity high. | |
| **02h (0605h)** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| **03h (0606h)** | **REG0606** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | RGB_SELF_CAL_REF_CYC[7:0] | 7:0 | ADCA calibration trigger reference pulse cycle number. | |
| **03h (0607h)** | **REG0607** | **7:0** | **Default : 0x18** | **Access : R/W, WO** |
| | - | 7:6 | Reserved. | |
| | RGB_SELF_CAL_ALL_GAIN | 5 | 1=ADCA calibration all gain mode enable. | |
| | RGB_SELF_CAL_MODE[1:0] | 4:3 | [0]=1: ADCA linear calibration enable.<br>[1]=1: ADCA offset/gain calibration enable. | |
| | RGB_SELF_CAL_STOP | 2 | 1=ADCA calibration stop in live mode. | |
| | RGB_SELF_CAL_LIVE | 1 | 1=ADCA calibration live mode enable. | |
| | RGB_SELF_CAL_START | 0 | 1=ADCA calibration start. | |
| **04h (0608h)** | **REG0608** | **7:0** | **Default : 0x10** | **Access : R/W** |
| | RGB_SELF_CAL_DLY[7:0] | 7:0 | ADCA claibration delay from reference pulse to | |

## ADC_DTOP2 Register (Bank = 06)

| Index (Absolute) | Mnemonic | Bit | Description | |
|---|---|---|---|---|
| | | | linear/offset/gain calibration state. | |
| 04h (0609h) | **REG0609** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | RGB_SELF_CAL_LIVE_WAIT_DLY[7:0] | 7:0 | ADCA claibration wait delay number of reference pulse before re-starting new calibration in live mode. | |
| 05h (060Ah) | **REG060A** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | RGB_SELF_CAL_GPUSE_SEL | 3 | 1=ADCA SELF_CAL_G active high during linear calibration & gain calibration;.<br>Otherwise, ADCA SELF_CAL_G active high only during linear calibration. | |
| | RGB_SELF_CAL_BYPASS[2:0] | 2:0 | [0]=1: bypass ADC R calibration.<br>[1]=1: bypass ADC G calibration.<br>[2]=1: bypass ADC B calibration. | |
| 05h ~ 06h (060Bh ~ 060Dh) | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| 07h (060Eh) | **REG060E** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:1 | Reserved. | |
| | RGB_LINEAR_CAL_MODE | 0 | 1=ADCA linear calibration long mode. | |
| 07h (060Fh) | **REG060F** | **7:0** | **Default : 0xFE** | **Access : R/W** |
| | RGB_LINEAR_CAL_VREF_SEL[3:0] | 7:4 | ADCA VCAL setting during linear calibration. | |
| | RGB_LINEAR_CAL_PGA[3:0] | 3:0 | ADCA PGA setting during linear calibration. | |
| 08h (0610h) | **REG0610** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | ADCB_LCAL_EN | 2 | 1=ADC B linear calibration update enable. | |
| | ADCG_LCAL_EN | 1 | 1=ADC G linear calibration update enable. | |
| | ADCR_LCAL_EN | 0 | 1=ADC R linear calibration update enable. | |
| 09h (0612h) | **REG0612** | **7:0** | **Default : 0x1F** | **Access : R/W** |
| | RGB_LINEAR_CAL_DLY[7:0] | 7:0 | ADCA linear calibration delay samples after reference pulse rising. | |
| 09h (0613h) | **REG0613** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | RGB_LINEAR_CAL_DLY[11:8] | 3:0 | See description of '0612h'. | |
| 0Ah | **REG0614** | **7:0** | **Default : 0xFF** | **Access : R/W** |

| ADC_DTOP2 Register (Bank = 06) | | | | |
|---|---|---|---|---|
| **Index (Absolute)** | **Mnemonic** | **Bit** | **Description** | |
| **(0614h)** | RGB_LINEAR_CAL_DUR[7:0] | 7:0 | ADCA linear calibration duration samples after reference pulse rising. | |
| **0Bh ~ 0Ch (0616h ~ 0618h)** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| **0Dh ~ 12h (061Ah ~ 0625h)** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| **13h (0626h)** | **REG0626** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | ADCB_OCAL_EN | 3 | 1=ADC B offset calibration update enable. | |
| | ADCG_OCAL_EN | 2 | 1=ADC G offset calibration update enable. | |
| | ADCR_OCAL_EN | 1 | 1=ADC R offset calibration update enable. | |
| | RGB_OFFSET_CAL_MODE | 0 | 1=ADCA offset calibration long mode. | |
| **14h (0628h)** | **REG0628** | **7:0** | **Default : 0x1F** | **Access : R/W** |
| | RGB_OFFSET_CAL_DLY[7:0] | 7:0 | ADCA offset calibration delay samples after reference pulse rising. | |
| **14h (0629h)** | **REG0629** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | RGB_OFFSET_CAL_DLY[11:8] | 3:0 | See description of '0628h'. | |
| **15h (062Ah)** | **REG062A** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | RGB_OFFSET_CAL_DUR[7:0] | 7:0 | ADCA offset calibration duration samples after reference pulse rising. | |
| **16h ~ 18h (062Ch ~ 0630h)** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| **19h ~ 1Bh (0632h ~ 0636h)** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| **1Ch ~ 1Eh (0638h ~ 063Ch)** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| **1Fh** | **REG063E** | **7:0** | **Default : 0x00** | **Access : R/W** |

## ADC_DTOP2 Register (Bank = 06)

| Index (Absolute) | Mnemonic | Bit | Description | |
|---|---|---|---|---|
| (063Eh) | - | 7:5 | Reserved. | |
| | RGB_GAIN_CAL_MISMATCH_ONLY | 4 | 1=ADCA gain calibration only calibrate channel0/channel1 mismatch. | |
| | ADCB_GCAL_EN | 3 | 1=ADC B gain calibration update enable. | |
| | ADCG_GCAL_EN | 2 | 1=ADC G gain calibration update enable. | |
| | ADCR_GCAL_EN | 1 | 1=ADC R gain calibration update enable. | |
| | RGB_GAIN_CAL_MODE | 0 | 1=ADCA gain calibration long mode. | |
| 20h (0640h) | **REG0640** | **7:0** | **Default : 0x1F** | **Access : R/W** |
| | RGB_GAIN_CAL_DLY[7:0] | 7:0 | ADCA gain calibration delay samples after reference pulse rising. | |
| 20h (0641h) | **REG0641** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | RGB_GAIN_CAL_DLY[11:8] | 3:0 | See description of '0640h'. | |
| 21h (0642h) | **REG0642** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | RGB_GAIN_CAL_DUR[7:0] | 7:0 | ADCA gain calibration duration samples after reference pulse rising. | |
| 21h (0643h) | **REG0643** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | RGB_GAIN_CAL_DUR[15:8] | 7:0 | See description of '0642h'. | |
| 22h ~ 25h (0644h ~ 064Ah) | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| 26h ~ 29h (064Ch ~ 0652h) | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| 2Ah ~ 2Dh (0654h ~ 065Ah) | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| 3Fh (067Eh) | **REG067E** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | RGB_GAIN_CAL_LVREF[3:0] | 7:4 | ADCA gain calibration low VCAL write value. | |
| | RGB_GAIN_CAL_HVREF[3:0] | 3:0 | ADCA gain calibration high VCAL write value. | |
| 3Fh (067Fh) | **REG067F** | **7:0** | **Default : 0x00** | **Access : R/W, WO** |
| | RGB_GAIN_CAL_VREF_WP | 7 | ADCA gain calibration VCAL write enable. | |
| | - | 6:4 | Reserved. | |

## ADC_DTOP2 Register (Bank = 06)

| Index (Absolute) | Mnemonic | Bit | Description | |
|---|---|---|---|---|
| | RGB_GAIN_CAL_VREF_WG[3:0] | 3:0 | ADCA gain calibration VCAL write related gain setting. | |
| **40h (0680h)** | **REG0680** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | RGB_GAIN_CAL_TARGET[7:0] | 7:0 | ADCA gain calibration VCAL_HIGH-VCAL_LOW target digital code write value. | |
| **40h (0681h)** | **REG0681** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | RGB_GAIN_CAL_TARGET[11:8] | 3:0 | See description of '0680h'. | |
| **41h (0682h)** | **REG0682** | **7:0** | **Default : 0x00** | **Access : R/W, WO** |
| | RGB_GAIN_CAL_TARGET_WP | 7 | ADCA gain calibration (VCAL_HIGH-VCAL_LOW) target digital code write enable. | |
| | - | 6:4 | Reserved. | |
| | RGB_GAIN_CAL_TARGET_WG[3:0] | 3:0 | ADCA gain calibration VCAL_HIGH-VCAL_LOW target digital code write related gain setting. | |
| **42h ~ 43h (0684h ~ 0687h)** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| **45h ~ 4Dh (068Ah ~ 069Bh)** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| **7Bh (06F6h)** | **REG06F6** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | RGB_SELF_CAL_REF_DLY[7:0] | 7:0 | The delay samples of ADCA calibration reference pulse after Hsync/Vsync. | |
| **7Bh (06F7h)** | **REG06F7** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | RGB_SELF_CAL_REF_SEL[2:0] | 7:5 | [2:0]=1xx : ADCA using VSYNC as calibration reference pulse.<br>[2:0]=01x : ADCA using HSYNC as calibration reference pulse.<br>[2:0]=001 : ADCA using HSOUT as calibration reference pulse.<br>[2:0]=000 : ADCA calibration reference always high. | |
| | RGB_SELF_CAL_REF_EDGE | 4 | 1=ADCA calibration reference using trailing edge of hsync/vsync. | |
| | RGB_SELF_CAL_REF_DLY[11:8] | 3:0 | See description of '06F6h'. | |
| **7Dh ~ 7Fh** | **-** | **7:0** | **Default : -** | **Access : -** |

| ADC_DTOP2 Register (Bank = 06) | | | |
|---|---|---|---|
| **Index (Absolute)** | **Mnemonic** | **Bit** | **Description** |
| **(06FAh ~ 06FFh)** | - | - | Reserved. |

## CHIPTOP Register (Bank = 07)

| CHIPTOP Register (Bank = 07) | | | | |
|---|---|---|---|---|
| **Index (Absolute)** | **Mnemonic** | **Bit** | **Description** | |
| **01h (0702h)** | **REG0702** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | SAR_CH2_LOB_LSB2[1:0] | 7:6 | The LSB 2-bit of voltage lower bound in MCU sleep mode for channel 2 keypad wakeup. | |
| | SAR_CH2_UPB_LSB2[1:0] | 5:4 | The LSB 2-bit of voltage upper bound in MCU sleep mode for channel 2 keypad wakeup. | |
| | SAR_CH1_LOB_LSB2[1:0] | 3:2 | The LSB 2-bit of voltage lower bound in MCU sleep mode for channel 1 keypad wakeup. | |
| | SAR_CH1_UPB_LSB2[1:0] | 1:0 | The LSB 2-bit of voltage upper bound in MCU sleep mode for channel 1 keypad wakeup. | |
| **01h (0703h)** | **REG0703** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | SAR_CH3_LOB_LSB2[1:0] | 3:2 | The LSB 2-bit of voltage lower bound in MCU sleep mode for channel 3 keypad wakeup. | |
| | SAR_CH3_UPB_LSB2[1:0] | 1:0 | The LSB 2-bit of voltage upper bound in MCU sleep mode for channel 3 keypad wakeup. | |
| **02h (0704h)** | **REG0704** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | SAR_DIVCTRL[4:0] | 4:0 | SAR operation clock divider selection. | |
| **02h (0705h)** | **REG0705** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | POR_DEGLITCH[2:0] | 6:4 | For POR deglitch setting. | |
| | - | 3:1 | Reserved. | |
| | SAR_ONESHOT | 0 | One-shot for SAR one-shot mode. | |
| **03h (0706h)** | **REG0706** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | CP1_N_DRV[1:0] | 3:2 | Driving control for PAD_CP1_N. | |
| | CP1_P_DRV[1:0] | 1:0 | Driving control for PAD_CP1_P. | |
| **03h (0707h)** | **REG0707** | **7:0** | **Default : 0x0B** | **Access : R/W** |
| | TEST_9TO12_EN | 7 | Second test enable bit for test_bus[9:12]. (both of testmode enable and this enable are set, then just can enable test_bus[9:12]). | |
| | BT656_OUT_EN | 6 | Bt656 out enable bit. | |
| | - | 5 | Reserved. | |

| CHIPTOP Register (Bank = 07) | | | | |
|---|---|---|---|---|
| **Index (Absolute)** | **Mnemonic** | **Bit** | **Description** | |
| | PWM1D_SEL | 4 | PAD_PWM1D output select:.<br>0: Normal PWM1D output.<br>1: CABC output. | |
| | CP_DIV_CNTR[3:0] | 3:0 | CP1_P/N frequency divide counter.<br>Freq = XIN_freq / (CP_DIV_CNTR+1). | |
| **04h (0708h)** | **REG0708** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | NEW_GPIO_EN[7:0] | 7:0 | Gpio enable for each new gpio.<br>[0]: PAD_CLKIN.<br>[1]: PAD_VD0.<br>[2]: PAD_VD1.<br>[3]: PAD_VD2.<br>[4]: PAD_VD3.<br>[5]: PAD_VD4.<br>[6]: PAD_VD5.<br>[7]: PAD_VD6.<br>[8]: PAD_VD7.<br>[9]: PAD_INT.<br>[10]: PAD_PWM1D.<br>[11]: PAD_PWM2D.<br>[12]: PAD_ROUT0.<br>[13]: PAD_GOUT4.<br>[14]: PAD_CLKO.<br>[15]: PAD_DEO. | |
| **04h (0709h)** | **REG0709** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | NEW_GPIO_EN[15:8] | 7:0 | See description of '0708h'. | |
| **05h (070Ah)** | **REG070A** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | NEW_GPIO_EN[23:16] | 7:0 | See description of '0708h'. | |
| **05h (070Bh)** | **REG070B** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | NEW_GPIO_EN[31:24] | 7:0 | See description of '0708h'. | |
| **06h (070Ch)** | **REG070C** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | NEW_GPIO_EN[39:32] | 7:0 | See description of '0708h'. | |
| **06h (070Dh)** | **REG070D** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | NEW_GPIO_EN[47:40] | 7:0 | See description of '0708h'. | |
| **07h (070Eh)** | **REG070E** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | NEW_GPIO_EN[55:48] | 7:0 | See description of '0708h'. | |
| **07h** | **REG070F** | **7:0** | **Default : 0xFF** | **Access : R/W** |

| CHIPTOP Register (Bank = 07) | | | | |
|---|---|---|---|---|
| **Index (Absolute)** | **Mnemonic** | **Bit** | **Description** | |
| **(070Fh)** | NEW_GPIO_EN[63:56] | 7:0 | See description of '0708h'. | |
| **08h (0710h)** | **REG0710** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | NEW_GPIO_O[7:0] | 7:0 | The value of gpio output for each new gpio. | |
| **08h (0711h)** | **REG0711** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | NEW_GPIO_O[15:8] | 7:0 | See description of '0710h'. | |
| **09h (0712h)** | **REG0712** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | NEW_GPIO_O[23:16] | 7:0 | See description of '0710h'. | |
| **09h (0713h)** | **REG0713** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | NEW_GPIO_O[31:24] | 7:0 | See description of '0710h'. | |
| **0Ah (0714h)** | **REG0714** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | NEW_GPIO_O[39:32] | 7:0 | See description of '0710h'. | |
| **0Ah (0715h)** | **REG0715** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | NEW_GPIO_O[47:40] | 7:0 | See description of '0710h'. | |
| **0Bh (0716h)** | **REG0716** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | NEW_GPIO_O[55:48] | 7:0 | See description of '0710h'. | |
| **0Bh (0717h)** | **REG0717** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | NEW_GPIO_O[63:56] | 7:0 | See description of '0710h'. | |
| **0Ch (0718h)** | **REG0718** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | NEW_GPIO_OEN[7:0] | 7:0 | The value of gpio output enable for each new gpio.<br>0: Gpio as output.<br>1: Gpio as input. | |
| **0Ch (0719h)** | **REG0719** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | NEW_GPIO_OEN[15:8] | 7:0 | See description of '0718h'. | |
| **0Dh (071Ah)** | **REG071A** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | NEW_GPIO_OEN[23:16] | 7:0 | See description of '0718h'. | |
| **0Dh (071Bh)** | **REG071B** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | NEW_GPIO_OEN[31:24] | 7:0 | See description of '0718h'. | |
| **0Eh (071Ch)** | **REG071C** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | NEW_GPIO_OEN[39:32] | 7:0 | See description of '0718h'. | |
| **0Eh (071Dh)** | **REG071D** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | NEW_GPIO_OEN[47:40] | 7:0 | See description of '0718h'. | |
| **0Fh (071Eh)** | **REG071E** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | NEW_GPIO_OEN[55:48] | 7:0 | See description of '0718h'. | |

| CHIPTOP Register (Bank = 07) | | | | |
|---|---|---|---|---|
| **Index (Absolute)** | **Mnemonic** | **Bit** | **Description** | |
| **0Fh (071Fh)** | **REG071F** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | NEW_GPIO_OEN[63:56] | 7:0 | See description of '0718h'. | |
| **10h (0720h)** | **REG0720** | **7:0** | **Default : 0x00** | **Access : RO** |
| | NEW_GPIO_I[7:0] | 7:0 | The read value of for each new gpio. | |
| **10h (0721h)** | **REG0721** | **7:0** | **Default : 0x00** | **Access : RO** |
| | NEW_GPIO_I[15:8] | 7:0 | See description of '0720h'. | |
| **11h (0722h)** | **REG0722** | **7:0** | **Default : 0x00** | **Access : RO** |
| | NEW_GPIO_I[23:16] | 7:0 | See description of '0720h'. | |
| **11h (0723h)** | **REG0723** | **7:0** | **Default : 0x00** | **Access : RO** |
| | NEW_GPIO_I[31:24] | 7:0 | See description of '0720h'. | |
| **12h (0724h)** | **REG0724** | **7:0** | **Default : 0x00** | **Access : RO** |
| | NEW_GPIO_I[39:32] | 7:0 | See description of '0720h'. | |
| **12h (0725h)** | **REG0725** | **7:0** | **Default : 0x00** | **Access : RO** |
| | NEW_GPIO_I[47:40] | 7:0 | See description of '0720h'. | |
| **13h (0726h)** | **REG0726** | **7:0** | **Default : 0x00** | **Access : RO** |
| | NEW_GPIO_I[55:48] | 7:0 | See description of '0720h'. | |
| **13h (0727h)** | **REG0727** | **7:0** | **Default : 0x00** | **Access : RO** |
| | NEW_GPIO_I[63:56] | 7:0 | See description of '0720h'. | |
| **14h (0728h)** | **REG0728** | **7:0** | **Default : 0x00** | **Access : RO** |
| | TEST_24BIT_BUS_STATUS[7:0] | 7:0 | The read value of test 24bit bus. | |
| **14h (0729h)** | **REG0729** | **7:0** | **Default : 0x00** | **Access : RO** |
| | TEST_24BIT_BUS_STATUS[15:8] | 7:0 | See description of '0728h'. | |
| **15h (072Ah)** | **REG072A** | **7:0** | **Default : 0x00** | **Access : RO** |
| | TEST_24BIT_BUS_STATUS[23:16] | 7:0 | See description of '0728h'. | |
| **20h (0740h)** | **REG0740** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | BT656_OUT_CLK_GATE | 4 | 0: Enable BT656 out clock.<br>1: Disable BT656 out clock. | |
| | PWM_OUT_CLK_GATE | 3 | 0: Enable PWM out clock.<br>1: Disable PWM out clock. | |
| | MOD_CAL_CLK_GATE | 2 | 0: Enable MOD cal clock.<br>1: Disable MOD cal clock. | |
| | FSCCLK_DIV4_GATE | 1 | 0: Enable MVD digital front-end divide 4 clock. | |

| CHIPTOP Register (Bank = 07) | | | | |
|---|---|---|---|---|
| **Index (Absolute)** | **Mnemonic** | **Bit** | **Description** | |
| | | | 1: Disable MVD digital front-end divide 4 clock. | |
| | FSCCLK_DIV2_GATE | 0 | 0: Enable MVD digital front-end divide 2 clock.<br>1: Disable MVD digital front-end divide 2 clock. | |
| **21h (0742h)** | **REG0742** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:5 | Reserved. | |
| | BT656_OUT_CLK_INV | 4 | BT656 out clock inverting. | |
| | PWM_OUT_CLK_INV | 3 | PWM out clock inverting. | |
| | MOD_CAL_CLK_INV | 2 | MOD cal clock inverting. | |
| | FSCCLK_DIV4_INV | 1 | MVD digital front-end divide 4 clock inverting. | |
| | FSCCLK_DIV2_INV | 0 | MVD digital front-end divide 2 clock inverting. | |
| **22h (0744h)** | **REG0744** | **7:0** | **Default : 0x21** | **Access : R/W** |
| | MOD_CAL_CLK_SEL[1:0] | 7:6 | MOD cal clock selection.<br>0: XIN/8.<br>1: XIN/16.<br>2: XIN/32.<br>3: DFT Clock. | |
| | FSCCLK_SEL[1:0] | 5:4 | MVD digital front-end clock selection.<br>0: FSCCLK/4.<br>1: FSCCLK/2.<br>2: FSCCLK.<br>3: DFT Clock. | |
| | FSCCLK_DIV4_SEL[1:0] | 3:2 | MVD digital front-end divide 4 clock selection.<br>0: FSCCLK/4.<br>1: FSCCLK/2.<br>2: FSCCLK.<br>3: DFT Clock. | |
| | FSCCLK_DIV2_SEL[1:0] | 1:0 | MVD digital front-end divide 2 clock selection.<br>0: FSCCLK/4.<br>1: FSCCLK/2.<br>2: FSCCLK.<br>3: DFT Clock. | |
| **22h (0745h)** | **REG0745** | **7:0** | **Default : 0x60** | **Access : R/W** |
| | BT656_OUT_CLK_SEL[1:0] | 7:6 | ODCLK selection.<br>0: IDCLK.<br>1: LPLL/2.<br>2: LPLL.<br>3: DFT Clock. | |

| CHIPTOP Register (Bank = 07) | | | | |
|---|---|---|---|---|
| **Index (Absolute)** | **Mnemonic** | **Bit** | **Description** | |
| | ODGEN_CLK_SEL[1:0] | 5:4 | ODCLK selection.<br>0: IDCLK.<br>1: LPLL/2.<br>2: LPLL.<br>3: DFT Clock. | |
| | CLK_ATOP_SEL[1:0] | 3:2 | MOD cal clock selection.<br>0: 432MHz.<br>1: Null.<br>2: 216MHz.<br>3: DFT Clock. | |
| | PWM_OUT_CLK_SEL[1:0] | 1:0 | MOD cal clock selection.<br>0: ODCLK.<br>1: ODCLK/2.<br>2: DFT Clock.<br>3: DFT Clock. | |
| **30h ~ 33h (0760h ~ 0767h)** | **-** | **7:0** | **Default : -** | **Access : -** |
| | - | - | Reserved. | |
| **40h (0780h)** | **REG0780** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | V_BLK_ST1_VPOS[7:0] | 7:0 | Bt656 v blanking 1st start v position. | |
| **40h (0781h)** | **REG0781** | **7:0** | **Default : 0x0F** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | V_BLK_ST1_VPOS[11:8] | 3:0 | See description of '0780h'. | |
| **41h (0782h)** | **REG0782** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | V_BLK_ST1_HPOS[7:0] | 7:0 | Bt656 v blanking 1st start h position. | |
| **41h (0783h)** | **REG0783** | **7:0** | **Default : 0x0F** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | V_BLK_ST1_HPOS[11:8] | 3:0 | See description of '0782h'. | |
| **42h (0784h)** | **REG0784** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | V_BLK_END1_VPOS[7:0] | 7:0 | Bt656 v blanking 1st endt v position. | |
| **42h (0785h)** | **REG0785** | **7:0** | **Default : 0x0F** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | V_BLK_END1_VPOS[11:8] | 3:0 | See description of '0784h'. | |
| **43h (0786h)** | **REG0786** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | V_BLK_END1_HPOS[7:0] | 7:0 | Bt656 v blanking 1st end h position. | |

| CHIPTOP Register (Bank = 07) | | | | |
|---|---|---|---|---|
| **Index (Absolute)** | **Mnemonic** | **Bit** | **Description** | |
| **43h (0787h)** | **REG0787** | **7:0** | **Default : 0x0F** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | V_BLK_END1_HPOS[11:8] | 3:0 | See description of '0786h'. | |
| **44h (0788h)** | **REG0788** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | V_BLK_ST2_VPOS[7:0] | 7:0 | Bt656 v blanking 2nd start v position. | |
| **44h (0789h)** | **REG0789** | **7:0** | **Default : 0x0F** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | V_BLK_ST2_VPOS[11:8] | 3:0 | See description of '0788h'. | |
| **45h (078Ah)** | **REG078A** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | V_BLK_ST2_HPOS[7:0] | 7:0 | Bt656 v blanking 2nd start h position. | |
| **45h (078Bh)** | **REG078B** | **7:0** | **Default : 0x0F** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | V_BLK_ST2_HPOS[11:8] | 3:0 | See description of '078Ah'. | |
| **46h (078Ch)** | **REG078C** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | V_BLK_END2_VPOS[7:0] | 7:0 | Bt656 v blanking 2nd endt v position. | |
| **46h (078Dh)** | **REG078D** | **7:0** | **Default : 0x0F** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | V_BLK_END2_VPOS[11:8] | 3:0 | See description of '078Ch'. | |
| **47h (078Eh)** | **REG078E** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | V_BLK_END2_HPOS[7:0] | 7:0 | Bt656 v blanking 2nd end h position. | |
| **47h (078Fh)** | **REG078F** | **7:0** | **Default : 0x0F** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | V_BLK_END2_HPOS[11:8] | 3:0 | See description of '078Eh'. | |
| **48h (0790h)** | **REG0790** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | FLD_ST1_VPOS[7:0] | 7:0 | Bt656 field1 start v position. | |
| **48h (0791h)** | **REG0791** | **7:0** | **Default : 0x0F** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | FLD_ST1_VPOS[11:8] | 3:0 | See description of '0790h'. | |
| **49h (0792h)** | **REG0792** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | FLD_ST1_HPOS[7:0] | 7:0 | Bt656 field1 start h position. | |
| **49h (0793h)** | **REG0793** | **7:0** | **Default : 0x0F** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | FLD_ST1_HPOS[11:8] | 3:0 | See description of '0792h'. | |

| CHIPTOP Register (Bank = 07) | | | | |
|---|---|---|---|---|
| **Index (Absolute)** | **Mnemonic** | **Bit** | **Description** | |
| **4Ah (0794h)** | **REG0794** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | FLD_ST2_VPOS[7:0] | 7:0 | Bt656 field2 start v position. | |
| **4Ah (0795h)** | **REG0795** | **7:0** | **Default : 0x0F** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | FLD_ST2_VPOS[11:8] | 3:0 | See description of '0794h'. | |
| **4Bh (0796h)** | **REG0796** | **7:0** | **Default : 0xFF** | **Access : R/W** |
| | FLD_ST2_HPOS[7:0] | 7:0 | Bt656 field2 start h position. | |
| **4Bh (0797h)** | **REG0797** | **7:0** | **Default : 0x0F** | **Access : R/W** |
| | - | 7:4 | Reserved. | |
| | FLD_ST2_HPOS[11:8] | 3:0 | See description of '0796h'. | |
| **4Ch (0798h)** | **REG0798** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | MASK_Y_BLK_VA[7:0] | 7:0 | Bt656 mask y blk value. | |
| **4Ch (0799h)** | **REG0799** | **7:0** | **Default : 0x08** | **Access : R/W** |
| | - | 7 | Reserved. | |
| | BT656_8BIT | 6 | Bt656 8bit mode. | |
| | DDR_HL_SWAP | 5 | Bt656 ddr high low swap. | |
| | CRCB_SWAP | 4 | Swap crcb position in 422. | |
| | 444_BYPASS | 3 | Enable 444 to 422 conversion. | |
| | MASK_Y_BLK_EN | 2 | Bt656 mask y blk enable. | |
| | MASK_Y_BLK_VA[9:8] | 1:0 | See description of '0798h'. | |
| **4Dh (079Ah)** | **REG079A** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | MASK_C_BLK_VA[7:0] | 7:0 | Bt656 mask c blk value. | |
| **4Dh (079Bh)** | **REG079B** | **7:0** | **Default : 0x00** | **Access : R/W** |
| | - | 7:3 | Reserved. | |
| | MASK_C_BLK_EN | 2 | Bt656 mask c blk enable. | |
| | MASK_C_BLK_VA[9:8] | 1:0 | See description of '079Ah'. | |

## REGISTER TABLE REVISION HISTORY

| Date | Bank | Register |
|---|---|---|
| 10/28/10 | | Created first version. |

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